2.75V-42V, Low I_Q, LDO Linear Regulator

1 FEATURES

- Automotive AEC-Q100 Grade 1 Compliance
- Ultra-Low I_Q < 5.5μA
- Wide Input Voltage Range: 2.75V to 42V
- ±2%，3.3V, 5V and 15V Fixed Outputs and 0.6V to 24V Adjustable Output
- Up to 200mA/100mA Output Current
- Shutdown Current < 1μA
- PG Indicator with Adjustable Delay for MCU Applications
- High PSRR 70dB @ 100Hz
- Stable Close-Loop Operation with only 1μF Low-ESR Ceramic Output Capacitor
- Low Dropout：130mV @ 100mA
- Up to 42V High Voltage EN Pin with Logic Threshold
- Over-Current Protection
- Over Temperature Shutdown and Auto Restart
- Internal Soft Start
- -40˚C to 150˚C Junction Temperature
- Thermally Enhanced MSOP-EP8 Package

2 APPLICATIONS

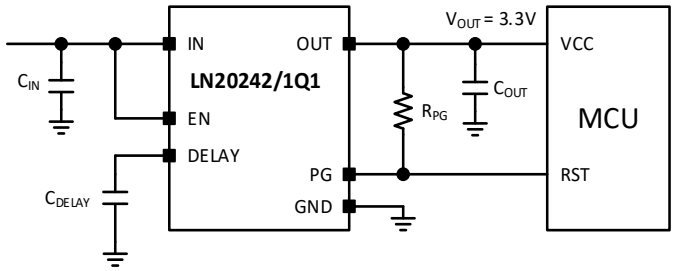
- Automotive Power Supplies
- Industrial Power Supplies
- Battery Powered Systems

3 DESCRIPTION

LN20X42/1Q1 are ultra-low quiescent current, low dropout linear regulators (LDOs) with a wide input voltage range of 2.75V to 42V. The series provides 3.3V, 5V and 15V fixed outputs or 0.6V to 24V adjustable output, and delivers up to 100mA or 200mA output current. The shutdown current of LN20X42/1Q1 is less than 1μA，while the quiescent current under no-load condition is less than 5.5μA.

LN20X42/1Q1 provides a power good indicator with programmable delay to directly drive the reset pin of a microprocessor (MCU), moreover, there are options of highly accurate fixed output of 5V or 3.3V.

LN20X42/1Q1 features over-current protection and over-temperature shutdown with auto restart. The product family is available in thermally enhanced MSOP-EP8 package.



Typical MCU Application Diagram

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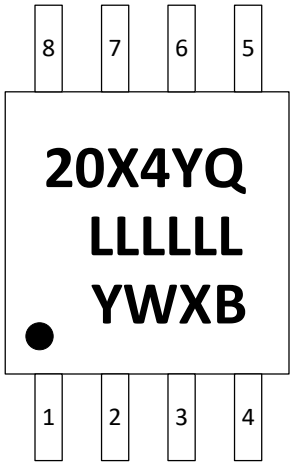
4 VERSION HISTORY

Version	Change Record	Time
1.0	Initial release	2021/10/12

5 PRODUCT AND ORDER INFORMATION

5.1 Product Infomation

Part Number	X	Y	DFR
LN20X4YQ1-DFR	0：Adjustable V_{OUT}, with PG and PG delay 1：Adjustable V_{OUT}, low I_Q 2：fixed 3.3V V_{OUT}, with PG and PG delay 3：fixed 3.3V V_{OUT}, low I_Q 4：fixed 5V V_{OUT}, with PG and PG delay 5：fixed 5V V_{OUT}, low I_Q 6：fixed 15V V_{OUT}, with PG and PG delay 7：fixed 15V V_{OUT}, low I_Q	1: 100mA 2: 200mA	IC Package：MSOP-EP8 MSL：Level-2-260C Material：RoHS Package：T@R Quantity：3000 Top Marking: as follows



20X4YQ: Part Number

LLLLLL: Lot ID

YWXB: Date Code

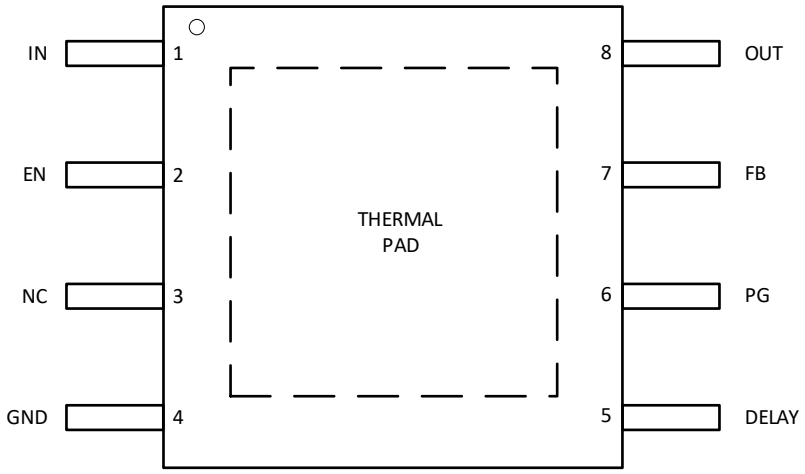
5.2 Ordering Information

Part Number	V_{OUT}	Max Load	PG	I_Q	Package	Package Qty
LN20041Q1-DFR	Adjustable	100mA	Yes	7.5uA	Tape & Reel	3000
LN20141Q1-DFR	Adjustable	100mA	No	5.5uA	Tape & Reel	3000
LN20241Q1-DFR	Fixed 3.3V	100mA	Yes	7.5uA	Tape & Reel	3000
LN20341Q1-DFR	Fixed 3.3V	100mA	No	5.5uA	Tape & Reel	3000
LN20441Q1-DFR	Fixed 5V	100mA	Yes	7.5uA	Tape & Reel	3000
LN20541Q1-DFR	Fixed 5V	100mA	No	5.5uA	Tape & Reel	3000
LN20641Q1-DFR	Fixed 15V	100mA	Yes	7.5uA	Tape & Reel	3000
LN20741Q1-DFR	Fixed 15V	100mA	No	5.5uA	Tape & Reel	3000
LN20042Q1-DFR	Adjustable	200mA	Yes	7.5uA	Tape & Reel	3000
LN20142Q1-DFR	Adjustable	200mA	No	5.5uA	Tape & Reel	3000
LN20242Q1-DFR	Fixed 3.3V	200mA	Yes	7.5uA	Tape & Reel	3000
LN20342Q1-DFR	Fixed 3.3V	200mA	No	5.5uA	Tape & Reel	3000
LN20442Q1-DFR	Fixed 5V	200mA	Yes	7.5uA	Tape & Reel	3000
LN20542Q1-DFR	Fixed 5V	200mA	No	5.5uA	Tape & Reel	3000
LN20642Q1-DFR	Fixed 15V	200mA	Yes	7.5uA	Tape & Reel	3000
LN20742Q1-DFR	Fixed 15V	200mA	No	5.5uA	Tape & Reel	3000

6 PIN CONFIGURATION AND FUNCTION

6.1 With PG and DELAY Pins

6.1.1 Pin Configuration



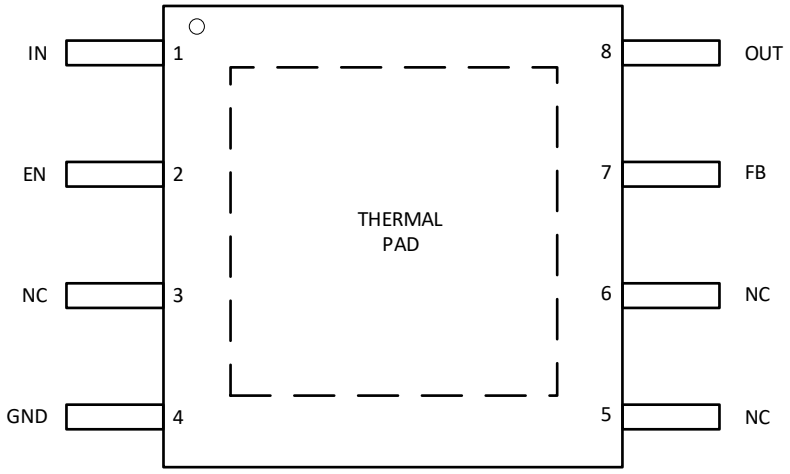
MSOP-EP8

6.1.2 Pin Function

Name	Number	Description
IN	1	Input pin, place a ceramic capacitor of at least 1μF between IN and GND.
EN	2	Enable pin, connect to a logic control signal or to IN directly.
NC	3	Connect to GND.
GND	4	Connect to GND.
DELAY	5	Power good delay pin, place a ceramic capacitor between DELAY and GND.
PG	6	Power good pin, open drain, connect a pull-up resistor between PG and an external supply or to OUT pin, if not used, keep floating.
FB	7	Feedback pin, connect to the center leg of the voltage divider between OUT and GND. This pin has no internal connection for fixed output versions
OUT	8	Output pin, place a ceramic capacitor of at 1μF between OUT and GND.

6.2 Low I_Q (Without PG and DELAY Pins)

6.2.1 Pin Configuration



MSOP-EP8

6.2.2 Pin Function

Name	Number	Description
IN	1	Input pin, place a ceramic capacitor of at least 1μF between IN and GND.
EN	2	Enable pin, connect to a logic control signal or to IN directly.
NC	3	Connect to GND.
GND	4	Connect to GND.
NC	5	Connect to GND.
NC	6	Connect to GND.
FB	7	Feedback pin, connect to the center leg of the voltage divider between OUT and GND. This pin has no internal connection for fixed output versions.
OUT	8	Output pin, place a ceramic capacitor of at 1μF between OUT and GND.

6.3 Package Thermal Parameters

Parameter (1)		MSOP-EP8	Units
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	58	˚C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	3	˚C/W

(1) Measurements are based on standard 2s2p PCB defined in JESD 51-7 2s2p, under no wind , 2W loss, and 25 ˚C ambient temperature.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Parameters	Min	Max	Unit
V_{IN}	-0.3	45	V
V_{EN}	-0.3	V_{IN}	
V_{FB}	-0.3	5.5	
V_{PG}	-0.3	5.5	
V_{OUT}	-0.3	V_{IN}	
V_{DELAY}	-0.3	2	
Junction Temperature	-40	150	˚C
Storage Temperature	-55	150	

7.2 ESD Ratings

Parameters	Min	Max	Unit
HBM Human Body Model		±3000	V
CDM Charge Device Model		±750	

7.3 Recommented Operating Condition

Parameters	Min	Max	Unit
V_{IN}	-0.3	42	V
V_{EN}	-0.3	V_{IN}	
V_{FB}	-0.3	0.7	
V_{PG}	-0.3	5.5	
V_{OUT}	-0.3	24	
V_{DELAY}	-0.3	2	
Junction Temperature	-40	150	˚C

7.4 Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 13.5V.

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN, VOUT (IN, OUT, GND PINS)						
V_{IN}	Operating Input Voltage Range		2.75		42	V
V_{OUT}	Operating Output Voltage Range for Adjustable Output		0.6		24	V
I_{Q-SH}	Input Shutdown Current	V_{EN} = 0V, V_{IN} = 13.5V		0.8	3	μA
I_{Q-NL}	Input Quiescent Current	V_{EN} = 5V, V_{IN} = 13.5V, I_{OUT} = 0A		5.5	15	μA
I_{Q-NL}	Input Quiescent Current with PG Function	V_{EN} = 5V, V_{IN} = 13.5V, I_{OUT} = 0A		7.5	17	μA
REGULATION, (OUT, FB PINS)						
V_{FB}	Regulated Feedback Voltage	V_{FB} = V_{OUT}, 28V > V_{IN} > 4.3V, IOUTMAX > I_{OUT} > 1mA	0.588	0.6	0.612	V
		V_{FB} = V_{OUT}, 42V > V_{IN} > 28V, 75%*IOUTMAX > I_{OUT} > 1mA				
I_{FB}	Feedback Input Leakage Current	V_{FB} = 0.6V	-0.1	0	0.1	μA
V_{OUT}%	Regulated Output Voltage Error for Fixed V_{OUT} Parts	28V > V_{IN} > V_{OUT} + 1V, IOUTMAX > I_{OUT} > 1mA	-2		2	%
		42V > V_{IN} > 28V, 75%*IOUTMAX > I_{OUT} > 1mA				
	Line Regulation	42V > V_{IN} > V_{OUT} + 1V, 75%*IOUTMAX > I_{OUT} > 1mA		±0.1		%
	Load Regulation	42V > V_{IN} > V_{OUT} + 1V, 75%*IOUTMAX > I_{OUT} > 1mA		±0.5		%
DROP OUT						
$V_{DO-100mA}$	Drop Out Voltage	I_{OUT} = 100mA, V_{IN} = 0.9*V_{OUT}, V_{OUT} >= 5V		130		mV
$V_{DO-200mA}$	Drop Out Voltage	I_{OUT} = 200mA, V_{IN} = 0.9*V_{OUT}, V_{OUT} >= 5V		260		mV
$V_{DO-100mA-3.3V}$	Drop Out Voltage	I_{OUT} = 100mA, V_{IN} = 0.9*V_{OUT}, V_{OUT} = 3.3V		200		mV
$V_{DO-200mA-3.3V}$	Drop Out Voltage	I_{OUT} = 200mA, V_{IN} = 0.9*V_{OUT}, V_{OUT} = 3.3V		400		mV

Electrical Characteristics (Continued)

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: V_{IN} = 13.5V.

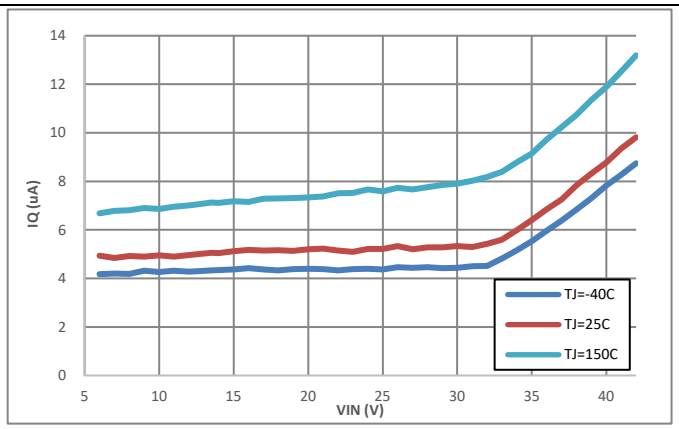
OVER CURRENT PROTECTION						
$I_{LIMIT-100mA}$	Current Limit Threshold	V_{OUT} = 90% * $V_{OUT-NOM}$, V_{IN} = 13.5V	100	180	250	mA
$I_{LIMIT-200mA}$	Current Limit Threshold	V_{OUT} = 90% * $V_{OUT-NOM}$, V_{IN} = 13.5V	200	280	500	mA
POWER SUPPLY REJECTION RATIO (PSRR)						
$G_{PSRR-100Hz}$	PSRR@100Hz	I_{OUT} = 50mA, V_{OUT} = 5 V or 3.3V		70 (1)		dB
ENABLE (EN PIN)						
V_{EN}	EN Pin Voltage Range		-0.3		V_{IN}	V
V_{EN-H}	EN Enable Threshold Voltage		2			V
V_{EN-L}	EN Disable Threshold Voltage				0.4	V
I_{EN-H}	EN Leakage Current	V_{EN} = 5V	0.5		2	µA
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold		151	170 (1)		˚C
	Thermal Shutdown Recovery Hysteresis			13 (1)		˚C
POWER GOOD (PG, DELAY PINS)						
$V_{PG-RISE}$	Power Good Rising Threshold	V_{FB} Ramping Up	87	92.5	98	%
$V_{PG-FALL}$	Power Good Falling Threshold	V_{FB} Ramping Down	83.5	88	92.5	%
R_{PG-DN}	Power Good Internal Pull-Down Resistor	V_{PG} = 1V		280		Ω
$I_{D-CHARGE}$	Delay Capacitor Charge Current	V_D = 1V		2.35		µA
$I_{D-DISCHARGE}$	Delay Capacitor Discharge Current	V_D = 1V		18		mA
V_{D-RISE}	Delay Rising Threshold			0.80		V
V_{D-FALL}	Delay Falling Threshold			0.70		V

(1) Not subject to production test, specified by bench characterization.

7.5 Typical Characteristics

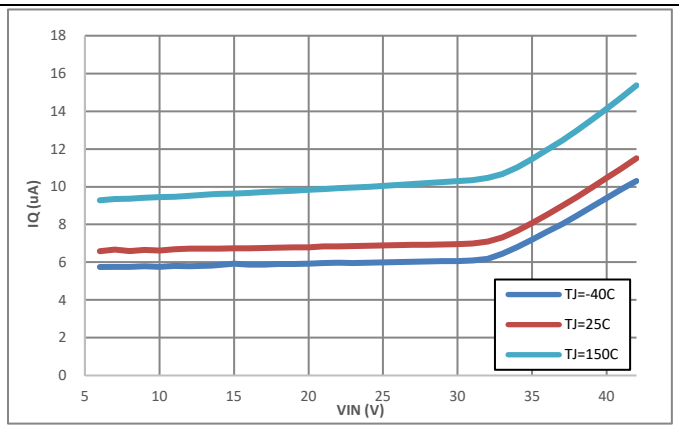
7.5.1 Characteristics Over Temperature

Unless otherwise stated, the test conditions are the same as Chapter 7.4. T_J = -40˚C to 150˚C.



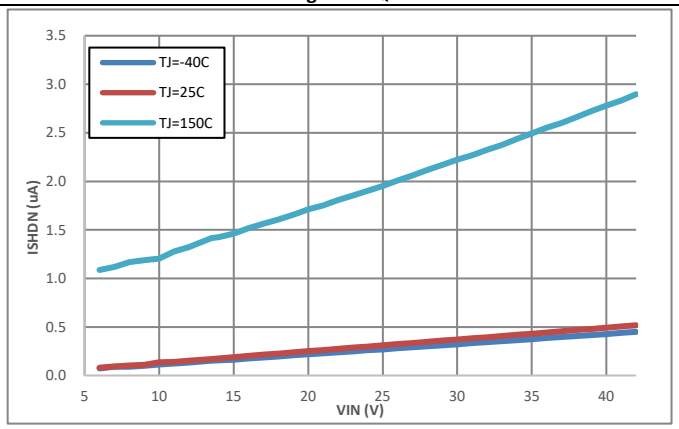
LN20542Q1, Fixed V_{OUT} = 5V, No load

Figure 1. I_Q



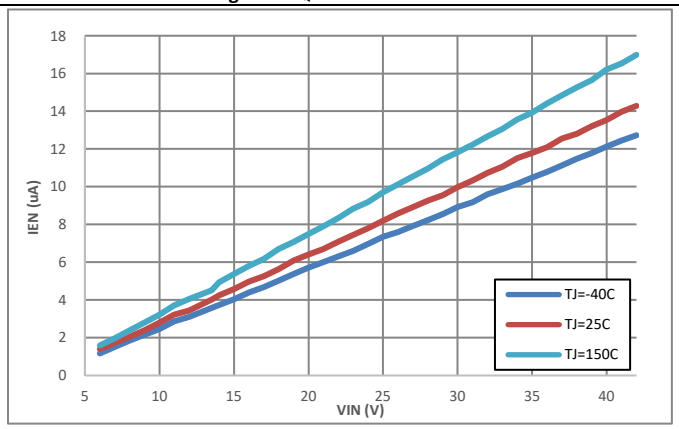
LN20442Q1, Fixed V_{OUT} = 5V, With PG, No load

Figure 2. I_Q WithPG Function



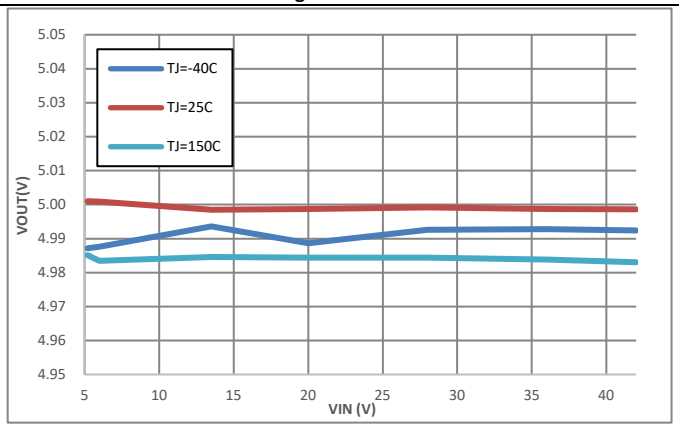
LN20442Q1, Fixed V_{OUT} = 5V, No load

Figure 3. I_{SHDN}



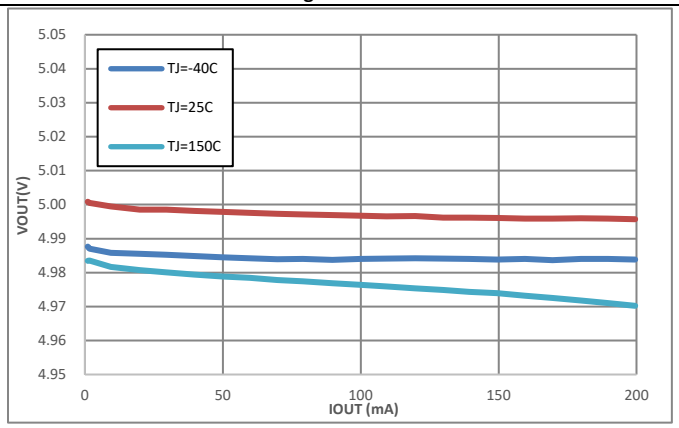
LN20442Q1, Fixed V_{OUT} = 5V, No load

Figure 4. I_{EN}



LN20042Q1, Adjustable V_{OUT} = 5V, I_{OUT} = 1mA

Figure 5. Line Regulation

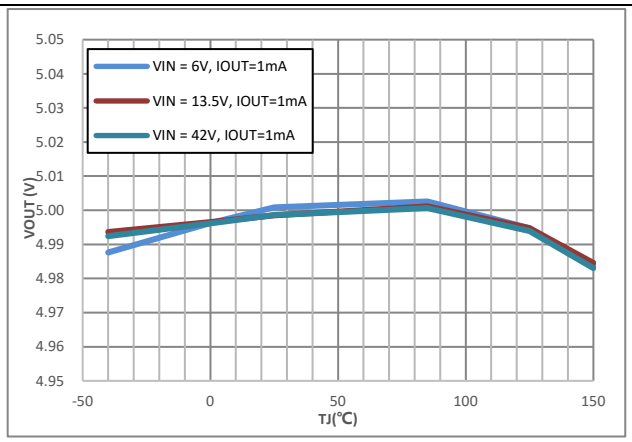


LN20042Q1, Adjustable V_{OUT} = 5V, V_{IN} = 13.5V

Figure 6. Load Regulation

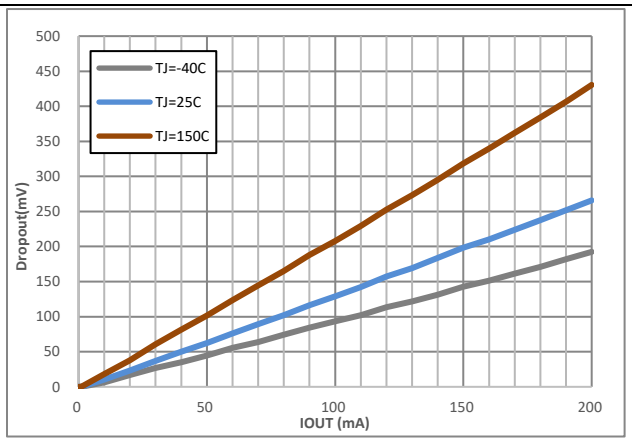
Characteristics Over Temperature (Continued)

Unless otherwise stated, the test conditions are the same as Chapter 7.4. T_J = -40˚C to 150˚C.



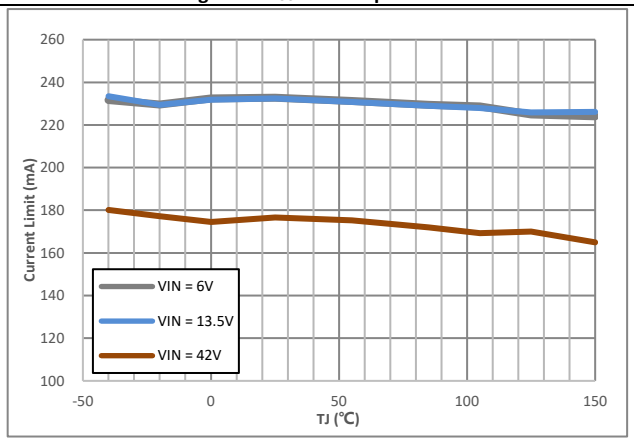
LN20042Q1, Adjustable V_{OUT} = 5V, I_{OUT} = 1mA

Figure 7. V_{OUT} vs. Temperature



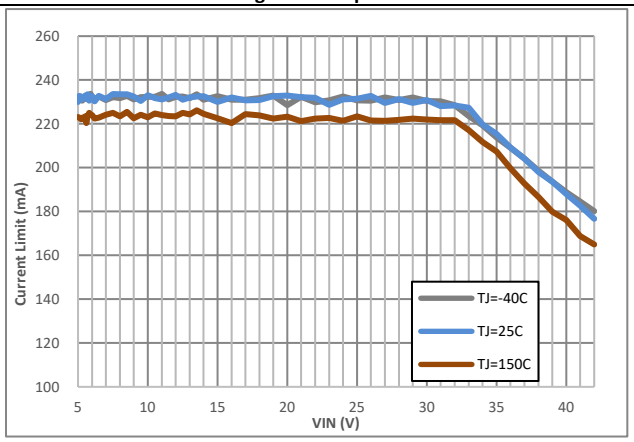
LN20042Q1, Adjustable V_{OUT} = 5V

Figure 8. Dropout



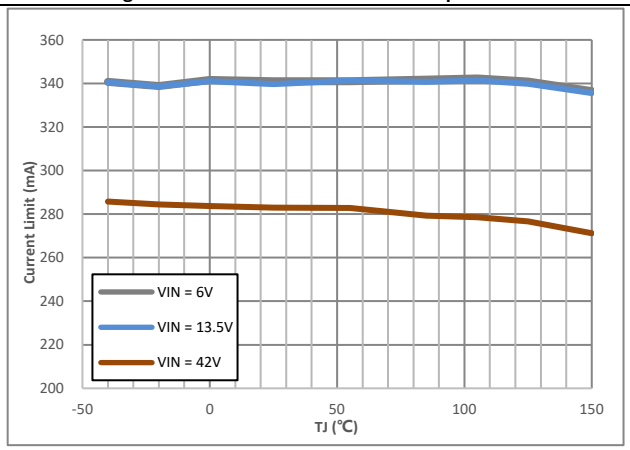
LN20041Q1, Adjustable V_{OUT} = 5V, Measured at V_{OUT} short

Figure 9. 100mA Current Limit vs. Temperature



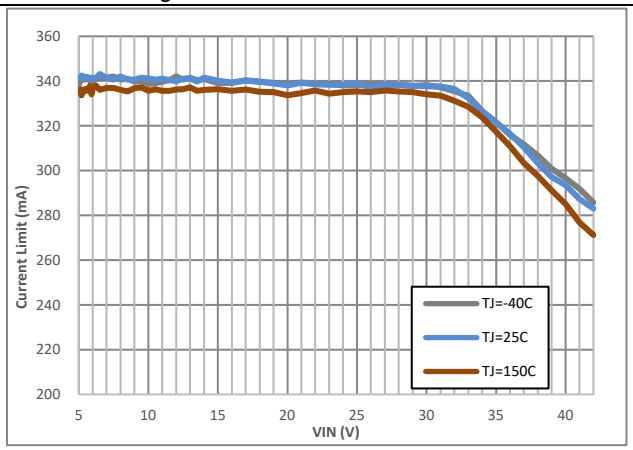
LN20041Q1, Adjustable V_{OUT} = 5V, Measured at V_{OUT} short

Figure 10. 100mA Current Limit vs. VIN



LN20542Q1, Fixed V_{OUT} = 5V, Measured at V_{OUT} short

Figure 11. 200mA Current Limit vs. Temperature

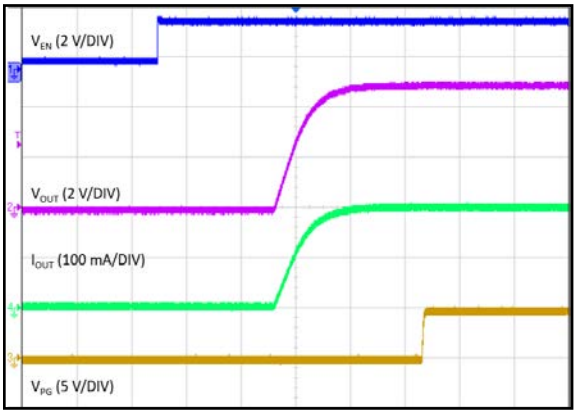


LN20052Q1, Fixed V_{OUT} = 5V, Measured at V_{OUT} short

Figure 12. 200mA Current Limit vs. VIN

7.5.2 Typical Characteristics

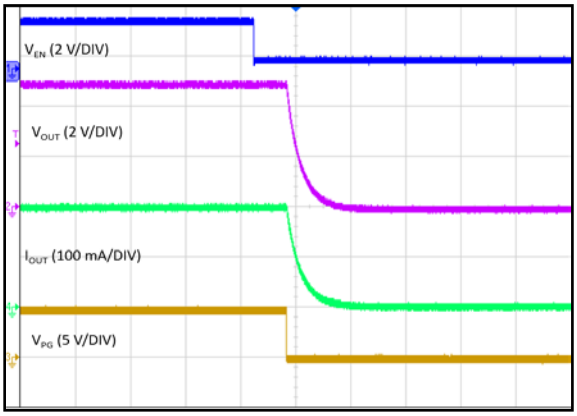
Unless otherwise stated, the test conditions are the same as Chapter 7.4. T_J = -40˚C to 150˚C.



Time (100µs/DIV)

LN20042Q1, Adjustable V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 25Ohm

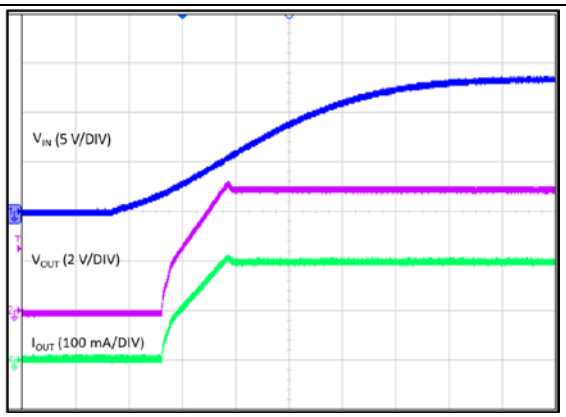
Figure 13. Startup with EN



Time (100µs/DIV)

LN20042Q1, Adjustable V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 25Ohm

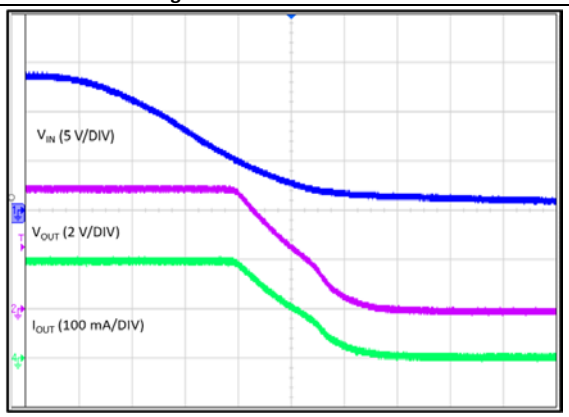
Figure 14. Shutdown with EN



Time (2ms/DIV)

LN20042Q1, Adjustable V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 25Ohm

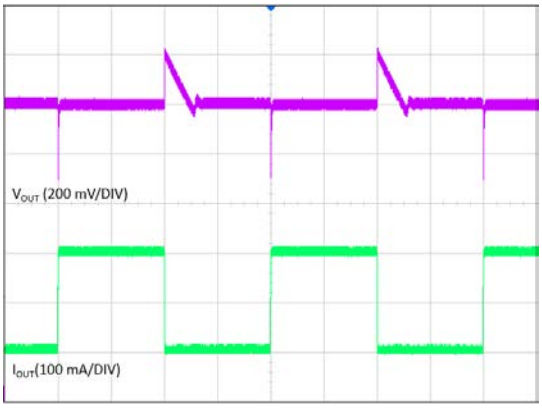
Figure 15. Startup with V_{IN}



Time (2ms/DIV)

LN20042Q1, Adjustable V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 25Ohm

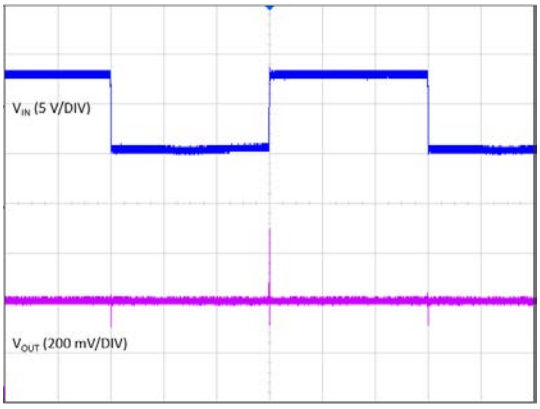
Figure 16. Shutdown with V_{IN}



Time (5ms/DIV)

LN20442Q1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, Slew Rate↑↓ = 0.1A/us

Figure 17. Load Transient 0 <-> 200mA



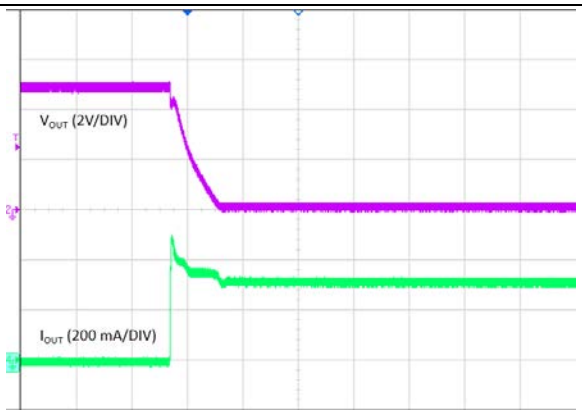
Time (1ms/DIV)

LN20442Q1, Fixed V_{OUT} = 5V, I_{OUT} = 200mA, Slew Rate↑ = 5V/us

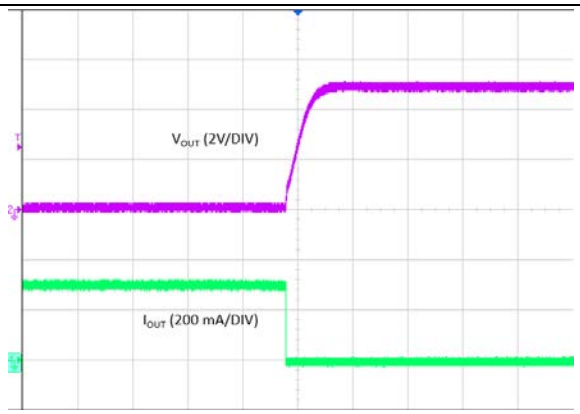
Figure 18. Line Transient 6 <-> 13.5V

Typical Characteristics (Continued)

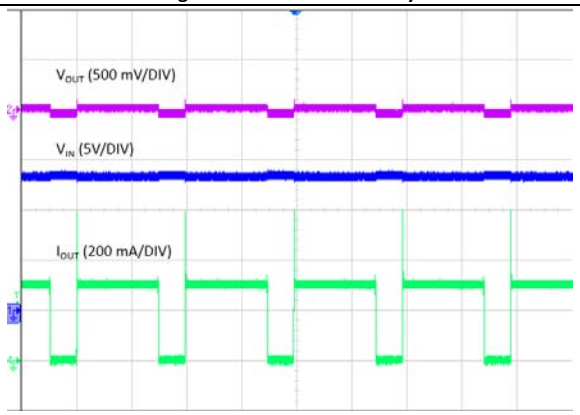
Unless otherwise stated, the test conditions are the same as Chapter 7.4. T_J = -40˚C to 150˚C.



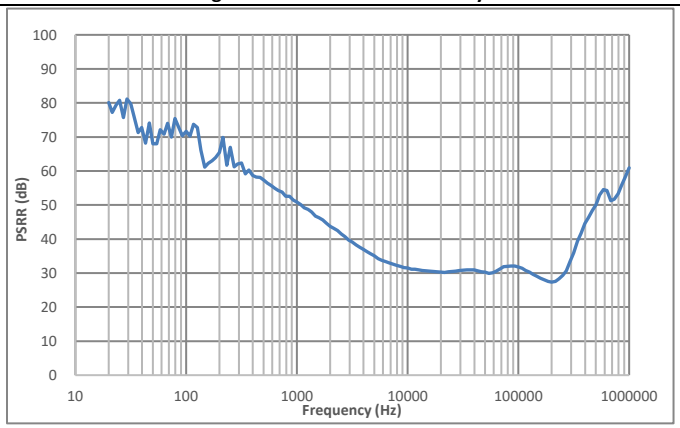
Time (200µs/DIV)
LN20042Q1, Adjustable V_{OUT} = 5V, V_{IN} = 13.5V
Figure 19. Short Circuit Entry



Time (200µs/DIV)
LN20042Q1, Adjustable V_{OUT} = 5V, V_{IN} = 13.5V
Figure 20. Short Circuit Recovery



Time (5ms/DIV)
LN20042Q1, Adjustable V_{OUT} = 5V, V_{IN} = 13.5V
Figure 21. Constant Short Circuit



LN20042Q1, Adjustable V_{OUT} = 5V, C_{IN} = 100pF, V_{IN} = 6V, I_{OUT} = 10mA
Figure 22. PSRR

8 FUNCTIONAL DESCRIPTION

8.1 Overview

LN20X42/1Q1 are ultra-low quiescent current, low dropout linear regulators (LDOs) with a wide input voltage range of 2.75V to 42V. The series provides 3.3V, 5V and 15V fixed outputs or 0.6V to 24V adjustable output, and delivers up to 100mA or 200mA output current. The shutdown current of LN20X42/1Q1 is less than 1μA, while the quiescent current under no-load condition is less than 5.5μA.

LN20X42/1Q1 provides a power good indicator with programmable DELAY pin to directly drive the reset pin of a microprocessor (MCU), moreover, there are options of highly accurate fixed output of 5V or 3.3V.

LN20X42/1Q1 features over-current protection and over-temperature shutdown with auto restart. The over-current threshold drops when the input voltage is above 28V.

The product family is available in thermally enhanced MSOP-EP8 package.

8.2 Funtional Diagram

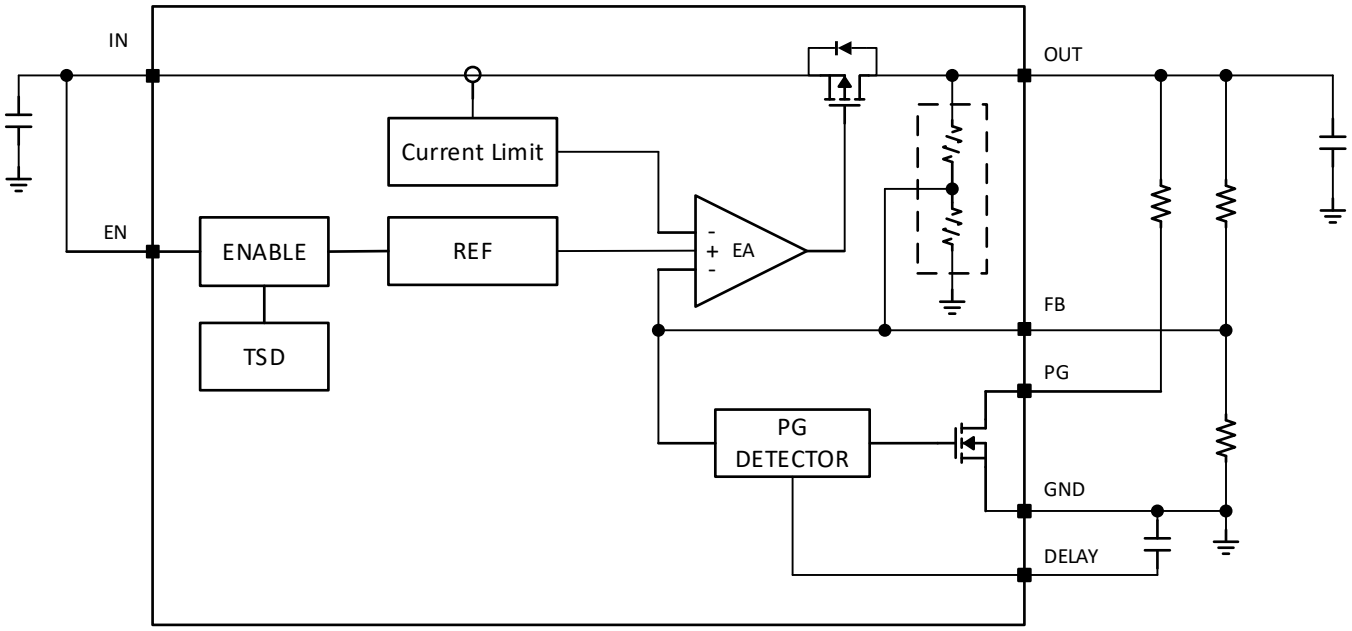


Figure 23. LN20X42/1Q1 Functional Diagram

9 APPLICATIONS

9.1 Applicaition Diagram with Full Features

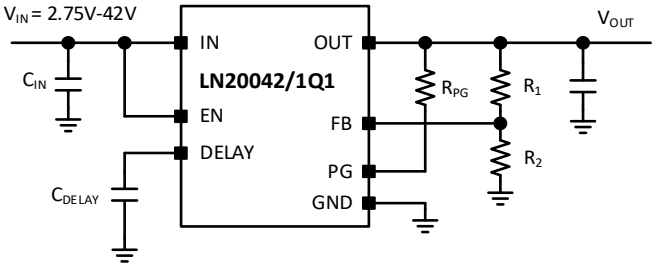


Figure 24. LN20042/1Q1 with full features

9.2 Minimum Application Diagram

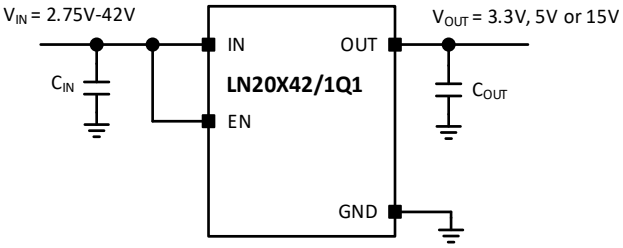


Figure 25. LN20X42/1Q1 with minimum external components

9.3 Application Considerations

9.3.1 Input and Ouput Decouple Capacitors

For control loop stabilities, LN20X42/1Q1 integrates internal compensation and only requires ceramic capacitors with minimum capacitance of 1uF between VIN and GND, and VOUT and GND, respectively. It is recommended that the capacitor is placed as close to the device pins as possible with minimum PCB trace length.

9.3.2 EN Pin

EN is the enable pin of the internal device supply and the output of the LDO. When the voltage on EN pin rises above the rising threshold V_{EN-H}, the LDO output is allowed; and when the voltage on EN falls below the falling threshold V_{EN-L}, the LDO output is disabled and the device goes into shutdown mode. Another way of using EN pin is connecting EN directly to the input voltage, the pin has the same maximum operating voltage of 42V as the LDO input.

9.3.3 OUT and FB Pins

To adjust the output voltage, connect a voltage divider between OUT and GND, and connect the center of the divider to FB pin. The steady state V_{FB} is typically at 0.6V. The output voltage can be derived from:

$$V_{OUT} = (1 + \frac{R_1}{R_2}) \times V_{FB}$$

To fully utilize the low I_Q capability of the product family, it is recommended to use resistors with tolerance better than 1%， and with temperature coefficients less than 100ppm for the divider design. A typical selection of R_2 is 1MΩ, R_1 can then be calculated from:

$$R_1 = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R_2$$

When using the fixed VOUT products, there is no external divider.

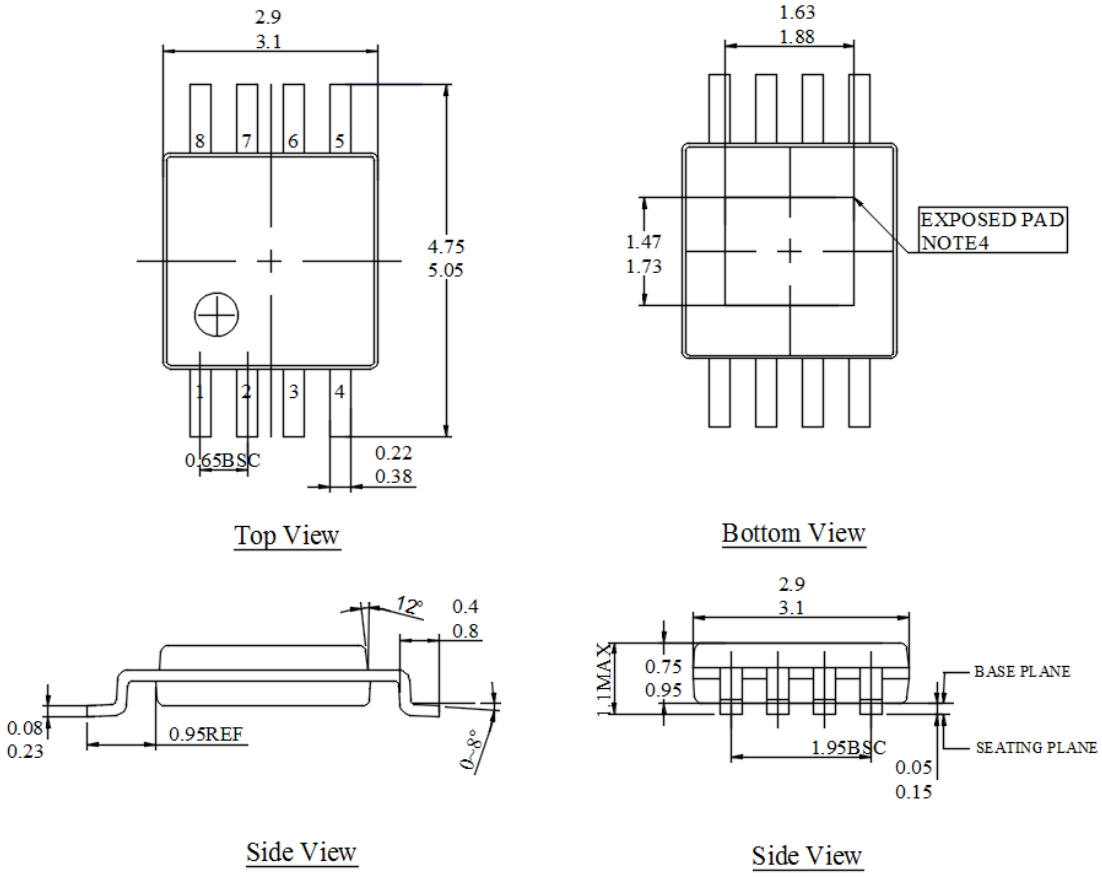
9.3.4 PG and DELAY Pins

The PG pin is connected to the open drain of an internal N-MOSFET. Externally, the PG pin needs to be pulled up to a voltage source by a resistor. The PG pin can directly drive the reset pin of a MCU. When EN is high and V_{OUT} rises above the power good threshold $V_{PG\text{-}RISE}$, the DELAY pin starts to output a current $I_{D\text{-}Charge}$ to charge the external delay capacitor, when the voltage on the DELAY pin rises across $V_{D\text{-}RISE}$， PG is pulled up. The external delay capacitor is selected based on the desired MCU delay t_{Delay} and is calculated based on:

$$C_{Delay} = \frac{I_{D-Charge} \times t_{Delay}}{V_{D-Rise}}$$

10 PACKAGE INFORMATION

10.1 Package Outline



Notes:

1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

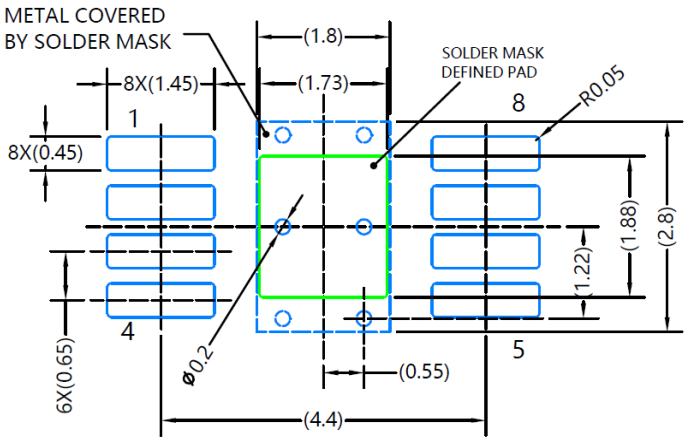
2. Both package length and width does not include mold flash.

3. Unremoved flash between leads & package end flash shall not exceed 0.15mm from bottom body per side.

4. Features may not present.

10.2 Footprint Example

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

