INA20x-Q1 Automotive Grade, –16-V to +80-V, Low- or High-Side, High-Speed, Voltage-Output, Current-Sense Amplifier With Comparator and Reference

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Current-Sense Amplifier:
  - Common-Mode Range: –16 V to +80 V
  - 3.5% Max Error Over Temperature
  - Bandwidth: 500 kHz (INA200-Q1)
  - Three Gain Options:
    - 20 V/V (INA200-Q1)
    - 50 V/V (INA201-Q1)
    - 100 V//V (INA202-Q1)
- Integrated Open-Drain Comparator
  - Latching Capability
  - 0.6-V Internal Voltage Reference
- Quiescent Current: 1800 µA (Max)
- Latch-Up Exceeds 100 mA per JESD78
- Package: VSSOP-8

2 Applications

- Electric Power Steering (EPS) Systems
- Body Control Modules
- Brake Systems
- Electronic Stability Control (ESC) Systems

3 Description

The INA200-Q1, INA201-Q1, and INA202-Q1 (INA20x-Q1) are low- or high-side current-shunt monitors with voltage output. The INA20x-Q1 devices can sense drops across shunts at common-mode voltages from –16 V to +80 V. The INA20x-Q1 are available with three output voltage scales: 20 V/V, 50 V/V, and 100 V/V, with up to a 500-kHz bandwidth.

The INA20x-Q1 also incorporate an open-drain comparator and internal reference that provides a 0.6-V threshold. External dividers set the current trip point. The comparator includes a latching capability, and can be made transparent by grounding (or leaving open) the $\overline{\text{RESET}}$ pin.

The INA20x-Q1 operate from a single 2.7-V to 18-V supply, drawing a maximum of 1800 µA of supply current. These devices are available in the very small VSSOP-8 package. Specifications for all devices extend over the operating temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA200-Q1	VSSOP (8)	3.00 mm x 3.00 mm
INA201-Q1		
INA202-Q1		

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Schematic

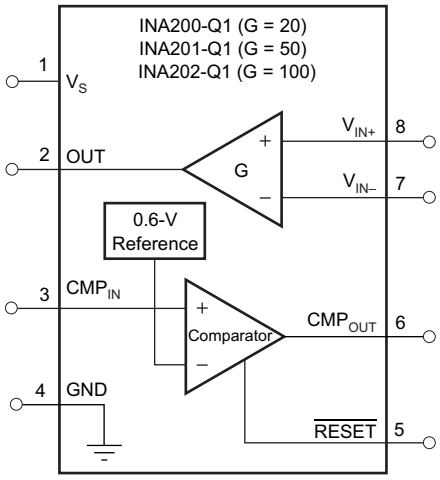


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2012) to Revision C — **Page**

- Added *Device Information* and*ESD Ratings*, and *Thermal Information* tables, and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Updated data sheet title ... 1
- Updated Features bullets for clarity ... 1
- Changed MSOP to VSSOP throughout data sheet to match industry-standard term ... 1
- Updated Applications bullets ... 1
- Updated Description section text for clarity ... 1
- Changed all figures in data sheet to show Q1 device names ... 1
- Changed pin names in Absolute Maximum Ratings to show correct names ... 4
- Added Operating Temperature to *Absolute Maximum Ratings* table ... 4
- Changed CMP V_{OUT} to CMP_{OUT} in *large-signal differential voltage gain* parameter condition ... 6
- Deleted package name from Figure 27 ... 15
- Changed Figure 28 caption ... 15
- Changed text from "R_{FILT} – 3%" to "R_{FILT} + 3%" in 2nd paragraph of *Input Filtering* section ... 15
- Changed 22-kΩ R_1 resistor to R_3 in Figure 31 ... 18

Changes from Revision A (September 2012) to Revision B — **Page**

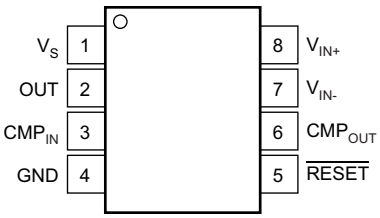
- Changed from Mixed Production status to Production Data. ... 1
- Changed device graphic from pair to single ... 1
- Added AEC-Q100 info to *Features* bullets ... 1
- Updated Applications bullets ... 1
- Removed D package from pin configuration image. ... 4

5 Device Comparison Table

DEVICE	DESCRIPTION
INA193A-Q1	Same amplifier performance as INA200-Q1 without integrated comparator
INA203-Q1	Dual comparator alternative to the INA200-Q1 single comparator
INA282-Q1	Automotive, 80-V, bidirectional, high-accuracy, low- or high-side, voltage out current shunt monitor
INA300-Q1	Automotive, 36-V, low- or high-side, overcurrent protection comparator
INA301	Overcurrent protection, high-speed, precision, current sense amplifier with integrated comparator

6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_S	Analog	Power supply
2	OUT	Analog output	Output voltage
3	CMP_{IN}	Analog input	Comparator input
4	GND	Analog	Ground
5	$\overline{RESET}$	Analog input	Comparator reset pin, active low
6	CMP_{OUT}	Analog output	Comparator output
7	$V_{IN–}$	Analog input	Negative input, connect to shunt low side
8	V_{IN+}	Analog input	Positive input, connect to shunt high side

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S		2.7	18	V
Current-shunt monitor analog inputs, V_{IN+}, V_{IN-}	Differential (V_{IN+} – V_{IN-})	–18	18	V
	Common mode(2), V_{CM} = (V_{IN+} + V_{IN-}) / 2	–16	80	V
Comparator analog input and reset pins, CMP_{IN} and $\overline{RESET}$(2)		GND – 0.3	(V_S) + 0.3	V
Analog output, OUT(2)		GND – 0.3	(V_S) + 0.3	V
Comparator output, CMP_{OUT}(2)		GND – 0.3	18	V
Input current into any pin(2)			5	mA
Operating temperature, T_A		–40	125	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This voltage may exceed the ratings shown if the current at that pin does not exceed 5 mA.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–16	12	80	V
V_S	Operating supply voltage	2.7	12	18	V
T_A	Operating free-air temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA20x-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	162.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: Current-Shunt Monitor

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{SENSE}	Full-scale sense input voltage	V_{SENSE} = V_{IN+} – $V_{IN–}$			0.15	(V_S – 0.25) / Gain	V
V_{CM}	Common-mode input range	T_A = –40°C to 125°C		–16		80	V
CMR	Common-mode rejection	V_{IN+} = –16 V to 80 V		80	100		dB
		V_{IN+} = 12 V to 80 V, T_A = –40°C to 125°C.		100	123		dB
V_{OS}	Offset voltage, RTI(1)	T_A = 25°C			±0.5	±2.5	mV
		T_A = 25°C to 125°C				±3	mV
		T_A = –40°C to 25°C				±3.5	mV
dV_{OS}/dT	Offset voltage, RTI, versus temperature	T_A = –40°C to 125°C			5		µV/°C
PSR	Offset voltage, RTI, versus power supply	V_{OUT} = 2 V, V_{IN+} = 18 V, 2.7 V, T_A = –40°C to 125°C			2.5	100	µV/V
I_B	Input bias current, $V_{IN–}$ Pin	T_A = –40°C to 125°C			±9	±16	µA
OUTPUT (V_{SENSE} ≥ 20mV)							
G	Gain	INA200-Q1			20		V/V
		INA201-Q1			50		V/V
		INA202-Q1			100		V/V
	Gain error	V_{SENSE} = 20 mV to 100 mV			±0.2%	±1%	
		V_{SENSE} = 20 mV to 100 mV, T_A = –40°C to 125°C				±2%	
	Total output error(2)	V_{SENSE} = 120 mV, V_S = 16 V			±0.75%	±2.2%	
		V_{SENSE} = 120 mV, V_S = 16 V, T_A = –40°C to 125°C				±3.5%	
	Nonlinearity error(3)	V_{SENSE} = 20 mV to 100 mV			±0.002%		
R_O	Output impedance				1.5		Ω
C_{LOAD}	Maximum capacitive load	No sustained oscillation			10		nF
OUTPUT (V_{SENSE} < 20 mV)(4)							
	Output	–16 V ≤ V_{CM} < 0 V	INA20x-Q1		300		mV
		0 V ≤ V_{CM} ≤ V_S, V_S = 5 V	INA200-Q1			0.4	V
			INA201-Q1			1	V
			INA202-Q1			2	V
		V_S < V_{CM} ≤ 80 V	INA20x-Q1		300		mV
VOLTAGE OUTPUT(5)							
	Output swing to the positive rail	$V_{IN–}$ = 11 V, V_{IN+} = 12 V, T_A = –40°C to 125°C			(V_S) – 0.15	(V_S) – 0.25	V
	Output swing to GND(6)	$V_{IN–}$ = 0 V, V_{IN+} = –0.5 V, T_A = –40°C to 125°C			(V_{GND}) + 0.004	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	C_{LOAD} = 5 pF	INA200-Q1		500		kHz
			INA201-Q1		300		kHz
			INA202-Q1		200		kHz
	Phase margin	C_{LOAD} < 10 nF			40		Degrees
SR	Slew rate				1		V/µs
	Settling time (1%)	V_{SENSE} = 10 mV_{PP} to 100 mV_{PP}, C_{LOAD} = 5 pF			2		µs
NOISE, RTI							
	Voltage noise density				40		nV/√Hz

(1) Offset is extrapolated from measurements of the output at 20 mV and 100 mV V_{SENSE}.
(2) Total output error includes effects of gain error and V_{OS}.
(3) Linearity is best fit to a straight line.
(4) For details on this region of operation, see the *Accuracy Variations* section in the *Device Functional Modes*.
(5) See Figure 7.
(6) Specified by design.

7.6 Electrical Characteristics: Comparator

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
	Threshold	T_A = 25°C	590	608	620	mV
		T_A = –40°C to 125°C	586		625	mV
	Hysteresis(1)	T_A = –40°C to 85°C		–8		mV
INPUT BIAS CURRENT(2)						
	CMP_{IN} pin			0.005	10	nA
		T_A = –40°C to 125°C			15	nA
INPUT VOLTAGE RANGE						
	CMP_{IN} pin			0 to V_S – 1.5		V
OUTPUT (OPEN-DRAIN)						
	Large-signal differential voltage gain	CMP_{OUT} = 1 V to 4 V, R_L ≥ 15 kΩ connected to 5 V		200		V/mV
I_{LKG}	High-level leakage current(3)(4)	V_{ID} = 0.4 V, V_{OH} = V_S		0.0001	1	µA
V_{OL}	Low-level output voltage(3)	V_{ID} = –0.6 V, I_{OL} = 2.35 mA		220	300	mV
RESPONSE TIME						
	Response time(5)	R_L to 5 V, C_L = 15 pF, 100-mV input step with 5-mV overdrive		1.3		µs
$\overline{\text{RESET}}$						
	$\overline{\text{RESET}}$ threshold(6)			1.1		V
	Logic input impedance			2		MΩ
	Minimum $\overline{\text{RESET}}$ pulse duration			1.5		µs
	$\overline{\text{RESET}}$ propagation delay			3		µs

(1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator; see Figure 25.
(2) Specified by design.
(3) V_{ID} refers to the differential voltage at the comparator inputs.
(4) Pulling the open-drain output to the range of 2.7 V to 18 V is permissible, regardless of V_S.
(5) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.
(6) The $\overline{\text{RESET}}$ input has an internal 2-MΩ (typical) pulldown. Leaving $\overline{\text{RESET}}$ open results in a low state, with transparent comparator operation.

7.7 Electrical Characteristics: General

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = 1 V (unless otherwise noted)

GENERAL PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current	V_{OUT} = 2 V		1350	1800	µA
		V_{SENSE} = 0 mV, T_A = –40°C to 125°C			1850	µA
	Comparator power-on reset threshold(1)			1.5		V

(1) The INA20x-Q1 devices power up with the comparator in a defined reset state as long as the $\overline{\text{RESET}}$ pin is open or grounded. The comparator is in reset as long as the power supply is below the voltage shown here. The comparator assumes a state based on the comparator input above this supply voltage. If $\overline{\text{RESET}}$ is high at power up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.

7.8 Typical Characteristics

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted)

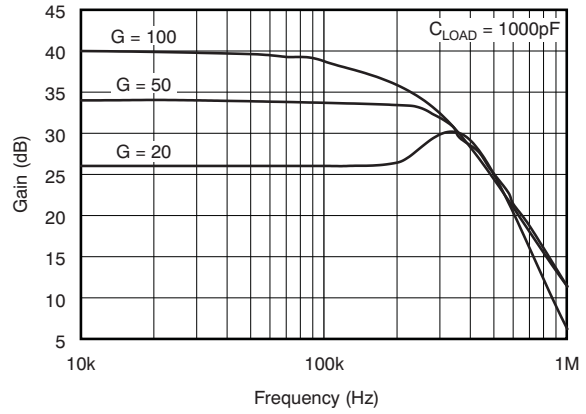


Figure 1. Gain vs Frequency

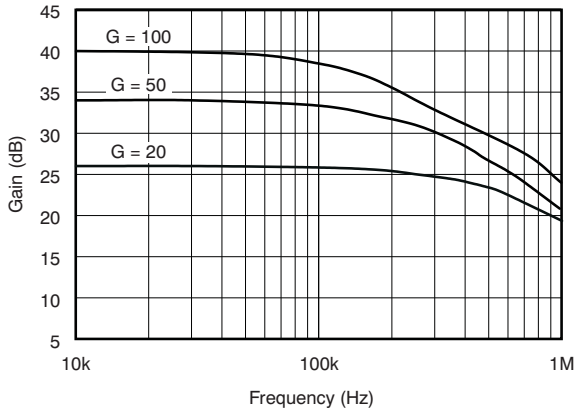


Figure 2. Gain vs Frequency

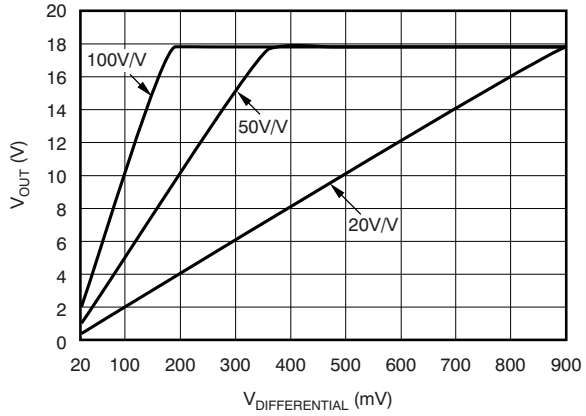


Figure 3. Gain Plot

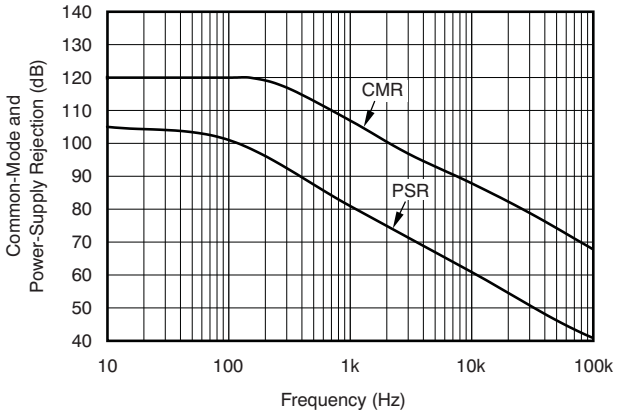


Figure 4. Common-Mode and Power-Supply Rejection vs Frequency

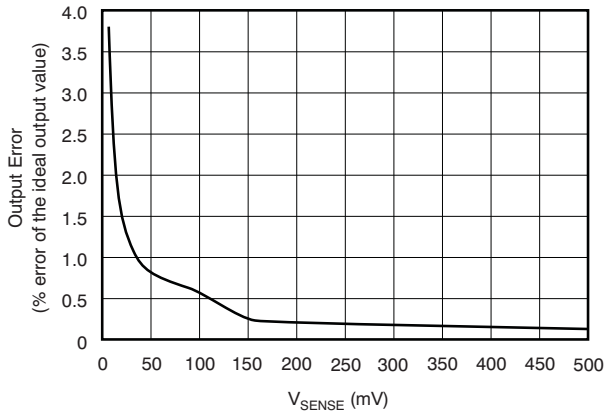


Figure 5. Output Error vs V_{SENSE}

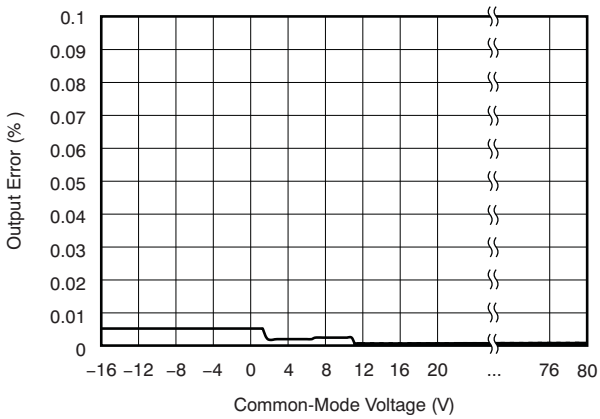


Figure 6. Output Error vs Common-Mode Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted)

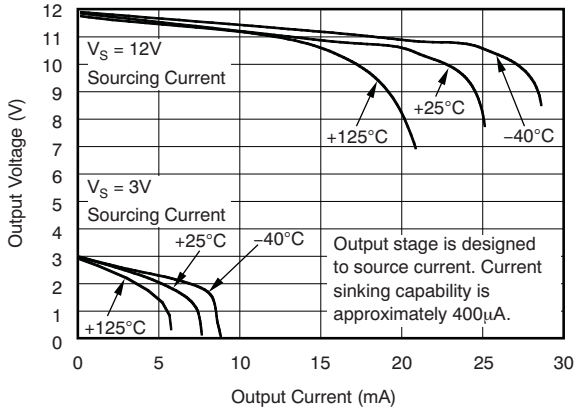


Figure 7. Positive Output Voltage Swing vs Output Current

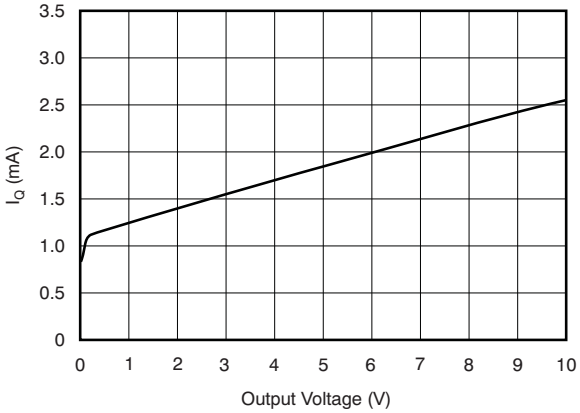


Figure 8. Quiescent Current vs Output Voltage

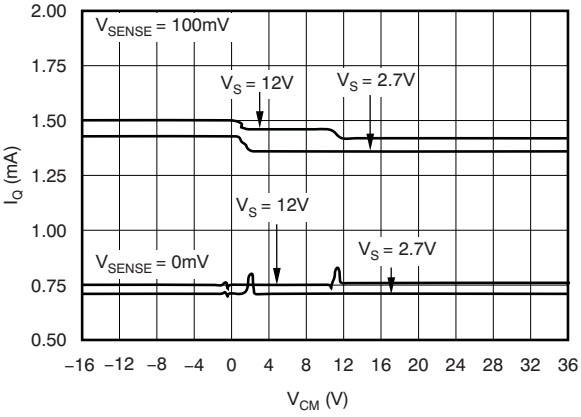


Figure 9. Quiescent Current vs Common-Mode Voltage

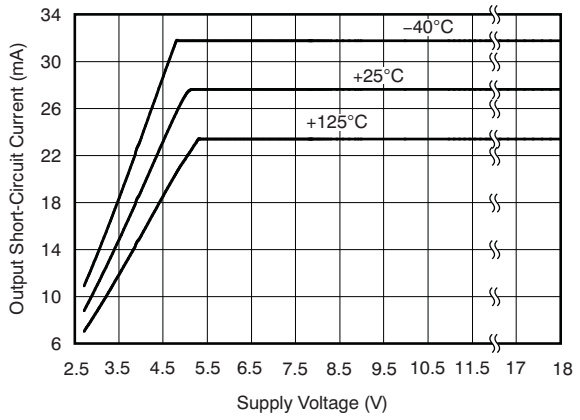


Figure 10. Output Short-Circuit Current vs Supply Voltage

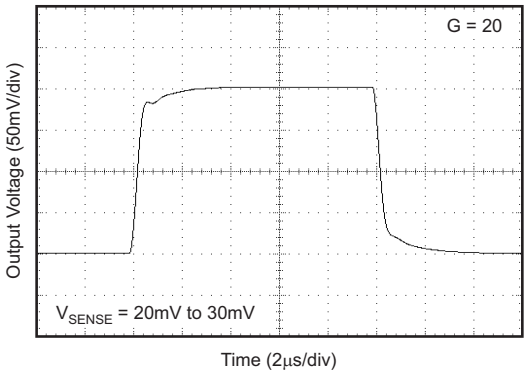


Figure 11. Step Response

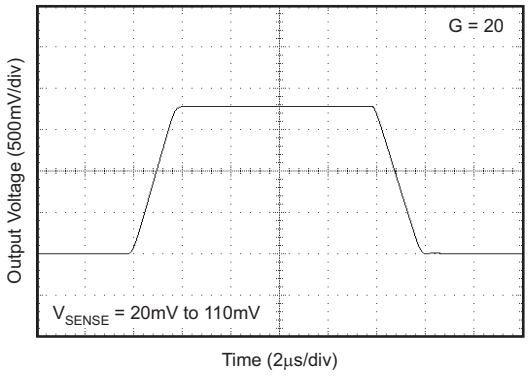


Figure 12. Step Response

Typical Characteristics (continued)

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted)

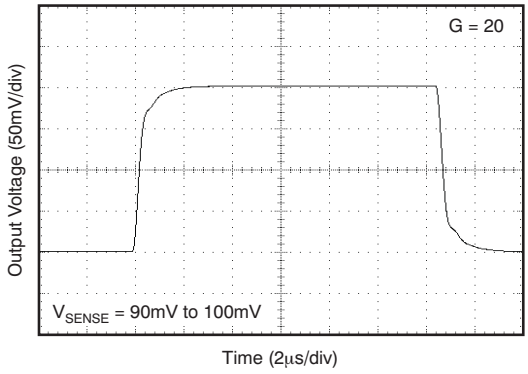


Figure 13. Step Response

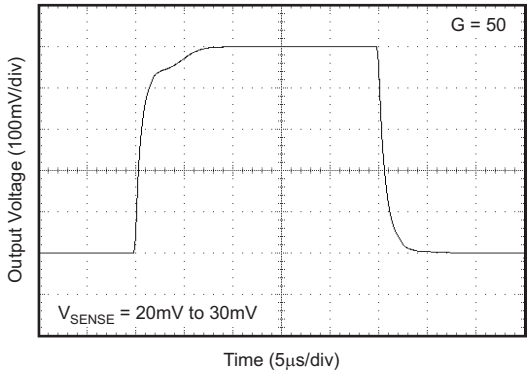


Figure 14. Step Response

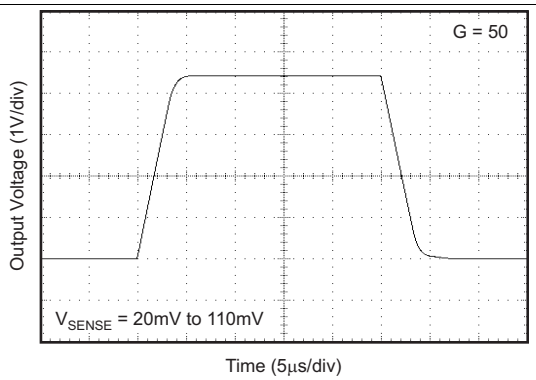


Figure 15. Step Response

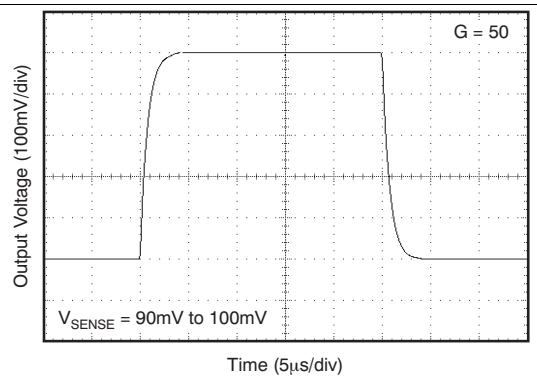


Figure 16. Step Response

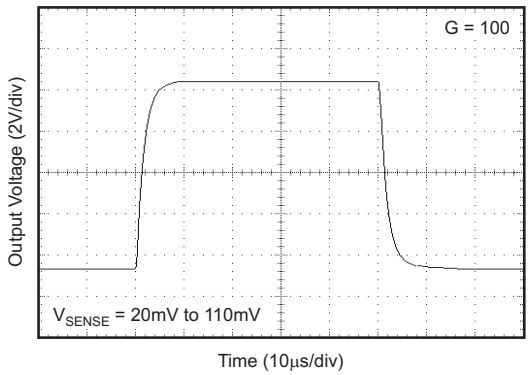


Figure 17. Step Response

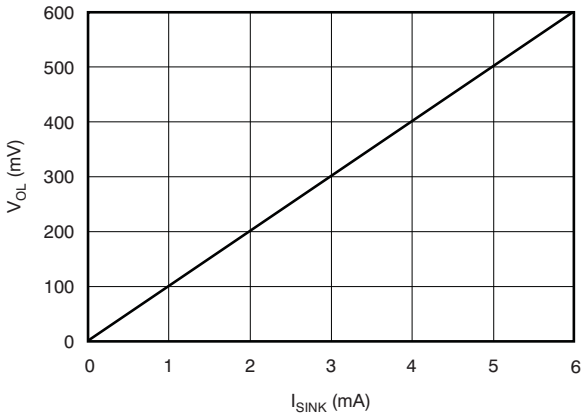


Figure 18. Comparator V_{OL} vs I_{SINK}

Typical Characteristics (continued)

At T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV (unless otherwise noted)

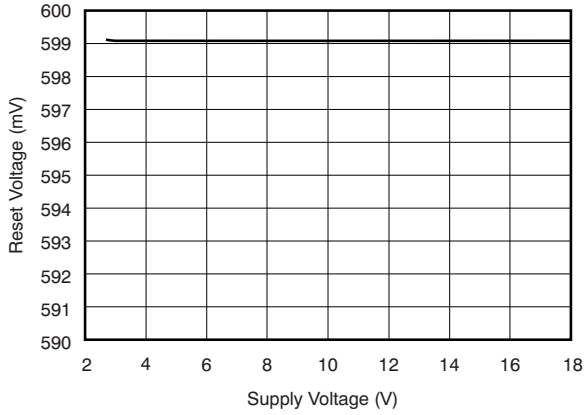


Figure 19. Comparator Trip Point vs Supply Voltage

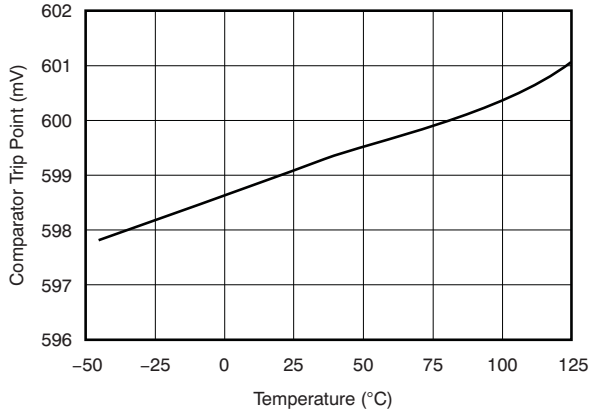


Figure 20. Comparator Trip Point vs Temperature

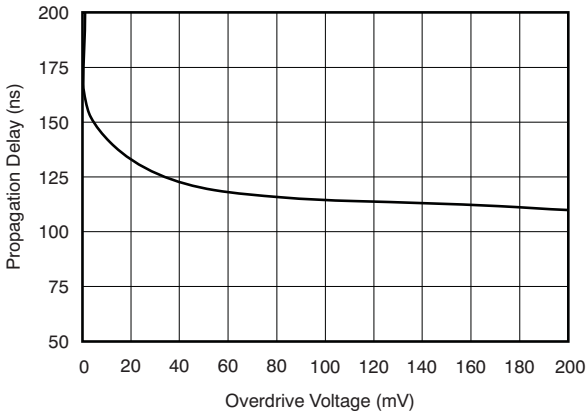


Figure 21. Comparator Propagation Delay vs Overdrive Voltage

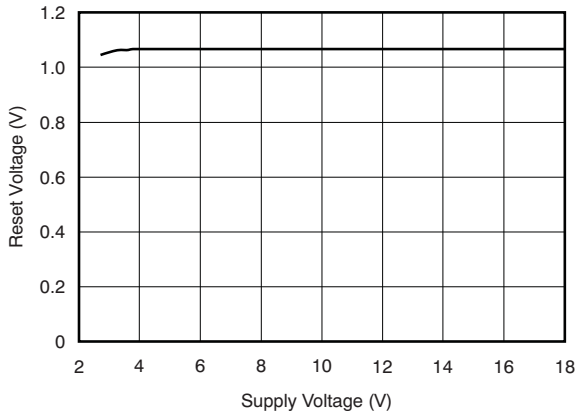


Figure 22. Comparator Reset Voltage vs Supply Voltage

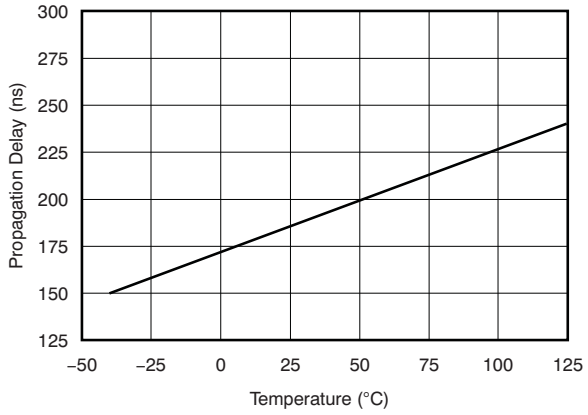


Figure 23. Comparator Propagation Delay vs Temperature

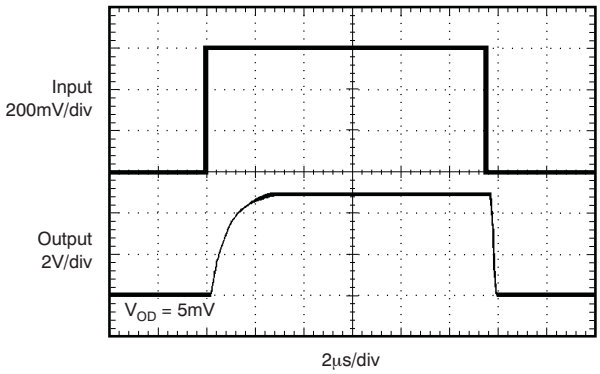


Figure 24. Comparator Propagation Delay

8 Parameter Measurement Information

8.1 Hysteresis

Figure 25 shows the typical comparator hysteresis.

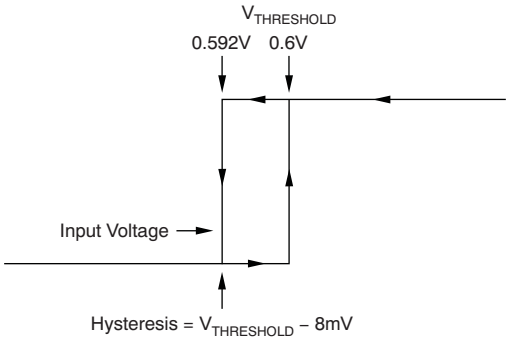


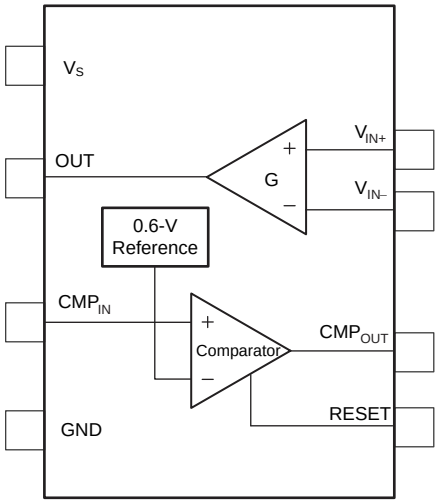
Figure 25. Typical Comparator Hysteresis

9 Detailed Description

9.1 Overview

The INA20x-Q1 current-shunt monitors operate over a wide common-mode voltage range (–16 V to +80 V). These devices integrate an open-drain comparator with an internal 0.6-V reference at the negative input. Use external dividers from the output of the current shunt monitor to the positive input of the comparator to set the positive input for overcurrent detection. The comparator includes a latching capability, but can also be made transparent by grounding (or floating) the $\overline{\text{RESET}}$ pin.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Comparator

The INA200-Q1, INA201-Q1, and INA202-Q1 devices incorporate an open-drain comparator. This comparator typically has 2 mV of offset and a 1.3 µs (typical) response time. The $\overline{\text{RESET}}$ pin latches and resets the output of the comparator; see Figure 26.

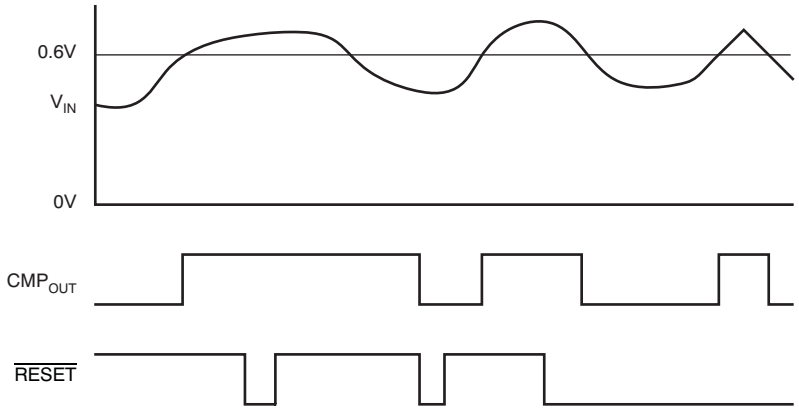


Figure 26. Comparator Latching Capability

9.3.2 Output Voltage Range

The output of the INA20x-Q1 is accurate within the output voltage swing range set by the power supply pin, V_S. Best illustration of this performance occurs when using the INA202-Q1 (gain-of-100 version), where a 100-mV full-scale input from the shunt resistor requires an output voltage swing of 10 V, and a power-supply voltage sufficient to achieve 10 V on the output.

9.4 Device Functional Modes

The INA20x-Q1 have a single functional mode and are operational when the power-supply voltage is greater than 2.7 V. The common-mode voltage must be between –16 V and +80 V. The maximum power supply voltage for the INA20x-Q1 is 18 V.

10 Application Information

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The INA20x-Q1 series is designed to enable easy configuration for detecting overcurrent conditions and current monitoring in an application. This device is individually targeted towards overcurrent detection of a single threshold. However, this device can also be paired with additional devices and circuitry to create more complex monitoring functional blocks.

10.1.1 Basic Connections

Figure 27 shows the basic connections of the INA200-Q1, INA201-Q1, and INA202-Q1. Connect the input pins, V_{IN+} and $V_{IN–}$, as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Stability requires the use of power-supply bypass capacitors. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

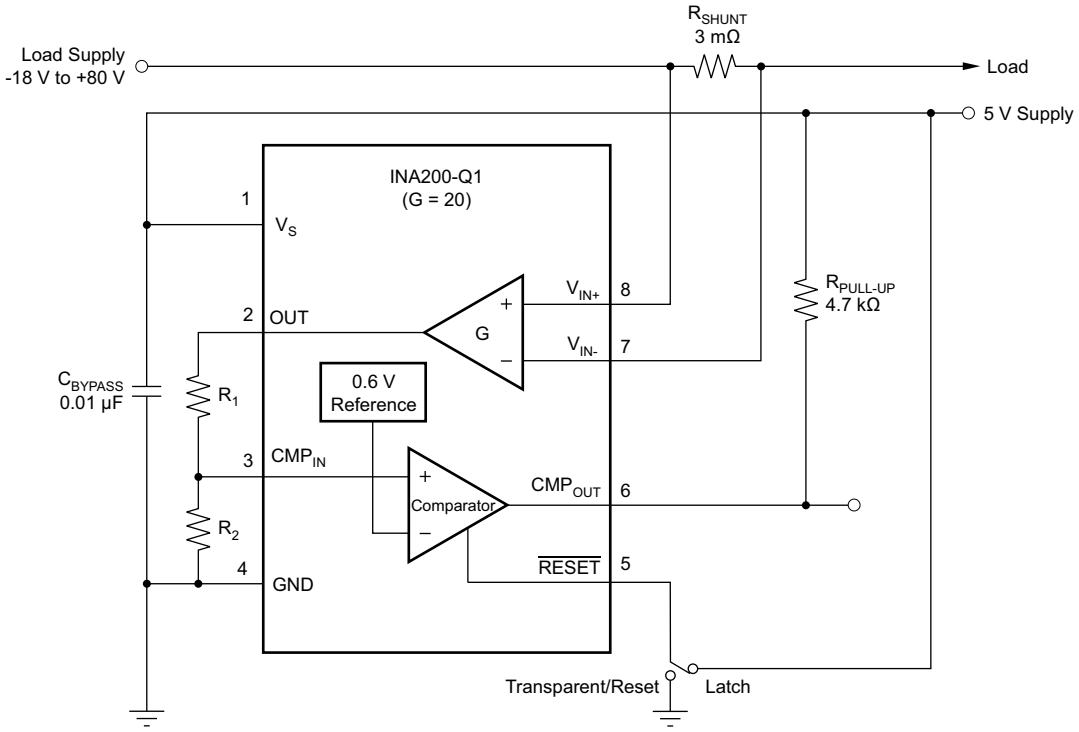


Figure 27. INA200-Q1 Basic Connections

10.1.2 Selecting R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, whereas low values of R_S minimize voltage loss in the supply line. Most applications attain best performance with an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is 500 mV, but output voltage is limited by supply.

Application Information (continued)

10.1.3 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA20x-Q1 series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA20x-Q1, but the internal 5-kΩ + 30% input impedance complicates input filtering, as illustrated in Figure 28. Use the lowest possible resistor values to minimize both the initial shift in gain and effects of tolerance. Equation 1 gives the effect on initial gain:

$$\text{Gain Error \%} = 100 - \left(100 \times \frac{5\text{k}\Omega}{5\text{k}\Omega + R_{FILT}}\right) \quad (1)$$

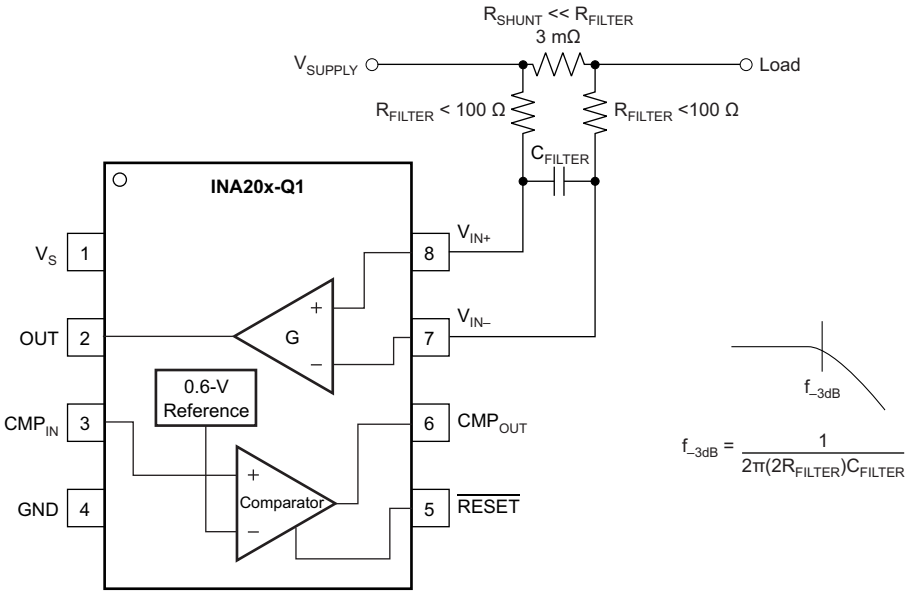


Figure 28. Input Filter

To calculate the total effect on gain error, replace the 5-kΩ term with 5 kΩ – 30%, (or 3.5 kΩ) or 5 kΩ + 30% (or 6.5 kΩ). One can also be insert the tolerance extremes of R_{FILT} into the equation. If using a pair of 100-Ω 1% resistors on the inputs, the initial gain error is 1.96%. Worst-case tolerance conditions always occur at the lower excursion of the internal 5-kΩ resistor (3.5-kΩ), and the higher excursion of R_{FILT} + 3% in this case.

Note that one must then combine the specified accuracy of the INA20x-Q1 in addition to these tolerances. Although this discussion treated worst-case accuracy conditions by combining the extremes of the resistor values, it is appropriate to use geometric-mean or root-sum-square calculations to total the effects of accuracy variations.

10.1.4 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA20x-Q1 current-shunt monitors is a function of two main variables: V_{SENSE} (V_{IN+} – $V_{IN–}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. The expression for V_{CM} is (V_{IN+} + $V_{IN–}$) / 2; however, in practice, V_{CM} is effectively the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
- Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $-16\text{ V} \leq V_{CM} < 0$
- Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\text{V} \leq V_{CM} \leq V_S$
- Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Application Information (continued)

10.1.4.1 Normal Case 1: V_{SENSE} ≥ 20 mV, V_{CM} ≥ V_S

This region of operation provides the highest accuracy. Here, use of a two-step method characterizes and measures the input offset voltage. First, Equation 2 determines the gain.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100mV - 20mV} \quad (2)$$

where:

V_{OUT1} = output voltage with V_{SENSE} = 100 mV

V_{OUT2} = output voltage with V_{SENSE} = 20 mV

Then the offset voltage is measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current shunt monitor, as shown in Equation 3.

$$V_{OS}\text{RTI (Referred-To-Input)} = \left[\frac{V_{OUT1}}{G}\right] - 100mV \quad (3)$$

In the *Typical Characteristics*, Figure 6 (*Output Error versus Common-Mode Voltage* curve) shows the highest accuracy for the this region of operation. In this plot, V_S = 12 V; for V_{CM} ≥ 12 V, the output error is at its minimum. Using this case also creates the V_{SENSE} ≥ 20 mV output specifications in the *Electrical Characteristics: Current-Shunt Monitor* table.

10.1.4.2 Normal Case 2: V_{SENSE} ≥ 20 mV, V_{CM} < V_S

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the Figure 6 *(Output Error versus Common-Mode Voltage* curve). As noted, for this graph V_S = 12 V; for V_{CM} < 12 V, the output error increases as V_{CM} becomes less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

10.1.4.3 Low V_{SENSE} Case 1: V_{SENSE} < 20 mV, –16 V ≤ V_{CM} < 0 V; and Low V_{SENSE} Case 3: V_{SENSE} < 20 mV, V_S < V_{CM} ≤ 80 V

Although not designed for accurate operation in either of these regions, the INA20x-Q1 family of devices may have exposure to these conditions in some applications. For example, when monitoring power supplies being switched on and off with V_S still applied to the INA20x-Q1, it is important to know what the device behavior is in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 300 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy, as specified in the *Electrical Characteristics: Current-Shunt Monitor*. Figure 29 illustrates this effect using the INA202-Q1 (gain = 100).

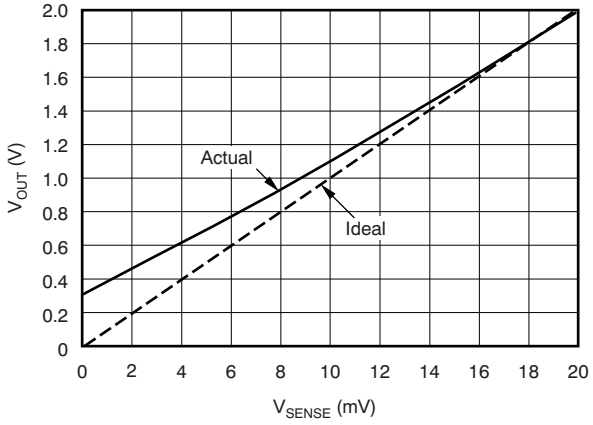
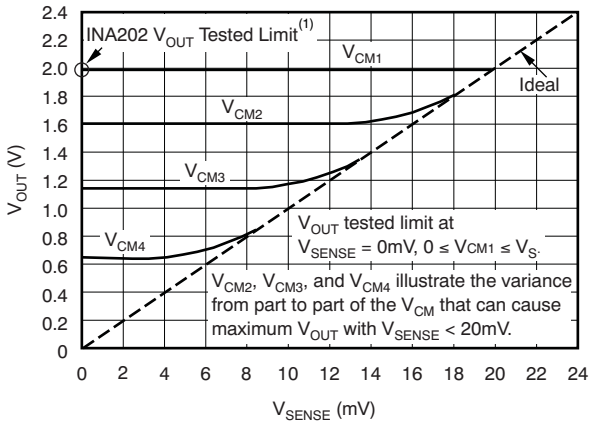


Figure 29. Example for Low V_{SENSE} Cases 1 and 3 (INA202-Q1, Gain = 100)

Application Information (continued)

10.1.4.4 Low V_{SENSE} Case 2: V_{SENSE} < 20 mV, 0 V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA20x-Q1 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive-input common-mode voltage range, and the other in the negative-input region. For this case, neither of these two internal amplifiers dominates, and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for *normal case 2*. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer to that described by *normal case 2*. Figure 30 illustrates this behavior for the INA202-Q1. To test the V_{OUT} maximum peak for this case, maintain a constant V_S, set V_{SENSE} = 0 mV, and sweep V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this test varies from part to part, but the tested V_{OUT} maximum peak for any part is less than the specified V_{OUT} test limit.



NOTE: (1) INA200 V_{OUT} Tested Limit = 0.4V. INA201 V_{OUT} Tested Limit = 1V.

Figure 30. Example for Low V_{SENSE} Case 2 (INA202-Q1, Gain = 100)

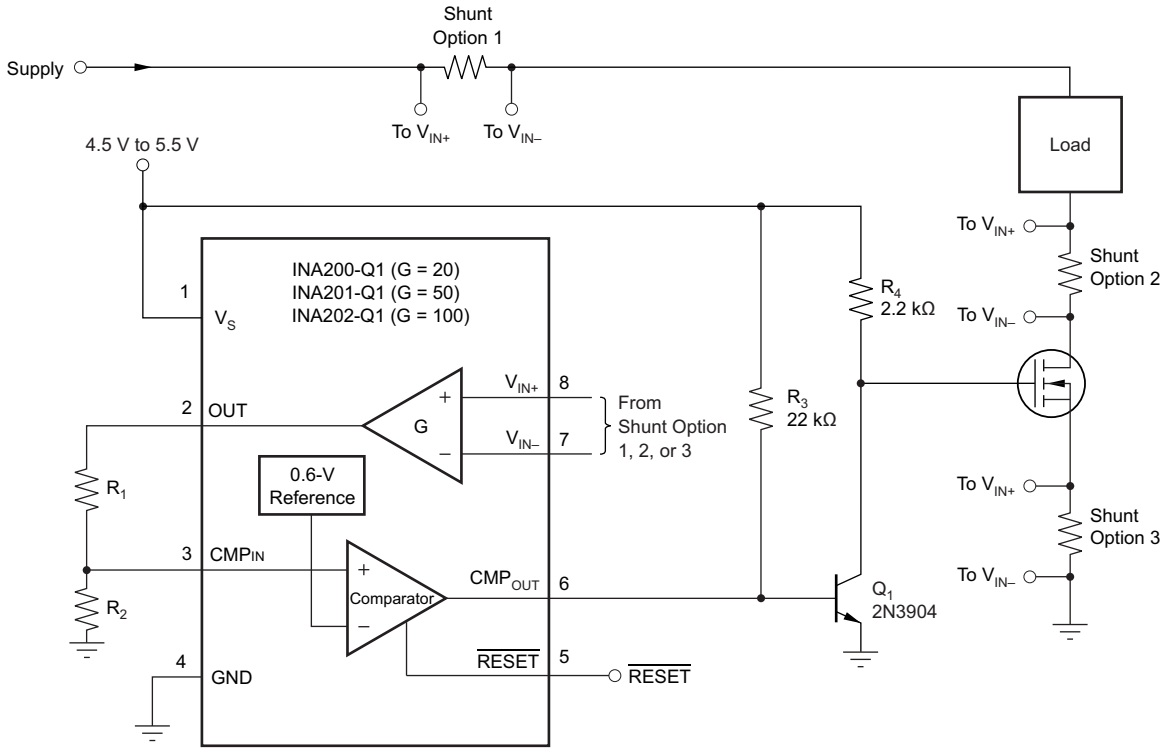
10.1.5 Transient Protection

The –16-V to +80-V common-mode range of the INA20X-Q1 is ideal for withstanding automotive fault conditions, ranging from 12-V battery reversal up to 80-V transients, because there is need for additional protective components up to those levels. In the event that the INA20x-Q1 are exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (such as Zeners) is necessary. Do not use metal-oxide varistors (MOVs) or voltage-dependent resistors (VDRs) except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it never allows exposure of the INA20X-Q1 to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage due to transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA20x-Q1 do not lend themselves to using external resistors in series with the inputs, because the internal gain resistors can vary up to ±30%. (If gain accuracy is not important, then one can add resistors in series with the INA20x-Q1 inputs with two equal resistors on each input.)

10.2 Typical Applications

10.2.1 Low-Side Switch Overcurrent Shutdown

The INA20x-Q1 measures current through a resistive shunt with current flowing in one direction, thus enabling detection of an overcurrent event only when the differential input voltage exceeds the threshold limit. When the current reaches the set limit of the divider R_1 / R_2, the output of CMP_{OUT} transitions high and Q1 turns on and pull the gate of the Pass-FET low and turn off the flow off current.



NOTE: In this case, Q1 is used to invert the comparator output.

Figure 31. Low-Side Switch Overcurrent Shutdown

10.2.1.1 Design Requirements

For this design example, use the input parameters shown in Table 1. All other register settings are default.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, V_S	3.3 V
R_2 / R_1	1.5
R2	15 kΩ
R1	10 kΩ
Gain	20 V/V (INA200-Q1)
Shunt resistor, R_{SHUNT}	5 mΩ
Desired trip current, I_{TRIP}	1 A

10.2.1.2 Detailed Design Procedure

Figure 31 shows the basic connections for a low-side, switch overcurrent shutdown application. Connect input pins IN+ and IN– as close as possible to the current-sensing resistor (R_{SHUNT}) to minimize any resistance in series with the shunt resistance. Additional resistance between the current-sensing resistor and input pins can result in errors in the measurement. When input current flows through this external input resistance, the voltage developed across the shunt resistor can differ from the voltage reaching the input pins. Connect the input pins to one of the three shunt options shown in Figure 31.

Use the device gain and shunt resistor value to calculate the OUT pin voltage, V_{OUT_TRIP}, for the desired trip current, as shown in Equation 4:

$$V_{OUT_TRIP} = I_{TRIP} \times R_{SHUNT} \times \text{Gain} \quad (4)$$

where

- I_{TRIP} = Desired trip current
- R_{SHUNT} = Shunt resistor value

Configure R_1 and R_2 so that the current trip point is equal to the 0.6-V reference voltage, as shown in Equation 5:

$$(R_2 / (R_1 + R_2) \times V_{OUT_TRIP} = 0.6\ V \quad (5)$$

10.2.1.3 Application Curves

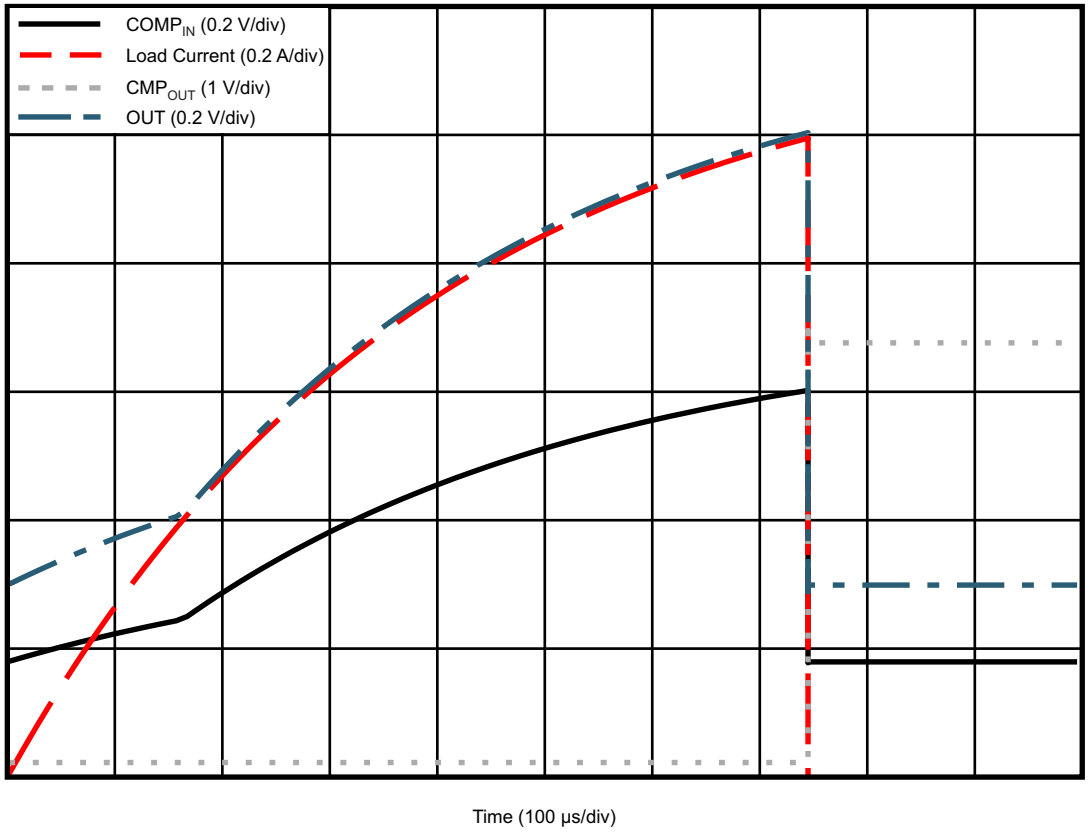
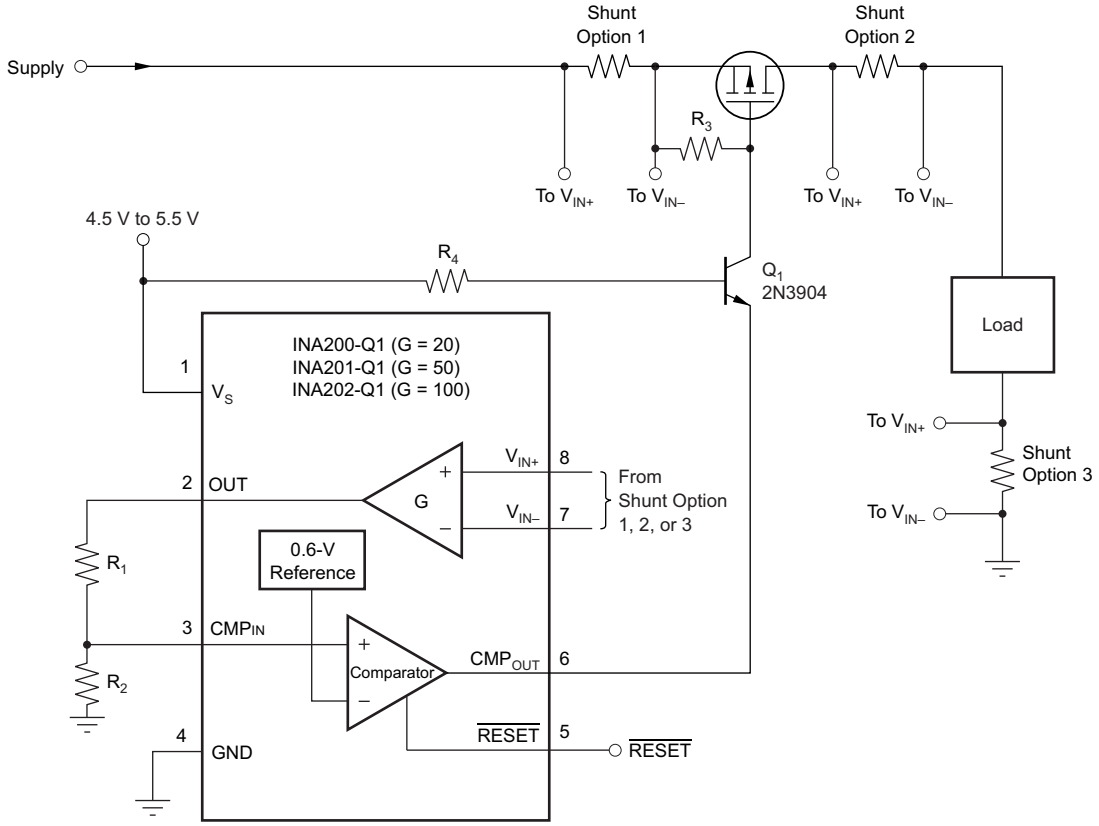


Figure 32. Low-Side Switch Overcurrent Shutdown Response

10.2.2 High-Side Switch Overcurrent Shutdown

Figure 33 shows the basic connection for a high-side, switch overcurrent shutdown application. The high-side PMOS switch disconnects when an overcurrent event occurs. The previous *Detailed Design Procedure* section describes how to apply this application example. The difference is that the current is sensed on the high side of the bus in this application, and the low side of the bus in the previous application example.

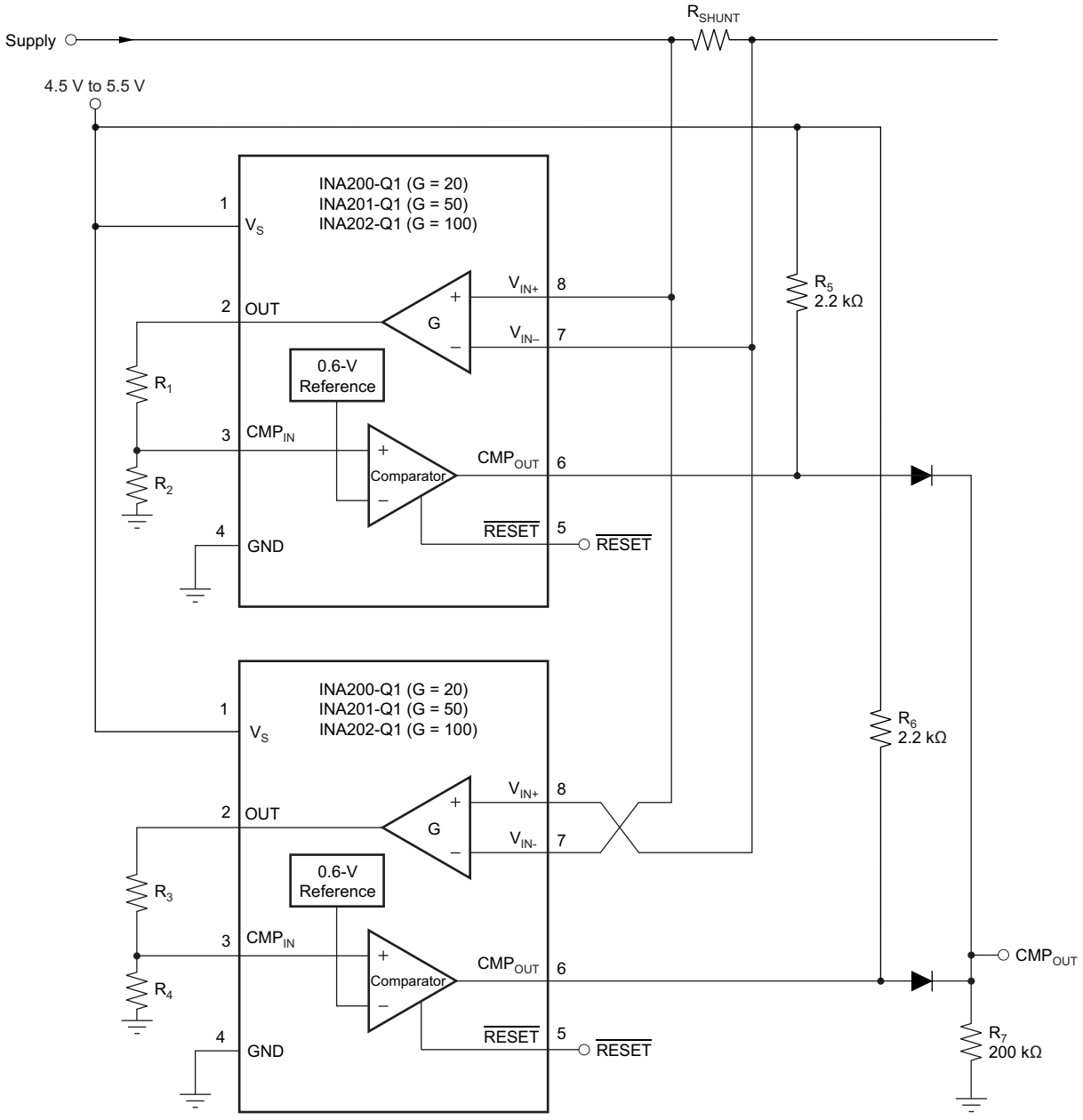


NOTE: Q cascodes the comparator output to drive a high-side FET (the 2N3904 shown is good up to 60 V). The shunt can be located in any one of the three locations shown. Use the latching capability in shutdown applications to prevent oscillation at the trip point.

Figure 33. High-Side Switch Overcurrent Shutdown

10.2.3 Bidirectional Overcurrent Comparator

Figure 34 shows the basic connection for a bidirectional overcurrent comparator using two INA20x-Q1 devices of the same gain.



NOTE: It is possible to set different limits for each direction.

Figure 34. Bidirectional Overcurrent Comparator

11 Power Supply Recommendations

The input circuitry of the INA20x-Q1 accurately measures beyond the power-supply voltage, V_S. For example, the V_S power supply can be 5 V, whereas the load power-supply voltage goes up to 80 V. However, the voltages on the power-supply pins limit the output voltage range of the OUT pin.

12 Layout

12.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or four-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Add additional decoupling capacitance to compensate for noisy or high-impedance power supplies.

12.2 Layout Example

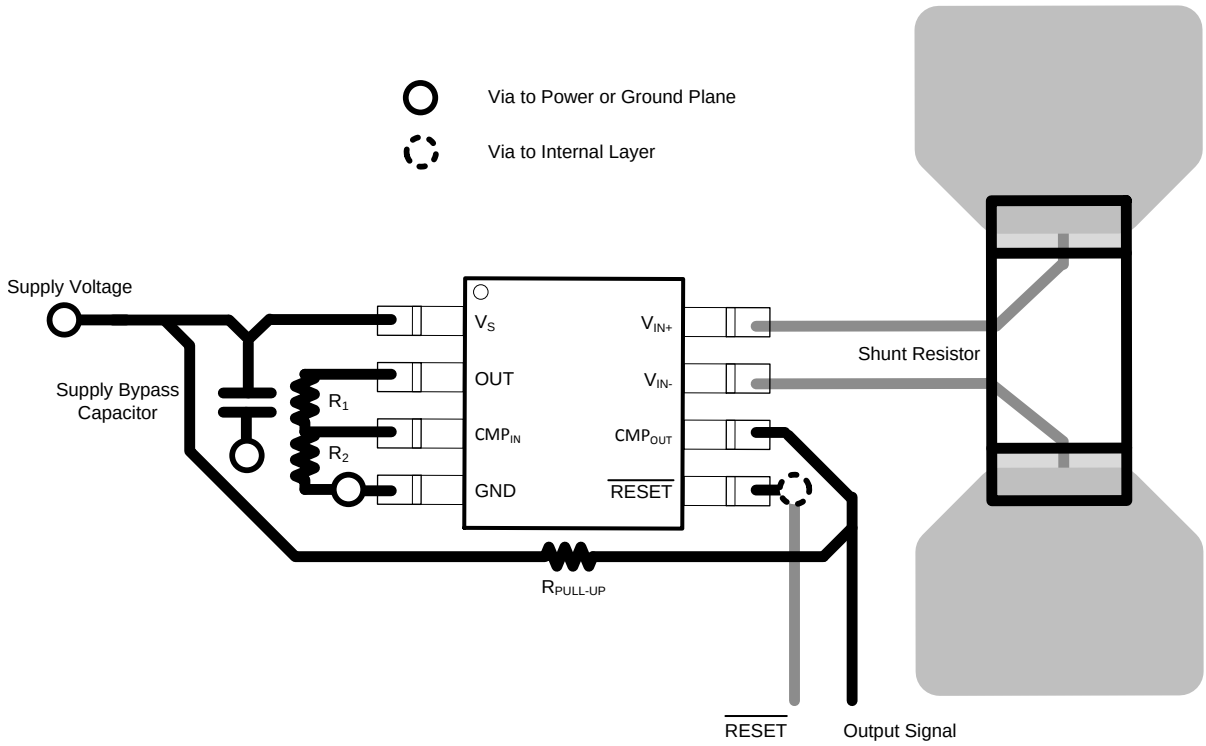


Figure 35. INA20x-Q1 Layout Example

13 Device and Documentation Support

13.1 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA200-Q1	Click here	Click here	Click here	Click here	Click here
INA201-Q1	Click here	Click here	Click here	Click here	Click here
INA202-Q1	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA200AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHZ	Samples
INA201AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QWV	Samples
INA202AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SIA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA200-Q1, INA201-Q1, INA202-Q1 :

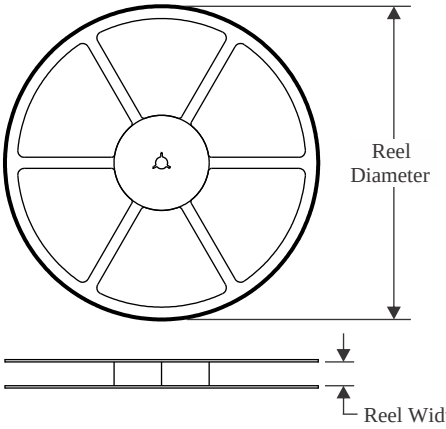
- Catalog: INA200, INA201, INA202

NOTE: Qualified Version Definitions:

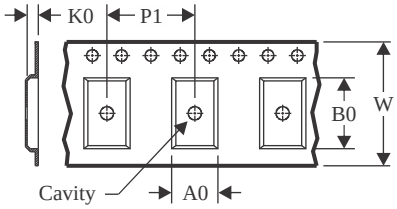
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

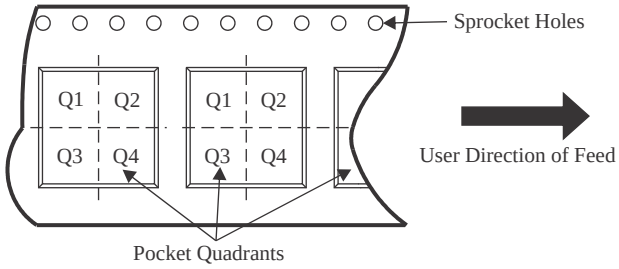


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



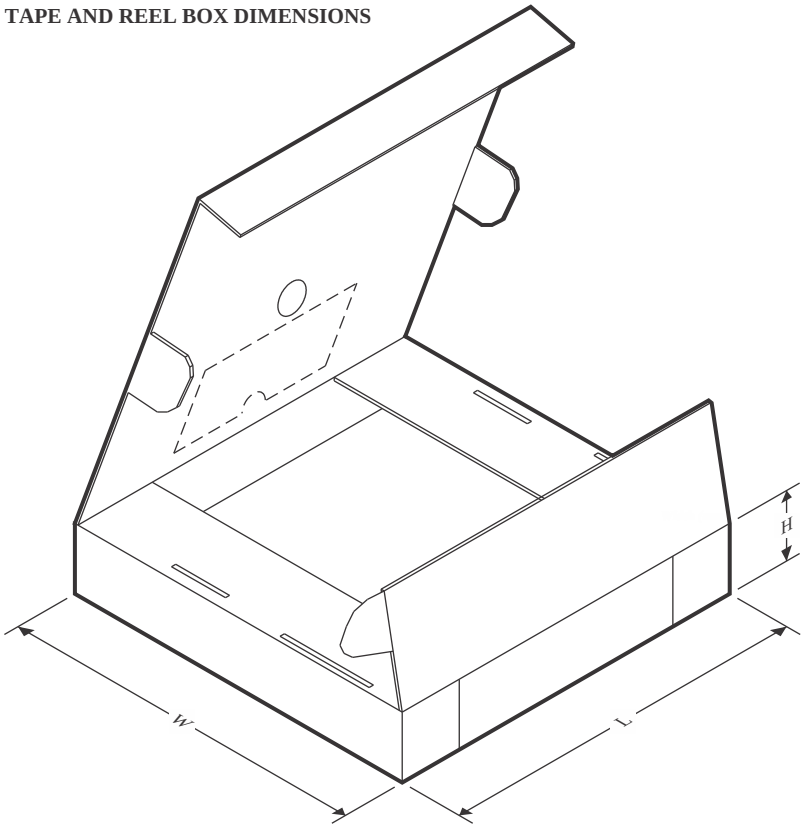
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA200AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA201AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA202AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

9-Aug-2022

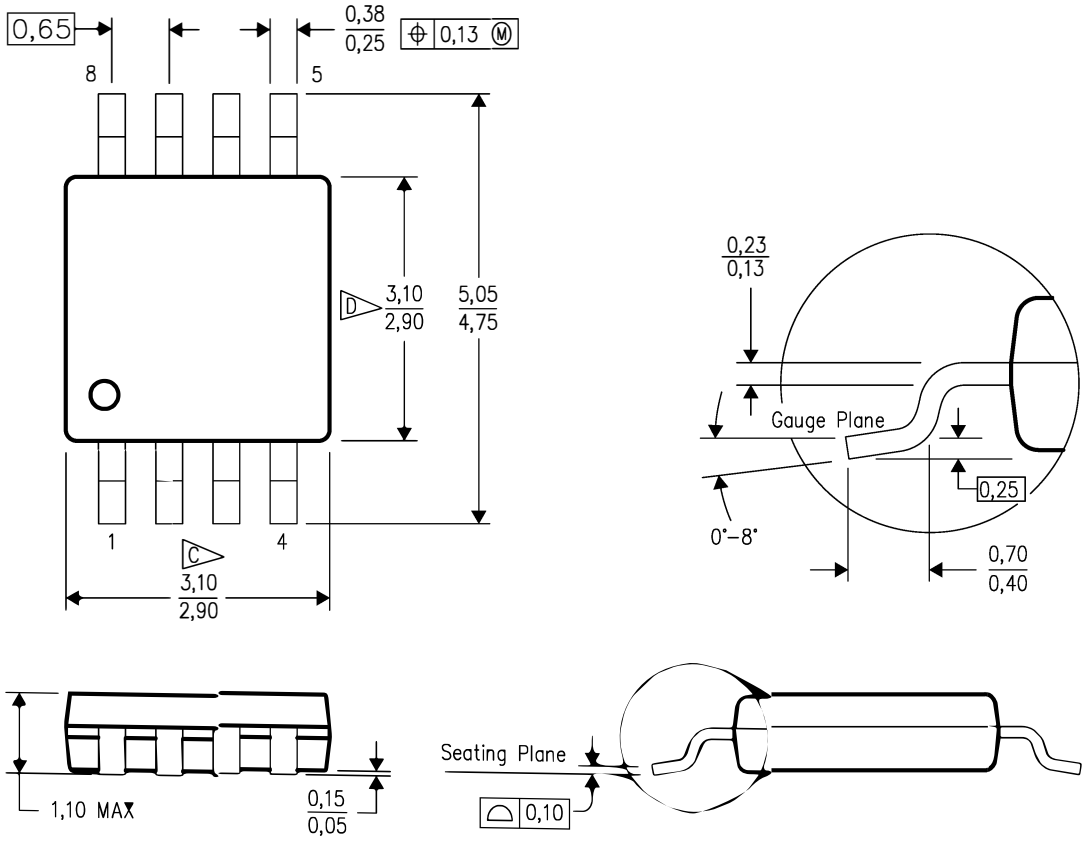
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA200AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA201AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA202AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

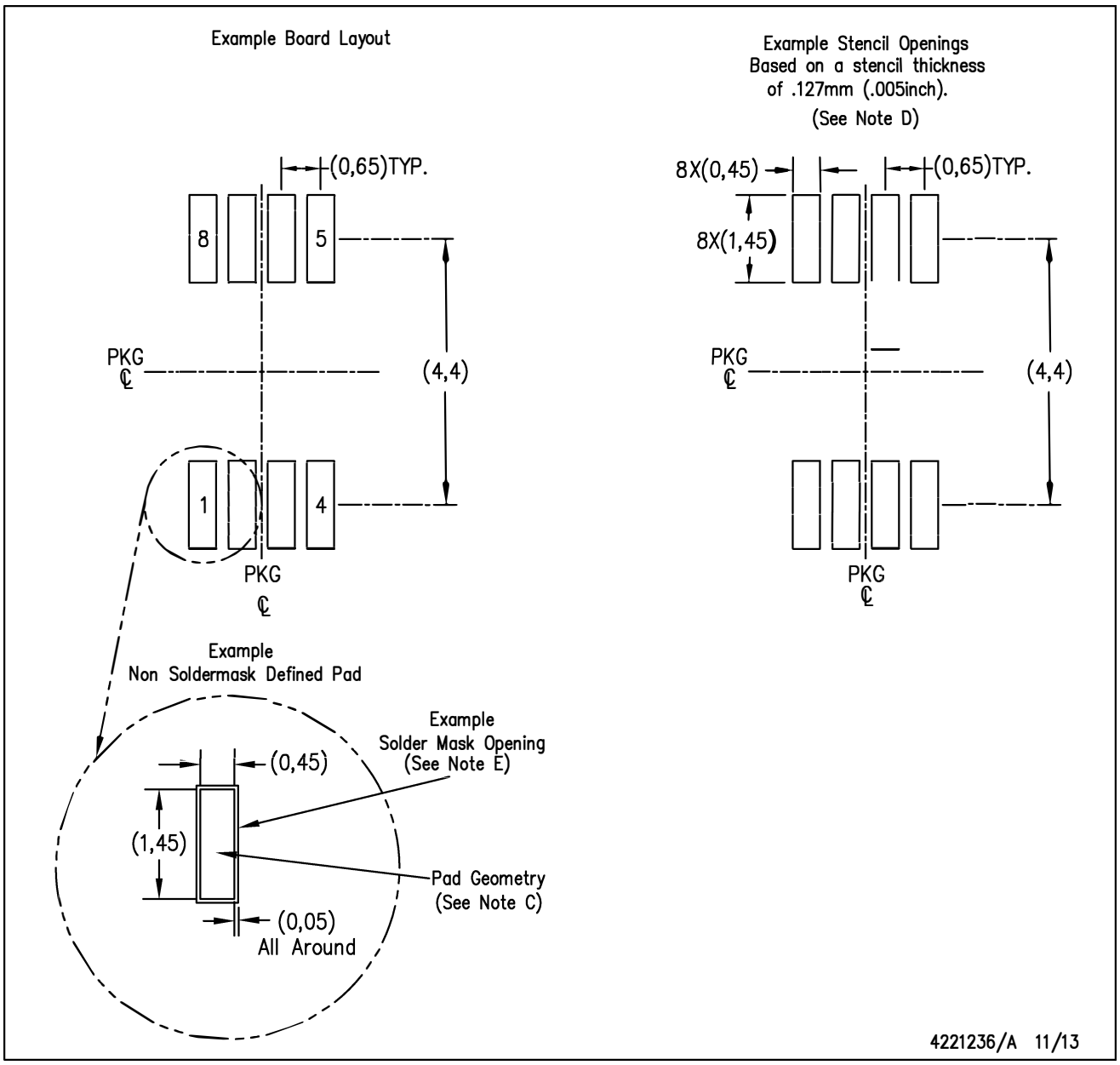
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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