CD1030

33-channel multiple switch detection interface with programmable wetting current

Rev. 6.0 — 20 August 2024 **Product data sheet**

1 General description

The CD1030 is designed to detect the closing and opening of up to 33 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). This SMARTMOS device also features a 35-to-1 analog multiplexer for reading the input channels as analog inputs. The analog selected input signal is buffered and provided on the AMUX output pin for the MCU to read.

Independent programmable wetting currents are available as needed for the application. A battery and temperature monitor are included in the IC and available via the AMUX pin.

The CD1030 device has several modes of operation: Normal mode, Low-power mode (LPM), and Polling mode. Normal mode allows programming of the device and supplies switch contacts with pullup or pulldown current as it monitors the change of state on the switches. The LPM provides low quiescent current, which makes the CD1030 ideal for automotive and industrial products requiring low sleep-state currents. Polling mode periodically interrogates the input pins to determine the state the pins are in, and to decide whether there was a change of state from Normal mode.

2 Features and benefits

- Fully functional operation from 4.5 V to 36 V
- Full parametric operation from 6.0 V to 28 V
- Low-power mode current I_{BATP} = 50 µA and I_{DDQ} = 10 µA
- 33 switch detection channels
  - 21 switch-to-Ground (SG) inputs with configurable pull-up current sources
  - 12 programmable switch (SP) inputs
    - Switch-to-Ground (SG) or Switch-to-Battery (SB)
  - Operating switch input voltage range from -1.0 V to 36 V
  - Selectable wetting current (2.0, 6.0, 8.0, 10, 12, 14, 16, or 20 mA)
  - Programmable wetting operation (Pulse or continuous)
  - Selectable wake-up on change of state
- 35 to 1 Analog Multiplexer
  - Buffered AMUX output from SG/SP channels
  - Integrated divider by six on SG5 for battery voltage sensing
  - Integrated die temperature sensing through AMUX output
  - Optional two or three pin hardwire AMUX selection
- Active interrupt (INT_B) on switch's change of state
- Direct MCU Interface through 3.3 V / 5.0 V SPI protocol

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3 Ordering information

This section describes the part numbers available to be purchased along with their differences.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Notes
MC33CD1030AE	-40 °C to 125 °C	LQFP 48 pins	(1)

Notes
1. To order parts in tape and reel, add the R2 suffix to the part number.

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4 Functional block diagram

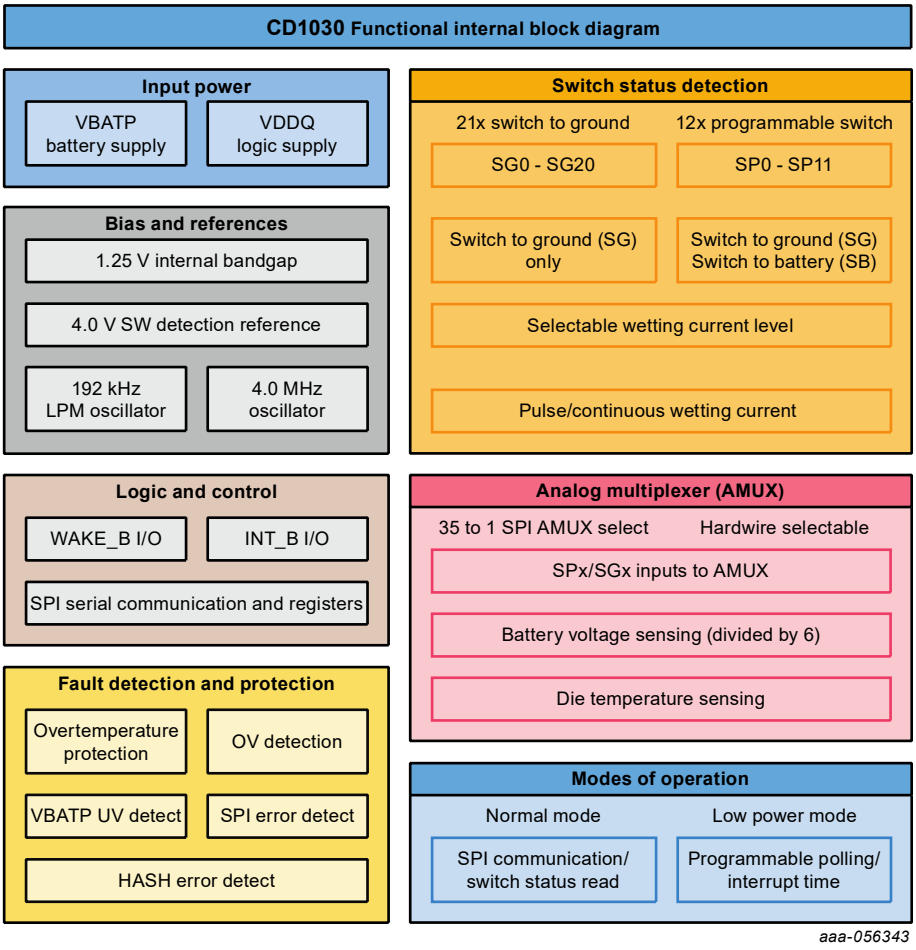


Figure 1. Functional block diagram

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5 Internal block diagram

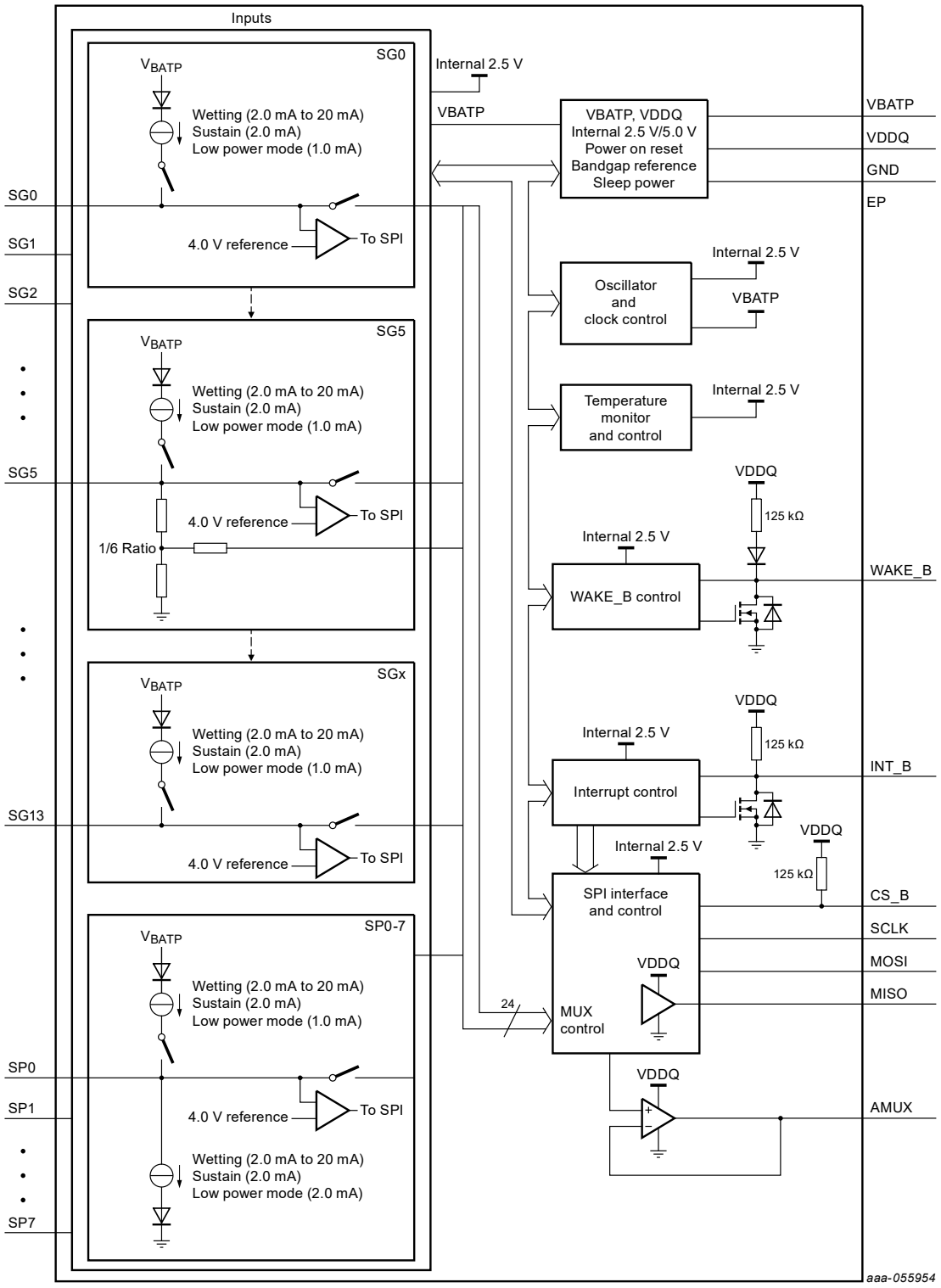


Figure 2. CD1030 internal block diagram

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6 Pinning information

6.1 Pinout

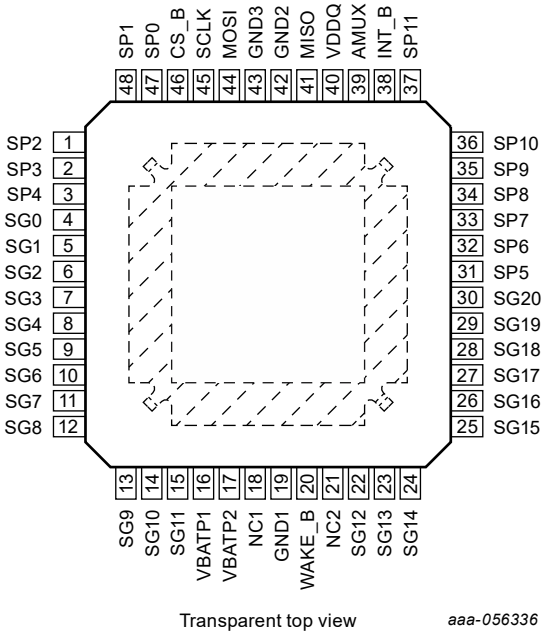


Figure 3. CD1030 LQFP-48 package pinout

6.2 Pin definitions

Table 2. CD1030 pin definitions

Pin number	Pin name	Function	Formal name	Definition
1 - 3 47 48	SP2 - SP4 SP0 SP1	Input	Programmable Switches 0 – 4	Switch to programmable input pins (SB or SG)
4 - 15	SG0 - SG11	Input	Switch-to-Ground Inputs 0 – 11	Switch-to-ground input pins
18	NC1	-	Not Connect	Not connect
19	GND1	Ground	Ground	Ground for logic, analog
20	WAKE_B	Input/ Output	Wake-up	Open drain wake-up output. Designed to control a power supply enable pin. Input used to allow a wake-up from an external event.
21	NC2	-	Not Connect	Not connect
22 - 30	SG12 - SG20	Input	Switch-to-Ground Inputs 12– 20	Switch-to-ground input pins
31 - 37	SP5 - SP11	Input	Programmable Switches 5 – 11	Switch to programmable input pins (SB or SG)
38	INT_B	Input/ Output	Interrupt	Open-drain output to MCU. Used to indicate an input switch change of state. Used as an input to allow wake-up from LPM via an external INT_B falling event.

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Table 2. CD1030 pin definitions*...continued*

Pin number	Pin name	Function	Formal name	Definition
39	AMUX	Output	Analog Multiplex Output	Analog multiplex output.
40	VDDQ	Input	Voltage Drain Supply	3.3 V/ 5.0 V supply. Sets SPI communication level for the MISO driver and I/O level buffer
41	MISO	Output/SPI	SPI Secondary Out	Provides digital data from the CD1030 to the MCU
44	MOSI	Input/SPI	SPI Secondary In	SPI control data input pin from the MCU
45	SCLK	Input/SPI	Serial Clock	SPI control clock input pin
46	CS_B	Input/SPI	Chip Select	SPI control chip select input pin
16 17	VBATP1 VBATP2	Power	Battery Input	Battery supply input pin. Pin requires external reverse battery protection
42 43	GND2 GND3	Ground	Ground	Ground for logic, analog
EP	EP	Ground	Exposed Pad	It is recommended to terminated the exposed pad to GND and system ground.

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7 General IC functional description

The CD1030 device interacts with many connections outside the module and near the end user. The IC detects changes in switch state and reports the information to the MCU via the SPI protocol. The input pins generally connected to switches located outside the module and in proximity to battery in car harnesses. Consequently, the IC must have some external protection including an ESD capacitor and series resistors, to ensure the energy from the various pulses are limited at the IC.

The IC requires a blocking diode be used on the VBATP pin to protect from a reverse battery condition. The inputs are capable of surviving reverse battery without a blocking diode and also contain an internal blocking diode from the input to the power supply (V_{BATP}). This ensures there is no back feeding of voltage/current into the IC, when the voltage on the input is higher than the VBATP pin.

7.1 Battery voltage ranges

The CD1030 device operates from 4.5 V ≤ V_{BATP} ≤ 36 V and is capable of withstanding up to 40 V. The IC operates functionally from 4.5 V < V_{BATP} < 6.0 V, but with degraded parametrics values. Voltages in excess of 40 V must be clamped externally to protect the IC from destruction. The VBATP pin must be isolated from the main battery node by a diode.

7.1.1 Load dump (overvoltage)

During load dump the CD1030 operates properly up to the V_{BATP} overvoltage. Voltages greater than load dump (~32 V) causes the current sources to be limited to ~2.0 mA, but the register values are maintained. Upon leaving this overvoltage condition, the original setup is returned and normal operation begins again.

7.1.2 Jump start (double battery)

During a jump start (double battery) condition, the device must functions normally and meets all the specified parametric values. No internal faults are set and no abnormal operation noted as a result of operating in this range.

7.1.3 Normal battery range

The normal voltage range is fully functional with all parametrics in the given specification.

7.1.4 Low voltage range (degraded parametrics)

In the V_{BATP} range between 4.5 V to 6.0 V the CD1030 functions normally, but has some degraded parametric values. The SPI functions normally with no false reporting. The degraded parameters are noted in Table 7 and Table 8. During this condition, the input comparator threshold is reduced from 4.0 V and remain ratiometrically adjusted, according to the battery level.

7.1.5 Undervoltage lockout

During undervoltage lockout, the MISO output is tristated to avoid any data from being transmitted from the CD1030. Any CS_B pulses are ignored in this voltage range. If the battery enters this range at any point (even during a SPI word), the CD1030 ignores the word and enters lockout mode. A SPI bit register is available to notify the MCU the CD1030 has seen an undervoltage lockout condition, once the battery is high enough to leave this range. During this mode, the input comparator and current sources are turned off.

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7.1.6 Power On Reset (POR) activated

The Power on Reset is activated when the VBATP is within the 2.7 V to 3.8 V range. The CD1030 is initialized in undervoltage lockout after the POR is de-asserted. A SPI bit in the device configuration register is used to note a POR occurrence, all SPI registers are reset to the default values, and SPI operation is disabled.

7.1.7 No operation

The device does not function and no switch detection is possible.

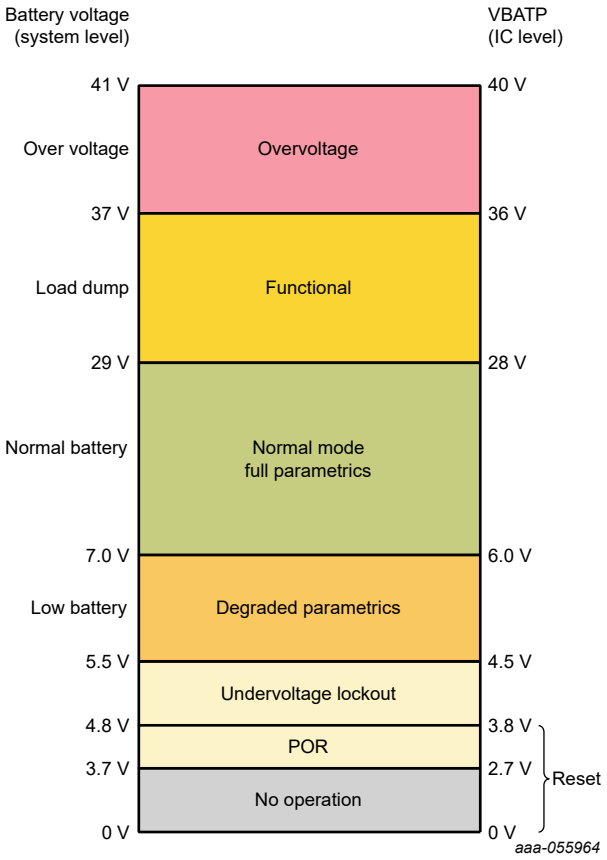


Figure 4. Battery voltage range

7.2 Power sequencing conditions

The chip uses two supplies as inputs into the device for various usage. These pins are VBATP and VDDQ. The VBATP pin is the power supply for the chip where the internal supplies are generated and power supply for the SG circuits. The VDDQ pin is used for the I/O buffer supply to talk to the MCU or other logic level devices, as well as AMUX. The INT_B pin is held low upon POR until the IC is ready to operate and communicate. Power can be applied in various ways to the CD1030 and the following conditions are possible.

7.2.1 V_{BATP} before V_{DDQ}

The normal condition for operation is the application of V_{BATP} and then V_{DDQ}.The chip operates logically in the default state, but without the ability to drive logic pins. When the V_{DDQ} supply is available, the chip is able to communicate correctly. The IC maintains its logical state (register settings) with functional behavior consistent with the logical state. No SPI communications can occur.

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7.2.2 V_{DDQ} before V_{BATP}

In some cases, the V_{DDQ} supply may be available before the V_{BATP} supply is ready. There is no back feeding current into the VDDQ pin which could potentially turn on the device into an unknown state, in this scenario. VDDQ is isolated from VBATP circuits and the device is off until V_{BATP} is applied. When V_{BATP} is available the device powers up the internal rails and logic within t_{ACTIVE} time. Communication is undefined until the t_{ACTIVE} time and becomes available after this time frame.

7.2.3 V_{BATP} okay, V_{DDQ} lost

After power up, it is possible the V_{DDQ} may turn off or be lost. In this case, the chip remains in the current state, but is not able to communicate. After the VDDQ pin is available again, the chip is ready to communicate.

7.2.4 V_{DDQ} okay, V_{BATP} lost

After power up, the V_{BATP} supply could be lost. The operation is consistent when V_{DDQ} is available before V_{BATP}.

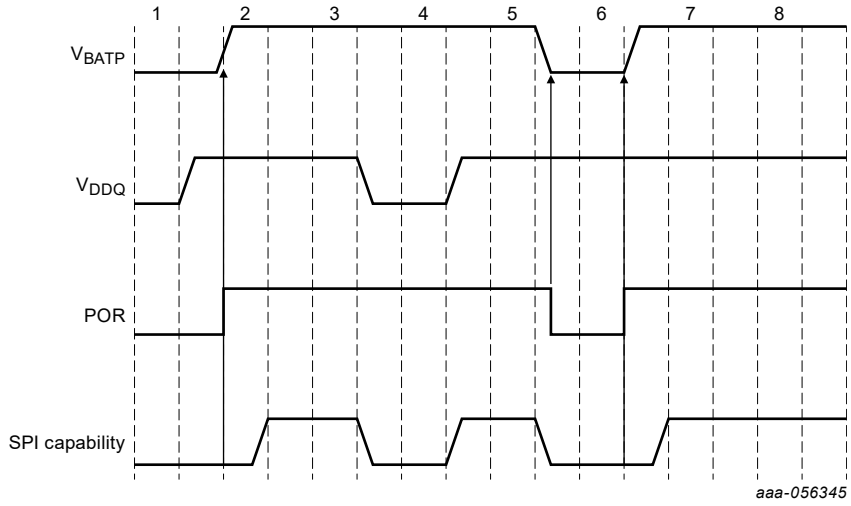


Figure 5. VDDQ power up first

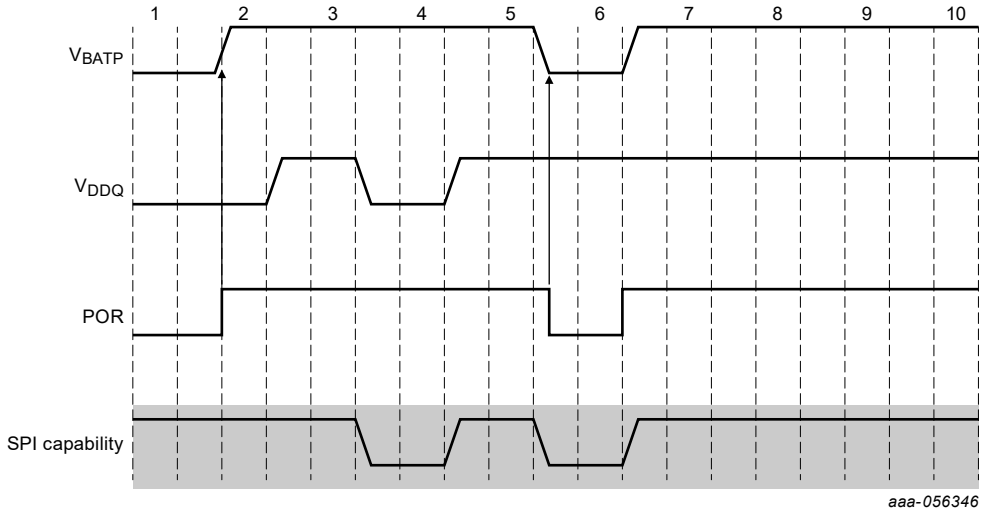


Figure 6. VBATP power up first

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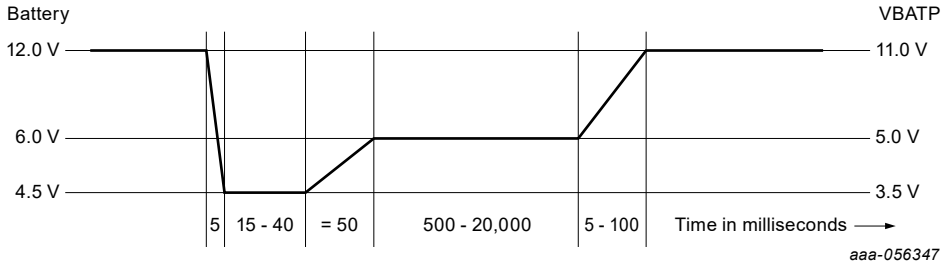


Figure 7. Battery crank profile

7.3 Low-power mode operation

Low-power mode (LPM) is used to reduce system quiescent currents. LPM can be entered only by sending the Enter Low-power mode command. All register settings programmed in Normal mode are maintained while in LPM.

The CD1030 exits LPM and enters Normal mode when any of the following events occur:

- Input switch change of state (when enabled)
- Interrupt timer expire
- Falling edge of WAKE_B (as set by the device configuration register)
- Falling edge of INT_B (with V_{DDQ} = 5.0 V)
- Falling edge of CS_B (with V_{DDQ} = 5.0 V)
- Power-ON Reset (POR)

The V_{DDQ} supply may be removed from the device during LPM, however removing V_{DDQ} from the device disables a wake-up from falling edge of INT_B and CS_B. The IC checks the status of V_{DDQ} after a falling edge of WAKE_B (as selected in the device configuration register), INT_B and CS_B. If V_{DDQ} is low, the IC returns to LPM and does not report a Wake event. If V_{DDQ} is high, the IC wakes up and reports the Wake event. In cases where CS_B is used to wake the device, the first MISO data message is not valid.

The LPM command contains settings for two programmable registers: the interrupt timer and the polling timer, as shown in Table 30. The interrupt timer is used as a periodic wake-up timer. When the timer expires, an interrupt is generated and the device enters Normal mode. The polling timer is used periodically to poll the inputs during Low-power mode to check for change of states. The $t_{ACTIVEPOLL}$ time is the length of time the part is active during the polling timer to check for change of state. The polling pulse is set at 1.0 mA for SG channels and 2.0 mA for SB channels. If a switch closure is detected during the low-power mode, the CD1030 detects the change of state and starts providing the sustain current (2.0 mA) for about 416 µs until the device returns to the Normal mode (WAKE_B pulled low). Once in Normal mode, the input channel keeps supplying the sustain current (2.0 mA) for 270 µs more and then forces the corresponding wetting current. This mechanism protects against excessive inrush current, when the input capacitors discharge during the long polling cycles, and need to be recharged all at once upon waking up from the LPM.

The Low-power mode voltage threshold allows the user to determine the noise immunity versus lower current levels that polling allows. Figure 16 shows the polling operation.

When polling and Interrupt timer coincide, the Interrupt timer wakes the device and the polling does not occur. When an input is determined to meet the Open condition (when entering LPM), yet while Open (on polling event), the chip does not continue the polling event for this input(s) to lower current in the chip.

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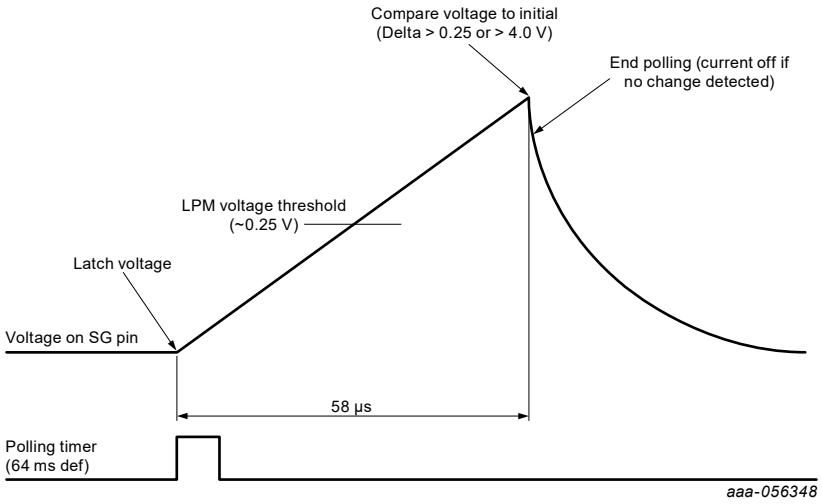


Figure 8. Low-power mode polling check

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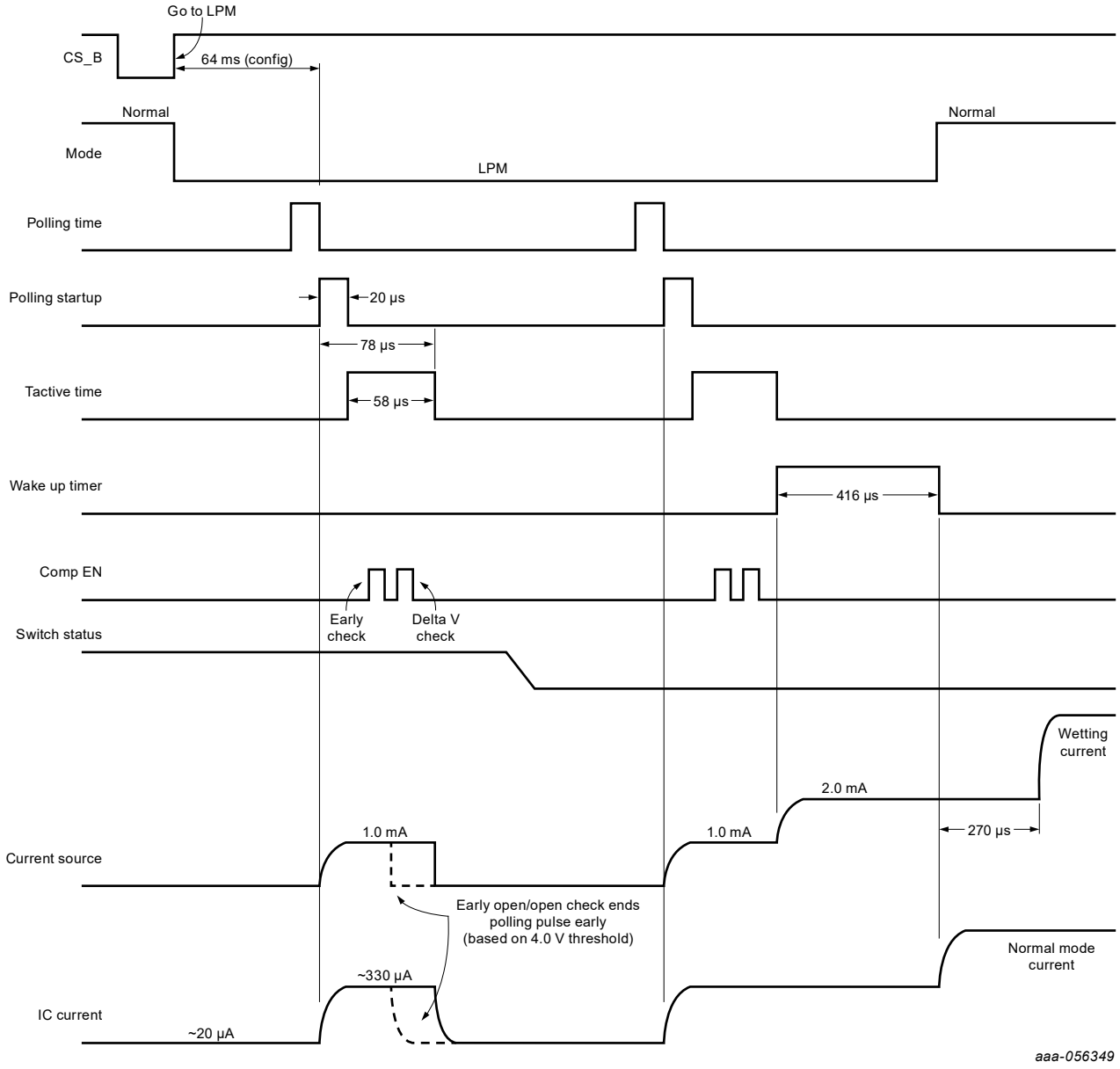


Figure 9. Low-power mode typical timing

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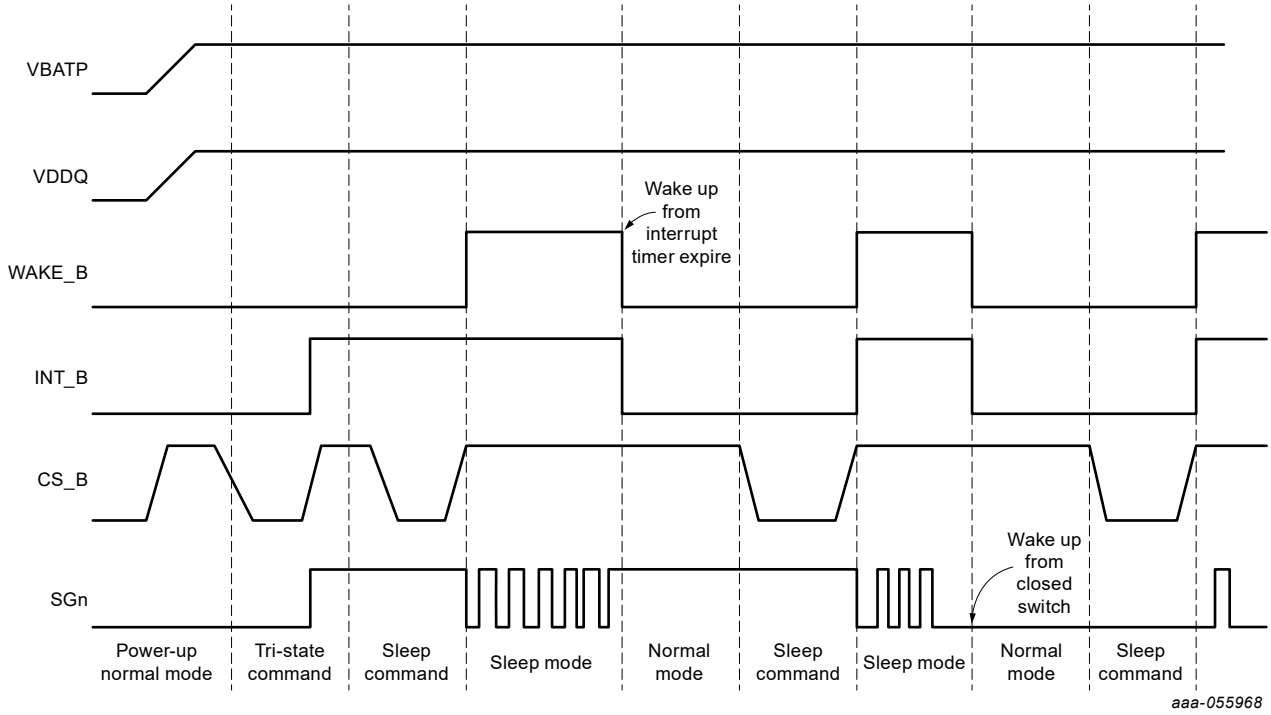


Figure 10. Low-power mode to Normal mode operation

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8 Functional block description

8.1 State machine

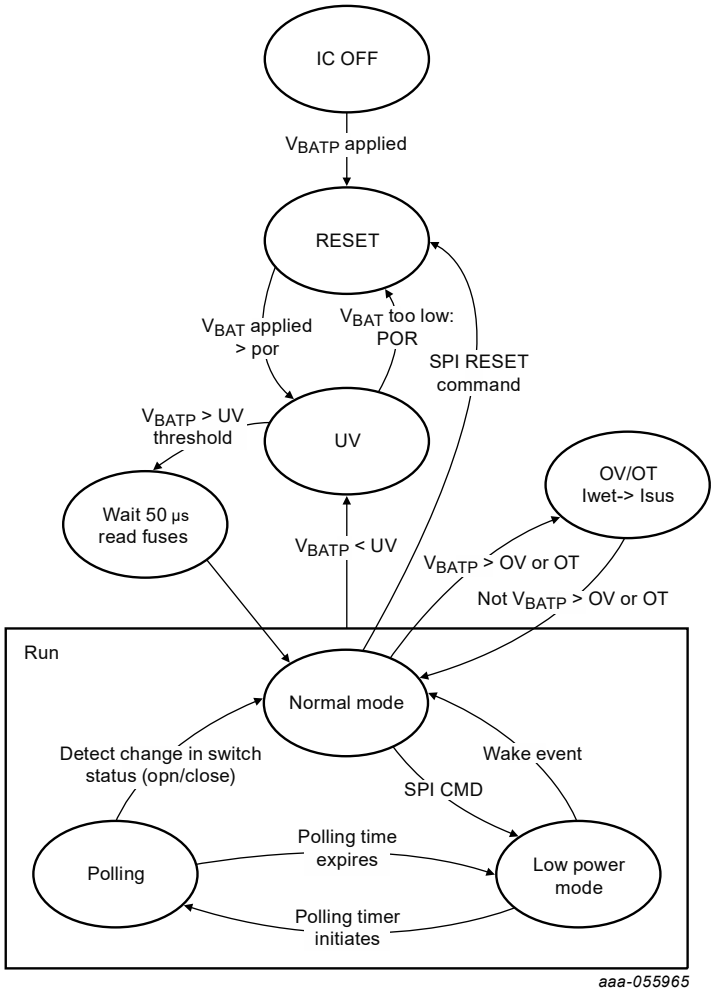


Figure 11. CD1030 state diagram

After power up, the IC enters into the device state machine, as illustrated in Figure 18. The voltage on VBATP begins to power the internal oscillators and regulator supplies. The POR is based on the internal 2.5 V digital core rail. When the internal logic regulator reaches approximately 1.8 V (typically 3.3 V on the VBATP node), the IC enters into the UV range. Below the POR threshold, the IC is in RESET mode where no activity occurs.

8.1.1 UV: undervoltage lockout

After the POR circuit has reset the logic, the IC is in undervoltage. In this state, the IC remembers all register conditions, but is in a lockout mode, where no SPI communication is allowed. AMUX is inactive and the current sources are off. The user does not receive a valid response from the MISO, as it is disabled in this state. The chip oscillators (4.0 MHz for most normal mode activities, 192 kHz for LPM, and limited normal mode functions) are turned on in the UV state. The chip moves to the Read fuses state when the V_{BATP} voltage rises above the UV threshold (~4.3 V rising). The internal fuses read in approximately 50 µs and the chip enters the Normal mode.

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8.1.2 Normal mode

In Normal mode, the chip operates as selected in the available registers. Any command may be loaded in Normal mode, although not all (Low-power mode) registers are used in the Normal mode. All the LPM registers must be programmed in Normal mode, as the SPI is not active in LPM. The Normal mode of the chip is used to operate AMUX, communicate via the SPI, Interrupt the IC, wetting and sustain currents, as well as the thresholds available to use. The WAKE_B pin is asserted (low) in Normal mode and can be used to enable a power supply (ENABLE_B). Various fault detections are available in this mode including overvoltage, overtemperature, thermal warning, SPI errors, and Hash faults.

8.1.3 Low-power mode

When the user needs to lower the IC current consumption, a Low-power mode is used. The only method to enter LPM is through a SPI word. After the chip is in Low-power mode, the majority of circuitry is turned off including most power rails, the 4.0 MHz oscillator, and all the fault detection circuits. This mode is the lowest current consumption mode on the chip. If a fault occurs while the chip is in this mode, the chip does not see or register the fault (does not report via the SPI when awakened). Some items may wake the IC in this mode, including the interrupt timer, falling edge of INT_B, CS_B, or WAKE_B (configurable), or a comparator only mode switch detection.

8.1.4 Polling mode

The CD1030 uses a polling mode, which periodically (selectable in LPM config register) interrogates the input pins to determine in what state the pins are, and decide if there was a change of state from when the chip was in Normal mode. There are various configurations for this mode, allowing the user greater flexibility in operation. This mode uses the current sources to pull-up (SG) or down (SB) to determine if a switch is open or closed. More information is available on section 6.3, Low-power mode operation, page 24.

In the case of a low V_{BATP}, the polling pauses and waits until the V_{BATP} rises out of UV or a POR occurs. The pause of the polling ensures all of the internal rails, currents, and thresholds are up at the required levels to accurately detect open or closed switches. The chip does not wake-up in this condition and simply waits for the V_{BATP} voltage to rise or cause a POR.

After the polling ends, the chip either returns to the Low-power mode, or enters Normal mode when a wake event was detected. Other events may wake the chip as well, such as the falling edge of CS_B, INT_B, or WAKE_B (configurable). A comparator only mode switch detection is always on in LPM or Polling mode, so a change of state for those inputs would effectively wake the IC in Polling mode as well.

If the wake-up enable bits are disabled on all channels (SG and SP), the device does not wake-up with a change of state on any of the input pins. In this case, the device disables the polling timer to allow the lowest current consumption during Low-power mode.

8.2 Input functional block

The SGx pins are switch-to-ground inputs only (pull-up current sources). The SPx pins are configurable as either switch to ground or switch to battery (pull-up current source or pull-down current sink). The input is compared with a 4.0 V (input comparator threshold) reference. Voltages greater than the input comparator threshold value are considered open for SG pins and closed for SB configuration. Voltages less than the input comparator threshold value are considered closed for SG pins and open for the SB configurations.

Programming features are defined in section 7.9, SPI control register definition, page 35 of this datasheet. The input comparator has hysteresis with the thresholds based on the closing of the switch (falling on SG, rising on SB). The user must take care to keep power conditions within acceptable limits (package is capable of 2.0 W). Using many of the inputs with continuous wetting current levels causes overheating of the IC and may cause an overtemperature (OT) event to occur.

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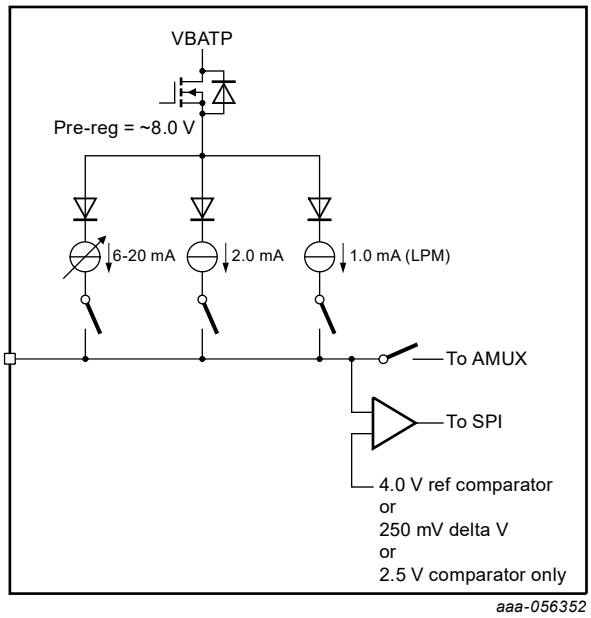


Figure 12. SG block diagram

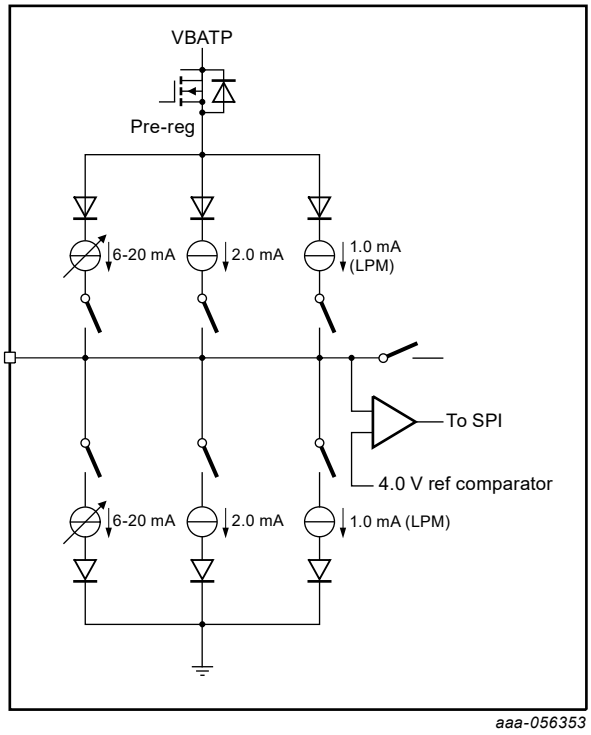


Figure 13. SP block diagram

8.3 Oscillator and timer control functional block

Two oscillators are generated in this block. A 4.0 MHz clock is used in Normal mode only, as well as a Low-power mode 192 kHz clock, which is on all the time. All timers are generated from these oscillators. The oscillator accuracy is 15% for both, the 4.0 MHz clock and the 192 kHz clock. No calibration is needed and the

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accuracy is overvoltage and temperature. The timers in Low-power mode are generated from a base timer such that all timers coincide with other times. When polling and Interrupt timer coincide, the Interrupt timer wakes the device and the polling does not occur.

8.4 Temperature monitor and control functional block

The device has multiple thermal limit (t_{LIM}) cells to detect thermal excursions in excess of 155 °C. The t_{LIM} cells from various locations on the IC are logically ORed together and communicated to the MCU as one t_{LIM} fault. When the t_{LIM} value is detected, the wetting current is lowered to 2.0 mA until the temperature has decreased beyond the $t_{LIM(HYS)}$ value (the sustain current remains on or as selected). A hysteresis value of 15 °C exists to keep the device from cycling. A thermal flag also exists to alert the system to increasing temperature. The thermal flag is set at a typical value of 120 °C.

8.5 WAKE_B control functional block

The WAKE_B functions as an input (wake-up) or an output (open drain) pin. In Normal mode, the WAKE_B pin is low. In Low-power mode, the WAKE_B pin is pulled high. The WAKE_B pin has an internal pull-up to the V_{DDQ} supply, with an internal series diode to allow an external pull-up to V_{BATP}, if the specific application requires it.

As an input, with V_{DDQ} present, when the device is in Low-power mode and WAKE_B is pulled high (internally or externally), a falling edge of the WAKE_B pin brings the CD1030 into Normal mode. In Low-power mode, if V_{DDQ} goes low, the WAKE_B V_{DDQ} check bit in the Device configuration register can be used to ignore or allow a wake-up event upon a falling edge of the WAKE_B pin. Setting the WAKE_B V_{DDQ} check bit to 0, ignores the falling edge of WAKE_B when V_{DDQ} is low. Setting the WAKE_B V_{DDQ} check to 1, allows the WAKE_B falling edge to wake-up the device and go into Normal mode regardless of the status of VDDQ. This allows the user to pull the WAKE_B pin up to V_{BATP} so it can be used in a setup in which V_{DDQ} is supposed to shut down during Low-power mode.

As an output, WAKE_B pin can drive either an MCU input or the EnableB of a regulator (possibly for V_{DDQ}). WAKE_B is driven LOW during Normal mode regardless of the state of V_{DDQ}. When the CD1030 is in LPM, the WAKE_B pin is released and is expected to be pulled up internally to $_{VDDQ}$ or externally to V_{BATP}. When a valid wake-up event is detected, the CD1030 should wake-up from LPM and the WAKE_B should be driven LOW (regardless of the state of V_{DDQ}).

8.6 INT_B functional block

INT_B is an input/output pin in the CD1030 device to indicate an interrupt event has occurred, as well as receiving interrupts from other devices when the INT_B pins are wired ORed.The INT_B pin is an open-drain output with an internal pull-up to V_{DDQ}. In Normal mode, a switch state change triggers the INT_B pin (when enabled). The INT_B pin and INT_B bit in the SPI register are latched on the falling edge of CS_B, which permits the MCU to determine the origin of the interrupt. When two CD1030 devices are used, only the device initiating the interrupt has the INT_B bit set. The INT_B pin and INTflg bit are cleared 1.0 µs after the falling edge of CS B. The INT_B pin does not clear with the rising edge of CS_B if a switch contact change has occurred while CS_B was Low.

In a multiple CD1030 device system with WAKE_B high and V_{DDQ} in Low-power mode, the falling edge of INT_B places all CD1030s in Normal mode.The INT_B has the option of a pulsed output (pulsed low for INT_{PULSE} duration) or a latched low output.The default case is the latched low operation; the INT_B operation is selectable via the SPI. An INT_B request by the MCU can be done by a SPI word and results in an INT_{PULSE} of 100 µs duration on the INT_B pin.

The chip causes an INT_B assertion for the following cases:

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1. A change of state is detected
   a. Interrupt timer expires
   b. Any wake-up event
   c. Any faults detected
   d. After a POR, the INT_B pin is asserted during startup until the chip is ready to communicate

8.7 AMUX functional block

The analog voltage on switch inputs may be read by the MCU using the analog command (Table 47). Internal to the IC is a 35-to-1 analog multiplexer. The voltage present on the selected input pin is buffered and made available on the AMUX output pin. The output pin is clamped to a maximum of V_{DDQ} regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next MISO data stream is logic [0]. When selecting a channel to be read as analog input, the user can enable the current source to provide a current flow through the specific channel. Current level can be set to the programmed wetting current for the selected channel or set to high-impedance, as defined in Table 46.

When selecting an input to be sent to the AMUX output, this input is not polled or wake-up from Low-power mode. The user should set AMUX to "No input selected" or "Temp diode" before entering Low-power mode.The AMUX pin is not active during Low-power mode. The SG5 pin can also be used as a VBATP sense pin. An internal resistor divider of 1/6 is provided for conditioning the V_{BATP} higher voltage to a level within the 0 V to V_{DDQ} range.

Along with the default SPI input selection method, the AMUX has two hardwire operation such that the user can select an specific input channel by physically driving the SG1, SG2, or SG3 pin (HW 3-bit), or by driving the SG1 and SG2 pins (HW 2-bit), as shown in Table 10 and Table 11. When using the AMUX hardwired options, the SG1, SG2, and SG3 inputs use a 2.5 V input voltage threshold to read a logic 0 or logic 1. Table 9 shows the AMUX selection methods configurable by the Aconfig0 and Aconfig1 bits in the Device configuration register.

Table 3. AMUX selection method

Aconfig1	Aconfig0	AMUX selection method
0	0	SPI (def)
0	1	SPI
1	0	HW 2-bit
1	1	HW 3-bit

Table 4. AMUX hardware 3-bit

Pins [SG3, SG2, SG1]	Output of AMUX
000	SG0
001	SG5
010	SG6
011	SG7
100	SG8
101	SG9
110	Temperature Diode
111	Battery Sense

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Table 5. AMUX hardware 2-bit

Pins [SG2, SG1]	Output of AMUX
00	SG0
01	SG5
10	SG6
11	SG7

Since the device is required to meet the ±1.0 V offset with ground, it is imperative the user bring the sensor ground back to the CD1030 when using AMUX for accurate measurements, to ensure any ground difference does not impact the device operation.

8.8 Serial peripheral interface (SPI)

The CD1030 contains a serial peripheral interface consisting of Serial Clock (SCLK), Serial Data Out (MISO), Serial Data In (MOSI), and Chip Select Bar (CS_B).The SPI interface is used to provide configuration, control, and status functions. The user may read the registers contents as well as read some status bits of the IC. The CD1030 is configured as a SPI secondary device.

All SPI transmissions to the CD1030 must be done in exact increments of 32 bits (modulo 0 is ignored as well). The CD1030 contains a data valid method via SCLK input to keep non-modulo 32-bit transmissions from being written into the IC. The SPI module also provides a daisy chain capability to accommodate MOSI to MISO wrap around (see Figure 24). The SPI registers have a hashing technique to ensure the registers are consistent with the programmed values. If the hashed value does not match the register status, a SPI bit is set, as well as an interrupt to alert the MCU to this issue.

8.8.1 Chip select low (CS_B)

The CS_B input selects this device for serial transfers. On the falling edge of CS_B, the MISO pin is released from tri-state mode, and all status information are latched in the SPI shift register. While CS_B is asserted, register data is shifted in the MOSI pin and shifted out the MISO pin on each subsequent SCLK. On the rising edge of CS_B, the MISO pin is tri-stated and the fault register reloaded (latched) with the current filtered status data. To allow sufficient time to reload the fault registers, the CS_B pin must remain low for a minimum of t_{CSN} prior to going high again.

The CS_B input contains a pull-up current source to VDDQ to command the de-asserted state should an open-circuit condition occur. This pin has threshold compatible voltages allowing proper operation with microprocessors using a 3.3 V to 5.0 V supply.

8.8.2 Serial clock (SCLK)

The SCLK input is the clock signal input for synchronization of serial data transfer. This pin has a threshold compatible voltage allowing proper operation with microprocessors using a 3.3 V to 5.0 V supply.

When CS_B is asserted, both the Primary Microprocessor and the CD1030 latch input data on the rising edge of SCLK. The SPI primary device typically shifts data out on the falling edge of SCLK. The CD1030 shifts data out on the falling edge of SCLK as well, to allow more time to drive the MISO pin to the proper level.

This input is used as the input for the modulo 32-bit counter validation. Any SPI transmissions which are NOT exact multiples of 32 bits (clock edges) are treated as illegal transmissions. The entire frame is aborted and no information is changed in the configuration or control registers.

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8.8.3 Serial data output (MISO)

The MISO output pin is in a tri-state condition when CS_B is negated. When CS_B is asserted, MISO is driven to the state of the MSB of the internal register and starts shifting out the requested data from the MSB to the LSB. This pin supplies a "rail to rail" output, depending on the voltage at the VDDQ pin.

8.8.4 Serial data input (MOSI)

The MOSI input takes data from the primary microprocessor while CS_B is asserted. The MSB is the first bit of each word received on MOSI and the LSB is the last bit of each word received on MOSI. This pin has threshold level compatible input voltages allowing proper operation with microprocessors using a 3.3 V to 5.0 V (V_{DDQ}) supply.

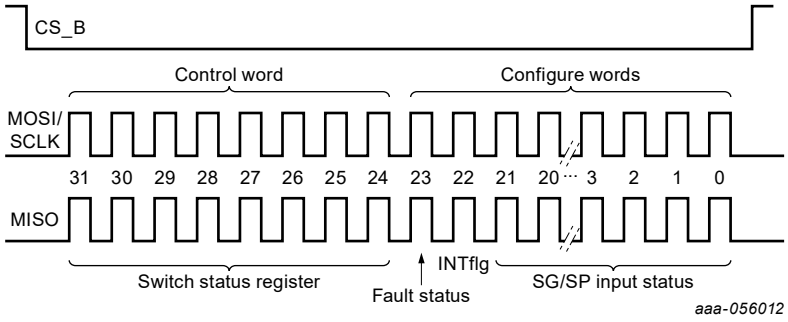


Figure 14. First SPI operation (After POR)

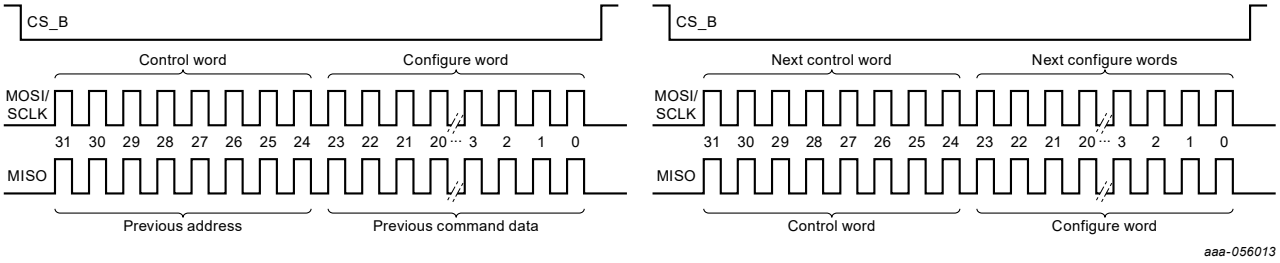


Figure 15. SPI write operation

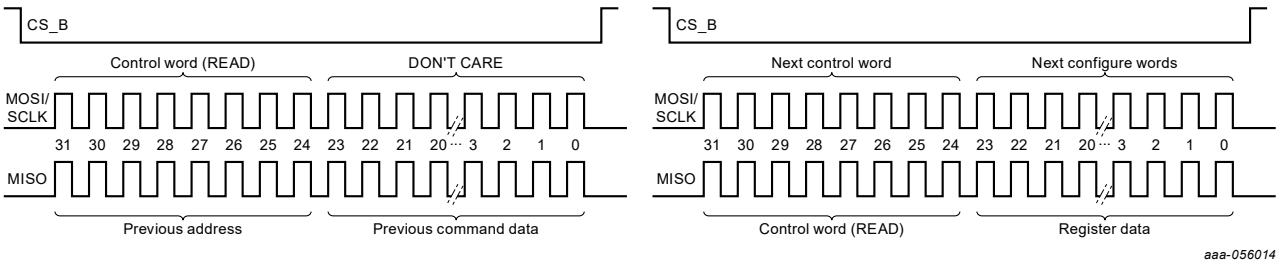


Figure 16. SPI read operation

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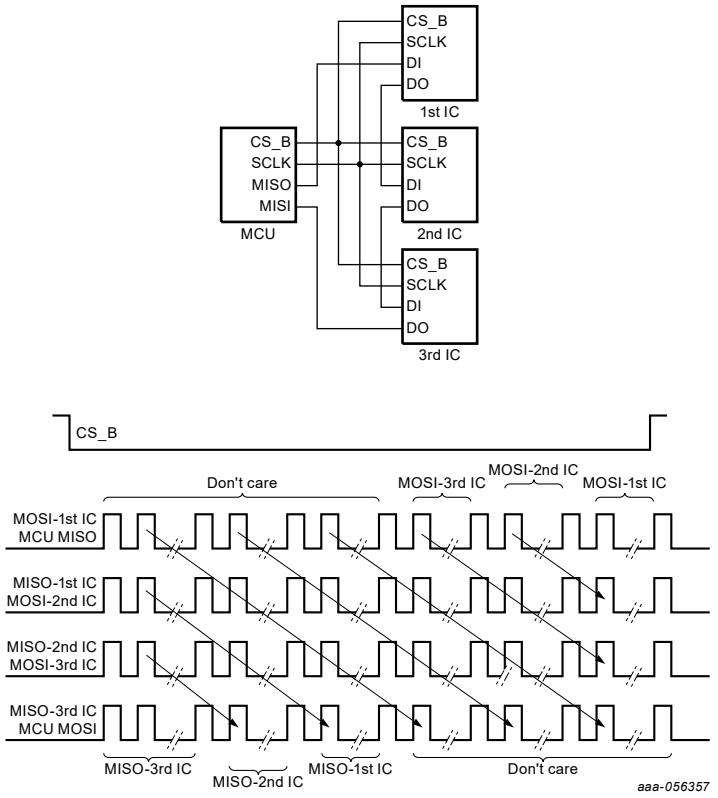


Figure 17. Daisy Chain SPI operation

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8.9 SPI control register definition

A 32-bit SPI allows the system microprocessor to configure the CD1030 for each input as well as read out the status of each input. The SPI also allows the Fault Status and INTflg bits to be read via the SPI. The SPI MOSI bit definitions are given in Table 12:

Table 6. MOSI input register bit definition

Register #	Register name	Address							Rb/W
0	SPI check	0	0	0	0	0	0	0	0
02/03	Device configuration register	0	0	0	0	0	0	1	0/1
04/05	Tri-state SP register	0	0	0	0	0	1	0	0/1
06/07	Tri-state SG register	0	0	0	0	0	1	1	0/1
08/09	Wetting current level SP register 0	0	0	0	0	1	0	0	0/1
0A/0B	Wetting current level SG register 0	0	0	0	0	1	0	1	0/1
0C/0D	Wetting current level SG register 1	0	0	0	0	1	1	0	0/1
0E/0F	Wetting current level SG register 2	0	0	0	0	1	1	1	0/1
10/11	Wetting current level SP register 1	0	0	0	1	0	0	0	0/1
16/17	Continuous wetting current SP register	0	0	0	1	0	1	1	0/1
18/19	Continuous wetting current SG register	0	0	0	1	1	0	0	0/1
1A/1B	Interrupt enable SP register	0	0	0	1	1	0	1	0/1
1C/1D	Interrupt enable SG register	0	0	0	1	1	1	0	0/1
1E/1F	Low-power mode configuration	0	0	0	1	1	1	1	0/1
20/21	Wake-up enable register SP	0	0	1	0	0	0	0	0/1
22/23	Wake-up enable register SG	0	0	1	0	0	0	1	0/1
24/25	Comparator only SP	0	0	1	0	0	1	0	0/1
26/27	Comparator only SG	0	0	1	0	0	1	1	0/1
28/29	LPM voltage threshold SP configuration	0	0	1	0	1	0	0	0/1
2A/2B	LPM voltage threshold SG configuration	0	0	1	0	1	0	1	0/1
2C/2D	Polling current SP configuration	0	0	1	0	1	1	0	0/1
2E/2F	Polling current SG configuration	0	0	1	0	1	1	1	0/1

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Table 6. MOSI input register bit definition*...continued*

Register #	Register name	Address							Rb/W
30/31	Slow polling SP	0	0	1	1	0	0	0	0/1
32/33	Slow polling SG	0	0	1	1	0	0	1	0/1
34/35	Wake-up debounce SP	0	0	1	1	0	1	0	0/1
36/37	Wake-up debounce SG	0	0	1	1	0	1	1	0/1
39	Enter Low-power mode	0	0	1	1	1	0	0	1
3A/3B	AMUX control register	0	0	1	1	1	0	1	0/1
3C	Read switch status registers SP	0	0	1	1	1	1	0	0
3E	Read switch status registers SG	0	0	1	1	1	1	1	0
42	Fault status register	0	1	0	0	0	0	1	0
47	Interrupt request	0	1	0	0	0	1	1	1
49	Reset register	0	1	0	0	1	0	0	1

The 32-bit SPI word consists of a command word (8-bit) and three configure words (24-bit). The 8 MSB bits are the command bits that select what type of configuration is to occur. The remaining 24-bits are used to select the inputs to be configured.

- Bit 31 - 24 = Command word: Use to select what configuration is to occur (example: setting wake-up enable command)
- Bit 23 - 0 = SGn input select word: Use these bits in conjunction with the command word to determine which input is setup.

Configuration registers may be read or written to. To read the contents of a configuration register, send the register address + ‘0’ on the LSB of the command word; the contents of the corresponding register is shifted out of the MISO buffer in the next SPI cycle. When a Read command is sent, the answer (in the next SPI transaction) includes the Register address in the upper byte (see Figure 23).

Read example:

- Send 0x0C00_0000 Receive: 8000_0000 (for example after a POR)
- Send 0x0000_0000 Receive: 0C00_0000 (address + register data)

The first response from the device after a POR event is a Read Status register (0x3Exxxxxx where x is the status of the inputs). This is the same for exiting the Low-power mode (see Figure 21).

To write into a configuration register, send the register Address + ‘1’ on the LSB of the command word and the configuration data on the next 24 bits. The new value of the register is shifted out of the MISO buffer in the next SPI cycle, along with the register address and the corresponding read or write bit.

The fault/status diagnostic capability consists of two Switch Status registers and one Fault status register (shown in Table 13).

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Table 7. Switch status and Fault registers

Commands	[31-25] Address	24 R	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Switch Status SP	0011110	0	FAULT STATUS	INTflg	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Read Switch Status SG	0011111	0	FAULT STATUS	INTflg	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Fault Status	0100001	0	X	INTflg	X	X	X	X	X	X	X	X	X	X	X	SPI Error	hash fault	X	UV	OV	TempFlag	OT	INT_B wake	WAKE_B	SpiWake	POR

In the Read Status Register SP, Bits 0 – 11 shows the status of each one of the SP inputs, where logic [1] is a closed switch and logic [0] is an open switch. In addition to input status information, Fault conditions and interrupts are reported through bits FAULT STATUS [23] and INTflg [22].

In the Read Status Register SG, Bits 0 - 20 show the status of each one of the SG input, where logic [1] is a closed switch and logic [0] is an open switch. In addition to input status information, fault conditions and interrupts are reported through bits FAULT STATUS [23] and INTflg [22].

The Fault Status Register latches the respective bit high when a specific fault event occurs. All possible fault events are described in Table 50. When a Fault Status command is sent, a SPI read cycle is initiated by a CS_B falling edge, followed by 32 SCLK cycles to shift the fault status register out the MISO pin. The INTflg bit is cleared 1.0 ms after the falling edge of CSB.

On most registers where the first two significant bits are available, bit 23 is an OR of all the fault status register bits and bit 22 is latched high following any interrupt event. Registers which have all bits dedicated for other purposes, such as the Wetting Current Level or the SPI check registers, do not have these interrupt or fault status bits.

When a register with a int flag (bit-22) set high is read, the INTflg bit is globally cleared. For the case of bit-23 high, it is cleared after the Fault Status Register is read, and the respective fault flag is cleared.

The Fault status bit sets any time a fault occurs. A read of the fault status register must be done to clear the Fault status bit. The fault bit immediately sets again if the fault condition is still present. The INTflg bit sets any time an interrupt event occurs (change of state on switch, or any fault status bit gets set). Any SPI command that returns INTflg bit clears this flag, even if the event is still occurring, for example, an overtemp causes an interrupt. The interrupt can be cleared but the chip does not interrupt again based on the overtemp until the Overtemp flag has been cleared. A thermal fault latches as soon as it occurs.

Table 14 provides a general overview of the functional SPI commands and configuration bits.

Table 8. Functional SPI register

Commands	[31-25] Address	24 R/W	23[26]	22[26]	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI check	0000000	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Device Configuration	0000001	0/1	X	X	X	X	X	X	SBPOLL TIME	VBATP OV Disable	WAKE_B Pull up	IntB_ Out	aconfig1	aconfig0	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Tri-state Enable SP	0000010	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Tri-state Enable SG	0000011	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Wetting Current Level SP 0	0000100	0/1	SP7[2-0]			SP6[2-0]			SP5[2-0]			SP4[2-0]			SP3[2-0]			SP2[2-0]			SP1[2-0]			SP0[2-0]		

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Table 8. Functional SPI register...*continued*

Commands	[31-25] Address	24 R/W	23[26]	22[26]	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Wetting Current Level SG 0	0000101	0/1	SG7[2-0]			SG6[2-0]			SG5[2-0]			SG4[2-0]			SG3[2-0]			SG2[2-0]			SG1[2-0]			SG0[2-0]		
Wetting Current Level SG 1	0000110	0/1	SG15[2-0]			SG14[2-0]			SG13[2-0]			SG12[2-0]			SG11[2-0]			SG10[2-0]			SG9[2-0]			SG8[2-0]		
Wetting Current Level SG 2	0000111	0/1	X	X	X	X	X	X	X	X	X	SG20[2-0]			SG19[2-0]			SG18[2-0]			SG17[2-0]			SG16[2-0]		
Wetting Current Level SP 1	0001000	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11[2-0			SP10[2-0]			SP9[2-0]			SP8[2-0]		
Cont Wetting Current Enable SP	0001011	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Cont Wetting Current Enable SG	0001100	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Interrupt Enable SP	0001101	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Interrupt Enable SG	0001110	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Low-power Mode configuration	0001111	0/1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	int3	int2	int2	int0	poll3	poll2	poll1	poll0
Wake-up Enable SP	0010000	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Wake-up Enable SG	0010001	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
LPM Comparator Only SP	0010010	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
LPM Comparator Only SG	0010011	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
LPM Voltage Threshold SP	0010100	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
LPM Voltage Threshold SG	0010101	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
LPM Polling current config SP	0010110	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
LPM Polling current config SG	0010111	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
LPM Slow Polling SP	0011000	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
LPM Slow Polling SG	0011001	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Wake-up Debounce SP	0011010	0/1	X	X	X	X	X	X	X	X	X	X	X	X	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Wake-up Debounce SG	0011011	0/1	X	X	X	SG20	SG19	SG18	SG17	SG16	SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Enter Low-power Mode	0011100	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
AMUX Channel Select SPI	0011101	0/1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	asett	asel5	asel4	asel3	asel2	asel1	asel0
Read Switch Status SP	0011110	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Read Switch Status SG	0011111	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Fault Status	0100001	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Interrupt Pulse Request	0100011	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Reset	0100100	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

26. Bits 23 and 22 are used for FAULT STATUS and INTflg global diagnostic flags (Read only) respectively. INTflg is cleared out upon reading of any register with this flag available. The FAULT STATUS flag is cleared upon reading the fault status register and no fault event present anymore.

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8.9.1 SPI check

The MCU may check the communication with the IC by using the SPI Check register. The MCU sends the command and the response during the next SPI transaction is 0x123456. The SPI Check command does not return Fault Status or INTflg bit, therefore this bit is not cleared upon a SPI check command.

Table 9. SPI check command

Register address	R	SPI data bits [23 - 0]
[31-25]	24	bits [23 - 16]
0000_000	0	0000_0000
		bits [15 - 8]
		0000_0000
		bits [7 - 0]
		0000_0000
MISO Return Word		0x00123456

8.9.2 Device configuration register

The device has various configuration settings that are global in nature. The configuration settings are as follows:

- When the SP channels are programmed to detect a Switch to Battery (SB), the SBPOLLTIME bit can be used to program the length of the polling pulse during the Low-power mode operation. A logic [0] sets the active polling timer to 1.2 ms and a logic [1] sets the active polling timer to 58 us.
- When the CD1030 is in the overvoltage region, a Logic [0] on the VBATP OV bit, limits the wetting current on all input channels to 2.0 mA, and the CD1030 is not able to enter into the Low-power mode. A Logic [1] allows the device to operate normally even on the overvoltage region. The OV flag sets when the device enters in the OV region, regardless the value of the VBATP OV bit.
- WAKE_B can be used to enable an external power supply regulator to supply the V_{DDQ} voltage rail. When the WAKE_B V_{DDQ} check bit is a Logic [0], the WAKE_B pin is expected to be pulled-up internally or externally to V_{DDQ}, and V_{DDQ} is expected to go low, and so the CD1030 does not wake-up on the falling edge of WAKE_B. A Logic [1], assumes the user uses an external pull-up to V_{BATP} or V_{DDQ} (when V_{DDQ} is not expected to be off) and the IC wakes up on a falling edge of WAKE_B.
- INT_B out is used to select how the INT_B pin operates when an interrupt occurs. The IC is able to pulse low [1] or latch low [0].
- A config[1-0] is used to determine the method of selecting the AMUX output, either a SPI command or using a hardwired setup with SG[3-1].
- SP0-7 inputs may be programmable for switch-to-battery or switch-to-ground. To set a SPx input for switch-to-battery, a logic [1] for the appropriate bit must be set. To set a SPx input for switch-to-ground, a logic [0] for the appropriate bit must be set. The MCU may change or update the programmable switch register via software at any time in Normal mode. Regardless of the setting, when the SPx input switch is closed, a logic [1] is placed in the serial output response register. If an SP is changed from SB or SG, the chip generates an interrupt, since the SPI registers for the switch status change due to the change of polarity of SB / SG.

Table 10. Device configuration register

Register address	R/ W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0000_001	0/1	FAULT STATUS	INTflg	Unused				SBPOLL TIME	VBATP OV disable

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Table 10. Device configuration register*...continued*

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		WAKE_B VDDQ Check	INT_B out	Aconfig1	Aconfig0	SP11	SP10	SP9	SP8
		1	0	0	0	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		1	1	1	1	1	1	1	1
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0000_001[R/W]		FAULT STATUS	INTflg	Register Data					

Table 11. Device configuration bits definition

Bit	Functions	Default value	Description
23	FAULT STATUS	X	The FAULT STATUS flag is a read only bit. It is set when a fault occurs and it is cleared upon reading the fault status register with no fault event is present anymore. It is a global variable and clearing the flag once clears it for all registers.
22	INTflg	X	The INTflg is a read only bit. It is set when an interrupt event occurs and it is cleared upon a read/write transaction of a register containing the INTflg. It is a global variable and clearing the flag once clears it for all registers.
21-18	Unused	0	Unused
17	SBPOLLTIME	0	Select the polling time for SP channels configured as SB. • A logic [0] set the active polling timer to 1.0 ms, • A logic [1] sets the active polling timer to 55 µs.
16	VBATP OV Disable	0	VBATP Overvoltage protection • 0 - Enabled • 1 - Disable
15	WAKE_B VDDQ Check	1	Enable/Disable WAKE_B to wake-up the device on falling edge when V_{DDQ} is not present. • 0 - WAKE_B is pulled up to V_{DDQ} (internally and/or externally). WAKE_B is ignored while in LPM if V_{DDQ} is low. • 1 - WAKE_B is externally pulled up to V_{BATP} or V_{DDQ} and wakes upon a falling edge of the WAKE_B pin regardless of the V_{DDQ} status.(V_{DDQ} is not expected to go low)
14	Int_B_Out	0	Interrupt pin behavior • 0 - INT pin stays low when interrupt occurs • 1 - INT pin pulse low and return high
13-12	Aconfig(1-0)	00	Configure the AMUX output control method • 00 - SPI (default) • 01 - SPI • 10 - HW 2-bit • 11 - HW 3-bit Refer to section 7.7, AMUX functional block, page 31 for details on 2 and 3-bit hardwire configuration.
11-0	SP11 - SP0	111_1111_1111	Configure the SP pin as Switch to Battery (SB) or Switch to ground (SG) • 0 - Switch to Ground • 1 - Switch to Battery

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8.9.3 Tri-state SP register

The tri-state command is used to set the input nodes as high-impedance (Table 18). By setting the tri-state register bit to logic [1], the input is high-impedance regardless of the wetting current setting. The configurable comparator (4.0 V default) on each input remains active. The MCU may change or update the tri-state register via software at any time in Normal mode. The tri-state register defaults to 1 (inputs are tri-stated). Any input in tristate mode is still polled in LPM but the current source is not active during this time. The determination of change of state occurs at the end of the $t_{ACTIVEPOLL}$ and the wake-up decision is made.

Table 12. Tri-state SP register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0000_010	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		1	1	1	1	1	1	1	1
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0000_010[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.4 Tri-state SG register

The tri-state command is used to set the input nodes as high-impedance (Table 19). By setting the tri-state register bit to logic [1], the input is high-impedance regardless of the wetting command setting. The configurable comparator (4.0 V default) on each input remains active. The MCU may change or update the tri-state register via software at any time in Normal mode. The tri-state register defaults to 1 (inputs are tristated). Any input in tri-state is still polled in LPM but the current source is not active during this time. The determination of change of state occurs at the end of the $t_{ACTIVEPOLL}$ and the wake-up decision is made.

Table 13. Tri-state SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0000_011	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default on POR		X	X	0	1	1	1	1	1
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		1	1	1	1	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		1	1	1	1	1	1	1	1
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0000_011[R/W]		FAULT STATUS	INTflg	Register Data					

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8.9.5 Wetting current level SP register 0

Three bits are used to control the configurable wetting currents for each individual input pin with the values set in the Table 20. The default configuration is 16 mA for all channels. The MCU may change or update the wetting current register via software at any time in Normal mode.

Table 14. Wetting current level SP register 0

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit [23 - 21]			bit [20 - 18]			bit [17 - 16]	
0000_100	0/1	SP7 [2-0]			SP6[2-0]			SP5[2-1]	
Default on POR		110			110			11	
		bit [15]	bit [14 - 12]			bit [11 - 9]			bit [8]
		SP5[0]	SP4 [2-0]			SP3[2-0]			SP2[2]
		0	110			110			1
		bit [7 - 6]		bit [5 - 3]			bit [2 - 0]		
		SP2[1-0]		SP1[2-0]			SP0[2-0]		
		10		110			110		
MISO Return Word		bits [23 - 0]							
0000_100[R/W]		Register Data							

See Table 25 for the selectable wetting current level values for both SPx and SGx pins.

8.9.6 Wetting current level SP register 1

Three bits are used to control the configurable wetting currents for each individual input pin with the values set in the Table 21. The default configuration is 16 mA for all channels. The MCU may change or update the wetting current register via software at any time in Normal mode.

Table 15. Wetting current level SP register 1

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_000	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit [11 - 9]			bit [8]
		Unused				SP11[2-0]			SP10[2]
		0	0	0	0	110			1
		bit [7 - 6]		bit [5 - 3]			bit [2 - 0]		
		SP10[1-0]		SP9[2-0]			SP8[2-0]		
		10		110			110		
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0001_000[R/W]		FAULT STATUS	INTflg	Register Data					

See Table 25 for the selectable wetting current level values for both SPx and SGx pins.

8.9.7 Wetting current level SG register 0

Three bits are used to control the configurable wetting currents for each individual input pin with the values set in the Table 22. The default configuration is 16 mA for all channels. The MCU may change or update the wetting current register via software at any time in Normal mode.

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Table 16. Wetting current level SG register 0

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit [23 - 21]			bit [20 - 18]			bit [17 - 16]	
0000_101	0/1	SG7 [2-0]			SG6[2-0]			SG5[2-1]	
Default on POR		110			110			11	
		bit [15]	bit [14 - 12]			bit [11 - 9]			bit [8]
		SG5[0]	SG4 [2-0]			SG3[2-0]			SG2[2]
		0	110			110			1
		bit [7 - 6]		bit [5 - 3]			bit [2 - 0]		
		SG2[1-0]		SG1[2-0]			SG0[2-0]		
		10		110			110		
MISO Return Word		bits [23 - 0]							
0000_101[R/W]		Register Data							

See Table 25 for the selectable wetting current level values for both SPx and SGx pins.

8.9.8 Wetting current level SG register 1

Three bits are used to control the configurable wetting currents for each individual input pin with the values set in the Table 23. The default configuration is 16 mA for all channels. The MCU may change or update the wetting current register via software at any time in Normal mode.

Table 17. Wetting current level SG register 1

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit [23 - 21]			bit [20 - 18]			bit [17 - 16]	
0000_110	0/1	SG15[2-0]			SG14[2-0]			SG13[2-1]	
Default on POR		110			110			11	
		bit [15]	bit [14 - 12]			bit [11 - 9]			bit [8]
		SG13[0]	SG12 [2-0]			SG11[2-0]			SG10[2]
		0	110			110			1
		bit [7 - 6]		bit [5 - 3]			bit [2 - 0]		
		SG10[1-0]		SG9[2-0]			SG8[2-0]		
		10		110			110		
MISO Return Word		bits [23 - 0]							
0000_110[R/W]		Register Data							

See Table 25 for the selectable wetting current level values for both SPx and SGx pins.

8.9.9 Wetting current level SG register 2

Three bits are used to control the configurable wetting currents for each individual input pin with the values set in the Table 24. The default configuration is 16 mA for all channels. The MCU may change or update the wetting current register via software at any time in Normal mode.

Table 18. Wetting current level SG register 2

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 23	bit 23	bit 23	bit 23	bit 23	bit 23	bit 23
0000_111	0/1	FAULT STATUS	INTflg	Unused					

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Table 18. Wetting current level SG register 2*...continued*

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 23	bit 23	bit 23	bit 23	bit 23	bit 23	bit 23
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit [14 - 12]			bit [11 - 9]			bit 8
		Unused	SG20 [2-0]			SG19[2-0]			SG18[2]
		0	110			110			1
		bit [7 - 6]		bit [5 - 3]			bit [2 - 0]		
		SG18[1-0]		SG17[2-0]			SG16[2-0]		
		10		110			110		
MISO Return Word		bits [23 - 0]							
0000_111[R/W]		Register Data							

See Table 25 for the selectable wetting current level values for both SPx and SGx pins.

Table 19. SPx/SGx selectable wetting current levels

SPx/SGx[2-0]			Wetting current level
bit 2	bit 1	bit 0	
0	0	0	2.0 mA
0	0	1	6.0 mA
0	1	0	8.0 mA
0	1	1	10 mA
1	0	0	12 mA
1	0	1	14 mA
1	1	0	16 mA
1	1	1	20 mA

8.9.10 Continuous wetting current SP register

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparator threshold. When the 20 ms timer expires, the contact current is reduced from the configured wetting current (16 mA) to the sustain current. The wetting current is defined to be an elevated level reducing to the lower sustain current level after the timer has expired. With multiple wetting current timers disabled, power dissipation for the IC must be considered (see Figure 25).

The MCU may change or update the continuous wetting current register via software at any time in Normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the continuous wetting current bit to logic [0] operates normally with a higher wetting current followed by sustain current after 20 ms (pulsed Wetting current operation). Programming to logic [1] enables the continuous wetting current (Table 26) and result in a full time wetting current level. The continuous wetting current register defaults to 0 (pulse wetting current operation).

Table 20. Continuous wetting current SP register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_011	0/1	FAULT STATUS	INTflg	Unused					

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Table 20. Continuous wetting current SP register*...continued*

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0001_011[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.11 Continuous wetting current SG register

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparator threshold. When the 20 ms timer expires, the contact current is reduced from the configured wetting current (16 mA) to 2.0 mA. The wetting current is defined to be at an elevated level that reduces to the lower sustain current level after the timer has expired. With multiple wetting current timers disabled, power dissipation for the IC must be considered.

The MCU may change or update the continuous wetting current register via software at any time in Normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the continuous wetting current bit to logic [0] operates normally with a higher wetting current followed by sustain current after 20 ms (Pulse wetting current operation). Programming to logic [1] enables the continuous wetting current (Table 27) and results in a full time wetting current level. The continuous wetting current register defaults to 0 (pulse wetting current operation).

Table 21. Continuous wetting current SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_100	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0001_100[R/W]		FAULT STATUS	INTflg	Register Data					

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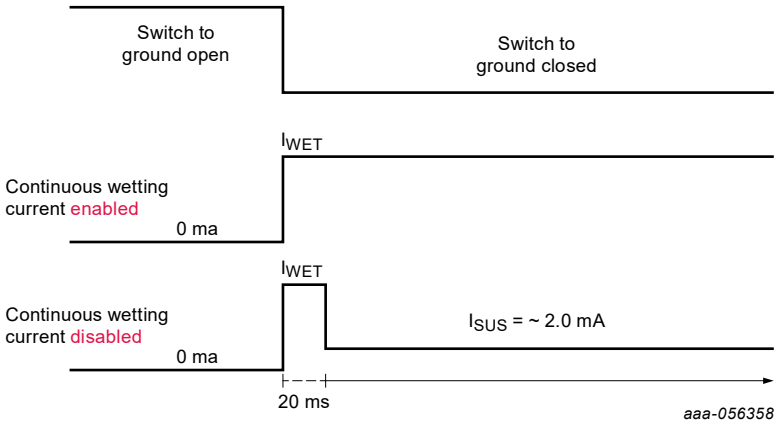


Figure 18. Pulsed/continuous wetting current configuration

8.9.12 Interrupt enable SP register

The interrupt register defines the inputs allowed to interrupt the CD1030 Normal mode. Programming the interrupt bit to logic [0] disables the specific input from generating an interrupt. Programming the interrupt bit to logic [1] enables the specific input to generate an interrupt with switch change of state. The MCU may change or update the interrupt register via software at any time in Normal mode. The Interrupt register defaults to 1 (Interrupt enabled).

Table 22. Interrupt enable SP register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_101	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		1	1	1	1	1	1	1	1
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0001_101[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.13 Interrupt enable SG register

The interrupt register defines the inputs allowed to interrupt the CD1030 Normal mode. Programming the interrupt bit to logic [0] disables the specific input from generating an interrupt. Programming the interrupt bit to logic [1] enables the specific input to generate an interrupt with switch change of state. The MCU may change or update the interrupt register via software at any time in Normal mode. The Interrupt register defaults to 1 (Interrupt enabled).

Table 23. Interrupt enable SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_110	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16

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Table 23. Interrupt enable SG register*...continued*

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
Default on POR		X	X	0	1	1	1	1	1
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		1	1	1	1	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		1	1	1	1	1	1	1	1
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0001_110[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.14 Low-power mode configuration

The device has various configuration settings for the Low-power mode operation. The configuration settings are as follows:

- int[3-0] is used to set the interrupt timer value. With the interrupt timer set, the IC wakes up after the selected timer expires and issues an interrupt. This register can be selected to be OFF such that the IC does not wake-up from an interrupt timer.
- poll[3-0] is used to set the normal polling rate for the IC. The polling rate is the time between polling events. The current sources become active at this time for a time of $t_{ACTIVEPOLLSG}$ or $t_{ACTIVEPOLLSB}$ for SG or SB channels respectively.

Table 24. Low-power mode configuration register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_111	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		int3	int2	int1	int0	poll3	poll2	poll1	poll0
		0	0	0	0	1	1	1	1
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0001_111[R/W]		FAULT STATUS	INTflg	Register Data					

Table 25. Low-power mode configuration bits definition

Bit	Functions	Default value	Description
23	FAULT STATUS	X	It is set when a fault occurs and it is cleared upon reading the fault status register with a fault event no longer present. It is a global variable and clearing the flag once clears it for all registers.
22	INTflg	X	It is set when an interrupt event occurs and it is cleared upon a read/write transaction of a register containing the INTflg. It is a global variable and clearing the flag once clears it for all registers.
21 - 8	Unused	0	Unused

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Table 25. Low-power mode configuration bits definition*...continued*

Bit	Functions	Default value	Description	
7 - 4	int[3-0]	0000	Set the Interrupt timer value	
			• 0000 - OFF • 0001 - 6.0 ms • 0010 - 12 ms • 0011 - 24 ms • 0100 - 48 ms • 0101 - 96 ms • 0110 - 192 ms • 0111 - 394 ms	• 1000 - 4.0 ms • 1001 - 8.0 ms • 1010 - 16 ms • 1011 - 32 ms • 1100 - 64 ms • 1101 - 128 ms • 1110 - 256 ms • 1111 - 512 ms
3 - 0	poll[3-0]	1111	Set the polling rate for switch detection	
			• 0000 - 3.0 ms • 0001 - 6.0 ms • 0010 - 12 ms • 0011 - 24 ms • 0100 - 48 ms • 0101 - 68 ms • 0110 - 76 ms • 0111 - 128 ms	• 1000 - 32 ms • 1001 - 36 ms • 1010 - 40 ms • 1011 - 44 ms • 1100 - 52 ms • 1101 - 56 ms • 1110 - 60 ms • 1111 - 64 ms (default)

8.9.15 Wake-up enable register SP

The wake-up register defines the inputs allowed to wake the CD1030 from Low-power mode. Programming the wake-up bit to logic [0] disables the specific input from waking the IC (Table 32). Programming the wake-up bit to logic [1] enables the specific input to wake-up with switch change of state. The MCU may change or update the wake-up register via software at any time in Normal mode. The Wake-up register defaults to 1 (wake-up enabled). If all channels (SG and SB) have the Wake-up bit disabled, the device disables the polling timer to reduce the current consumption during Low-power mode.

Table 26. Wake-up enable SP register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_000	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		1	1	1	1	1	1	1	1
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0010_000[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.16 Wake-up enable register SG

The wake-up register defines the inputs allowed to wake the CD1030 from Low-power mode. Programming the wake-up bit to logic [0] disables the specific input from waking the IC (Table 33). Programming the wake-up bit to logic [1] enables the specific input to wake-up with any switch change of state. The MCU may change or update the wake-up register via software at any time in Normal mode. The Wake-up register defaults to 1 (wake-up enabled). If all channels (SG and SB) have the Wake-up bit disabled, the device disables the polling timer to reduce the current consumption during Low-power mode.

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Table 27. Wake-up enable SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_001	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default on POR		X	X	0	1	1	1	1	1
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		1	1	1	1	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		1	1	1	1	1	1	1	1
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0010_001[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.17 Comparator only SP

The comparator only register allows the input comparators to be active during LPM with no polling current. In this case, the inputs can receive a digital signal on the order of the LPM clock cycle and wake-up on a change of state. This register is intended to be used for signals that are driven by an external chip and drive to 5.0 V.

Table 28. Comparator only SP register

Register Address	R/W	SPI Data Bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_010	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0010_010[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.18 Comparator only SG

The comparator only register allows the input comparators to be active during LPM with no polling current. In this case, the inputs can receive a digital signal on the order of the LPM clock cycle and wake-up on a change of state. This register is intended to be used for signals driven by an external chip and drive to 5.0 V.

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Table 29. Comparator only SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_011	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0010_011[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.19 LPM voltage threshold SP configuration

The CD1030 is able to use different voltage thresholds to wake-up from LPM. When configured as SG, a Logic [0] means the input uses the LPM delta voltage threshold to determine the state of the switch. A Logic [1] means the input uses the Normal threshold (VICTHR) to determine the state of the switch. When configured as an SB, it only uses the 4.0 V threshold regardless the status of the LPM voltage threshold bit. The user must ensure the correct current level is set to allow the crossing of the normal mode threshold (typ. 4.0 V).

Table 30. LPM voltage threshold configuration SP register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_100	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0010_100[R/W]		FAULT STATUS	INTflg	Register Data					

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8.9.20 LPM voltage threshold SG configuration

The CD1030 is able to use different voltage thresholds to wake-up from LPM. A Logic 0 means the input uses the LPM delta voltage threshold to determine the state of the switch. A Logic [1] means the input uses the Normal threshold (V_{ICTHR}) to determine the state of the switch. The user must ensure the correct current level is set to allow crossing of the normal mode threshold (typ. 4.0 V).

Table 31. LPM voltage threshold configuration SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_101	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0010_101[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.21 Polling current SP configuration

The normal polling current for LPM is 2.0 mA for SB channels and 1.0 mA for SG channels, A logic [0] selects the normal polling current for each individual channel. By writing a Logic [1], the user may choose to select the I_{WET} current value as defined in the wetting current level registers. This results in higher LPM currents, but may be used in cases when a higher polling current is needed.

Table 32. Polling current configuration SP register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_110	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					

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Table 32. Polling current configuration SP register*...continued*

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_110[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.22 Polling current SG configuration

A logic [0] selects the normal polling current for LPM =1.0 mA. By writing a logic [1], the user can select the I_{WET} current value as defined in the wetting current registers for LPM. This results in higher LPM currents, but may be used in cases when a higher polling current is needed.

Table 33. Polling current configuration SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_111	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	**bit 14**	**bit 13**	**bit 12**	**bit 11**	**bit 10**	**bit 9**	**bit 8**
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO Return Word		**bit 23**	**bit 22**	**bits [21 - 0]**					
0010_111[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.23 Slow polling SP

The normal polling rate is defined in the Low-power mode configuration register. If the user is able to poll at a slower rate (4x), the LPM current level decreases significantly. Setting the bit to [0] results in the input polling at the normal rate as selected. Setting the bit to [1] results in the input being polled at a slower frequency at 4x the normal rate.

Table 34. Slow polling SP register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_000	0/1	FAULT STATUS	INTflg	Unused					

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Table 34. Slow polling SP register...*continued*

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0011_000[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.24 Slow polling SG

The normal polling rate is defined in the Low-power mode configuration register. If the user is able to poll at a slower rate (4x), the LPM current level decreases significantly. Setting the bit to [0] results in the input polling at the normal rate as selected. Setting the bit to [1] results in the input being polled at a slower frequency at 4x the normal rate.

Table 35. Slow polling SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_001	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0011_001[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.25 Wake-up debounce SP

The IC is able to extend the time the active polling takes place to ensure a true change of state has occurred in LPM, and reduce the chance noise has impacted the measurement. If this bit is [0], the IC uses a voltage difference technique to determine if a switch has changed state. If this bit is set [1], the IC debounces the measurement by continuing to source the LPM polling current for an additional 1.2 ms and take the

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measurement based on the final voltage level. This helps to ensure the switch is detected correctly in noisy systems.

Table 36. Wake-up debounce SP register

Register Address	R/W	SPI Data Bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_010	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0011_010[R/W]		FAULT STATUS	INTflg	Register Data					

8.9.26 Wake-up debounce SG

The IC is able to extend the time the active polling takes place to ensure a true change of state has occurred in LPM, and reduce the chance noise has impacted the measurement. If this bit is [0], the IC uses a voltage difference technique to determine if a switch has changed state. If this bit is set [1], the IC debounces the measurement by continuing to source the LPM polling current for an additional 1.2 ms, and take the measurement based on the final voltage level. This helps to ensure the switch is detected correctly in noisy systems.

Table 37. Wake-up debounce SG register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_011	0/1	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					
0011_011[R/W]		FAULT STATUS	INTflg	Register Data					

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8.9.27 Enter Low-power mode

Low-power mode (LPM) is used to reduce system quiescent currents. Low-power mode may be entered only by sending the Low-power command. When returning to Normal mode, all register settings are maintained.

The Enter Low-power mode register is write only and has the effect of going to LPM and beginning operation as selected (polling, interrupt timer). When returning from Low-power mode, the CD1030 returns the Read switch status SG register on the first valid SPI transaction. The user should ensure the Read switch status SP register command is sent in the first SPI transaction after POR, to get the remaining SP switch status information in the second SPI transaction.

Table 38. Enter Low-power mode command

Register address	W	SPI data bits [23 - 0]
[31-25]	[24]	bits [23 - 16]
0011_100	1	0000_0000
		bits [15 - 8]
		0000_0000
		bits [7 - 0]
		0000_0000
MISO Return Word		-

8.9.28 AMUX control register

The analog voltage on switch inputs may be read by the MCU using the analog command (Table 45). Internal to the CD1030 is a 35-to-1 analog multiplexer. The voltage present on the selected input pin is buffered and made available on the AMUX output pin. The AMUX output pin is clamped to a maximum of V_{DDQ} volts regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next MISO data stream is logic [0].

Setting the current to wetting current (configurable) may be useful for reading sensor inputs. Analog currents set by the analog command are pull-up currents for all inputs. The MCU may change or update the analog select register via software at any time in Normal mode. The analog select defaults to no input.

Table 39. AMUX control register

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_101	0/1	FAULT STATUS	INTflg	Unused					
Default on POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		Unused	asett0	asel[5-0]					
		0	0	0	0	0	0	0	0
MISO Return Word		bit 23	bit 22	bits [21 - 0]					

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Table 39. AMUX control register...*continued*

Register address	R/W	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_101[R/W]		FAULT STATUS	INTflg	Register Data					

Table 40. AMUX current select

asett[0]	Zsource
0	hi Z (default)
1	I_{WET}

Table 41. AMUX channel select

asel 5	asel 4	asel3	asel 2	asel 1	asel 0	Analog channel select
0	0	0	0	0	0	No Input Selected
0	0	0	0	0	1	SG0
0	0	0	0	1	0	SG1
0	0	0	0	1	1	SG2
0	0	0	1	0	0	SG3
0	0	0	1	0	1	SG4
0	0	0	1	1	0	SG5
0	0	0	1	1	1	SG6
0	0	1	0	0	0	SG7
0	0	1	0	0	1	SG8
0	0	1	0	1	0	SG9
0	0	1	0	1	1	SG10
0	0	1	1	0	0	SG11
0	0	1	1	0	1	SG12
0	0	1	1	1	0	SG13
0	0	1	1	1	1	SG14
0	1	0	0	0	0	SG15
0	1	0	0	0	1	SG16
0	1	0	0	1	0	SG17
0	1	0	0	1	1	SG18
0	1	0	1	0	0	SG19
0	1	0	1	0	1	SG20
0	1	0	1	1	0	SP0
0	1	0	1	1	1	SP1

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Table 41. AMUX channel select*...continued*

asel 5	asel 4	asel3	asel 2	asel 1	asel 0	Analog channel select
0	1	1	0	0	0	SP2
0	1	1	0	0	1	SP3
0	1	1	0	1	0	SP4
0	1	1	0	1	1	SP5
0	1	1	1	0	0	SP6
0	1	1	1	0	1	SP7
0	1	1	1	1	0	SP8
0	1	1	1	1	1	SP9
1	0	0	0	0	0	SP10
1	0	0	0	0	1	SP11
1	0	0	0	1	0	Temp Diode
1	0	0	0	1	1	Battery Sense

8.9.29 Read switch status registers

The CD1030 uses two status registers to provide the status of all 33 input channels. The Read switch status SP register is used to determine the state of each one of the SP inputs and is read only. All of the SP inputs are returned after the next command is sent. A Logic [1] means the switch is closed while a Logic [0] is an open switch.

The Read switch status SG register is used to determine the state of each one of the SG inputs and is read only. All of the SG inputs are returned after the next command is sent. A Logic [1] means the switch is closed while a Logic [0] is an open switch.

Both status registers include two more bits, the Fault Status bit and INTflg bit. The Fault Status bit is a combination of various Fault Status bits in the Fault status register. If any of these bits are set, the Fault Status bit is set. The INTflg bit is set when an interrupt occurs on this device. After POR both the Fault Status bit and the INTflg bit are set high to indicate an interrupt due to a POR occurred.The CD1030 returns the Read switch status SG register on the first valid SPI transaction and the INTflg bit is cleared, the Fault Status bit remains high until the Fault status register is read and thus the POR fault bit and all other fault flags are cleared. User must ensure the Read switch status SP register command is sent in the first SPI transaction after POR in order to get the remaining SP switch status information in the second SPI transaction.

Table 42. Read switch status SP register

Register address	R	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_110	0	FAULT STATUS	INTflg	Unused					

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Table 42. Read switch status SP register*...continued*

Register address	R	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
Default After POR		X	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused				SP11	SP10	SP9	SP8
		0	0	0	0	X	X	X	X
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		X	X	X	X	X	X	X	X
MISO Return Word		bit 23	bit 22	bits [21-12]		bits [11-0]			
0011_1100		FAULT STATUS	INTflg	Unused		SP11- SP0 Switch Status			

Table 43. Read switch status SG register

Register address	R	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_111	0	FAULT STATUS	INTflg	Unused	SG20	SG19	SG18	SG17	SG16
Default After POR		1	1	0	X	X	X	X	X
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		SG15	SG14	SG13	SG12	SG11	SG10	SG9	SG8
		X	X	X	X	X	X	X	X
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		X	X	X	X	X	X	X	X
MISO Return Word		bit 23	bit 22	bit [21]	bits [20-0]				
0011_1110		FAULT STATUS	INTflg	Unused	SG20 - SG0 Switch Status				

8.9.30 Fault status register

To read the fault status bits the user should first sent a message to the IC with the fault status register address followed by any given second command. The MISO response from the second command contains the fault flag information.

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Table 44. Fault status register

Register address	R	SPI data bits [23 - 0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0100_001	0	Unused	INTflg	Unused					
Default After POR		0	X	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused					SPI error	Hash Fault	Unused
		0	0	0	0	0	X	X	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		UV	OV	TempFlag	OT	INT_B Wake	WAKE_B Wake	SPI Wake	POR
		X	X	X	X	X	X	X	X
MISO Return Word		bit 23	bit 22	bits [21-0]					
0100_0010		FAULT STATUS	INTflg	FAULT/FLAG BITS					

Table 45. MISO response for fault status command

Bit	Functions	Default value	Description
23	Unused	0	Unused
22	INTflg	X	Reports an Interrupt has occurred, user should read the status register to determine cause. • Set: Various (SGx change of state, SPx change of state, Extended status bits). • Reset: Clear of fault or read of Status register
21-11	Unused	0	Unused
10	SPI error	X	Any SPI error generates a bit (Wrong address, incorrect modulo). • Set: SPI message error. • Reset: Read fault status register and no SPI errors.
9	Hash Fault	X	SPI register and hash mismatch. • Set: Mismatch between SPI registers and hash. • Reset: No mismatch and SPI flag read.
8	Unused	0	Unused
7	UV	X	Reports a low V_{BATP} voltage was in undervoltage range • Set: Voltage drops below UV level. • Reset: VBATP rises above UV level and flag read (SPI)
6	OV	X	Report the voltage on VBATP was higher than the OV threshold • Set: Voltage at VBATP rises above overvoltage threshold. • Reset: Overvoltage condition is over and flag read (SPI)
5	Temp Flag	X	Temperature warning to note elevated IC temperature • Set: t_{LIM} warning threshold is passed. • Reset: Temperature drops below thermal warning threshold + hysteresis and flag read (SPI)

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Table 45. MISO response for fault status command*...continued*

Bit	Functions	Default value	Description
4	OT	X	T_{LIM} event occurred on the IC • Set: T_{LIM} warning threshold is passed. • Reset: Temperature drops below thermal warning threshold + hysteresis and flag read (SPI)
3	INT_B Wake	X	Part awakens via an external INT_B falling edge • Set: INT_B Wakes the part from LPM (external falling edge) • Reset: flag read (SPI).
2	WAKE_B Wake	X	Part awakens via an external WAKE_B falling edge • Set: External WAKE_B falling edge seen • Reset: flag read (SPI).
1	SPI Wake	X	Part awaken via a SPI message • Set: SPI message wakes the IC from LPM • Reset: flag read (SPI).
0	POR	X	Reports a POR event occurred. • Set: Voltage at VBATP pin dropped below VBATP(POR) voltage • Reset: flag read (SPI)

8.9.31 Interrupt request

The MCU may request an Interrupt pulse duration of 100 µs by sending the Interrupt request command. After an Interrupt request command, the CD1030 returns the Interrupt request command word, as well as the Fault status and INTflg bits set, if a fault/interrupt event occurred. Sending an interrupt request command does not set the INTflg bit itself.

Table 46. Interrupt request command

Register address	W	SPI data bits [23 - 0]		
[31-25]	[24]	bits [23 - 16]		
0100_011	1	0000_0000		
		bits [15 - 8]		
		0000_0000		
		bits [7 - 0]		
		0000_0000		
MISO Return Word		bit 23	bit 22	bits [21-0]
0100_0111		FAULT STATUS	INTflg	0x000000

8.9.32 Reset register

Writing to this register causes all of the SPI registers to reset. The CD1030 behaves in the same way as if a POR has occurred. Both the Fault Status bit and the INTflg bit are set high to indicate an interrupt due to a POR occurred.The CD1030 returns the Read switch status SG register on the first valid SPI transaction and the INTflg bit is cleared, the Fault Status bit remains high until the Fault status register is read and thus the POR fault bit and all other fault flags are cleared. User must ensure the Read switch status SP register command is

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sent in the first SPI transaction after POR, to get the remaining SP switch status information in the second SPI transaction.

Table 47. Reset command

Register address	W	SPI data bits [23 - 0]			
[31-25]	[24]	bits [23 - 16]			
0100_100	1	0000_0000			
		bits [15 - 8]			
		0000_0000			
		bits [7 - 0]			
		0000_0000			
MISO Return Word		bit 23	bit 2	bit 21	bits [20-0]
0011_1110		FAULT STATUS	INTflg	Unused	SG20 - SG0 Switch Status

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9 General product characteristics

9.1 Maximum ratings

Table 48. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
Electrical Ratings					
VBATP	Battery Voltage	-0.3	40	V	
VDDQ	Supply Voltage	-0.3	7.0	V	
CS_B, MOSI, MISO, SCLK	SPI Inputs/Outputs	-0.3	7.0	V	
SGx, SPx	Switch Input Range	-14[(2)]	38	V	
AMUX	AMUX	-0.3	7.0	V	
INT_B	INT_B	-0.3	7.0	V	
WAKE_B	WAKE_B	-0.3	40	V	
V_{ESD1-2} V_{ESD1-3} V_{ESD2-1} V_{ESD2-2}	ESD Voltage • Human Body Model (HBM) (VBATP versus GND) • Human Body Model (HBM) (All other pins) • Charge Device Model (CDM) (Corners pins) • Charge Device Model (CDM) (All other pins)		±4000 ±2000 ±750 ±500	V	(3)
V_{ESD5-3} V_{ESD5-4} V_{ESD6-1} V_{ESD6-2}	Contact Discharge • VBATP • WAKE_B (series resistor 10 kΩ) • SGx and SPx pins with 100 nF capacitor (100 Ω series R) based on external protection performance • SGx and SPx pins with 47 nF capacitor (50 Ω series R)		±8000 ±8000 ±8000 ±8000[(5)]	V	(4),(6)

Notes
2. Minimum value of -18 V is guaranteed by design for switch input voltage range (SGx, SPx).
3. ESD testing is performed in accordance AEC Q100, with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM).
4. C_{ZAP} = 330 pF, R_{ZAP} = 2.0 kΩ (Powered and unpowered) / C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω (Unpowered)
5. C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω (Unpowered)
6. See Table 4 for minimum external component requirements at system level.

Table 49. External component requirements

VBATP Pin	C_{BULK} = 100 µF minimum aluminum electrolytic C_{BYPASS} = 100 nf ±37% minimum ceramic Reverse blocking diode [0.6 V < V_{FWD} < 1.0 V)
VDDQ Pin	C_{BULK} 10 µF Typical aluminum electrolytic (If required by the application) C_{BYPASS} 100 nF minimum ceramic
SGx/SPx Pins	47 nf < C_{ESD} < 100 nF typ ±37% 50 Ω < R_{ESD} < 100 Ω typical

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Table 49. External component requirements*...continued*

Switch Load	5.0 Ω < R_{SW} < 100 Ω Lumped element, includes wire harness 100 kΩ < R_{SW} isolation < ∞
AMUX Output	External capacitor at AMUX Output C_{AMUX} = 1.0 nF

9.2 Thermal characteristics

Table 50. Thermal ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
Thermal Ratings					
T_A T_J	Operating Temperature • Ambient • Junction	-40 -40	125 150	°C	
T_{STG}	Storage Temperature	-65	150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	–	–	°C	
Thermal Resistance					
$R_{\Theta JA}$	Junction-to-Ambient, Natural Convection, Single-layer Board • 48 LQFP		75.4	°C/W	(7) (8)
$R_{\Theta JB}$	Junction-to-Board		13.8	°C/W	(9)
$R_{\Theta JC}$	Junction-to-Case (Bottom) • 48 LQFP		1.5	°C/W	(10)
Ψ_{JT}	Junction-to-Package (Top), Natural convection • 48 LQFP		4.7	°C/W	(11)
Package Dissipation Ratings					
T_{SD}	Thermal Shutdown • 48 LQFP	155	185	°C	
T_{SDH}	Thermal Shutdown Hysteresis • 48 LQFP	3.0	15	°C	

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Table 50. Thermal ratings *...continued*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
Moisture Sensitivity Level					
Moisture	Moisture Sensitivity Level per AEC-Q-100		Level 3		

Notes

7. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
8. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
9. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
10. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
11. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

9.3 Operating conditions

This section describes the operating conditions of the device. Conditions apply to all the following data, unless otherwise noted.

Table 51. Operating conditions

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
VBATP	Battery Voltage	4.5	36	V	
VDDQ	Supply Voltage	3.0	5.25	V	
CS_B, MOSI, MISO, SCLK	SPI Inputs / Outputs	3.0	5.25	V	
SGx, SPx	Switch Input Range	-1.0	36	V	
AMUX, INT_B	AMUX, INT_B	0.0	5.25	V	
WAKE_B	WAKE_B	0.0	36	V	

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9.4 Electrical characteristics

9.4.1 Static electrical characteristics

Table 52. Static electrical characteristics

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
Power Input						
$V_{BATP(POR)}$	VBATP Supply Voltage POR • VBATP Supply Power on Reset voltage	2.7	3.3	3.8	V	
V_{BATPUV}	VBATP Undervoltage Rising Threshold	—	4.3	4.5	V	
$V_{BATPUVHYS}$	VBATP Undervoltage Hysteresis	250	—	500	mV	
V_{BATPOV}	VBATP Overvoltage Rising Threshold	32	—	37	V	
$V_{BATPOVHYS}$	VBATP Overvoltage Hysteresis	1.5	—	3.0	V	
$I_{BAT(on)}$	VBATP Supply Current • All switches open, Normal mode, Tri-state disabled all channels	—	12	16	mA	
$I_{BATP,IQ,LPM,P}$ $I_{BATP,IQ,LPM,F}$	VBATP Low-power Mode Supply Current (polling disabled) • Parametric V_{BATP}, 6.0 V < V_{BATP} < 28 V • Functional Low V_{BATP}, 4.5 V < V_{BATP} < 6.0 V	— —	— —	60 60	µA	(14)
$I_{POLLING,IQ}$	VBATP Polling Quiescent Current (no load) • Polling rate = 3.0 ms • Wake-up enable all channels • All switches open	—	—	20	µA	(12) (13)
$I_{VDDQ,NORMAL}$	Normal Mode (I_{VDDQ}) • SCLK, MOSI, WAKE_B = 0 V, CS_B, INT_B = V_{DDQ}, no SPI communication, AMUX selected no input	—	—	500	µA	
$I_{VDDQ,LPM}$	Logic Low-power Mode Supply Current • SCLK, MOSI = 0 V, CS_B, INT_B, WAKE_B = V_{DDQ}, no SPI communication	—	—	10	µA	
$VDDQ_{UV}$	VDDQ Undervoltage Falling Threshold	2.2	—	2.8	V	
$VDDQ_{UVHYS}$	VDDQ Undervoltage Hysteresis	150	—	350	mV	
$V_{GNDOFFSET}$	Ground Offset • Ground offset of Global pins to IC ground	-1.0	—	1.0	V	
Switch Detection Interface (SG and SP)						
V_{ICTHR}	Switch Detection Threshold	3.7	4.0	4.3	V	(20)
$V_{ICTHRLV}$	Switch Detection Threshold Low Battery • VBATP 4.5 V to 6.0 V	0.55 * V_{BATP}	—	4.3	V	
$V_{ICTHRLPM}$	Switch Detection Threshold Low-power Mode (SG only)	100	—	300	mV	(21)
V_{ICTHRH}	Switch Detection Threshold Hysteresis (4.0 V threshold)	80	—	300	mV	
$V_{ICTH2P5}$	Input Threshold 2.5 V, • Used for Comp Only	2.0	2.5	3.0	V	

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Table 52. Static electrical characteristics...*continued*

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
Switch to ground Input (SG pins)						
I_{LEAKSG_GND}	Leakage to GND • Inputs tristated, voltage at SGx = 36 V; VBATP = 0 V	—	—	2.0	µA	
I_{LEAKSG_BAT}	Leakage to Battery • Inputs tristated, voltage at SGx = GND	—	—	2.0	µA	
I_{SUSSG}	SG Sustain Current • VBATP 6.0 V to 28 V	1.6	2.0	2.4	mA	
$I_{SUSSGLV}$	SG Sustain Current LV(15) • VBATP 4.5 V to 6.0 V	1.0	—	2.4	mA	
I_{WETSG}	Wetting Current Level • Mode 0 = 2.0 mA • Mode 1 = 6.0 mA • Mode 2 = 8.0 mA • Mode 3 = 10 mA • Mode 4 = 12 mA • Mode 5 = 14 mA • Mode 6 = 16 mA • Mode 7 = 20 mA	—	2.0 6.0 8.0 10 12 14 16 20	—	mA	
$I_{WETSGTOL}$	SG Wetting Current Tolerance • Mode 0 • Mode 1 to 7	-20 -10	— —	20 10	%	
$I_{WETSGLV}$	SG Wetting Current Tolerance LV (VBATP 4.5 V to 6.0 V)(15) • Mode 0 = 2.0 mA • Mode 1 = 6.0 mA • Mode 2 = 8.0 mA • Mode 3 = 10 mA • Mode 4 = 12 mA • Mode 5 = 14 mA • Mode 6 = 16 mA • Mode 7 = 20 mA	1.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0	— — — — — — — —	2.4 6.6 8.8 11.0 13.2 15.4 17.6 22.0	mA	
$I_{MATCH(SUS)}$	Sustain Current Matching Between SG Channels	—	—	10	%	(16), (17)
$I_{MATCH(WET)}$	Wetting Current Matching Between SG Channels	—	—	6.0	%	(18), (19)
$I_{ACTIVEPOLLSG}$	Low-power Mode Polling Current SG • VBATP 4.5 V to 28 V	0.7	1.0	1.44	mA	

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Table 52. Static electrical characteristics...*continued*

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
Programmable Input (SP pins)						
I_{LEAKSP_GND}	Leakage to GND • Inputs tristated, voltage at SPx = 36 V; VBATP = 0 V	—	—	2.0	µA	
I_{LEAKSP_BAT}	Leakage to Battery • Inputs tristated, voltage at SPx = GND	—	—	2.0	µA	
I_{SUSSP}	SP Sustain current (VBATP 6.0 V to 28 V) • SP programmed as SG • SP programmed as SB	1.6 1.75	2.0 2.2	2.4 2.85	mA	
$I_{SUSSPLV}$	SP Sustain current - LV (VBATP 4.5 V to 6.0 V) • SP programmed as SG	1.0	—	2.4	mA	(15)
I_{WET0SP}	Wetting Current Level Mode 0 • SP programmed as SG • SP programmed as SB	— —	2.0 2.2	— —	mA	
I_{WETSP}	Wetting Current Level (SG & SB) • Mode 1 = 6.0 mA • Mode 2 = 8.0 mA • Mode 3 = 10 mA • Mode 4 = 12 mA • Mode 5 = 14 mA • Mode 6 = 16 mA • Mode 7 = 20 mA	—	6.0 8.0 10 12 14 16 20	—	mA	
$I_{WETSPTOL}$	Wetting Current Tolerance • SG/SB Mode 0 • SG Mode 1 to 7 • SB Mode 1 to 7	-20 -10 -20	— — —	20 10 20	%	
$I_{WETSPLV}$	Wetting Current Tolerance - LV (VBATP 4.5 V to 6.0 V) (SG configuration) • Mode 0 = 2.0 mA • Mode 1 = 6.0 mA • Mode 2 = 8.0 mA • Mode 3 = 10 mA • Mode 4 = 12 mA • Mode 5 = 14 mA • Mode 6 = 16 mA • Mode 7 = 20 mA Wetting Current Tolerance - LV (VBATP 4.5 V to 6.0 V) (SB configuration) • Mode 0 to 7 = 20 mA	 1.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 -20	 — — — — — — — — —	 2.4 6.6 8.8 11.0 13.2 15.4 17.6 22.0 20	 mA % 	 (15)
$I_{MATCHSUSSP}$	Sustain Current Matching Between SP Channels	—	—	10	%	(16), (17)
$I_{MATCHWETSP}$	Wetting Current Matching Between SP Channels	—	—	6.0	%	(18), (19)
$I_{ACTIVEPOLLSP}$	Low-power Mode Polling Current • SP programmed as SG • SP Programmed as SB	0.7 1.75	1.0 2.2	1.44 2.85	mA	

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Table 52. Static electrical characteristics...*continued*

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
Digital Interface						
I_{HZ}	Tri-state Leakage Current (MISO) • VDDQ = 0.0 to V_{DDQ}	-2.0	—	2.0	µA	
$V_{INLOGIC}$	Input Logic Voltage Thresholds • SI, SCLK, CS_B, INT_B	V_{DDQ} * 0.25	—	V_{DDQ} * 0.7	V	
$V_{INLOGICHYS}$	Input Logic Hysteresis • SI, SCLK, CS_B, INT_B	300	—	—	mV	
$V_{INLOGICWAKE}$	Input Logic Voltage Threshold WAKE_B	0.8	1.25	1.7	V	
V_{INWAKE_BHYS}	Input Logic Voltage Hysteresis WAKE_B	200	—	800	mV	
I_{SCLK}, I_{MOSI}	SCLK / MOSI Input Current • SCLK / MOSI = 0 V	-3.0	—	3.0	µA	
I_{SCLK}, I_{MOSI}	SCLK / MOSI Pull-down Current • SCLK / MOSI = V_{DDQ}	30	—	100	µA	
I_{CS_BH}	CS_B Input Current • CS_B = V_{DDQ}	-10	—	10	µA	
R_{CS_BL}	CS_B Pull-up Resistor to VDDQ • CS_B = 0.0 V	40	125	270	kΩ	
V_{OHMISO}	MISO High-side Output Voltage • I_{OHMISO} = -1.0 mA	V_{DDQ} – 0.8	—	V_{DDQ}	V	
V_{OLMISO}	MISO Low-side Output Voltage • I_{OLMISO} = 1.0 mA	—	—	0.4	V	
C_{IN}	Input Capacitance on SCLK, MOSI, Tri-state MISO (GBD)	—	—	20	pF	
Analog MUX Output						
V_{OFFSET}	Input Offset Voltage When Selected as Analog	-15	—	15	mV	
V_{OLAMUX}	Analog Operational Amplifier Low Output Voltage • Sink 1.0 mA	—	—	50	mV	
V_{OHAMUX}	Analog Operational Amplifier High Output Voltage • Source 1.0 mA	V_{DDQ} – 0.1	—	—	V	
AMUX Selectable Outputs						
Temp-Coeff	Chip Temperature Sensor Coefficient	—	8.0	—	mV/°C	
$V_{BATSNSACC}$	Battery Sense (SG5 config) Accuracy • Battery voltage (SG5 input) divided by 6 • Accuracy over full temperature range	-5.0	—	5.0	%	
$V_{BATSNSDIV}$	Divider By 6 coefficient accuracy • Offset over operating voltage range (VBATP = 6.0 V to 28 V)	-3.0	—	3.0	%	(22)
INT_B						
V_{OLINT}	INT_B Output Low Voltage • I_{OUT} = 1.0 mA	—	0.2	0.5	V	
V_{OHINT}	INT_B Output High Voltage • INT_B = Open-circuit	V_{DDQ} – 0.5	—	V_{DDQ}	V	
R_{PU}	Pull-up Resistor to VDDQ	40	125	270	kΩ	
$I_{LEAKINT_B}$	Leakage Current INT_B • INT_B pulled up to VDDQ	—	—	1.0	µA	

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Table 52. Static electrical characteristics...*continued*

T_A = - 40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Units	Notes
Temperature Limit						
t_{FLAG}	Temperature Warning • First flag to trip	105	120	135	°C	
t_{LIM}	Temperature Monitor	155	—	185	°C	(23)
$t_{LIM(HYS)}$	Temperature Monitor Hysteresis	5.0	—	15	°C	(23)
WAKE_B						
$R_{WAKE_B(RPU)}$	WAKE_B Internal pull-up Resistor to VDDQ	40	125	270	kΩ	
$V_{WAKE_B(VOH)}$	WAKE_B Voltage High • WAKE_B = Open-circuit	V_{DDQ} -1.0	—	V_{DDQ}	V	
$V_{WAKE_B(VOL)}$	WAKE_B Voltage Low • WAKE_B = 1.0 mA (R_{PU} to V_{BATP} = 16 V)	—	—	0.4	V	
I_{WAKE_BLEAK}	WAKE_B Leakage • WAKE_B pulled up to V_{BATP} = 16 V through 10 kΩ	—	—	1.0	µA	

Notes

12. Guaranteed by design
13. Polling quiescent current refers to the additional current in low-power mode due to the polling mechanism without any loading. $I_{POLLING,IQ}$ depends directly on the Polling rate and it increases as the polling pulse is more frequent. Worst case scenario is polling rate = 3.0 ms, with all channels set to wake-up enable.
14. Total maximum quiescent current with polling enabled in LPM is given by $I_{BATP,LPM,IQ}$ + $I_{POLLING,IQ}$
15. During low voltage range operation SG wetting current may be limited when there is not enough headroom between VBATP and SG pin voltage.
16. ($I_{SUS(MAX)}$– $I_{SUS(MIN)}$) X 100/$I_{SUS(MIN)}$
17. Sustain current source (SGs only)
18. ($I_{WET(MAX)}$ – $I_{WET(MIN)}$) X 100/$I_{WET(MIN)}$
19. Wetting current source (SGs only)
20. The input comparator threshold decreases when V_{BATP} ≤ 6.0 V.
21. SP (as SB) only use the 4.0 V V_{ICTHR} for LPM wake-up detection.
22. Calibration of divider ratio can be done at V_{BAT} = 12 V, 25 °C to achieve a higher accuracy. See Figure 4 for AMUX offset linearity waveform through the operating voltage range.
23. Guaranteed by characterization in the development phase, parameter not tested.

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9.4.2 Dynamic electrical characteristics

Table 53. Dynamic electrical characteristics

T_A = -40 °C to +125 °C. VDDQ = 3.1 V to 5.25 V, VBATP = 4.5 V to 28 V, unless otherwise specified. SPI timing is performed with a 100 pF load on MISO, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
General						
t_{ACTIVE}	POR to Active time • Undervoltage to Normal mode	250	340	450	µs	
Oscillator						
OSC_{TOLNOR}	Oscillator Tolerance Normal Mode at 4.0 MHz	-15	—	15	%	
OSC_{TOLLPM}	Oscillator Tolerance at 192 kHz in Low-power Mode	-15	—	15	%	
Switch Input						
$t_{PULSE(ON)}$	Pulse Wetting Current Timer • Normal mode	17	20	23	ms	
$t_{INT-DLY}$	Interrupt Delay Time • Normal mode	—	—	18.5	µs	
$t_{POLLING_TIMER}$	Polling Timer Accuracy • Low-power mode	—	—	15	%	
$t_{INT-TIMER}$	Interrupt Timer Accuracy • Low-power mode	—	—	15	%	
$t_{ACTIVEPOLLSG}$	Tactivepoll Timer SG	49.5	58	66.5	µs	
$t_{ACTIVEPOLLSB}$	Tactivepoll Timer SB • SBPOLLTIME=0 • SBPOLLTIME=1	1.0 49.5	1.2 58	1.4 66.5	ms µs	
$t_{GLITCHTIMER}$	Input Glitch Filter Timer • Normal mode	5.0	—	18	µs	
$t_{DEBOUNCE}$	LPM Debounce Additional Time • Low-power mode	1.0	1.2	1.4	ms	
AMUX Output						
$AMUX_{VALID}$	AMUX Access Time (Selected Output to Selected Output) • C_{MUX} = 1.0 nF, Rising edge of CS_B to selected	—	(25)	—	µs	
$AMUX_{VALIDTS}$	AMUX Access Time (Tristate to ON) • C_{MUX} = 1.0 nF, Rising edge of CS_B to selected	—	—	20	µs	
Interrupt						
INT_{PULSE}	Interrupt Pulse Duration • Interrupt occurs or INT_B request	90	100	110	µs	

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Table 53. Dynamic electrical characteristics...*continued*

T_A = -40 °C to +125 °C. VDDQ = 3.1 V to 5.25 V, VBATP = 4.5 V to 28 V, unless otherwise specified. SPI timing is performed with a 100 pF load on MISO, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
SPI Interface						
f_{OP}	Transfer Frequency	—	—	8.0	MHz	
t_{SCK}	SCLK Period • Figure 7 - 1	160	—	—	ns	
t_{LEAD}	Enable Lead Time • Figure 7 - 2	140	—	—	ns	
t_{LAG}	Enable Lag Time • Figure 7 - 3	50	—	—	ns	
t_{SCKHS}	SCLK High Time • Figure 7 - 4	56	—	—	ns	
t_{SCKLS}	SCLK Low Time • Figure 7 - 5	56	—	—	ns	
t_{SUS}	MOSI Input Setup Time • Figure 7 - 6	16	—	—	ns	
t_{HS}	MOSI Input Hold Time • Figure 7 - 7	20	—	—	ns	
t_A	MISO Access Time • Figure 7 - 8	—	—	116	ns	
t_{DIS}	MISO Disable Time (24) • Figure 7 - 9	—	—	100	ns	
t_{VS}	MISO Output Valid Time • Figure 7 - 10	—	—	116	ns	
t_{HO}	MISO Output Hold Time (No cap on MISO) • Figure 7 - 11	20	—	—	ns	
t_{RO}	Rise Time • Figure 7 - 12	—	—	30	ns	(24)
t_{FO}	Fall Time • Figure 7 - 13	—	—	30	ns	(24)
t_{CSN}	CS_B Negated Time • Figure 7 - 14	500	—	—	ns	

Notes

24. Guaranteed by characterization.

25. AMUX settling time to be within the 10 mV offset specification. $AMUX_{VALID}$ is dependent of the voltage step applied on the input SGx/SPx pin or the difference between the first and second channel selected as the multiplexed analog output. See Figure 9 for a typical AMUX access time versus voltage step waveform.

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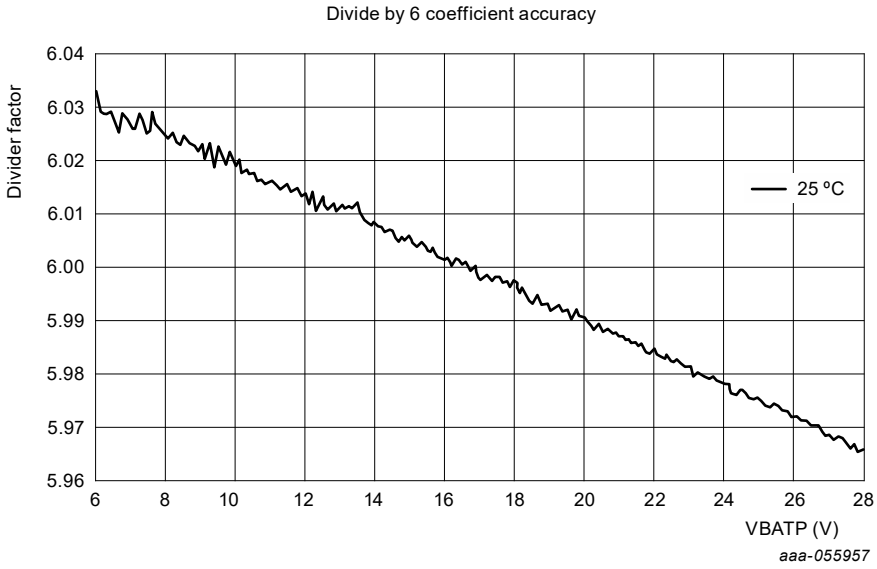


Figure 19. Divide by 6 coefficient accuracy

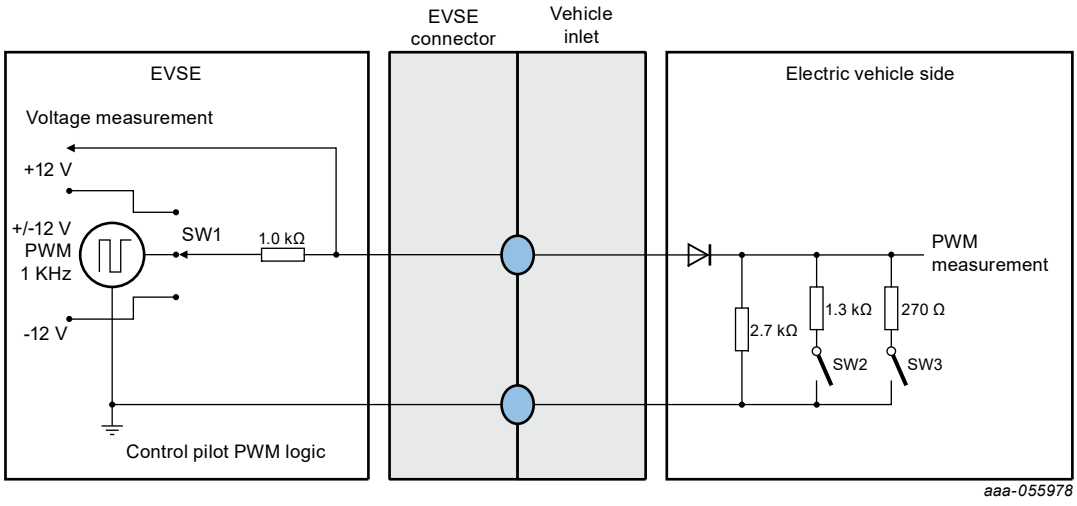


Figure 20. Glitch filter and interrupt delay timers

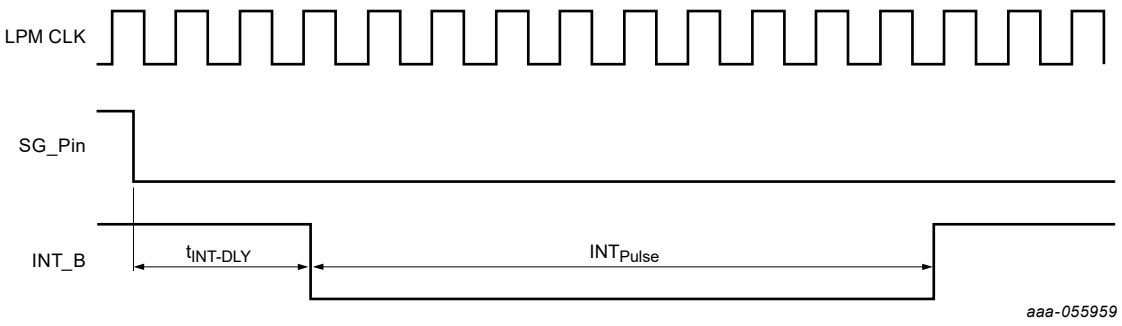


Figure 21. Interrupt pulse timer

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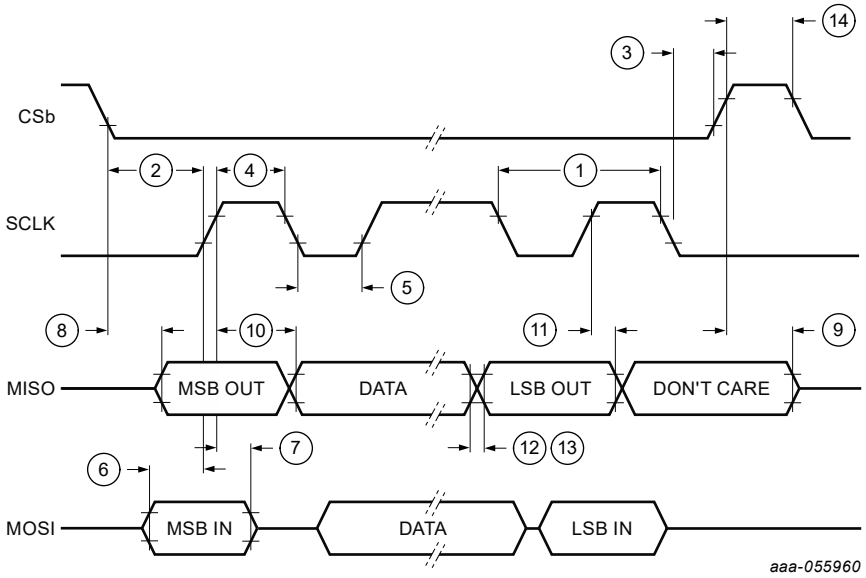


Figure 22. SPI timing diagram

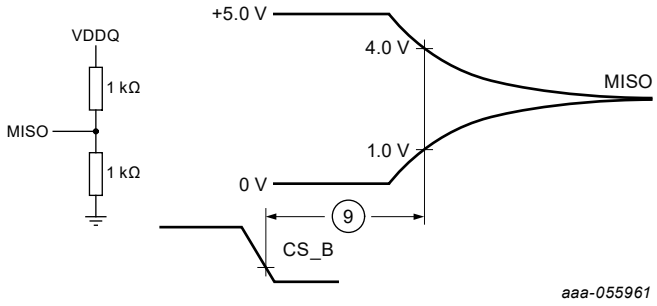


Figure 23. MISO loading for disable time measurement

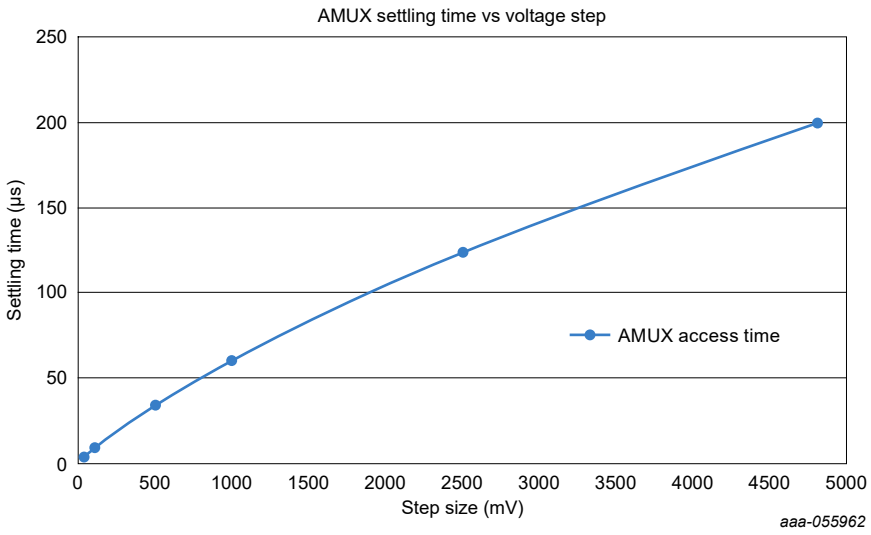


Figure 24. AMUX access time waveform

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10 Typical applications

10.1 Simplified application diagram

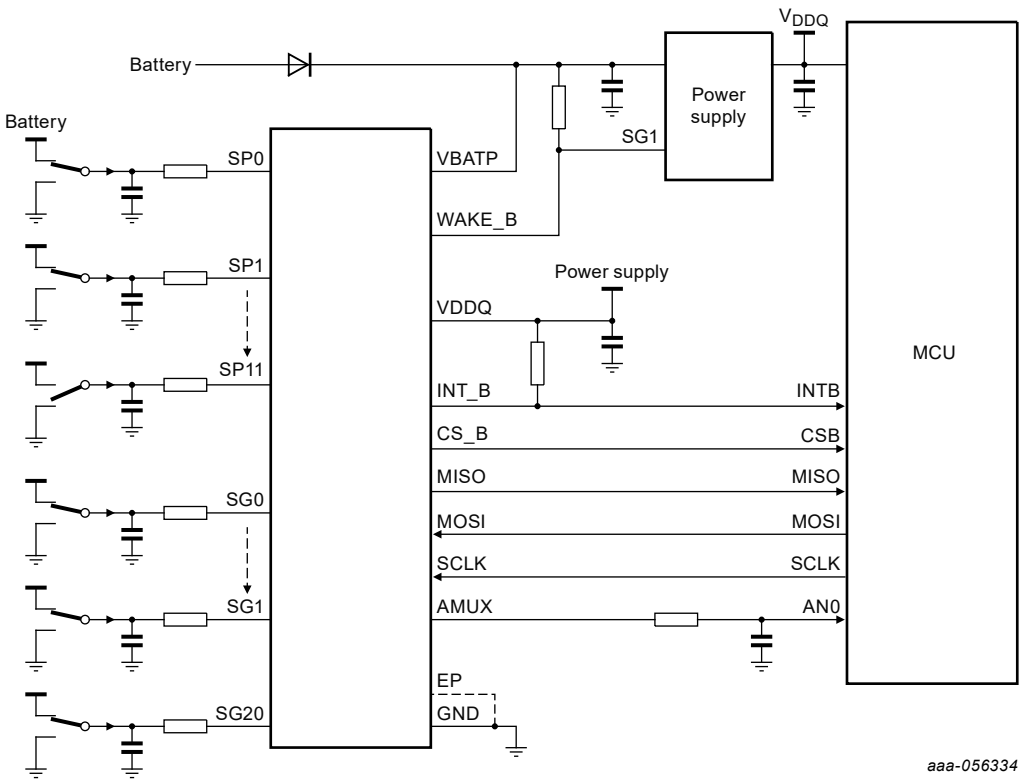


Figure 25. CD1030 simplified application diagram

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10.2 Application diagram

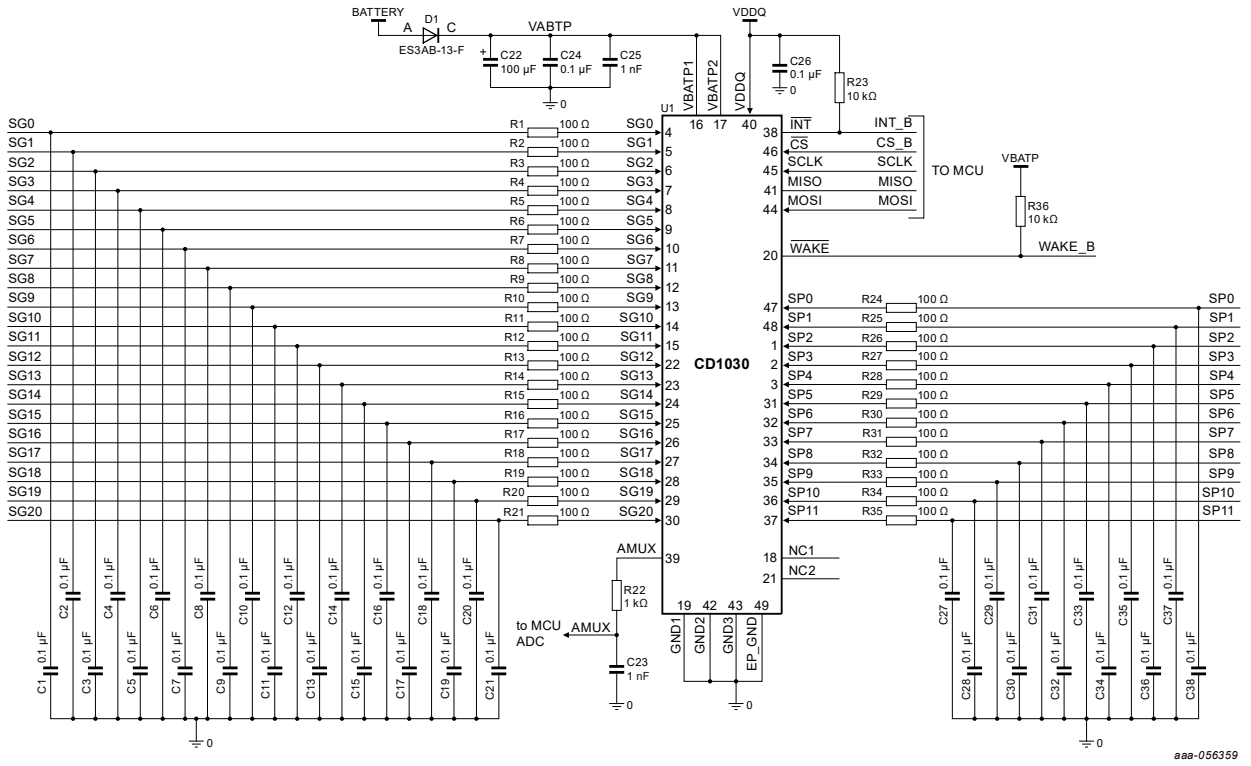


Figure 26. Typical application diagram

10.3 Bill of materials

Table 54. Bill of materials

Item	Quantity	Reference	Value	Description
1	35	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C24, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38	0.1 µF	CAP CER 0.1 µF 100 V X7R 10% 0603
2	1	C22	100 µF	CAP ALEL 100 µF 50 V 20% -- SMD
3	2	C23, C25	1.0 nF	CAP CER 1000 PF 100 V 10% X7R 0603
4	1	D1	ES3AB-13-F	DIODE RECT 3.0 A 50 V AEC-Q101 SMB
5	33	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35	100	RES MF 100 Ω 1/10 W 1% 0805
6	1	R22	1.0 k	RES MF 1.0 kΩ 1/10 W 5% 0805
7	2	R36, R23	10 k	RES MF 10 kΩ 1/10 W 5% 0805
8	1	U1	CD1030	IC MULTIPLE DETECTION SWITCH INT ERFACE LQFP48

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10.4 Abnormal operation

The CD1030 could be subject to various conditions considered abnormal as defined within this section.

10.4.1 Reverse battery

This device with applicable external components is not damaged by exposure to reverse battery conditions of -14 V. This test is performed for a period of one minute at 25 °C. In addition, this negative voltage condition does not force any of the logic level I/O pins to a negative voltage less than -0.6 V at 10 mA or to a positive voltage greater than 5.0 V. This ensures protection of the digital device interfacing with this device.

10.4.2 Ground offset

The applicable driver outputs and/or current sense inputs are capable of operation with a ground offset of ±1.0 V. The device is not damaged by exposure to this condition and maintains specified functionality.

10.4.3 Shorts to ground

All I/Os of the device that are available at the module connector are protected against shorts to ground with maximum ground offset considered (-1.0 V referenced to device ground or other application specific value). The device is not damaged by this condition.

10.4.4 Shorts to battery

All I/Os of the device available at the module connector are protected against a short to battery (voltage value is application dependent, although there may be cases where short to jump start or load dump voltage values are required). The device is not damaged by this condition.

10.4.5 Unpowered shorts to battery

All I/Os of the device available at the module connector are protected against unpowered (battery to the module is open) shorts to battery per application specifics. The device is not damaged by this condition, and does not enable any outputs nor backfeed onto the power rails (VBATP, VDDQ) or the digital I/O pins.

10.4.6 Loss of module ground

The definition of a loss of ground condition at the device level is all pins of the IC detects very low-impedance to battery. The nomenclature is suited to a test environment. In the application, a loss of ground condition results in all I/O pins floating to battery voltage, while all externally referenced I/O pins are at worst case pulled to ground. All applicable driver outputs and current sense inputs are protected against excessive leakage current due to loads referenced to an external ground (high-side drivers).

10.4.7 Loss of module battery

The loss of battery condition at the parts level is the power input pins of the IC see infinite impedance to the battery supply voltage (depending upon the application), but there is some undefined impedance looking from these pins to ground. All applicable driver outputs and current sense inputs are protected against excessive leakage current due to loads referenced to an external battery connection (low-side drivers).

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11 Packaging

11.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 55. Packaging information

Package	Suffix	Package outline drawing number
48-Pin LQFP-EP	AE	98ASA00173D

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11.2 Package drawing

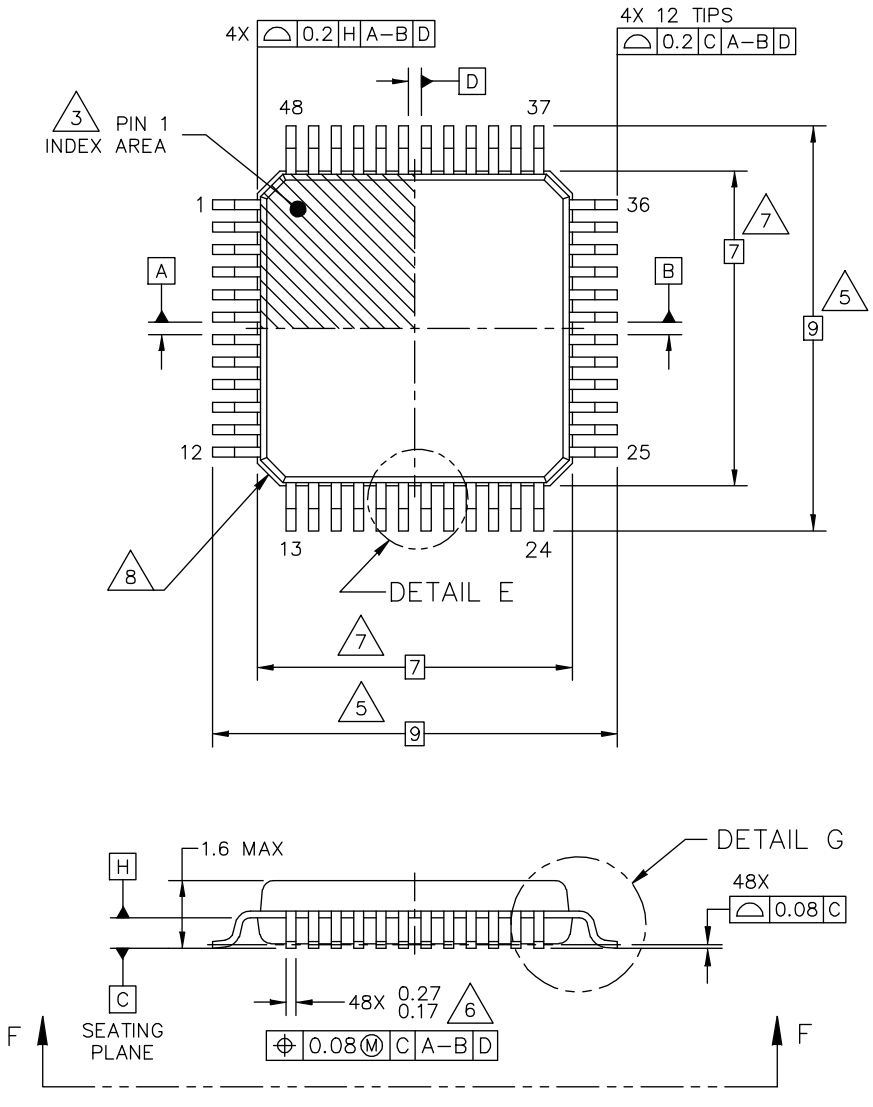


Figure 27. 98ASA00173D package outline

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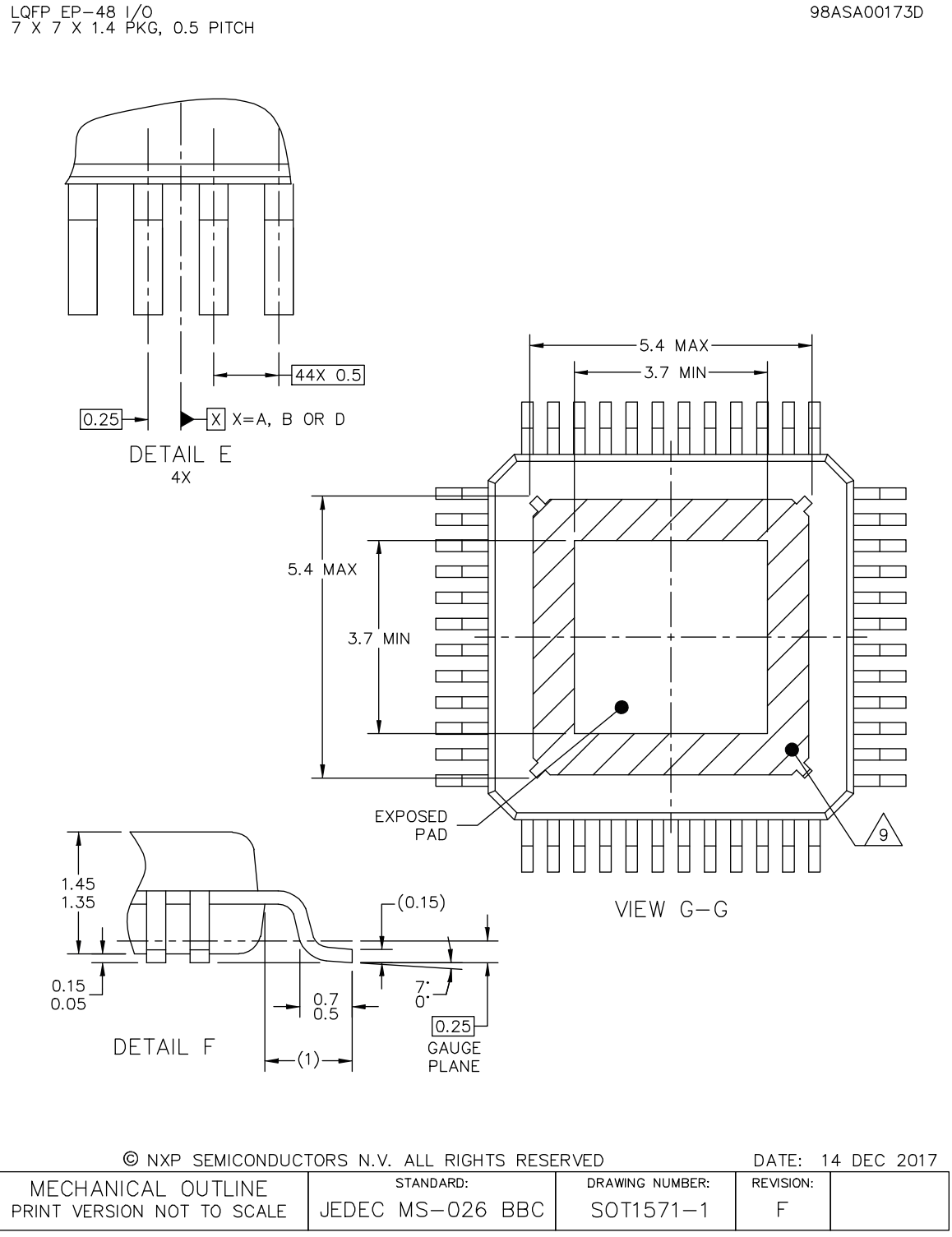


Figure 28. 98ASA00173D detail

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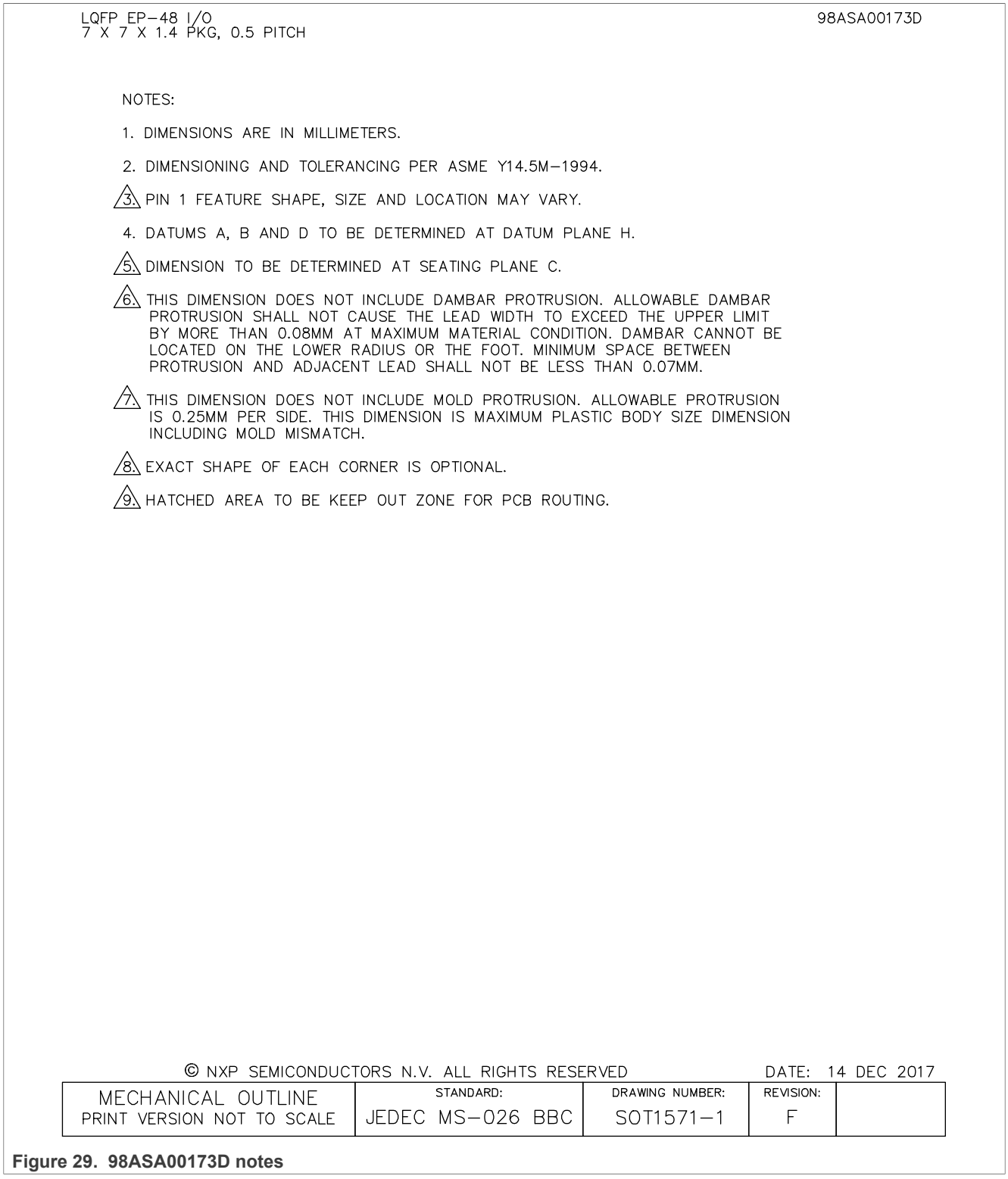


Figure 29. 98ASA00173D notes

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12 Reference section

Table 56. CD1030 reference documents

Reference	Description
CDF-AEC-Q100	Stress Test Qualification For Automotive Grade Integrated Circuits
Q-1000	Qualification Specification for Integrated Circuits
SQ-1001	Specification Conformance

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13 Revision history

Revision	Date	Description
6.0	20 August 2024	• CIN 202407013I • Corrected Section 1 to include Polling state • Replaced all instances of *master* with *primary* or *primary device* – Section 8.8.2 (two instances) – Section 8.8.4 (one instance) • Replaced all instances of *slave* with *secondary* or *secondary device* – Section 6.2 (two instances) – Section 8.8 (one instance) • Updated format and organization to match current NXP template • Updated Section 11.2 to rev F • Updated legal information
5.0	July 2018	• Changed document status from Advance Information to Technical Data
4.0	March 2017	• Corrected typo in Figure 2 • Added Note 2 to switch input voltage range in Table 3
3.0	January 2016	• Relaxed AMUX offset specification to ±15 mV • Updated Figure 16 to clarify LPM operation • Clarified 20% tolerance for SB wetting current in LV condition • Corrected MISO operation description, the CD1030 also shift data out on the Falling edge of SCLK • Deleted PC34CD1030AE from the Orderable Part Variations table
2.0	July 2015	• Deleted statement: Short to ground is detectable by internal diagnostics • Deleted statement: Short to battery is detectable by internal diagnostics • Changed test conditions on $I_{POLLING,IQ}$ to make sure the worst case is being considered (3.0 ms) • Added Note 13 and Note 14 to clarify LPM current specification • VDDQ bulk capacitor marked a 10 µF typical value if required by the application • Updated $I_{BATP(ON)}$ to Typ = 12 mA, Max = 16 mA • Clarified WAKE_B operation • Updated VBATP HBM specification to 4.0 KV
1.0	July 2015	• Initial Release

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Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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