SGM51223Q
Automotive, 12-Bit, 2MSPS, 1-Channel, Single-Ended, Serial Interface ADC

GENERAL DESCRIPTION

The SGM51223Q is a 12-bit, 1-channel input, successive approximation (SAR) analog-to-digital converter (ADC).

The SGM51223Q analog power supply range is 2.35V to 3.6V. The SGM51223Q has an SPI-compatible interface with the digital power supply range of 1.65V to 3.6V.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM51223Q is available in a Green VSSOP-8 package. It operates over an ambient temperature range -40℃ to +125℃.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Unipolar Input Range: 0V to AVDD**
- **Support Single-Ended Input**
- **Ultra-Low Power Consumption:**
  3.96mW (TYP) at 2MSPS with 3.6V AVDD
- **Throughput:**
  2MSPS with Zero Data Latency
- **Excellent Performance:**
  - **12-Bit Resolution with NMC**
  - **INL: ±0.8LSB (TYP)**
  - **DNL: ±0.5LSB (TYP)**
  - **SNR: 72dB (TYP) at f_{IN} = 2kHz**
  - **THD: -80dB (TYP) at f_{IN} = 2kHz**
- **Integrated Offset Calibration**
- **SPI-Compatible Serial Interface**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in a Green VSSOP-8 Package**

代理商 威尔迈 www.visvie.com
联系电话 138 2526 5270

APPLICATIONS

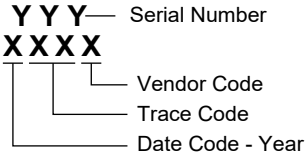
Automotive Infotainment
Automotive Sensors
Portable Medical Equipment
Ultrasonic Flow Meters
Motor Control
Level Sensors

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM51223Q	VSSOP-8	-40℃ to +125℃	SGM51223QVS8G/TR	0PB XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respected to GND)
- AVDD ..... -0.3V to 3.9V
- DVDD ..... -0.3V to 3.9V
- AINP ..... -0.3V to AVDD + 0.3V
- AINM ..... -0.3V to 0.3V
- Digital Input Voltage ..... -0.3V to DVDD + 0.3V

Package Thermal Resistance
- VSSOP-8, θ_{JA} ..... 166.2℃/W
- VSSOP-8, θ_{JB} ..... 98℃/W
- VSSOP-8, θ_{JC} ..... 68.5℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage Range, AVDD ..... 2.35V to 3.6V
Digital Supply Voltage Range, DVDD ..... 1.65V to 3.6V
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

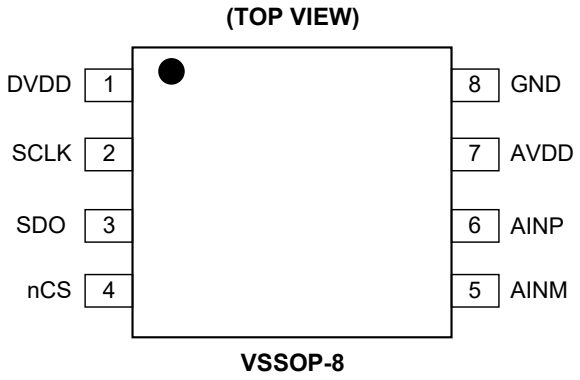
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	DVDD	P	Digital Supply Voltage Pin.
2	SCLK	DI	Serial Clock Pin.
3	SDO	DO	Serial Data Out Pin.
4	nCS	DI	Chip Select Pin. Active low.
5	AINM	AI	Negative Analog Signal Input Pin.
6	AINP	AI	Positive Analog Signal Input Pin.
7	AVDD	P	Analog Power Supply Input Pin. It also provides the reference voltage for the ADC.
8	GND	P	Ground.

NOTE: AI = analog input, DI = digital input, DO = digital output, P = power.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, AVDD = 2.35V to 3.6V, DVDD = 1.8V to 3.6V, f_{SAMPLE} = 2MSPS, and V_{AINM} = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input						
Full-Scale Input Voltage Span (1)		AINP - AINM	0		AVDD	V
Absolute Input Voltage Range		AINP to GND	-0.1		AVDD + 0.1	V
		AINM to GND	-0.1		0.1	
Sampling Capacitance (6)	C_S			18		pF
System Performance						
Resolution				12		Bits
No Missing Codes	NMC		12			Bits
Integral Nonlinearity	INL		-3.5	±0.8	3.2	LSB (2)
Differential Nonlinearity	DNL		-0.999	±0.5	1	LSB
Offset Error	E_O	Uncalibrated		±16		LSB
		Calibrated (3)	-2.5	0.5	3	
Offset Error Drift with Temperature	dV_{OS}/dT			1.8		ppm/℃
Gain Error	E_G		-0.22	-0.1	0.033	%FS
Gain Error Drift with Temperature		No calibration		1.9		ppm/℃
Sampling Dynamics						
Acquisition Time	t_{ACQ}		90			ns
Maximum Throughput Rate		32MHz SCLK, AVDD = 2.35V to 3.6V			2	MHz
Dynamic Characteristics						
Signal-to-Noise Ratio (4)	SNR	f_{IN} = 250kHz		72		dB
		f_{IN} = 2kHz	66.5	72		
Total Harmonic Distortion (4) (5)	THD	f_{IN} = 250kHz		-79		dB
		f_{IN} = 2kHz	-67	-80		
Signal-to-Noise + Distortion (4)	SINAD	f_{IN} = 250kHz		71		dB
		f_{IN} = 2kHz	65	71		
Spurious Free Dynamic Range (4)	SFDR	f_{IN} = 250kHz		80		dB
		f_{IN} = 2kHz	67.5	80		
Full Power Bandwidth	$BW_{(fp)}$	At -3dB, AVDD = 2.35V to 3.6V		100		MHz

NOTES:

1. Ideal input range. It does not consider gain and offset error.

2. LSB = Least Significant Bit.

3. Refer to the Offset Calibration section. It is recommended to perform offset calibration during normal operation.

4. All specifications are tested with an input signal at 0.5dB below full-scale, unless otherwise noted. All available input ranges are described in full-scale input range (FSR), but not performance guaranteed.

5. Calculated on the first nine harmonics of the input frequency.

6. Guaranteed by design and characterization. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, AVDD = 2.35V to 3.6V, DVDD = 1.65V to 3.6V, f_{SAMPLE} = 2MSPS, and V_{AINM} = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input/Output (CMOS Logic Family)						
High-Level Input Voltage	V_{IH}		0.7 × DVDD		DVDD + 0.3	V
Low-Level Input Voltage	V_{IL}		-0.3		0.3 × DVDD	V
High-Level Output Voltage	V_{OH}	I_{SOURCE} = 500μA	0.8 × DVDD		DVDD	V
		I_{SOURCE} = 2mA	DVDD - 0.45		DVDD	
Low-Level Output Voltage	V_{OL}	I_{SINK} = 500μA	0		0.2 × DVDD	V
		I_{SINK} = 2mA	0		0.45	
Power Supply Requirements						
Analog Supply Voltage	AVDD		2.35	3	3.6	V
Digital I/O Supply Voltage	DVDD		1.65	3	3.6	V
Analog Supply Current	I_{AVDD}	At 2MSPS with AVDD = 3.6V		1100	1300	μA
Digital Supply Current	I_{DVDD}	AVDD = 3.6V, no load, no transitions		10		μA
Power Dissipation	P_D	At 2MSPS with AVDD = 3.6V		3.96	4.68	mW

TIMING REQUIREMENTS

(T_A = -40℃ to +125℃, AVDD = 2.35V to 3.6V, DVDD = 1.65V to 3.6V, and C_{LOAD} on SDO = 20pF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_2		90			ns
SCLK Frequency	f_{SCLK}		0.016		32	MHz
SCLK Period	t_6		31.25			ns
SCLK High Time	t_4		0.45		0.55	t_{SCLK}
SCLK Low Time	t_5		0.45		0.55	t_{SCLK}
nCS High Time	t_7		30			ns
Setup Time: nCS Falling to SCLK Falling	t_3		12			ns
Delay Time: Last SCLK Falling to nCS Rising	t_8		10			ns

SWITCHING CHARACTERISTICS

(T_A = -40℃ to +125℃, AVDD = 2.35V to 3.6V, DVDD = 1.65V to 3.6V, and C_{LOAD} on SDO = 20pF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Throughput	$f_{THROUGHPUT}$				2	MSPS
Cycle Time	t_C		0.5			μs
Conversion Time	t_1			$12.5 \times t_6 + t_3$		ns
Delay Time: nCS Falling to Data Enable	t_9	DVDD = 1.65V to 1.8V			20	ns
		DVDD = 1.8V to 3.6V			15	
Delay Time: SCLK Falling to (Next) Data Valid on DOUT	t_{10}	DVDD = 1.65V to 1.8V			30	ns
		DVDD = 1.8V to 3.6V			25	
Delay Time: nCS Rising to DOUT Going to Tri-State	t_{11}		5			ns

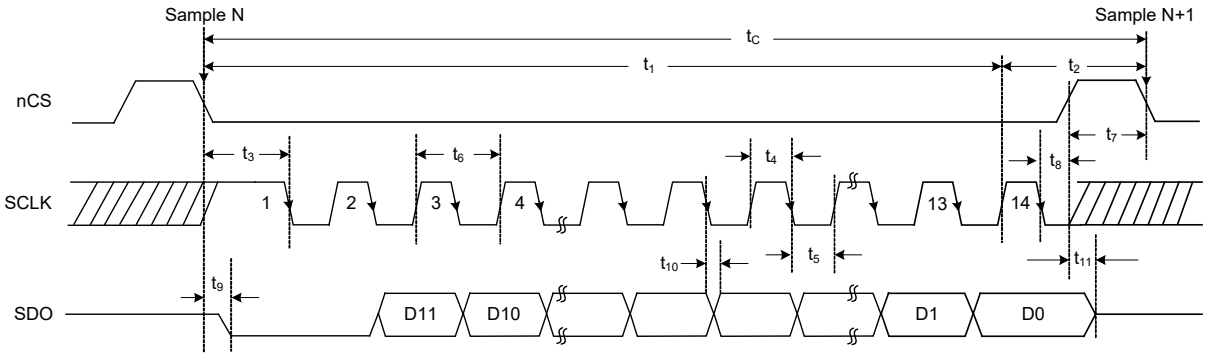
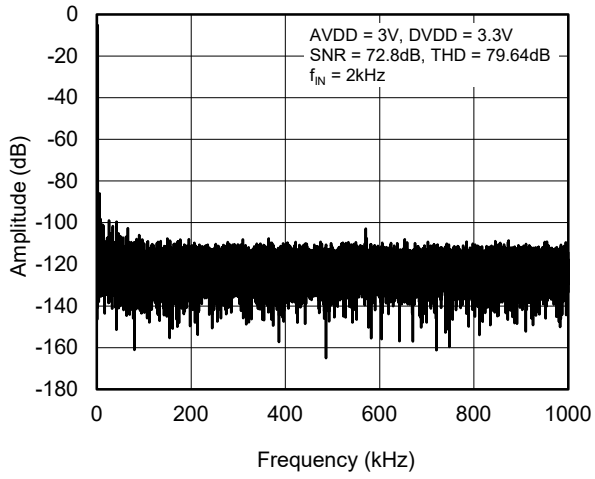


Figure 1. Serial Interface Timing Diagram

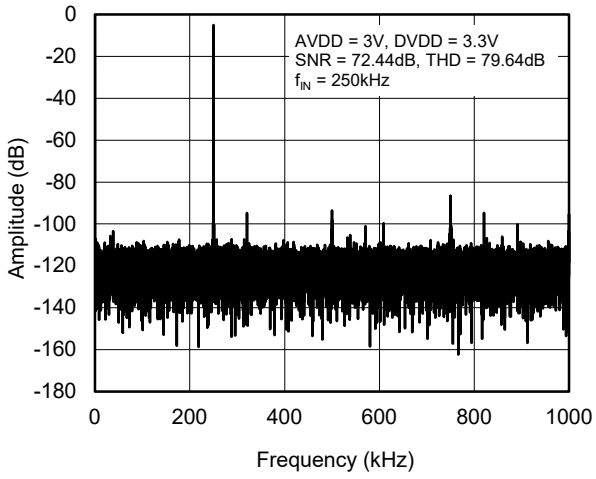
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, AVDD = 3V, DVDD = 3.3V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

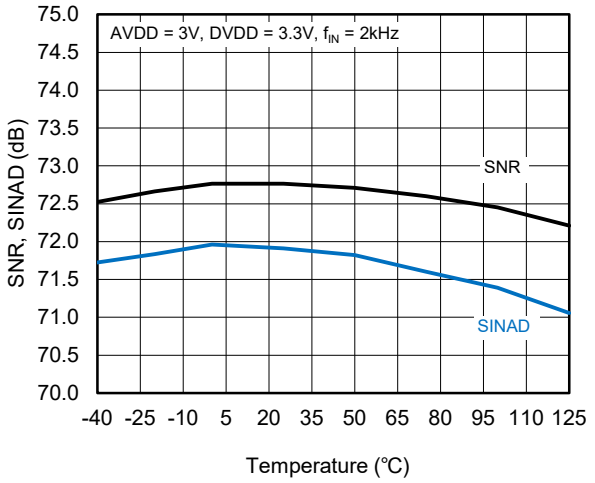
Typical FFT



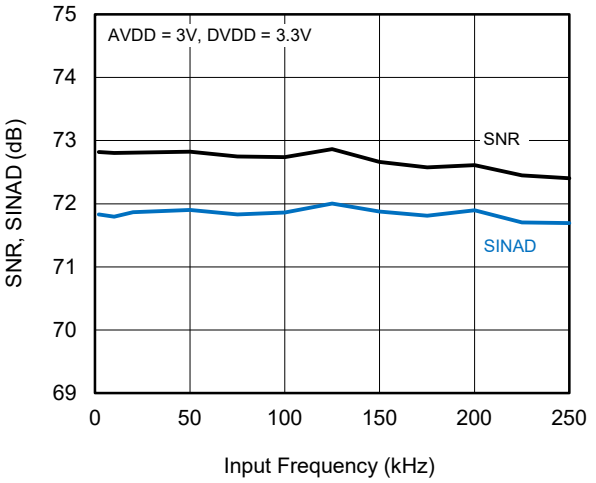
Typical FFT



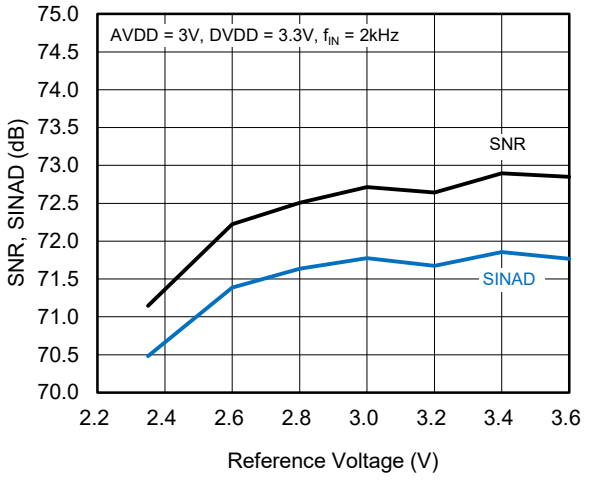
SNR, SINAD vs. Temperature



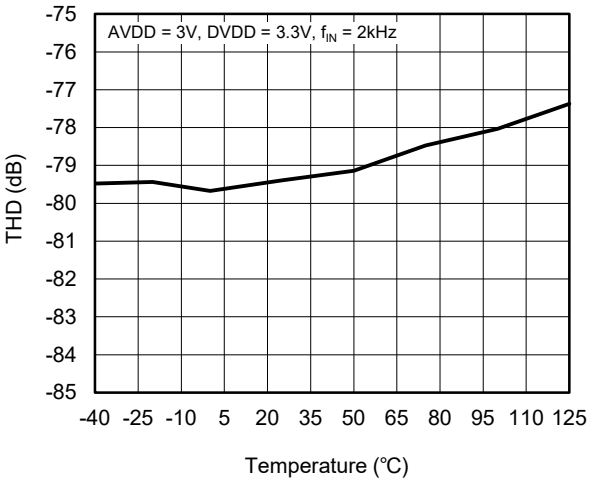
SNR, SINAD vs. Input Frequency



SNR, SINAD vs. Reference Voltage (AVDD)



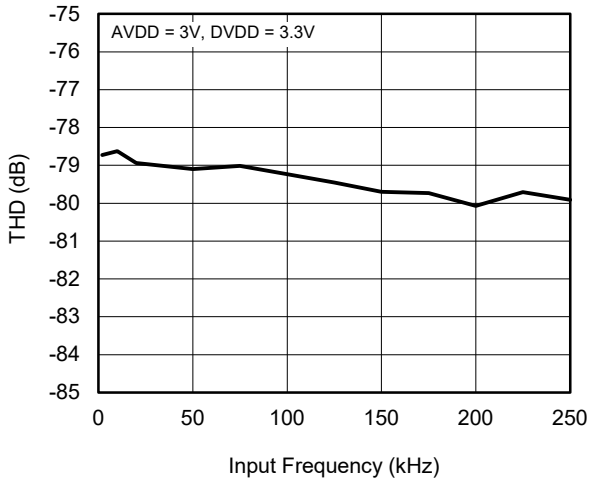
THD vs. Temperature



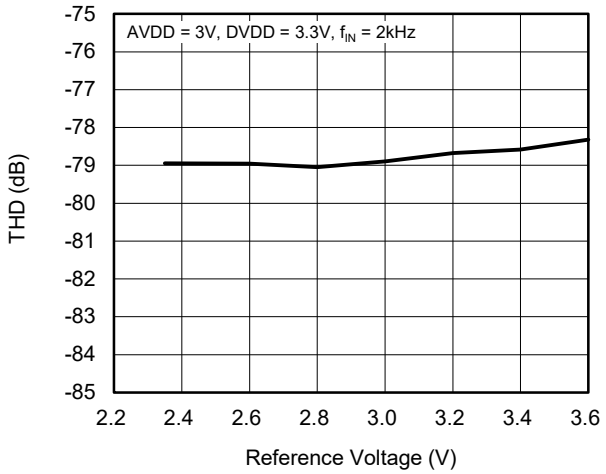
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3V, DVDD = 3.3V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

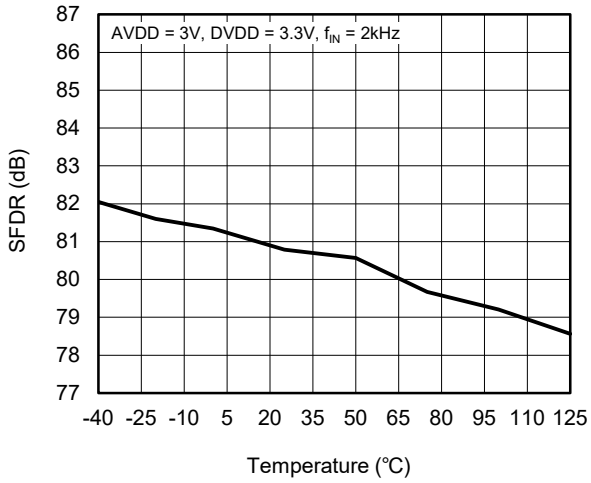
THD vs. Input Frequency



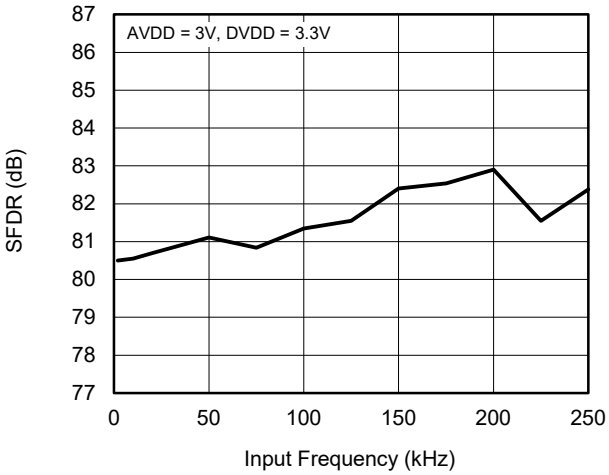
THD vs. Reference Voltage (AVDD)



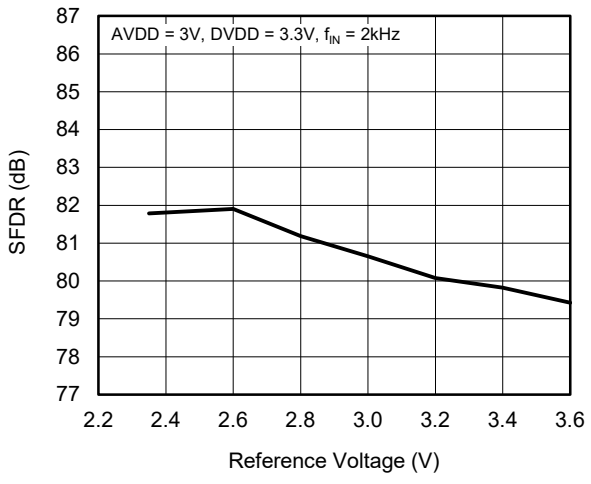
SFDR vs. Temperature



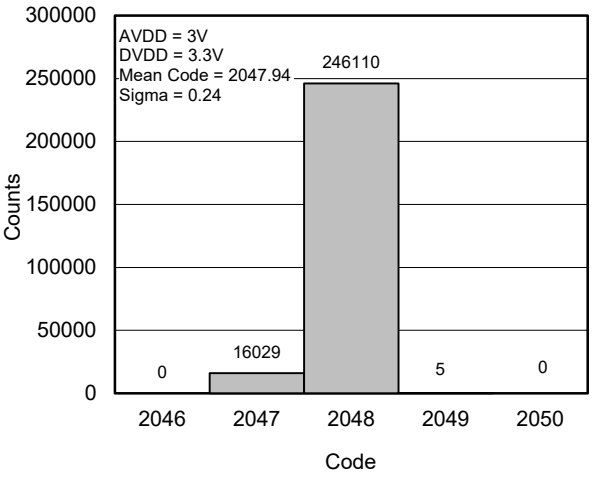
SFDR vs. Reference Voltage (AVDD)



SFDR vs. Input Frequency



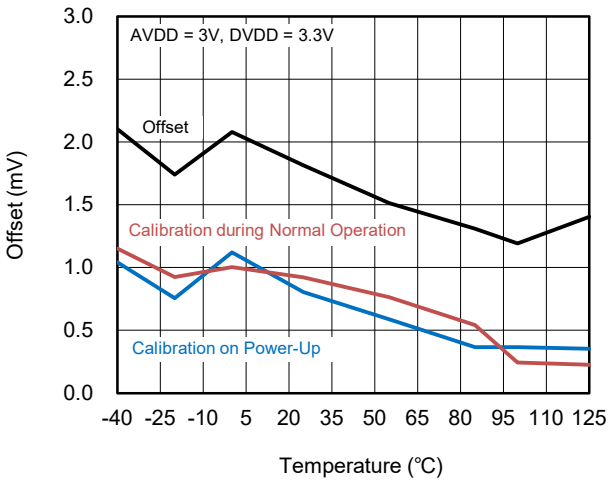
DC Input Histogram



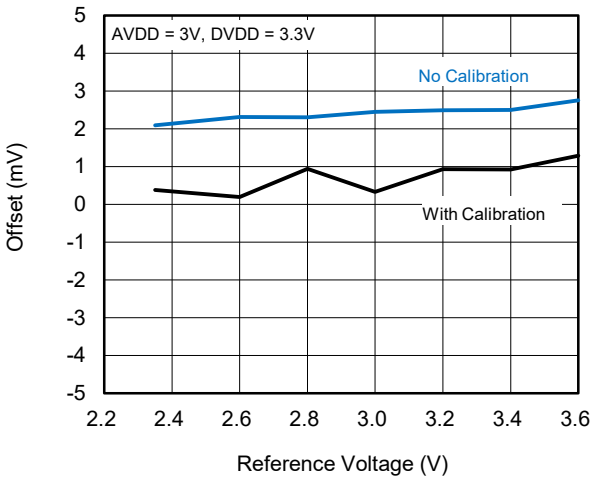
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T_A = +25℃, AVDD = 3V, DVDD = 3.3V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

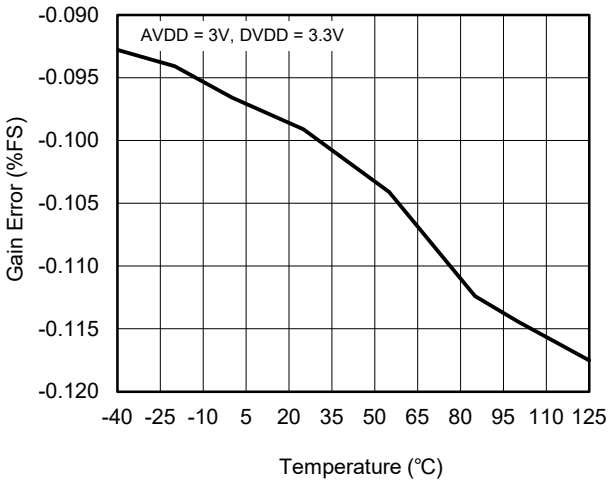
Offset vs. Temperature



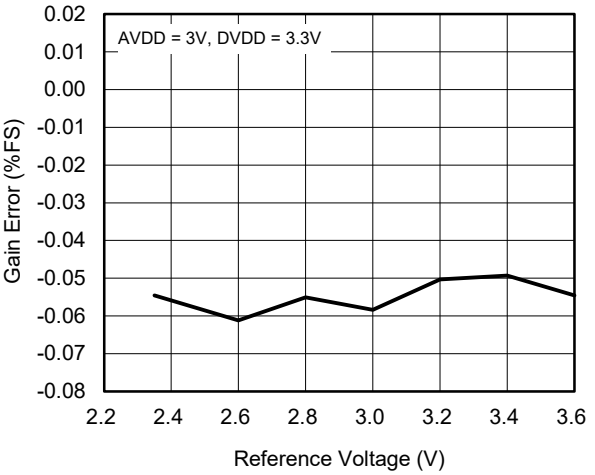
Offset vs. Reference Voltage (AVDD)



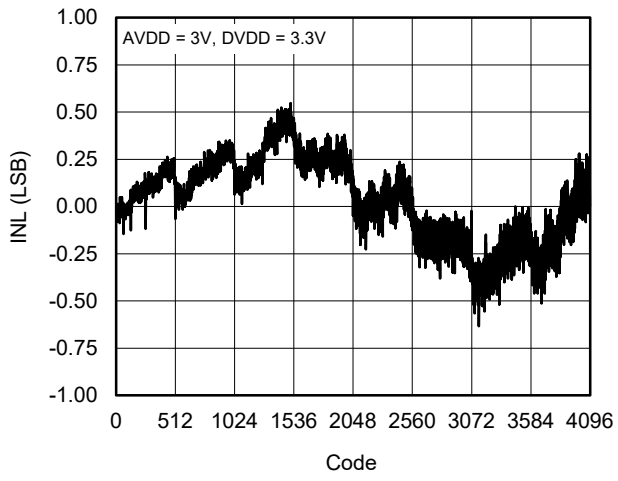
Gain Error vs. Temperature



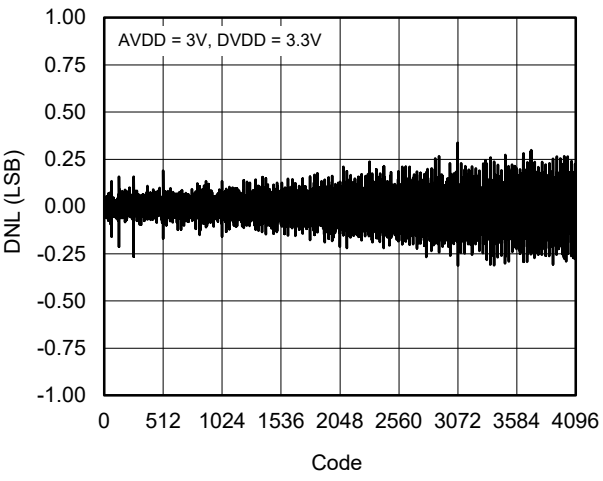
Gain Error vs. Reference Voltage (AVDD)



INL vs. Code



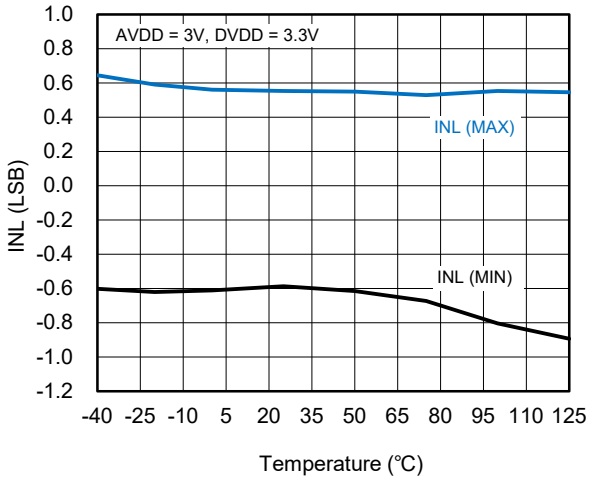
DNL vs. Code



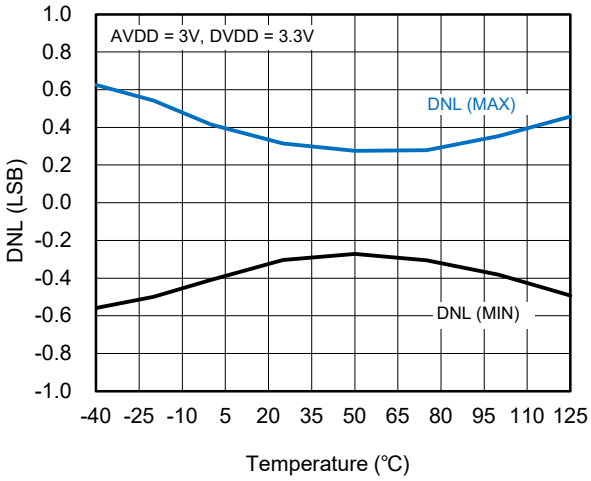
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3V, DVDD = 3.3V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

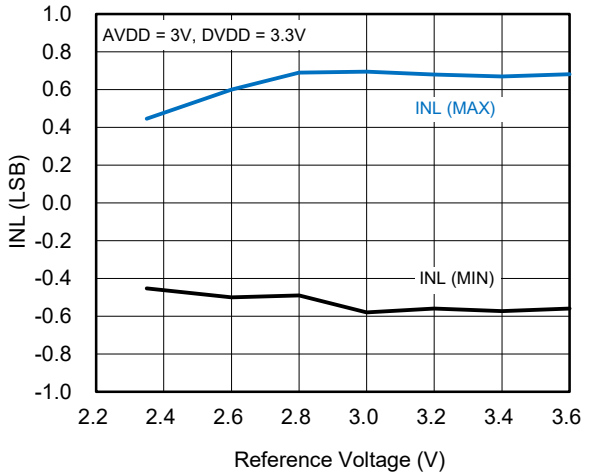
INL vs. Temperature



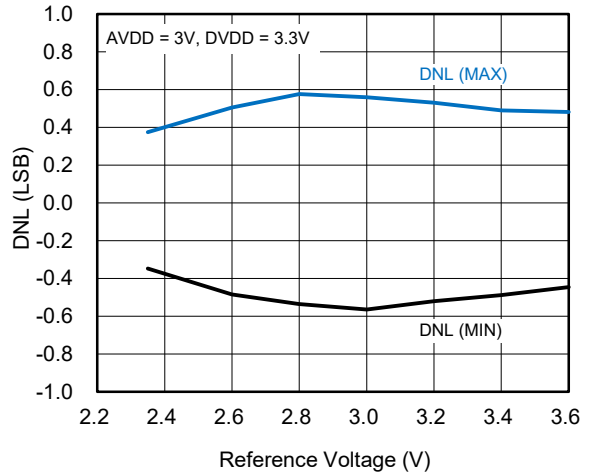
DNL vs. Temperature



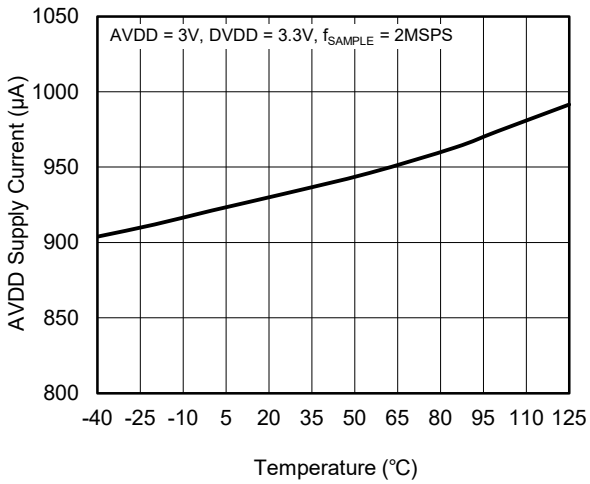
INL vs. Reference Voltage (AVDD)



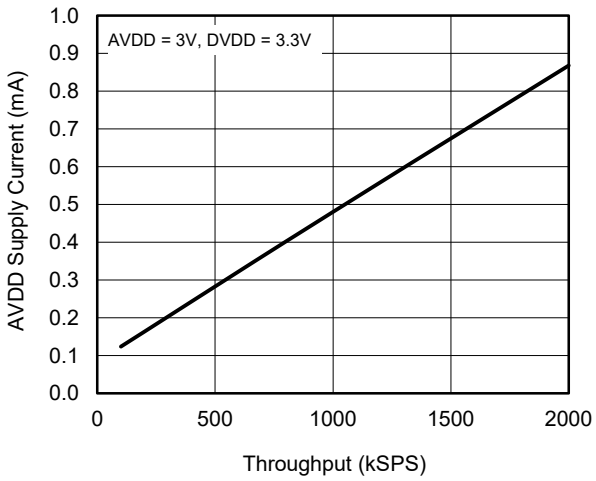
DNL vs. Reference Voltage (AVDD)



AVDD Supply Current vs. Temperature



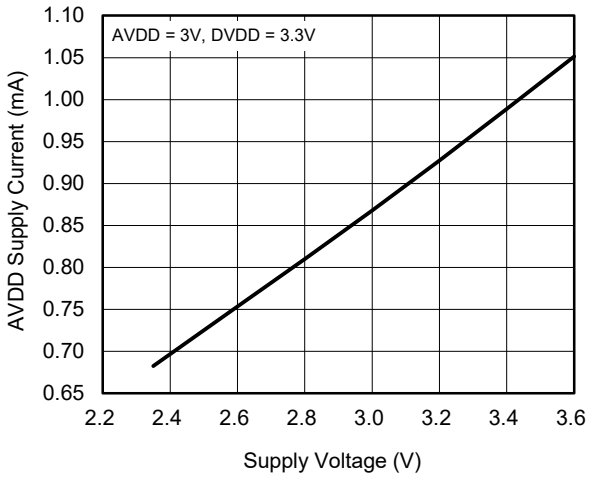
AVDD Supply Current vs. Throughput



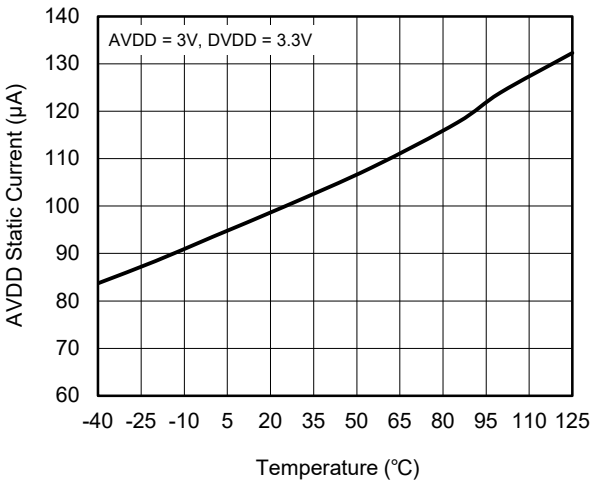
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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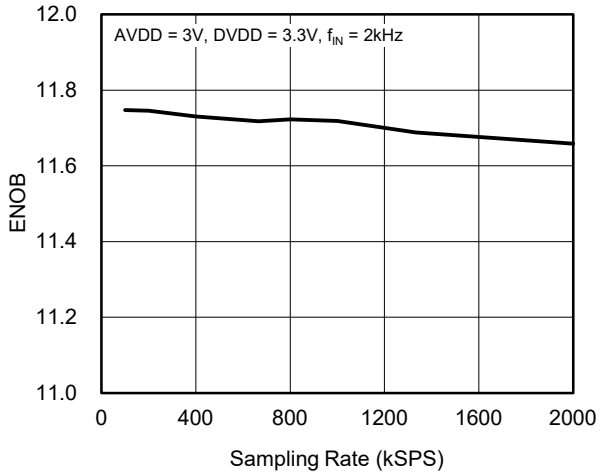
AVDD Supply Current vs. Supply Voltage



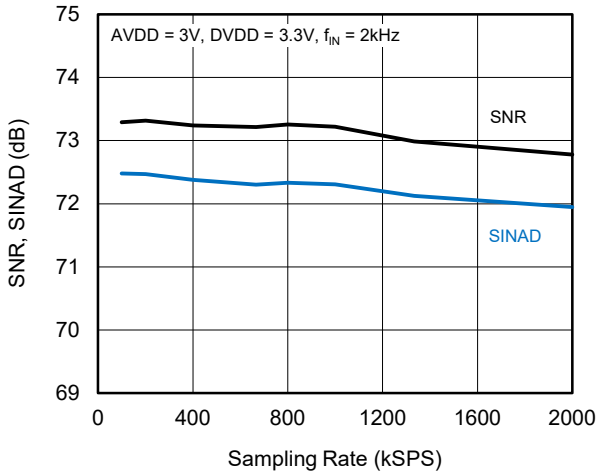
AVDD Static Current vs. Temperature



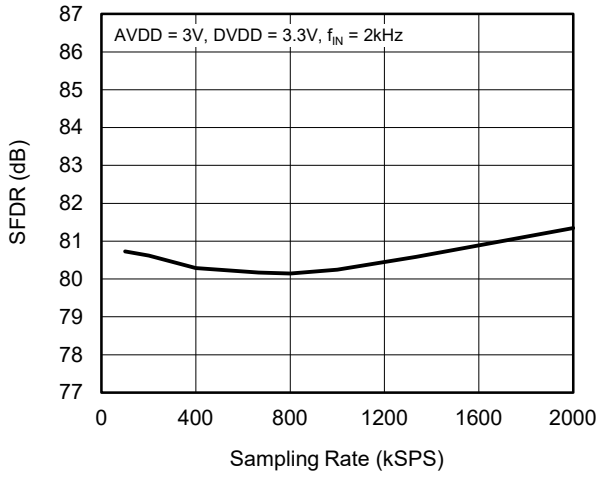
ENOB vs. Sampling Rate



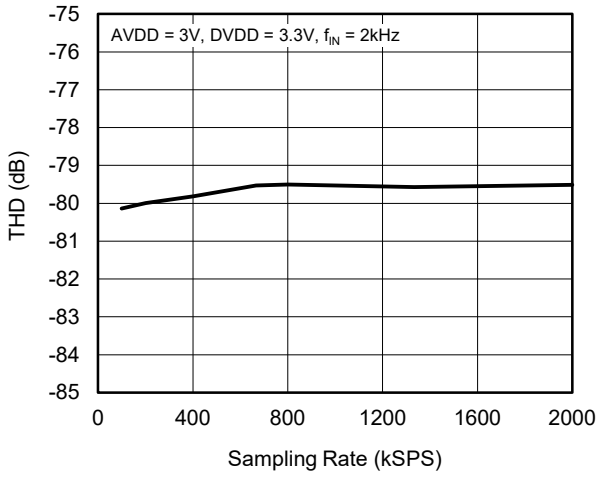
SNR, SINAD vs. Sampling Rate



SFDR vs. Sampling Rate



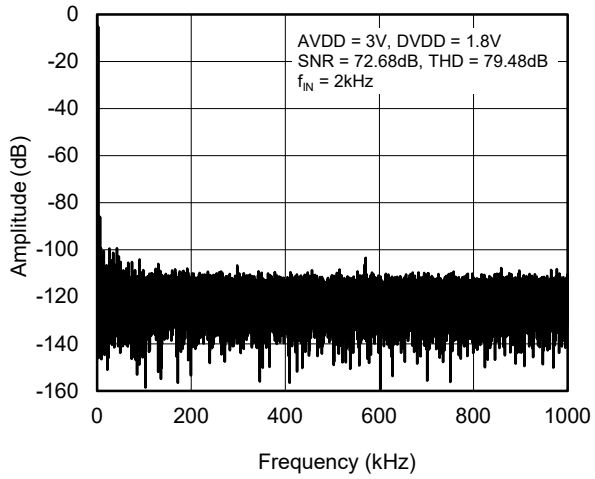
THD vs. Sampling Rate



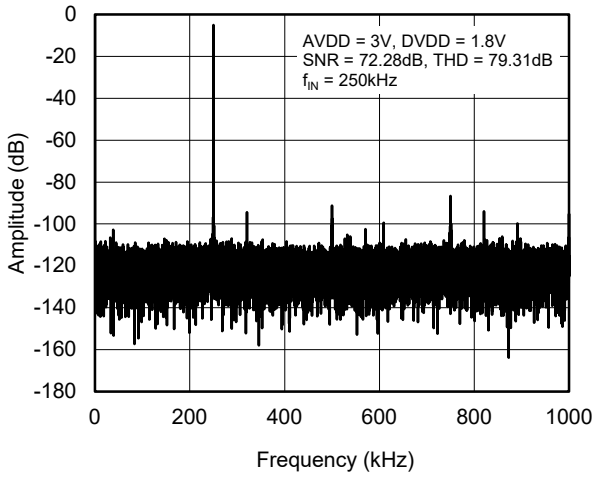
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3V, DVDD = 1.8V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

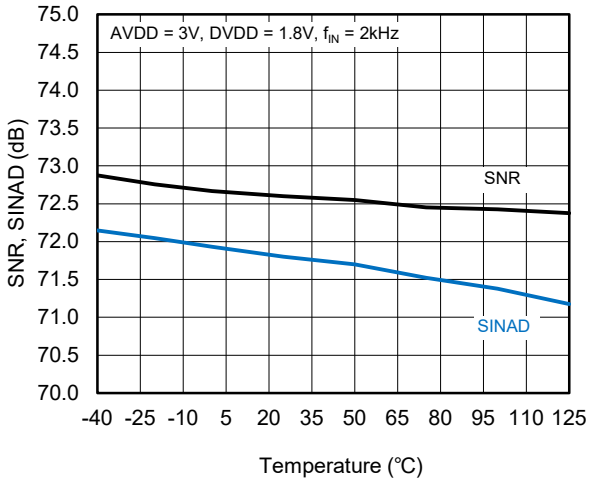
Typical FFT



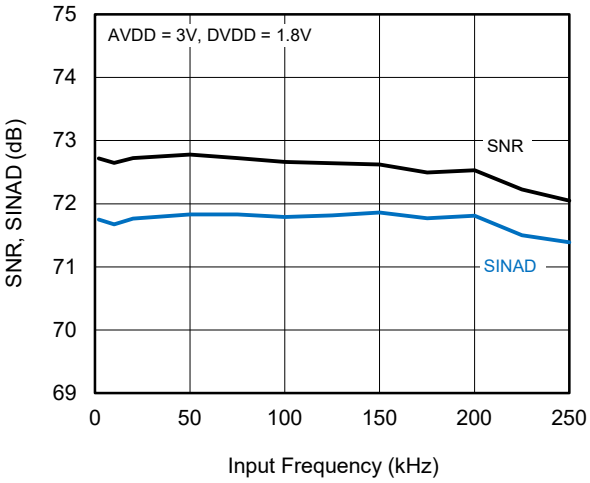
Typical FFT



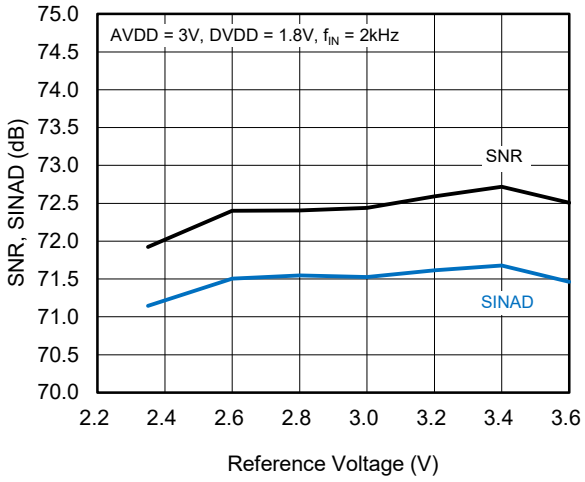
SNR, SINAD vs. Temperature



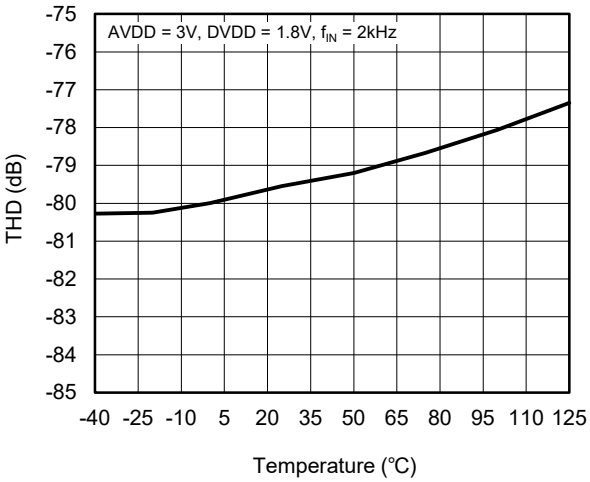
SNR, SINAD vs. Input Frequency



SNR, SINAD vs. Reference Voltage (AVDD)



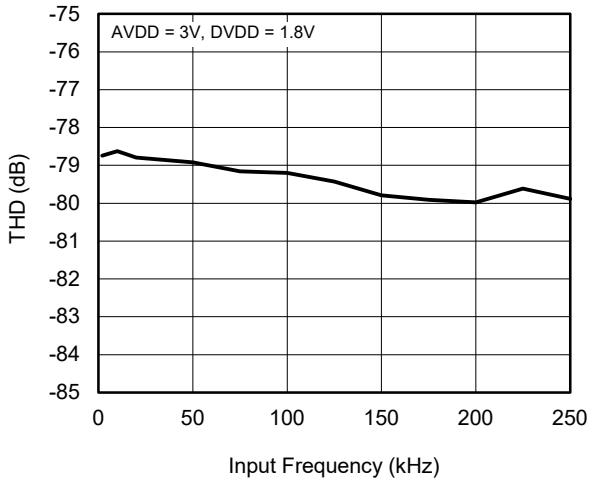
THD vs. Temperature



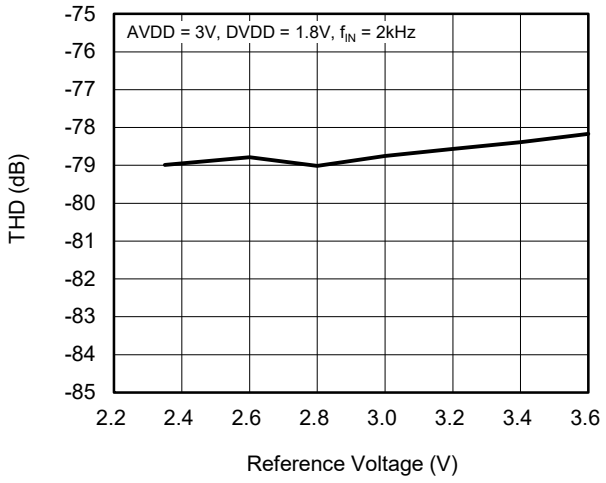
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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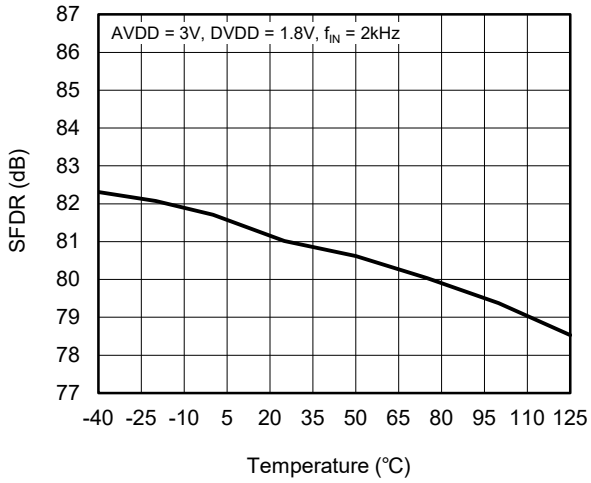
THD vs. Input Frequency



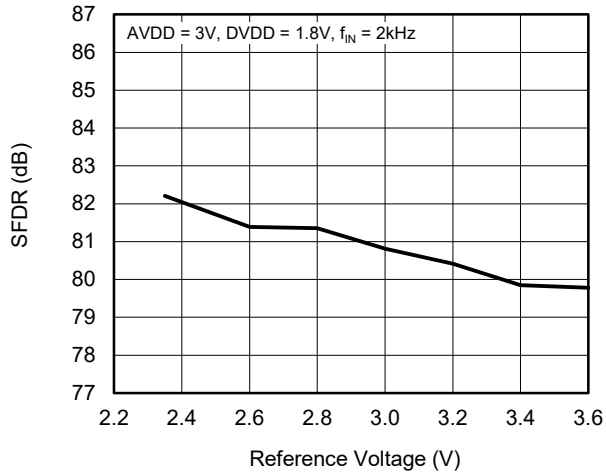
THD vs. Reference Voltage (AVDD)



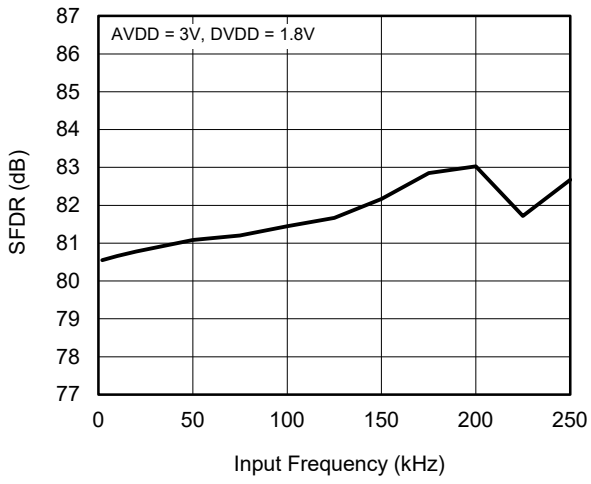
SFDR vs. Temperature



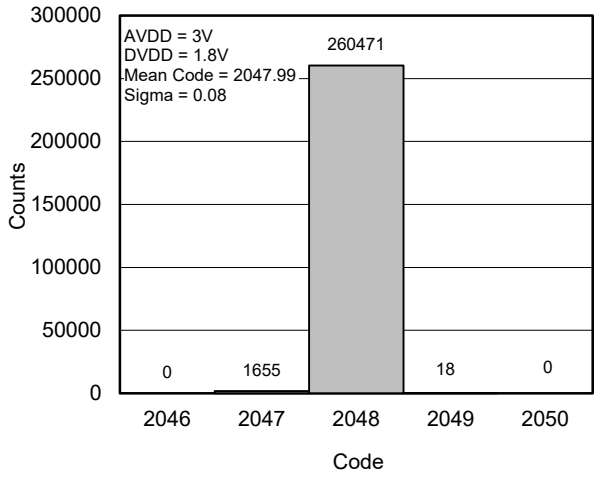
SFDR vs. Reference Voltage (AVDD)



SFDR vs. Input Frequency



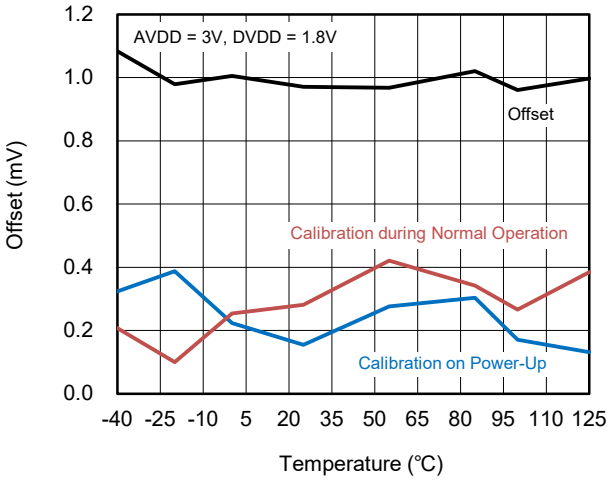
DC Input Histogram



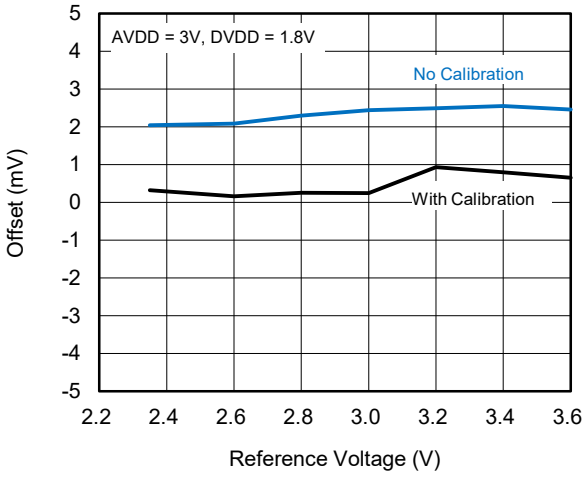
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3V, DVDD = 1.8V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

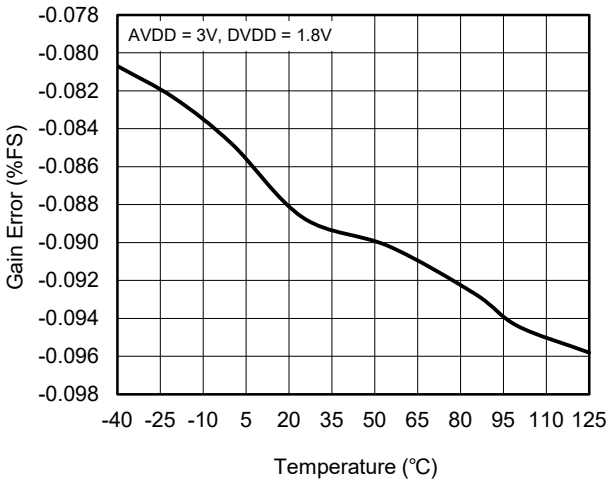
Offset vs. Temperature



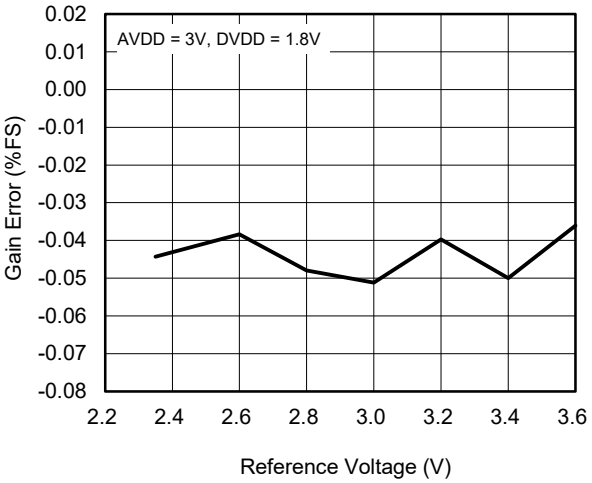
Offset vs. Reference Voltage (AVDD)



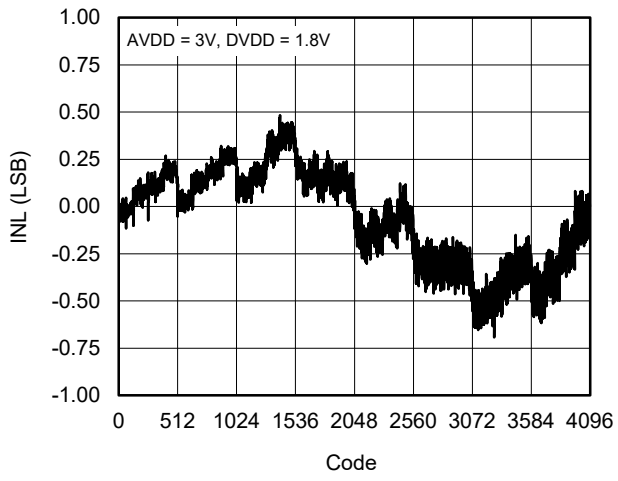
Gain Error vs. Temperature



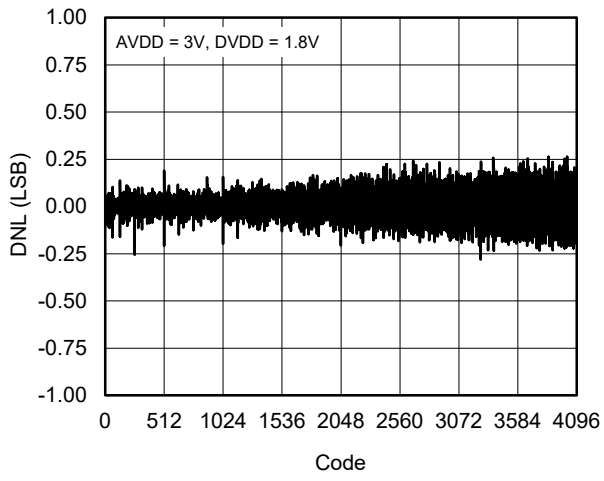
Gain Error vs. Reference Voltage (AVDD)



INL vs. Code



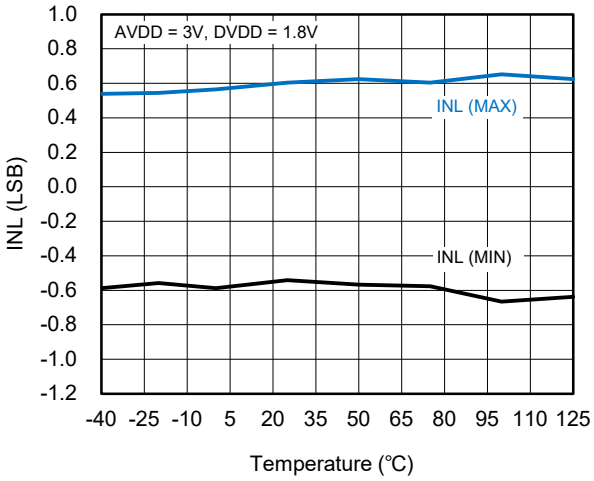
DNL vs. Code



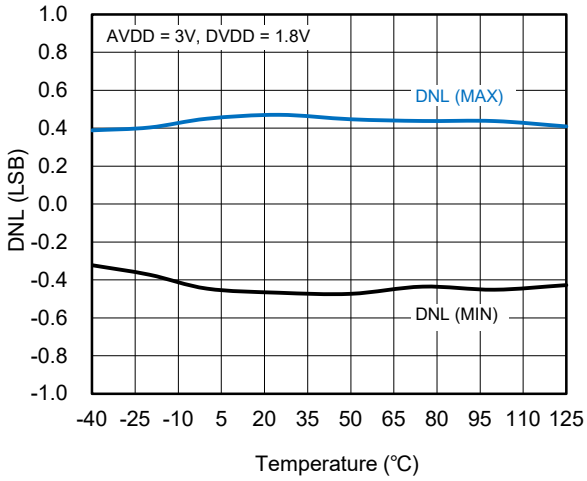
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3V, DVDD = 1.8V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

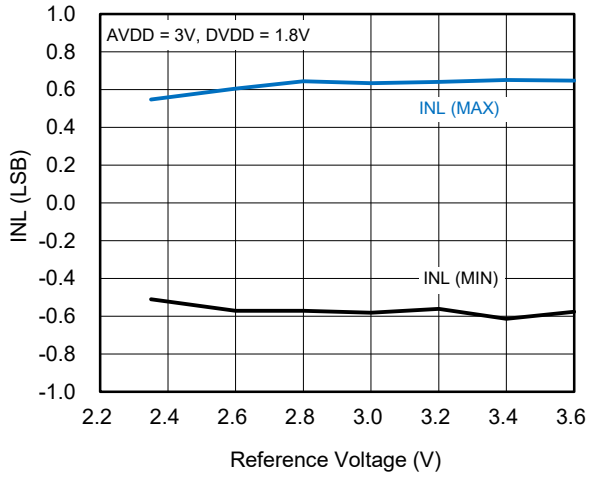
INL vs. Temperature



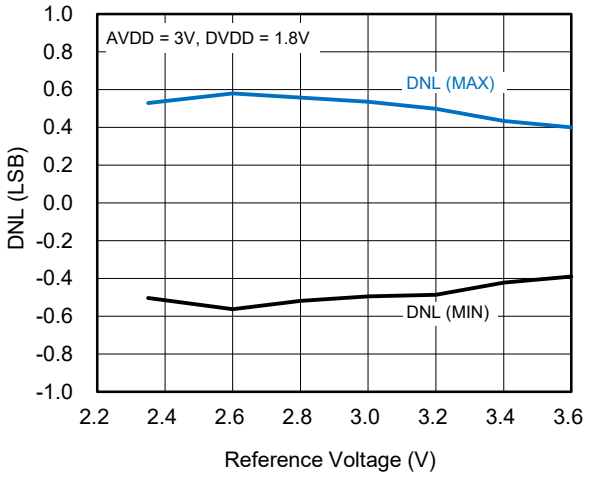
DNL vs. Temperature



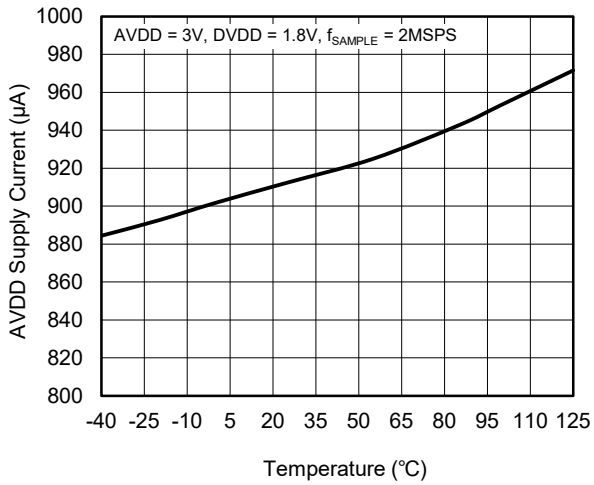
INL vs. Reference Voltage (AVDD)



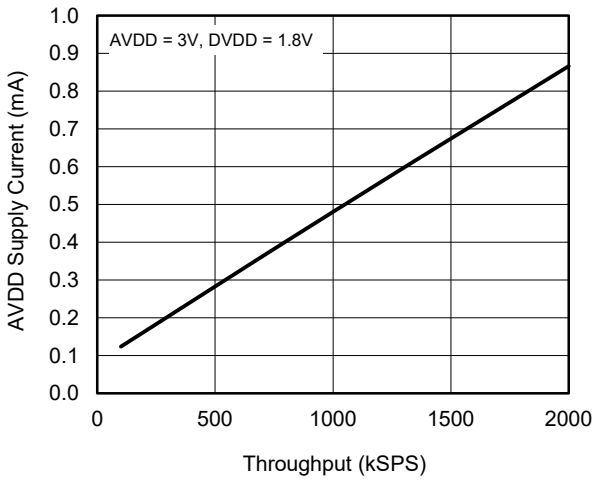
DNL vs. Reference Voltage (AVDD)



AVDD Supply Current vs. Temperature



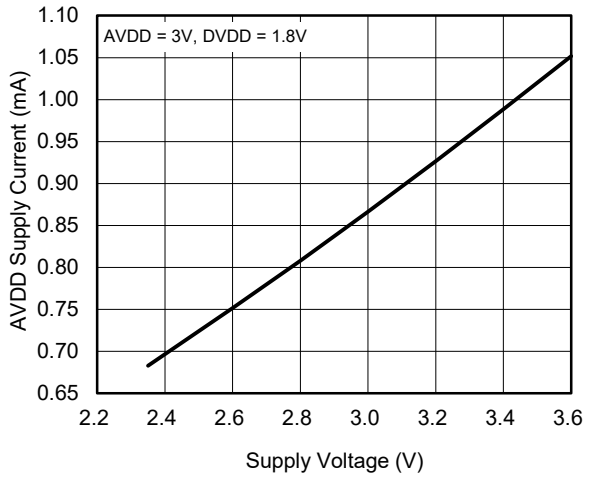
AVDD Supply Current vs. Throughput



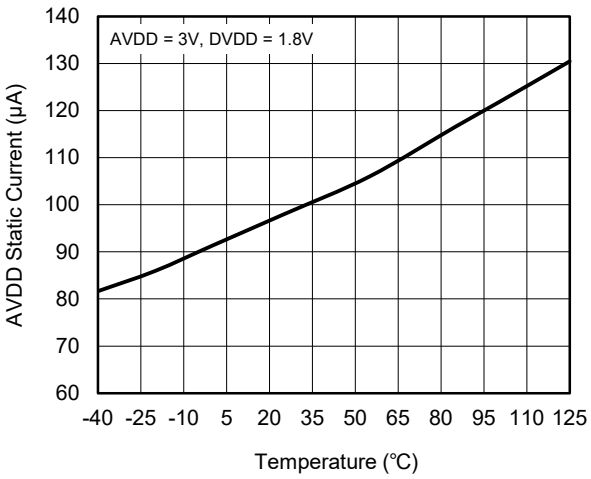
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3V, DVDD = 1.8V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

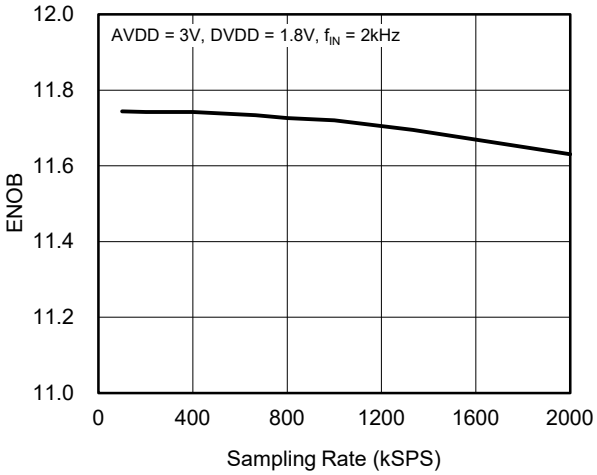
AVDD Supply Current vs. Supply Voltage



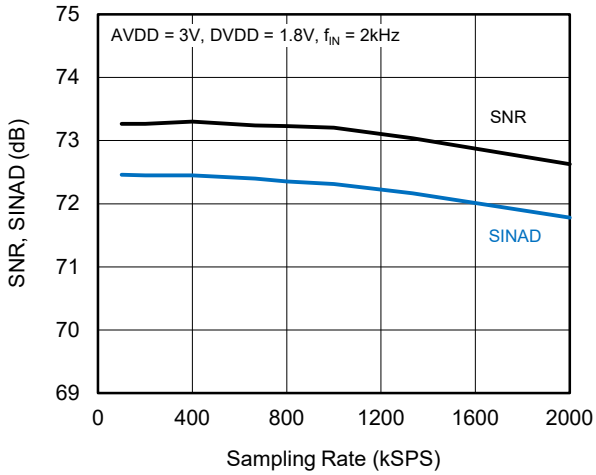
AVDD Static Current vs. Temperature



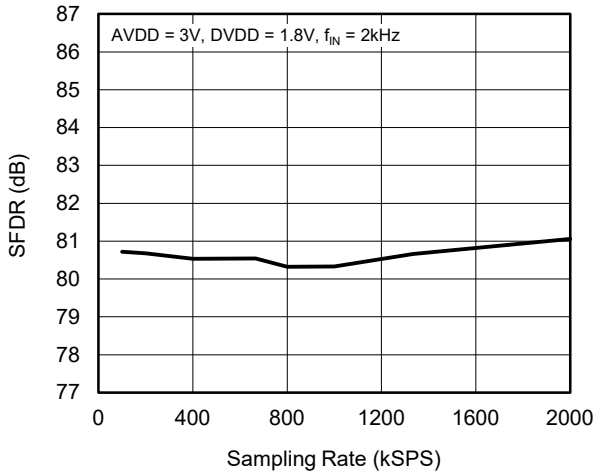
ENOB vs. Sampling Rate



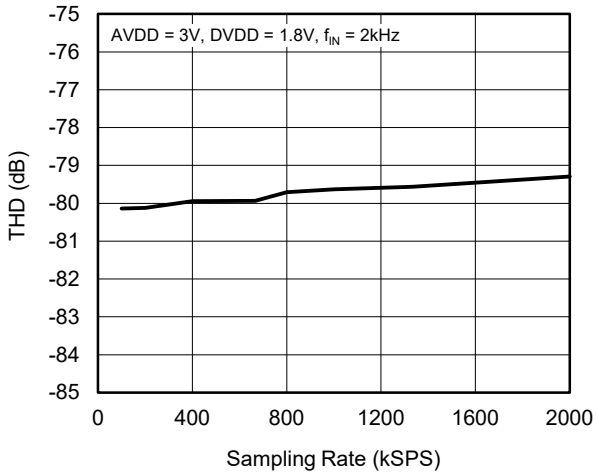
SNR, SINAD vs. Sampling Rate



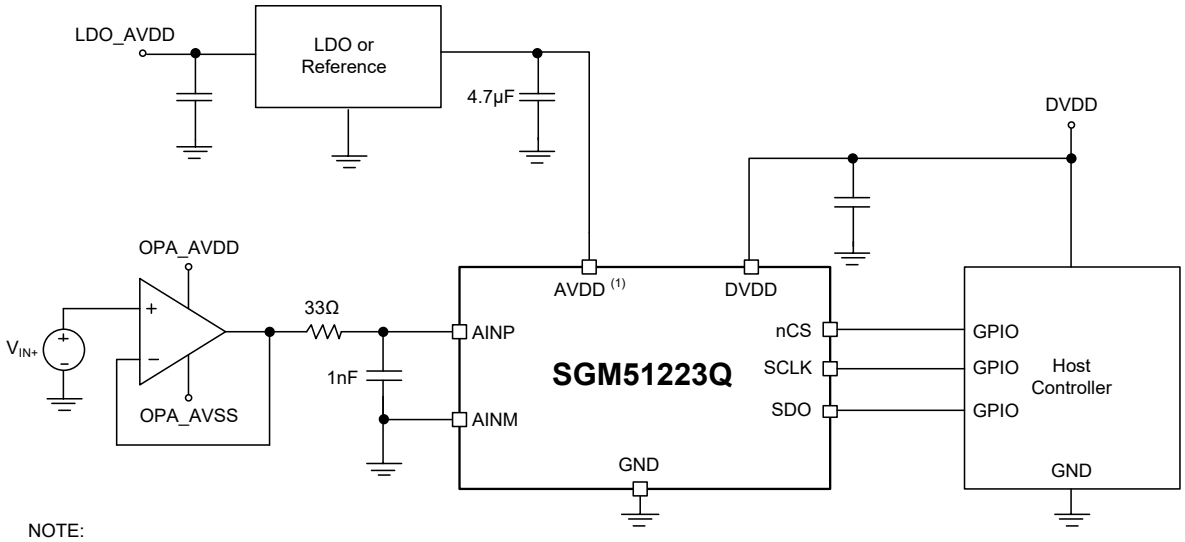
SFDR vs. Sampling Rate



THD vs. Sampling Rate



TYPICAL APPLICATION CIRCUIT



NOTE:
1. AVDD is used as reference for the device.

Figure 2. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

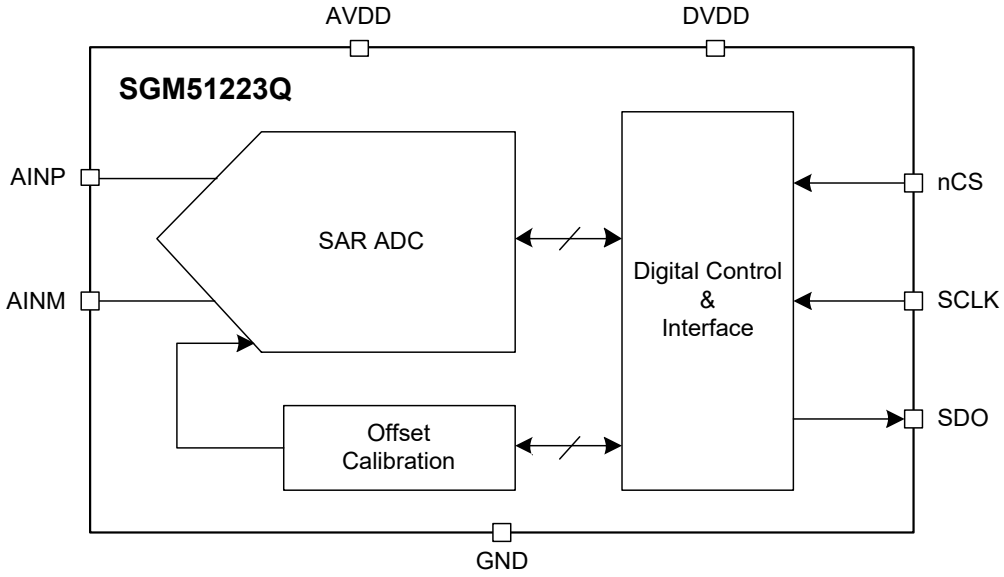


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM51223Q is a low power easy-to-use SAR ADC.

The SGM51223Q doesn't have internal oscillator, and its conversion and data transfer are driven by an external clock on the SCLK pin. To run at 2MSPS through output, it needs a 32MHz SCLK input.

The SGM51223Q features an offset calibration function. It can be performed either after power-up or during normal working. Refer to the Offset Calibration section for details.

Reference

The SGM51223Q doesn't have a separate reference input pin, neither have an internal reference. The AVDD pin is the analog power supply pin and also the ADC reference voltage input pin. A low noise regulator or a low noise voltage reference source is recommended for this pin. A low equivalent series resistance (ESR) capacitor is recommended to be connected to this pin at the same time. The decoupling capacitor should be 3.3μF or 4.7μF.

The SGM51223Q full input range is equal to the voltage potential at the VDD pin.

Analog Input

The SGM51223Q supports single-ended input. It allows the AINM pin voltage potential to be in the range of -100mV to +100mV reference to GND pin of the device. And the AINP - AINM must be in the range from 0V to AVDD at the same time.

A typical equivalent input circuit is shown in Figure 4. The ideal transfer characteristics are shown in Figure 5 and Table 1.

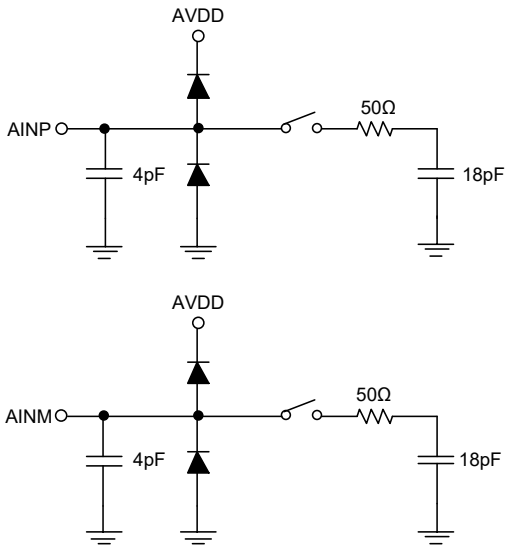


Figure 4. Equivalent Input Circuit for the Sampling Stage

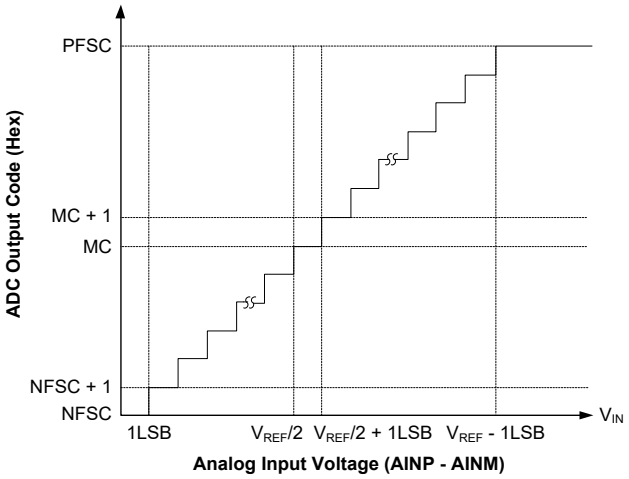


Figure 5. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

Analog Input Voltage (AINP - AINM)	Code	Description	Ideal Output Code
≤ 1LSB	NFSC	Negative full-scale code	000h
1LSB to 2LSBs	NFSC + 1	–	001h
(V_{REF}/2) to (V_{REF}/2) + 1LSB	MC	Mid code	800h
(V_{REF}/2) + 1LSB to (V_{REF}/2) + 2LSBs	MC + 1	–	801h
≥ V_{REF} - 1LSB	PFSC	Positive full-scale code	FFFh

DETAILED DESCRIPTION (continued)

Serial Interface

The SGM51223Q supports an SPI-compatible serial interface. The nCS is the data frame control signal. An operation data frame contains 14 clock falling edges. In the 14-bit data frame, the first data '0' is set by the falling edge of nCS, and the data from the 2nd bit to the 14th bit are set by the subsequent falling edges of the SCLKs. A rising edge of nCS stops the data frame. Figure 6 shows the serial interface timing diagram.

After power-up, the SGM51223Q will perform an offset calibration on the first operation frame. Refer to the Offset Calibration section for details.

Device Functional Modes

Offset Calibration

The SGM51223Q can compensate the offset by setting an internal offset calibration register (OCR). The OCR default value is zero. In order to make the device work properly, it is suggested to perform offset calibration after the chip is powered on, operating temperature changes significantly or power supply changes significantly.

During the offset calibration process, the input pins AINP and AINM are internally disconnected from the external connection, so it is not necessary to disconnect the ADC inputs from the external connection.

Offset Calibration on Power-Up

After the chip is powered up, the main host controller should issue a complete 32 SCLKs to perform offset calibration before the ADC conversion operation. If the 32 SCLKs of calibration are not provided enough, the OCR will not be updated on the following operation frame. During the calibration, the SDO output remains low. The timing parameters for the offset calibration on power-up are shown in Table 2. Figure 7 shows the offset calibration on power-up timing diagram.

Table 2. Offset Calibration on Power-Up

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency for Calibration	f_{CLK_CAL}			16	MHz
Calibration Time at Power-Up	$t_{POWERUP_CAL}$	32 × t_6			ns
Acquisition Time	t_2	90			ns
nCS High Time	t_7	t_{ACQ}			ns
Setup Time: nCS Falling to SCLK Falling	t_3	12			ns
Delay Time: Last SCLK Falling to nCS Rising	t_8	10			ns

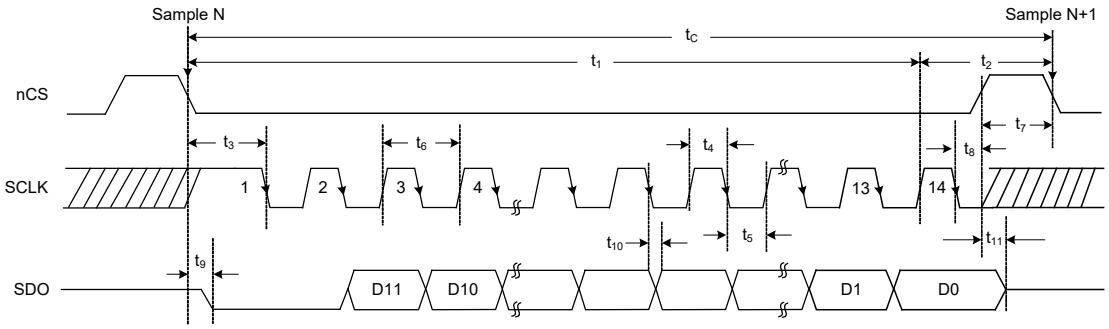


Figure 6. Serial Interface Timing Diagram

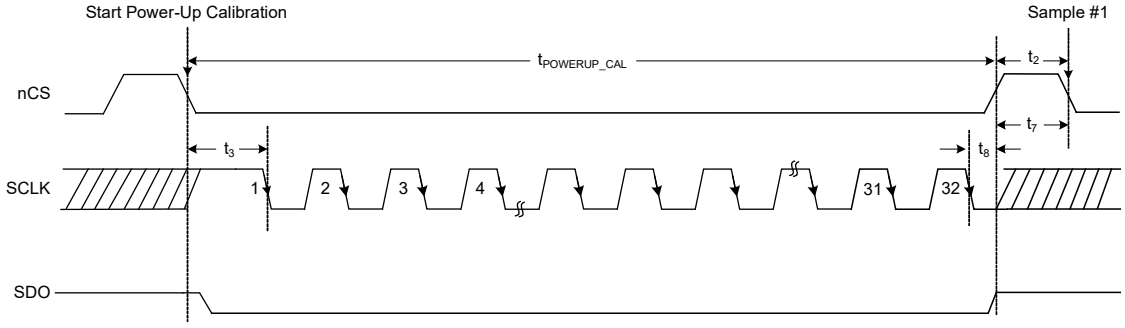


Figure 7. Offset Calibration on Power-Up Timing Diagram

DETAILED DESCRIPTION (continued)

Offset Calibration during Normal Operation

The offset calibration can also be performed during the ADC normal operation. Similar as the calibration on power-up, it will take 32 SCLKs to complete the offset calibration during ADC normal operation. During the calibration, for the first 14 SCLKs, the chip will output normal conversion results on the SDO pin. The calibration is performed between the 17th and 32nd SCLKs. The SDO output will remain low after the 14th SCLK. If the 32 SCLKs of calibration are not provided enough, the OCR will not be updated on the following operation frame. The timing parameters for the offset calibration during normal operation are shown in Table 3. Figure 8 shows the offset calibration during normal operation timing diagram.

Table 3. Offset Calibration during Normal Operation

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency for Calibration	f_{CLK_CAL}			16	MHz
Calibration Time during Normal Operation	t_{CAL}	15 × t_6			ns
Acquisition Time	t_2	90			ns
nCS High Time	t_7	t_{ACQ}			ns
Setup Time: nCS Falling to SCLK Falling	t_3	12			ns
Delay Time: Last SCLK Falling to nCS Rising	t_8	10			ns

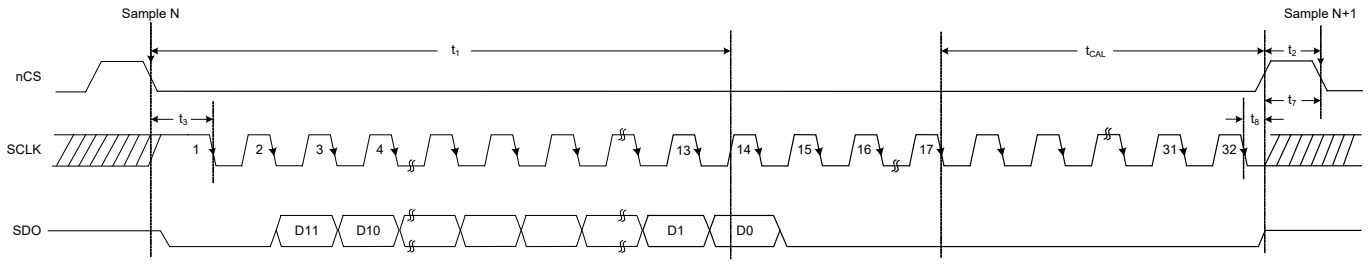


Figure 8. Offset Calibration during Normal Operation Timing Diagram

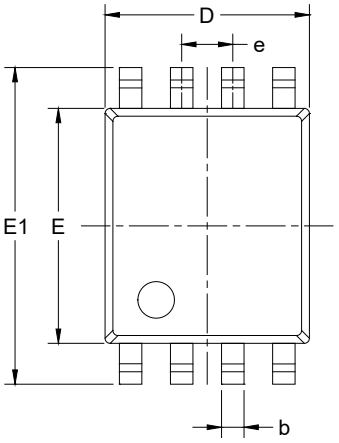
REVISION HISTORY

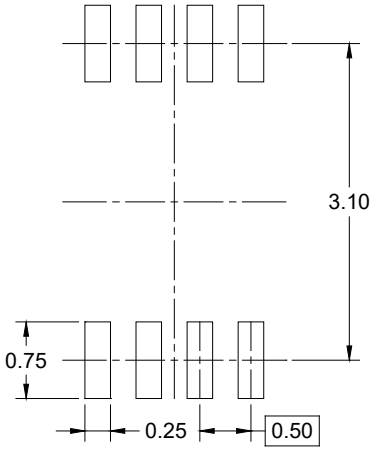
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (MARCH 2025) to REV.A	Page
Changed from product preview to production data	All

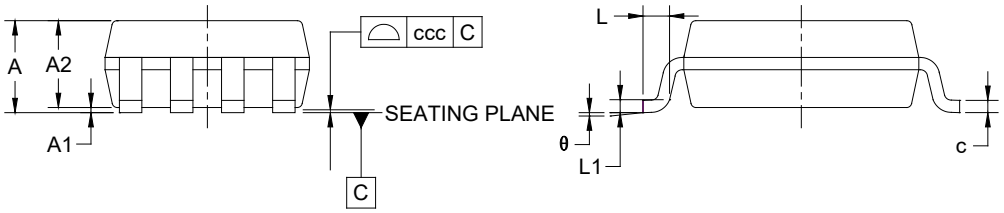
PACKAGE OUTLINE DIMENSIONS

VSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

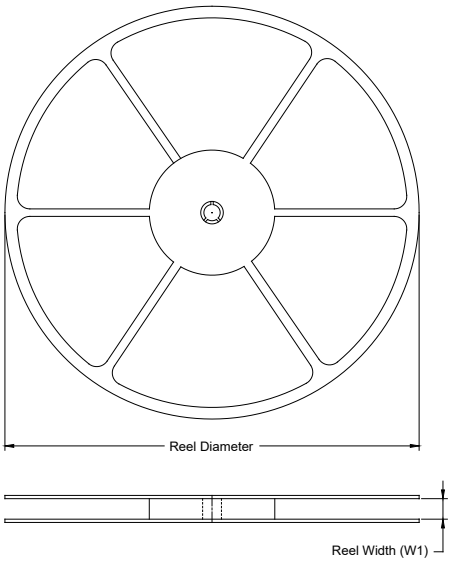


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.000
A1	0.000	-	0.150
A2	0.600		0.850
b	0.170	-	0.270
c	0.080		0.230
D	1.900	-	2.100
E	2.200	-	2.400
E1	3.000	-	3.200
e	0.500 BSC		
L	0.150	-	0.400
L1	0.120 BSC		
θ	0°	-	8°
ccc	0.100		

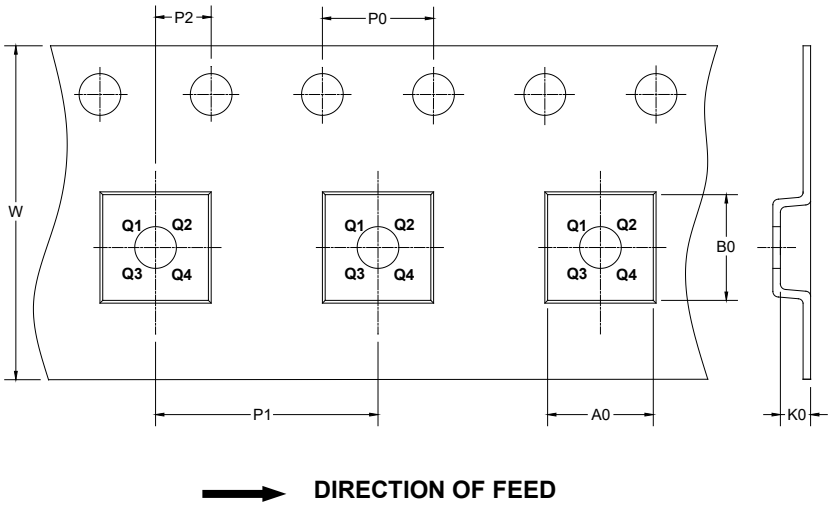
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187 CA.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



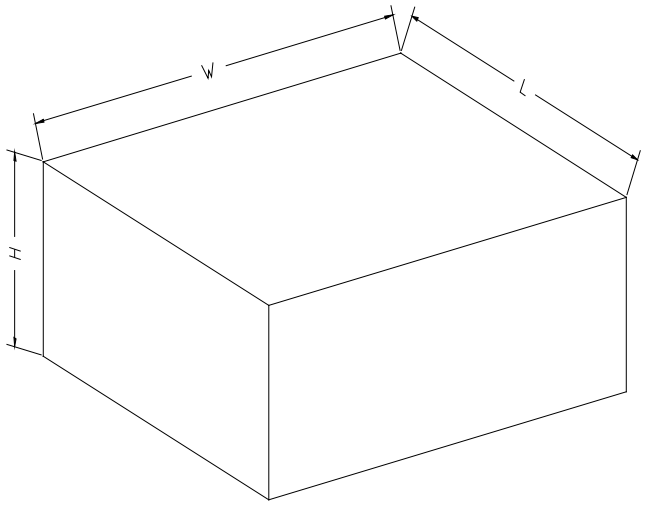
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP-8	7″	9.5	2.25	3.35	1.05	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002