ADS1118-Q1 Automotive, Low-Power, SPI-Compatible, 16-Bit Analog-to-Digital Converter With Internal Reference and Temperature Sensor

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Wide supply range: 2 V to 5.5 V
- Low current consumption:
  - Continuous mode: only 150 μA
  - Single-shot mode: automatic power-down
- Programmable data rate: 8 SPS to 860 SPS
- Single-cycle settling
- Internal low-drift voltage reference
- Internal temperature sensor: 2°C (maximum) error
- Internal oscillator
- Internal PGA
- Four single-ended or two differential inputs

2 Applications

- Battery management systems
- Automotive sensors:
  - Thermocouples
  - Resistance temperature detectors (RTDs)
  - Pressure and strain gauge sensors
  - Electrochemical gas sensors
  - Particulate matter sensors

3 Description

The ADS1118-Q1 is a precision, low power, 16-bit analog-to-digital converter (ADC) that provides all features necessary to measure the most common sensor signals. The ADS1118-Q1 integrates a programmable gain amplifier (PGA), voltage reference, oscillator, and high-accuracy temperature sensor. These features, along with a wide power-supply range from 2 V to 5.5 V, make the ADS1118-Q1 ideally suited for power- and space-constrained, sensor-measurement applications.

The ADS1118-Q1 performs conversions at data rates up to 860 samples per second (SPS). The PGA offers input ranges from ±256 mV to ±6.144 V, allowing both large and small signals to be measured with high resolution. An input multiplexer (mux) allows measurement of two differential or four single-ended inputs. The high-accuracy temperature sensor is used for system-level temperature monitoring, or cold-junction compensation for thermocouples.

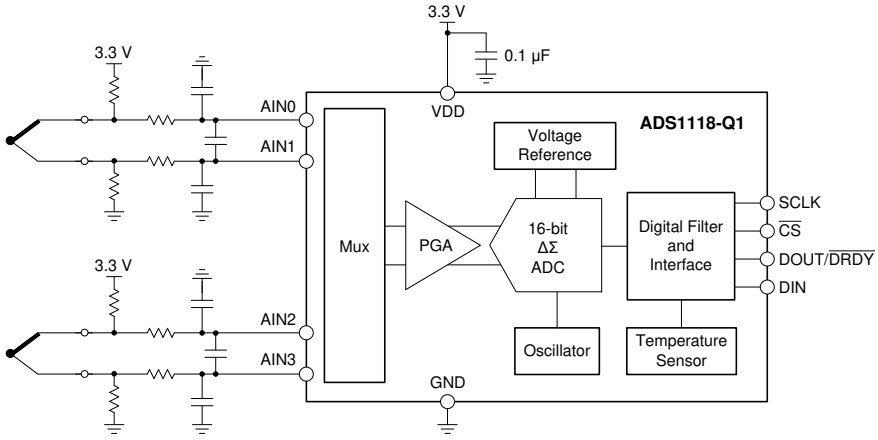
The ADS1118-Q1 operates either in continuous-conversion mode, or in a single-shot mode that automatically powers down after a conversion. Single-shot mode significantly reduces current consumption during idle periods. Data are transferred through a serial peripheral interface (SPI™). The ADS1118-Q1 is specified from –40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS1118-Q1	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

K-Type Thermocouple Measurement Using Integrated Temperature Sensor for Cold-Junction Compensation



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Timing Requirements: Serial Interface ... 7
7.7 Switching Characteristics: Serial Interface ... 7
7.8 Typical Characteristics ... 8
8 Parameter Measurement Information ... 13
8.1 Noise Performance ... 13
9 Detailed Description ... 14
9.1 Overview ... 14
9.2 Functional Block Diagram ... 14
9.3 Feature Description ... 15
9.4 Device Functional Modes ... 19
9.5 Programming ... 20
9.6 Register Maps ... 23
10 Application and Implementation ... 25
10.1 Application Information ... 25
10.2 Typical Application ... 30
11 Power Supply Recommendations ... 33
11.1 Power-Supply Sequencing ... 33
11.2 Power-Supply Decoupling ... 33
12 Layout ... 34
12.1 Layout Guidelines ... 34
12.2 Layout Example ... 35
13 Device and Documentation Support ... 36
13.1 Documentation Support ... 36
13.2 Receiving Notification of Documentation Updates 36
13.3 Support Resources ... 36
13.4 Trademarks ... 36
13.5 Electrostatic Discharge Caution ... 36
13.6 Glossary ... 36
14 Mechanical, Packaging, and Orderable Information ... 36

4 Revision History

Changes from Revision A (Nobember 2015) to Revision B **Page**

- Changed automotive-specific *Features* bullets, moved ESD data to *ESD Ratings* table ... 1
- Added *Functional Safety-Capable* bullets to *Features* section ... 1
- Changed maximum VDD voltage from 5.5 V to 7 V in the *Absolute Maximum Ratings* table ... 4
- Added ESD classification information to *ESD Ratings* table ... 4
- Changed maximum value of t_{SPWL} parameter in *Timing Requirements* table from *28 ms* to *30.8 ms* ... 7
- Changed SCLK low time to reset SPI from *28 ms* to *30.8 ms* in second footnote of *Timing Requirements* table ... 7
- Changed *Serial Interface Timing* figure ... 7
- Changed SCLK low time to reset SPI from *28 ms* to *30.8 ms* in *Serial Clock* section ... 20
- Added last paragraph to the *32-Bit Data Transmission Cycle* section ... 22
- Changed bit description of Config Register bit 0 ... 24
- Changed SCLK low time to reset SPI from *28 ms* to *30.8 ms* in the *GPIO Ports for Communication* section ... 26

Changes from Original (October 2015) to Revision A **Page**

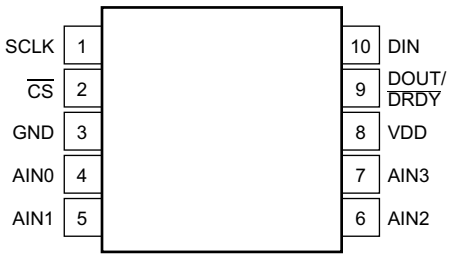
- Changed from product preview to production data ... 1

5 Device Comparison Table

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS Differential (Single-Ended)	PGA	INTERFACE	SPECIAL FEATURES
ADS1118-Q1	16	860	2 (4)	Yes	SPI	Temperature sensor
ADS1018-Q1	12	3300	2 (4)	Yes	SPI	Temperature sensor
ADS1115-Q1	16	860	2 (4)	Yes	I^2C	Comparator
ADS1015-Q1	12	3300	2 (4)	Yes	I^2C	Comparator

6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SCLK	Digital input	Serial clock input
2	$\overline{CS}$	Digital input	Chip select; active low. Connect to GND if not used.
3	GND	Supply	Ground
4	AIN0	Analog input	Analog input 0. Leave unconnected or tie to VDD if not used.
5	AIN1	Analog input	Analog input 1. Leave unconnected or tie to VDD if not used.
6	AIN2	Analog input	Analog input 2. Leave unconnected or tie to VDD if not used.
7	AIN3	Analog input	Analog input 3. Leave unconnected or tie to VDD if not used.
8	VDD	Supply	Power supply. Connect a 0.1-µF power supply decoupling capacitor to GND.
9	DOUT/$\overline{DRDY}$	Digital output	Serial data output combined with data ready; active low
10	DIN	Digital input	Serial data input

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	7	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	V
Digital input voltage	DIN, DOUT/$\overline{DRDY}$, SCLK, $\overline{CS}$	GND – 0.3	VDD + 0.3	V
Input current, continuous	Any pin except power supply pins	–10	10	mA
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Power supply	VDD to GND	2		5.5	V
ANALOG INPUTS(1)						
FSR	Full-scale input voltage(2)	$V_{IN} = V_{(AINP)} - V_{(AINN)}$	See Table 3			
$V_{(AINx)}$	Absolute input voltage		GND		VDD	V
DIGITAL INPUTS						
	Input voltage		GND		VDD	V
TEMPERATURE						
T_A	Operating ambient temperature		–40		125	°C

(1) AINP and AINN denote the selected positive and negative inputs. AINx denotes one of the four available analog inputs.
(2) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

7.4 Thermal Information

THERMAL METRIC(1)		ADS1118-Q1 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Maximum and minimum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at VDD = 3.3 V, data rate = 8 SPS, and FSR = ±2.048 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Common-mode input impedance	FSR = ±6.144 V(1)		8		MΩ
		FSR = ±4.096 V(1), FSR = ±2.048 V		6		
		FSR = ±1.024 V		3		
		FSR = ±0.512 V, FSR = ±0.256 V		100		
	Differential input impedance	FSR = ±6.144 V(1)		22		MΩ
		FSR = ±4.096 V(1)		15		
		FSR = ±2.048 V		4.9		
		FSR = ±1.024 V		2.4		
		FSR = ±0.512 V, FSR = ±0.256 V		710		kΩ
SYSTEM PERFORMANCE						
	Resolution (no missing codes)			16		Bits
DR	Data rate			8, 16, 32, 64, 128, 250, 475, 860		SPS
	Data rate variation	All data rates	–10%		10%	
	Output noise			See *Noise Performance* section		
INL	Integral nonlinearity	DR = 8 SPS, FSR = ±2.048 V(2)			1	LSB
	Offset error	FSR = ±2.048 V, differential inputs		±0.1	±2	LSB
		FSR = ±2.048 V, single-ended inputs		±0.25		
	Offset drift	FSR = ±2.048 V		0.002		LSB/°C
	Offset power-supply rejection	FSR = ±2.048 V, dc supply variation		0.2		LSB/V
	Offset channel match	Match between any two inputs		0.6		LSB
	Gain error(3)	FSR = ±2.048 V, T_A = 25°C		0.01%	0.15%	
	Gain drift(3)(4)	FSR = ±0.256 V		7		ppm/°C
		FSR = ±2.048 V		5	40	
		FSR = ±6.144 V(1)		5		
	Gain power-supply rejection			10		ppm/V
	Gain match(3)	Match between any two gains		0.01%	0.1%	
	Gain channel match	Match between any two inputs		0.01%	0.1%	
CMRR	Common-mode rejection ratio	At DC, FSR = ±0.256 V		105		dB
		At DC, FSR = ±2.048 V		100		
		At DC, FSR = ±6.144 V(1)		90		
		f_{CM} = 50 Hz, DR = 860 SPS		105		
		f_{CM} = 60 Hz, DR = 860 SPS		105		
TEMPERATURE SENSOR						
	Temperature range		–40		125	°C
	Temperature resolution			0.03125		°C/LSB
	Accuracy	T_A = 0°C to 70°C		0.2	±1	°C
		T_A = –40°C to +125°C		0.4	±2	
		vs supply		0.03125	±0.25	°C/V

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.
(2) Best-fit INL; covers 99% of full-scale.
(3) Includes all errors from onboard PGA and voltage reference.
(4) Maximum value specified by characterization.

Electrical Characteristics (continued)

Maximum and minimum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at VDD = 3.3 V, data rate = 8 SPS, and FSR = ±2.048 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{IH}	High-level input voltage		0.7 VDD		VDD	V
V_{IL}	Low-level input voltage		GND		0.2 VDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 VDD			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND		0.2 VDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	–10		10	µA
I_L	Input leakage, low	V_{IL} = GND	–10		10	µA
POWER SUPPLY						
I_{VDD}	Supply current	Power-down, T_A = 25°C		0.5	2	µA
		Power-down			5	
		Operating, T_A = 25°C		150	200	
		Operating			300	
P_D	Power dissipation	VDD = 5 V		0.9		mW
		VDD = 3.3 V		0.5		
		VDD = 2 V		0.3		

7.6 Timing Requirements: Serial Interface

over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
t_{CSSC}	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1)	100		ns
t_{SCCS}	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge	100		ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	200		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	Pulse duration, SCLK high	100		ns
t_{SPWL}	Pulse duration, SCLK low(2)	100		ns
			30.8	ms
t_{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t_{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) Holding SCLK low longer than 30.8 ms resets the SPI interface.

7.7 Switching Characteristics: Serial Interface

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CSDOD}	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	DOUT load = 20 pF || 100 kΩ to GND			100	ns
t_{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 100 kΩ to GND	0		50	ns
t_{CSDOZ}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20 pF || 100 kΩ to GND			100	ns

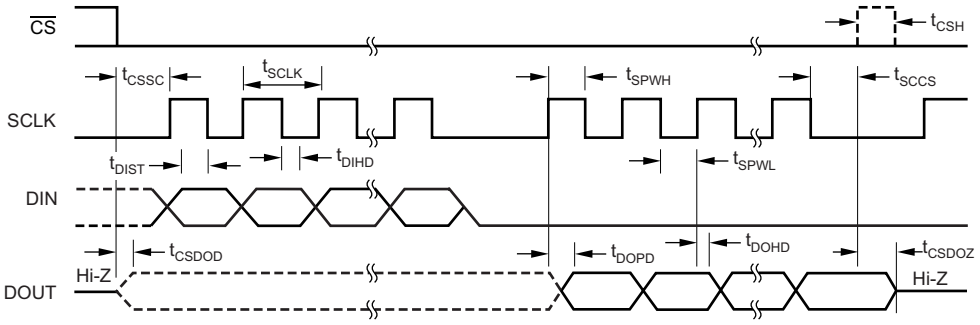
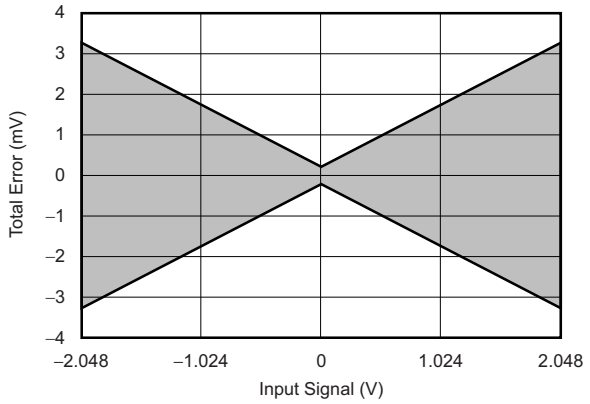


Figure 1. Serial Interface Timing

7.8 Typical Characteristics

at T_A = 25°C, VDD = 3.3 V, and FSR = ±2.048 V (unless otherwise noted)



DR = 860 SPS, diff Inputs; includes noise, offset, and gain errors

Figure 2. Total Error vs Input Signal

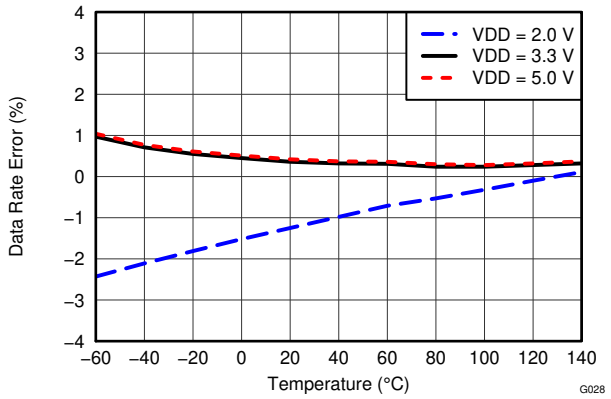


Figure 3. Data Rate vs Temperature

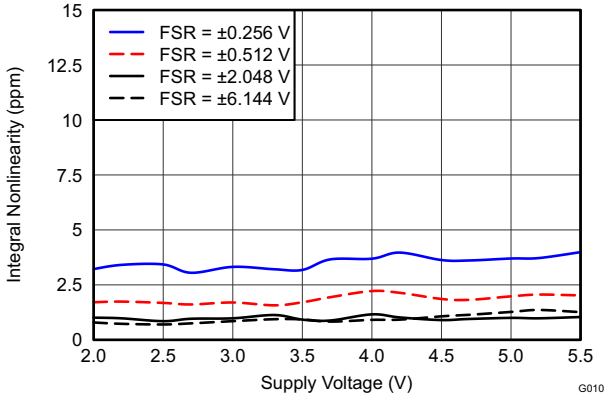
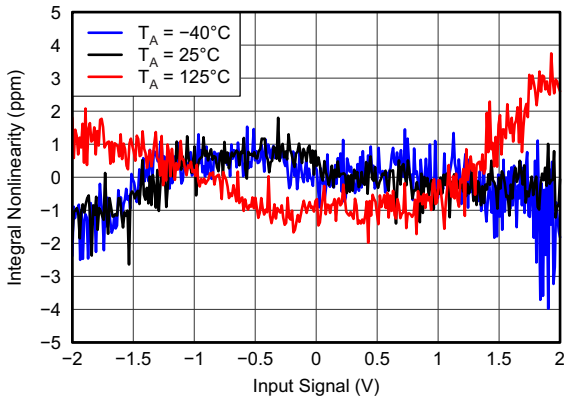
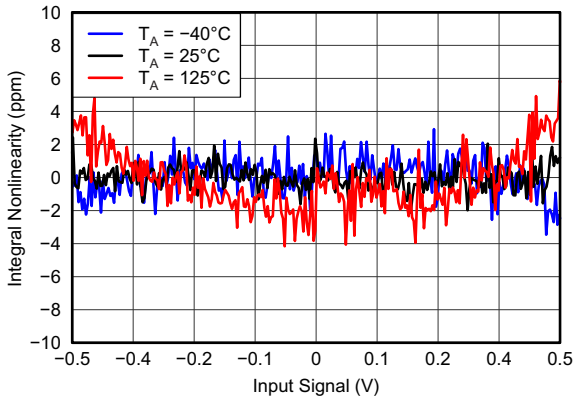


Figure 4. INL vs Supply Voltage



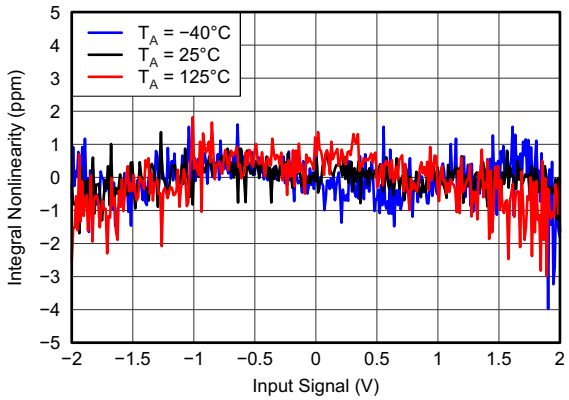
FSR = ±2.048 V, DR = 8 SPS, VDD = 3.3 V, best fit

Figure 5. INL vs Input Signal



FSR = ±0.512 V, DR = 8 SPS, VDD = 3.3 V, best fit

Figure 6. INL vs Input Signal

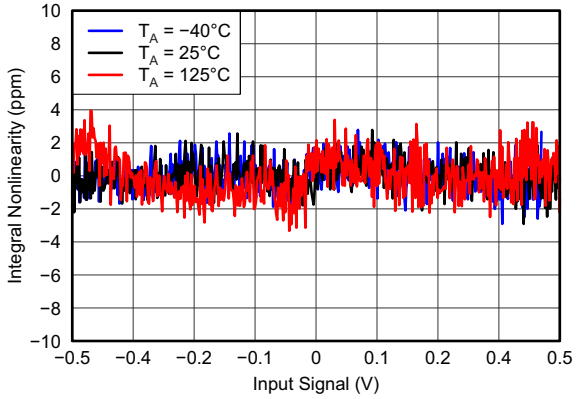


FSR = ±2.048 V, DR = 8 SPS, VDD = 5 V, best fit

Figure 7. INL vs Input Signal

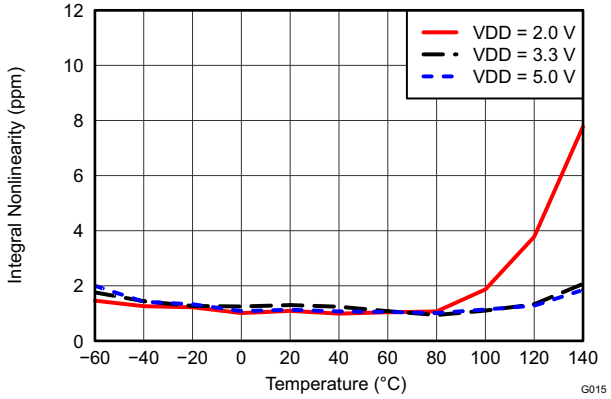
Typical Characteristics (continued)

at T_A = 25°C, VDD = 3.3 V, and FSR = ±2.048 V (unless otherwise noted)



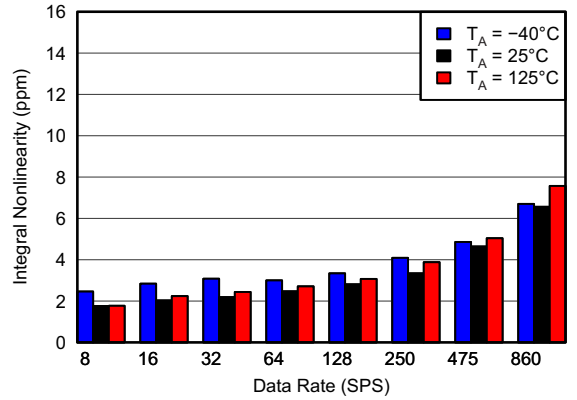
FSR = ±0.512 V, DR = 8 SPS, VDD = 5 V, best fit

Figure 8. INL vs Input Signal



FSR = ±2.048 V, DR = 8 SPS, best fit

Figure 9. INL vs Temperature



FSR = ±2.048 V, best fit

Figure 10. INL vs Data Rate

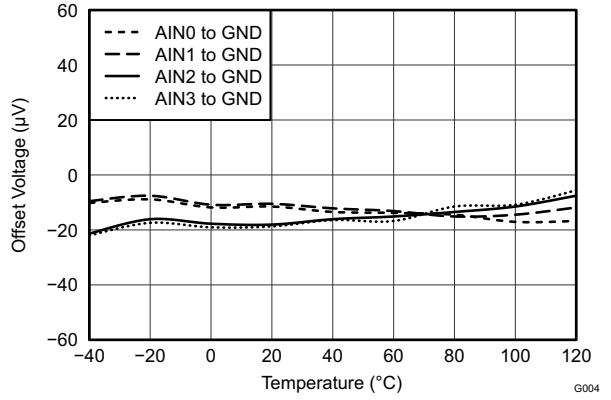


Figure 11. Single-Ended Offset Voltage vs Temperature

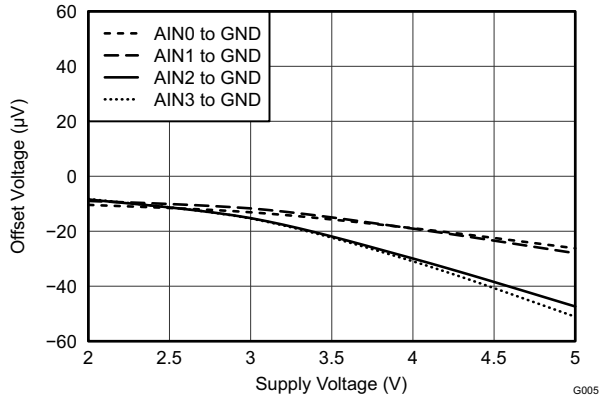


Figure 12. Single-Ended Offset Voltage vs Supply

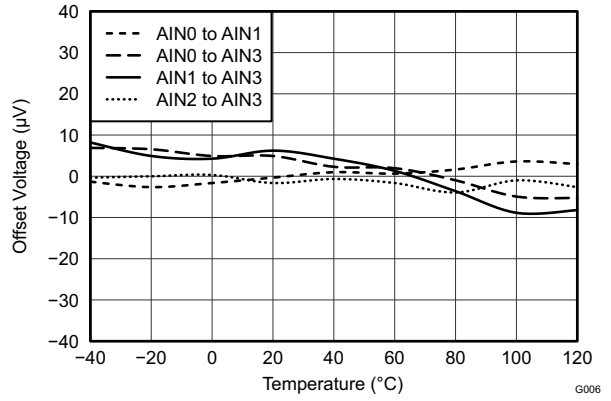


Figure 13. Differential Offset Voltage vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, VDD = 3.3 V, and FSR = ±2.048 V (unless otherwise noted)

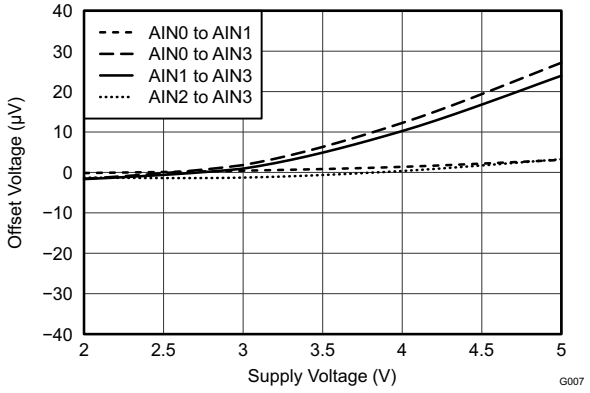
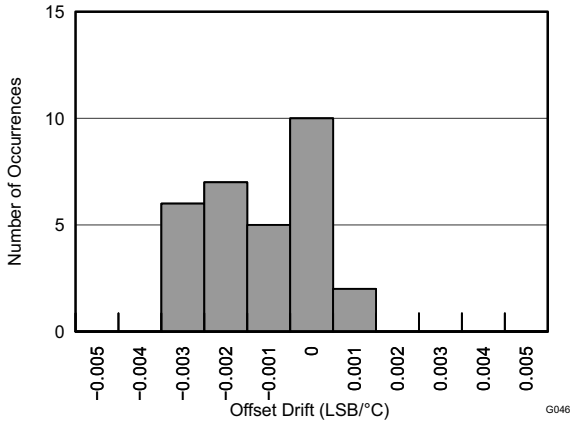
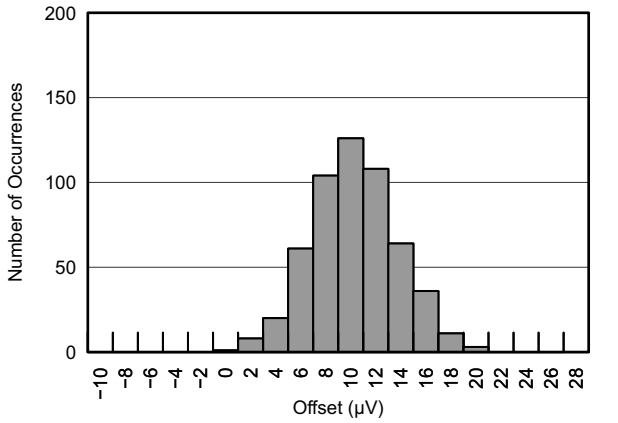


Figure 14. Differential Offset Voltage vs Supply



FSR = ±2.048 V, T_A = –40°C to +125°C, mux = AIN0 to AIN3,
540 units from 3 production lots

Figure 15. Offset Drift Histogram



FSR = ±2.048 V,
540 units from 3 production lots

Figure 16. Offset Histogram

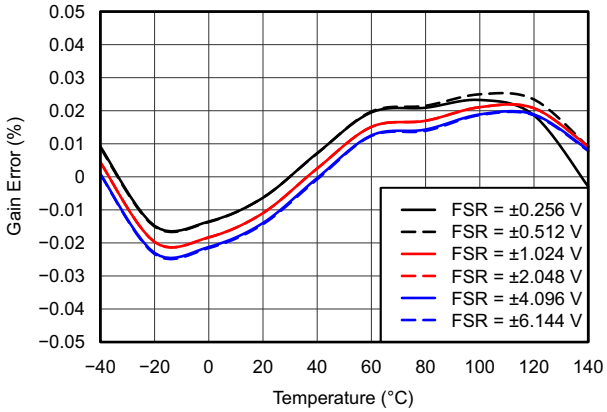


Figure 17. Gain Error vs Temperature

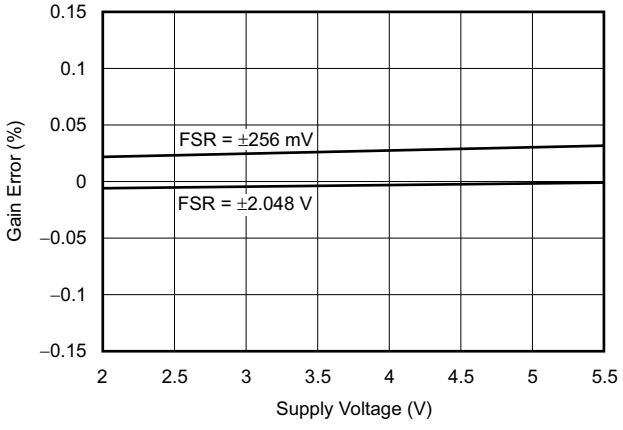
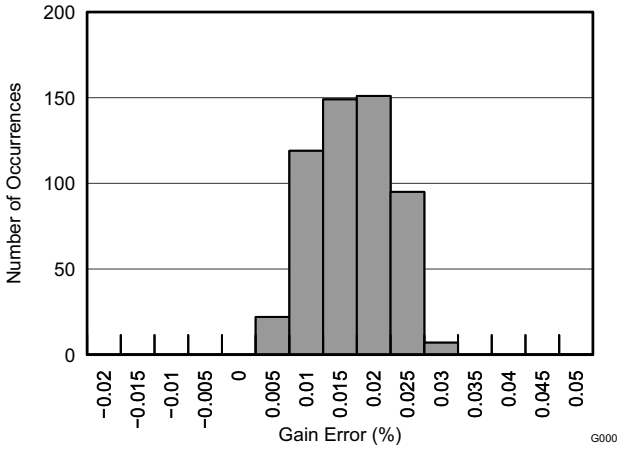


Figure 18. Gain Error vs Supply



FSR = ±2.048 V, 540 units from 3 production lots

Figure 19. Gain Error Histogram

Typical Characteristics (continued)

at T_A = 25°C, VDD = 3.3 V, and FSR = ±2.048 V (unless otherwise noted)

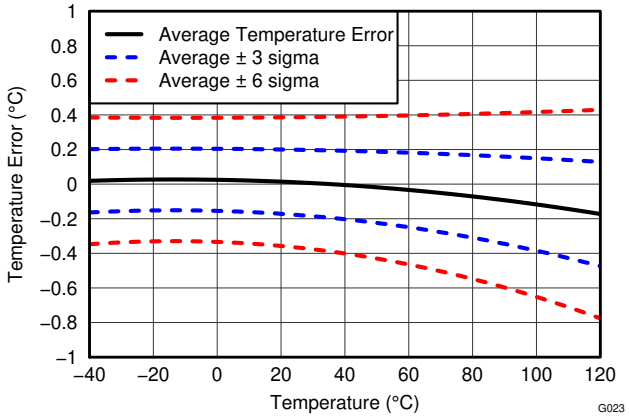
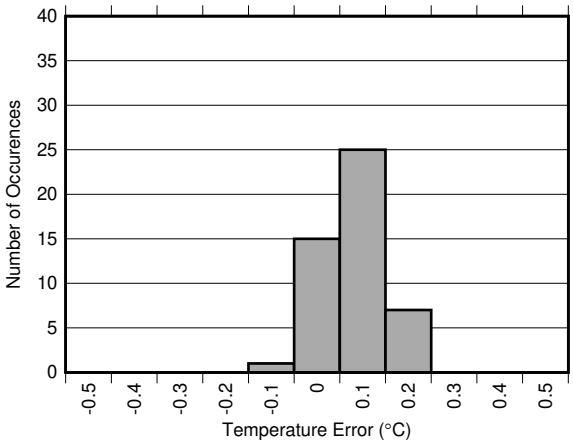
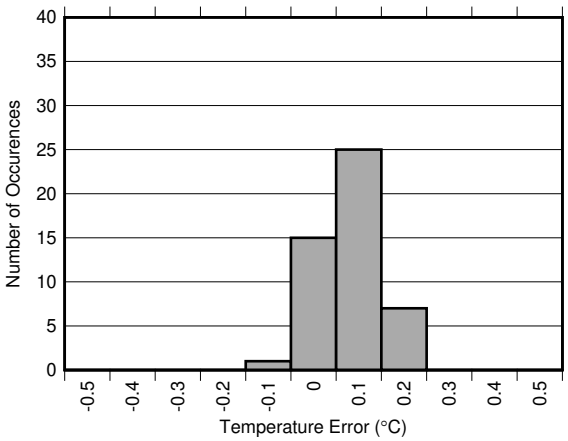


Figure 20. Temperature Sensor Error vs Temperature



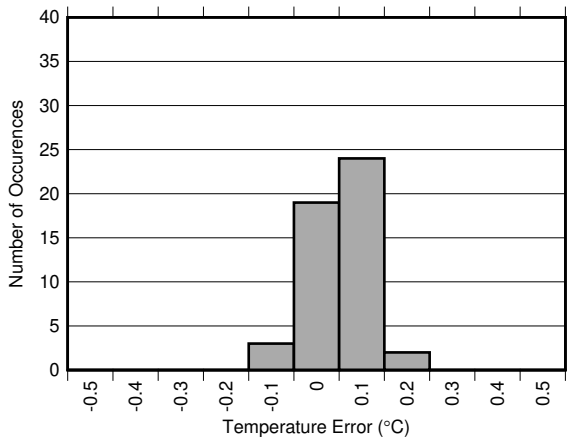
T_A = –40°C, 48 units from 3 production lots

Figure 21. Temperature Sensor Error Histogram



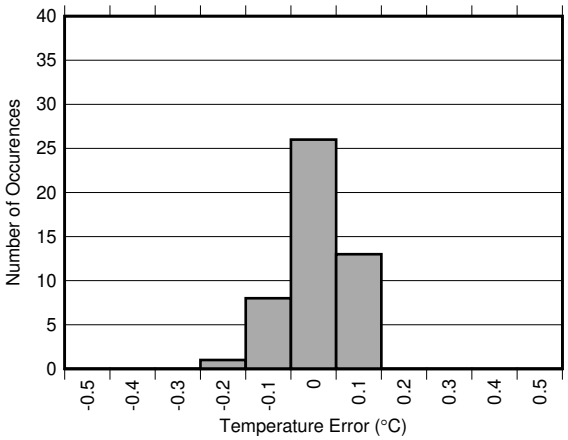
T_A = 0°C, 48 units from 3 production lots

Figure 22. Temperature Sensor Error Histogram



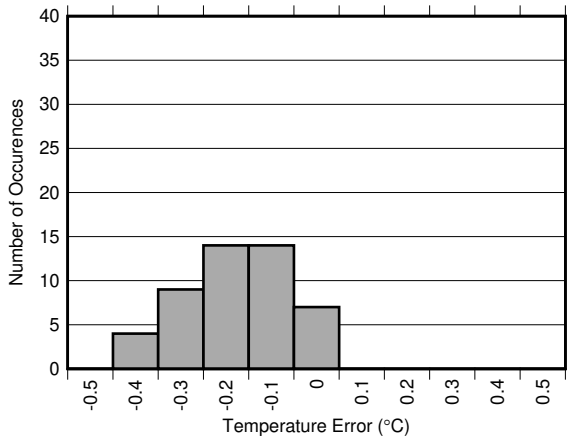
T_A = 25°C, 48 units from 3 production lots

Figure 23. Temperature Sensor Error Histogram



T_A = 70°C, 48 units from 3 production lots

Figure 24. Temperature Sensor Error Histogram



T_A = 125°C, 48 units from 3 production lots

Figure 25. Temperature Sensor Error Histogram

Typical Characteristics (continued)

at T_A = 25°C, VDD = 3.3 V, and FSR = ±2.048 V (unless otherwise noted)

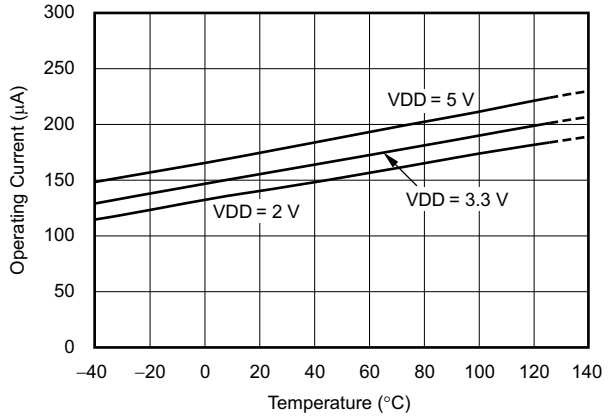


Figure 26. Operating Current vs Temperature

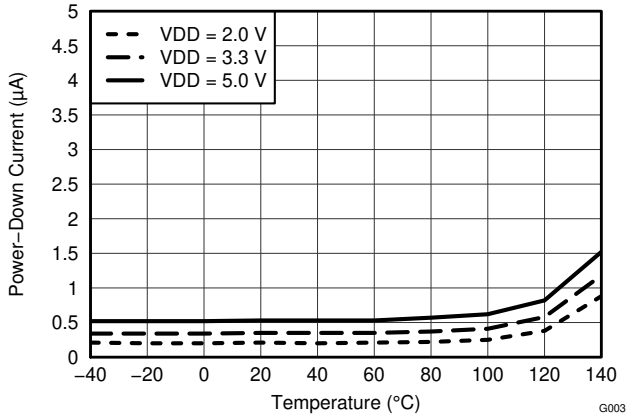


Figure 27. Power-Down Current vs Temperature

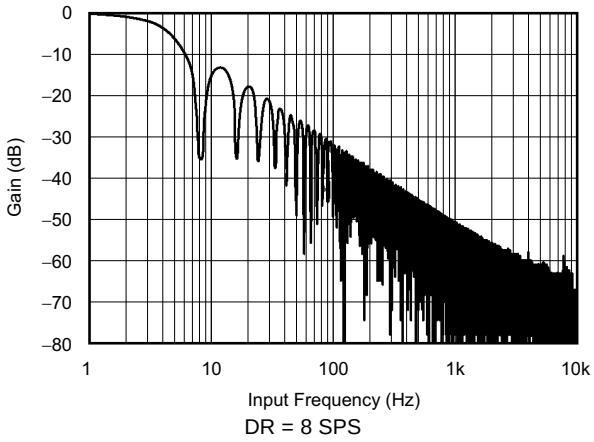


Figure 28. Digital Filter Frequency Response

8 Parameter Measurement Information

8.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converter (ADC) architecture is based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency), and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called the *oversampling ratio* (OSR). Increasing the OSR, and thus reducing the output data rate, optimizes the noise performance of the ADC. That is, the input-referred noise reduces when the output data rate is reduced because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, and is particularly useful when measuring low-level signals.

Table 1 and Table 2 summarize the device noise performance. Data are representative of typical noise performance at T_A = 25°C with the inputs shorted together externally. Table 1 show the input-referred noise in units of μV_{RMS} for the conditions shown. Note that μV_{PP} values are shown in parenthesis. Table 2 shows the corresponding data in effective number of bits (ENOB) calculated from μV_{RMS} values using Equation 1. The noise-free bits calculated from peak-to-peak noise values using Equation 2 are shown in parenthesis.

$$ENOB = \ln (FSR / V_{RMS\text{-}Noise}) / \ln(2) \quad (1)$$

$$\text{Noise-Free Bits} = \ln (FSR / V_{PP\text{-}Noise}) / \ln(2) \quad (2)$$

Table 1. Noise in μV_{RMS} (μV_{PP}) at VDD = 3.3 V

DATA RATE (SPS)	FULL-SCALE RANGE (FSR)					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8	187.5 (187.5)	125.0 (125.0)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
16	187.5 (187.5)	125.0 (125.0)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
32	187.5 (187.5)	125.0 (125.0)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
64	187.5 (187.5)	125.0 (125.0)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
128	187.5 (187.5)	125.0 (125.0)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (12.35)
250	187.5 (252.09)	125.0 (148.28)	62.5 (84.03)	31.25 (39.54)	15.62 (16.06)	7.81 (18.53)
475	187.5 (266.92)	125.0 (227.38)	62.5 (79.08)	31.25 (56.84)	15.62 (32.13)	7.81 (25.95)
860	187.5 (430.06)	125.0 (266.93)	62.5 (118.63)	31.25 (64.26)	15.62 (40.78)	7.81 (35.83)

Table 2. ENOB from RMS Noise (Noise-Free Bits from Peak-to-Peak Noise) at VDD = 3.3 V

DATA RATE (SPS)	FULL-SCALE RANGE (FSR)					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
32	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
64	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
128	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.33)
250	16 (15.57)	16 (15.75)	16 (15.57)	16 (15.66)	16 (15.96)	16 (14.75)
475	16 (15.49)	16 (15.13)	16 (15.66)	16 (15.13)	16 (14.95)	16 (14.26)
860	16 (14.8)	16 (14.9)	16 (15.07)	16 (14.95)	16 (14.61)	16 (13.8)

9 Detailed Description

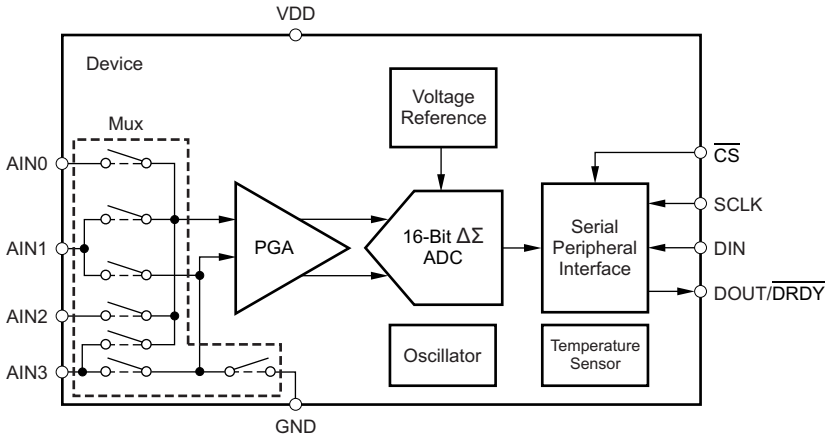
9.1 Overview

The ADS1118-Q1 is a very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1118-Q1 consists of a ΔΣ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. The *Functional Block Diagram* section shows the ADS1118-Q1 functional block diagram.

The ADS1118-Q1 ADC core measures a differential signal, V_{IN}, that is the difference of $V_{(AINP)}$ and $V_{(AINN)}$. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1118-Q1 has two available conversion modes: single-shot and continuous-conversion. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Multiplexer

The ADS1118-Q1 contains an input multiplexer (mux), as shown in Figure 29. Either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 can be measured differentially to AIN3. The multiplexer is configured by bits MUX[2:0] in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

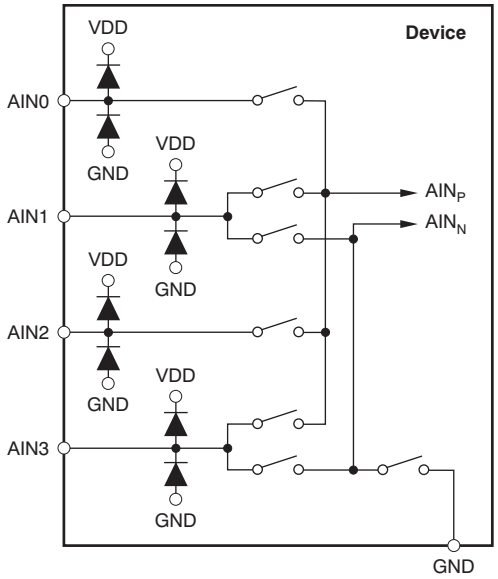


Figure 29. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes indicate negative differential signals; that is, $(V_{(AINP)} - V_{(AINN)}) < 0$. Electrostatic discharge (ESD) diodes to VDD and GND protect the ADS1118-Q1 inputs. To prevent the ESD diodes from turning on, keep the absolute voltage on any input within the range given in Equation 3:

$$GND - 0.3\ V < V_{(AINx)} < VDD + 0.3\ V \quad (3)$$

If the voltages on the input pins can possibly violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see the *Absolute Maximum Ratings* table).

Also, overdriving one unused input on the ADS1118-Q1 may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, clamp the signal with external Schottky diodes.

Feature Description (continued)

9.3.2 Analog Inputs

The ADS1118-Q1 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. This frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency ($f_{(MOD)}$). The ADS1118-Q1 has a 1 MHz internal oscillator which is further divided by a factor of 4 to generate the modulator frequency at 250 kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 30. The resistance is set by the capacitor values and the rate at which they are switched. Figure 31 shows the setting of the switches illustrated in Figure 30. During the sampling phase, switches S_1 are closed. This event charges C_{A1} to $V_{(AINP)}$, C_{A2} to $V_{(AINN)}$, and C_B to ($V_{(AINP)} – V_{(AINN)}$). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7 V and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the ADS1118-Q1 analog inputs. The average value of this current can be used to calculate the effective impedance (Z_{eff}), where $Z_{eff} = V_{IN} / I_{AVERAGE}$.

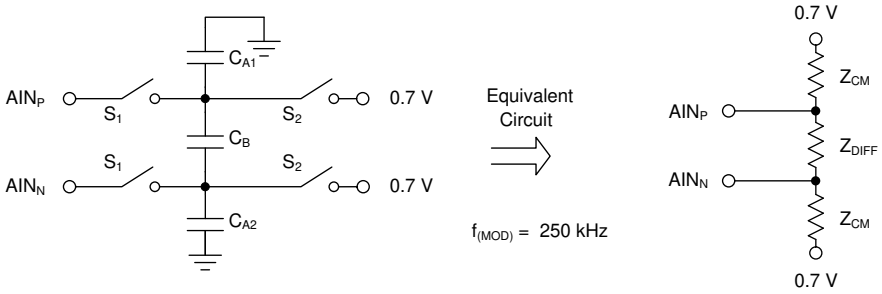


Figure 30. Simplified Analog Input Circuit

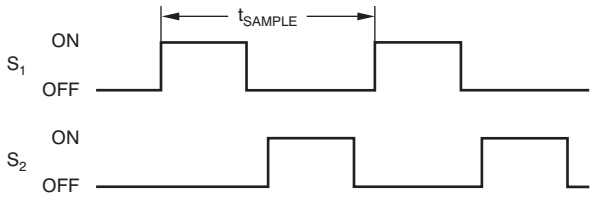


Figure 31. S_1 and S_2 Switch Timing

Common-mode input impedance is measured by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6 MΩ for the default full-scale range. In Figure 30, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the full-scale range. In Figure 30, the differential input impedance is Z_{DIFF}.

Make sure to consider the typical value of the input impedance. Unless the input source has a low impedance, the ADS1118-Q1 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible, and can be ignored.

Feature Description (continued)

9.3.3 Full-Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented in front of the ADS1118-Q1 ΔΣ ADC core. The full-scale range is configured by bits PGA[2:0] in the Config register, and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, or ±0.256 V.

Table 3 shows the FSR together with the corresponding LSB size. Calculate the LSB size from the full-scale voltage by the formula shown in Equation 4. However, make sure that the analog input voltage never exceeds the analog input voltage range limit given in the *Electrical Characteristics*. If VDD greater than 4 V is used, the ±6.144-V full-scale range allows input voltages to extend up to the supply. Note though that in this case, or whenever the supply voltage is less than the full-scale range (for example, VDD = 3.3 V and full-scale range = ±4.096 V), a full-scale ADC output code cannot be obtained. This inability means that some dynamic range is lost.

$$LSB = FSR / 2^{16} \quad (4)$$

Table 3. Full-Scale Range and Corresponding LSB Size

FSR	LSB SIZE
±6.144 V(1)	187.5 μV
±4.096 V(1)	125 μV
±2.048 V	62.5 μV
±1.024 V	31.25 μV
±0.512 V	15.625 μV
±0.256 V	7.8125 μV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

9.3.4 Voltage Reference

The ADS1118-Q1 has an integrated voltage reference. An external reference cannot be used with this device. Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics*.

9.3.5 Oscillator

The ADS1118-Q1 has an integrated oscillator running at 1 MHz. No external clock is required to operate the device. Note that the internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

9.3.6 Temperature Sensor

The ADS1118-Q1 offers an integrated precision temperature sensor. To enable the temperature sensor mode, set bit TS_MODE = 1 in the Config register. Temperature data are represented as a 14-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format, as shown in Table 4.

Table 4. 14-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
–0.25	11 1111 1111 1000	3FF8
–25	11 1100 1110 0000	3CE0
–40	11 1011 0000 0000	3B00

9.3.6.1 Converting from Temperature to Digital Codes

For positive temperatures:

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit, left justified format with the MSB = 0 to denote the positive sign.

Example: 50°C / (0.03125°C/count) = 1600 = 0640h = 00 0110 0100 0000

For negative temperatures:

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1.

Example: |–25°C| / (0.03125°C/count) = 800 = 0320h = 00 0011 0010 0000

Twos complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

9.3.6.2 Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all of the bits. Then, multiply the result by –0.03125°C.

Example: The device reads back 0960h: 0960h has an MSB = 0.

0960h × 0.03125°C = 2400 × 0.03125°C = 75°C

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.

Subtract 1 and complement the result: 3CE0h → 0320h

0320h × (–0.03125°C) = 800 × (–0.03125°C) = –25°C

9.4 Device Functional Modes

9.4.1 Reset and Power-Up

When the ADS1118-Q1 powers up, the device resets. As part of the reset process, the ADS1118-Q1 sets all bits in the Config register to the respective default settings. By default, the ADS1118-Q1 enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1118-Q1 relieves systems with tight power-supply requirements from encountering a surge during power-up.

9.4.2 Operating Modes

The ADS1118-Q1 operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the Config register selects the respective operating mode.

9.4.2.1 Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, the ADS1118-Q1 enters a power-down state, and operates in single-shot mode. This power-down state is the default state for the ADS1118-Q1 when power is first applied. Although powered down, the device still responds to commands. The ADS1118-Q1 remains in this power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is asserted, the device powers up, resets the SS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a 1 to the SS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the Config register.

9.4.2.2 Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0), the ADS1118-Q1 continuously performs conversions. When a conversion completes, the ADS1118-Q1 places the result in the Conversion register and immediately begins another conversion. To switch to single-shot mode, write a 1 to the MODE bit in the Config register, or reset the device.

9.4.3 Duty Cycling for Low Power

The noise performance of a $\Delta\Sigma$ ADC generally improves when lowering the output data rate because more samples of the internal modulator are averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADS1118-Q1 supports duty cycling that can yield significant power savings by periodically requesting high data-rate readings at an effectively lower data rate.

For example, an ADS1118-Q1 in power-down state with a data rate set to 860 SPS can be operated by a microcontroller that instructs a single-shot conversion every 125 ms (8 SPS). A conversion at 860 SPS only requires approximately 1.2 ms; therefore, the ADS1118-Q1 enters power-down state for the remaining 123.8 ms. In this configuration, the ADS1118-Q1 consumes approximately 1/100th the power that is otherwise consumed in continuous-conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADS1118-Q1 offers lower data rates that do not implement duty cycling and also offers improved noise performance, if required.

9.5 Programming

9.5.1 Serial Interface

The SPI-compatible serial interface consists of either four signals ($\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$), or three signals (SCLK, DIN, and DOUT/$\overline{DRDY}$, with $\overline{CS}$ tied low). The interface is used to read conversion data, read from and write to registers, and control device operation.

9.5.2 Chip Select ($\overline{CS}$)

The chip select pin ($\overline{CS}$) selects the ADS1118-Q1 for SPI communication. This feature is useful when multiple devices share the same serial bus. Keep $\overline{CS}$ low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT/$\overline{DRDY}$ enters a high-impedance state. In this state, DOUT/$\overline{DRDY}$ cannot provide data-ready indication. In situations where multiple devices are present and DOUT/$\overline{DRDY}$ must be monitored, lower $\overline{CS}$ periodically. At this point, the DOUT/$\overline{DRDY}$ pin either immediately goes high to indicate that no new data are available, or immediately goes low to indicate that new data are present in the Conversion register and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption.

9.5.3 Serial Clock (SCLK)

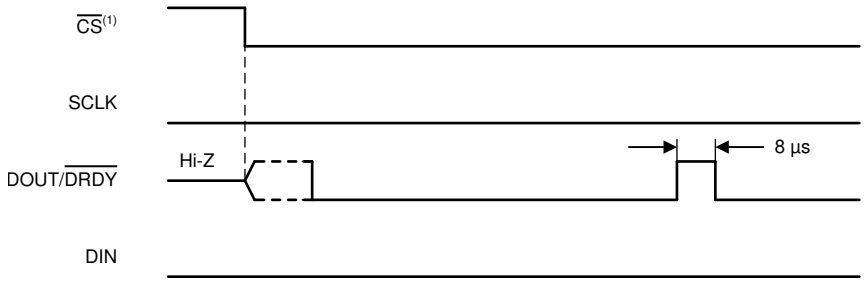
The serial clock pin (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/$\overline{DRDY}$ pins into and out of the ADS1118-Q1. Even though the input has hysteresis, keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. To reset the serial interface, hold SCLK low for 30.8 ms, and the next SCLK pulse starts a new communication cycle. Use this time-out feature to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

9.5.4 Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1118-Q1. The device latches data on DIN at the SCLK falling edge. The ADS1118-Q1 never drives the DIN pin.

9.5.5 Data Output and Data Ready (DOUT/$\overline{DRDY}$)

The data output and data ready pin (DOUT/$\overline{DRDY}$) is used with SCLK to read conversion and register data from the ADS1118-Q1. Data on DOUT/$\overline{DRDY}$ are shifted out on the SCLK rising edge. DOUT/$\overline{DRDY}$ is also used to indicate that a conversion is complete and new data are available. This pin transitions low when new data are ready for retrieval. DOUT/$\overline{DRDY}$ is also able to trigger a microcontroller to start reading data from the ADS1118-Q1. In continuous-conversion mode, DOUT/$\overline{DRDY}$ transitions high again 8 µs before the next data ready signal (DOUT/$\overline{DRDY}$ low) if no data are retrieved from the device. This transition is shown in Figure 32. Complete the data transfer before DOUT/$\overline{DRDY}$ returns high.



(1) $\overline{CS}$ can be held low if the ADS1118-Q1 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 32. DOUT/$\overline{DRDY}$ Behavior Without Data Retrieval in Continuous-Conversion Mode

When $\overline{CS}$ is high, DOUT/$\overline{DRDY}$ is configured by default with a weak internal pullup resistor. This feature reduces the risk of DOUT/$\overline{DRDY}$ floating near midsupply and causing leakage current in the master device. To disable this pullup resistor and place the device into a high-impedance state, set the PULL_UP_EN bit to 0 in the Config register.

Programming (continued)

9.5.6 Data Format

The ADS1118-Q1 provides 16 bits of data in binary twos complement format. A positive full-scale (+FS) input produces an output code of 7FFFh and a negative full-scale (–FS) input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 5 summarizes the ideal output codes for different input signals. Figure 33 shows code transitions versus input voltage.

Table 5. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ +FS (2^{15} – 1) / 2^{15}	7FFFh
+FS / 2^{15}	0001h
0	0
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

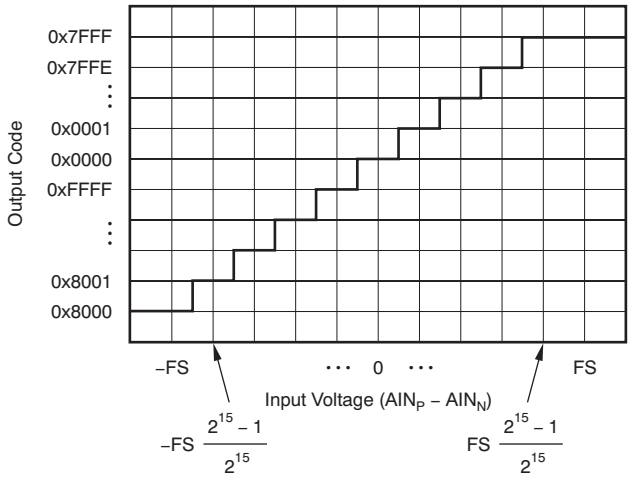


Figure 33. Code Transition Diagram

9.5.7 Data Retrieval

Data is written to and read from the ADS1118-Q1 in the same manner for both single-shot and continuous conversion modes, without having to issue any commands. The operating mode for the ADS1118-Q1 is selected by the MODE bit in the Config register.

Set the MODE bit to 0 to put the device in continuous-conversion mode. In continuous-conversion mode, the device is constantly starting new conversions even when $\overline{CS}$ is high.

Set the MODE bit to 1 for single-shot mode. In single-shot mode, a new conversion only starts by writing a 1 to the SS bit.

The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/$\overline{DRDY}$ asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/$\overline{DRDY}$. The MSB of the data (bit 15) on DOUT/$\overline{DRDY}$ is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/$\overline{DRDY}$, new Config register data are latched on DIN on the SCLK falling edge.

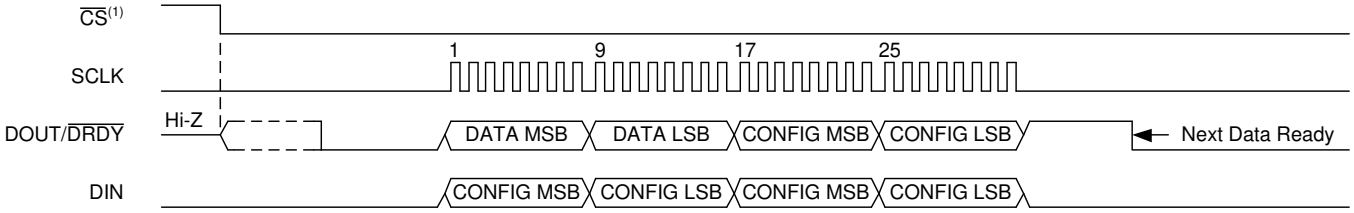
The ADS1118-Q1 also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits (only used when the $\overline{CS}$ line can be controlled and is not permanently tied low).

9.5.7.1 32-Bit Data Transmission Cycle

The data in a 32-bit data transmission cycle consist of four bytes: two bytes for the conversion result, and an additional two bytes for the Config register readback. The device always reads the MSB first.

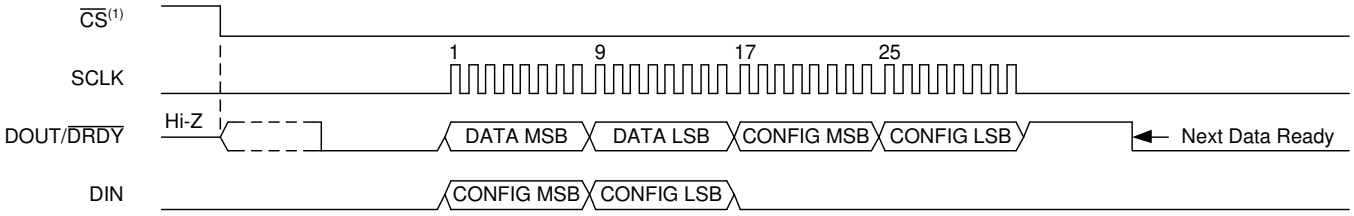
Write the same Config register setting twice during one transmission cycle as shown in Figure 34. If convenient, write the Config register setting once during the first half of the transmission cycle, and then hold the DIN pin either low (as shown in Figure 35) or high during the second half of the cycle. If no update to the Config register is required, hold the DIN pin either low or high during the entire transmission cycle. The Config register setting written in the first two bytes of a 32-bit transmission cycle is read back in the last two bytes of the same cycle.

A continuous SCLK can be used for the entire 32-bit data transfer as long as the SCLK frequency is less than 1 MHz. If an SCLK frequency greater than 1 MHz is used, add a delay between the transmission of the first 16 bits and the second 16 bits to allow for complete decoding of the Config register write prior to the readback of the Config register. Choose the delay such that the time between the SCLK rising edge of the first bit and the SCLK rising edge of the 17th bit is greater than 16 µs.



(1) $\overline{CS}$ can be held low if the ADS1118-Q1 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 34. 32-Bit Data Transmission Cycle With Config Register Readback



(1) $\overline{CS}$ can be held low if the ADS1118-Q1 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 35. 32-Bit Data Transmission Cycle: DIN Held Low

9.5.7.2 16-Bit Data Transmission Cycle

If Config register data are not required to be read back, the ADS1118-Q1 conversion data can be clocked out in a short 16-bit data transmission cycle, as shown in Figure 36. Take $\overline{CS}$ high after the 16th SCLK cycle to reset the SPI interface. The next time $\overline{CS}$ is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/$\overline{DRDY}$ is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/$\overline{DRDY}$ is high, the same result from the previous data transmission cycle is read.

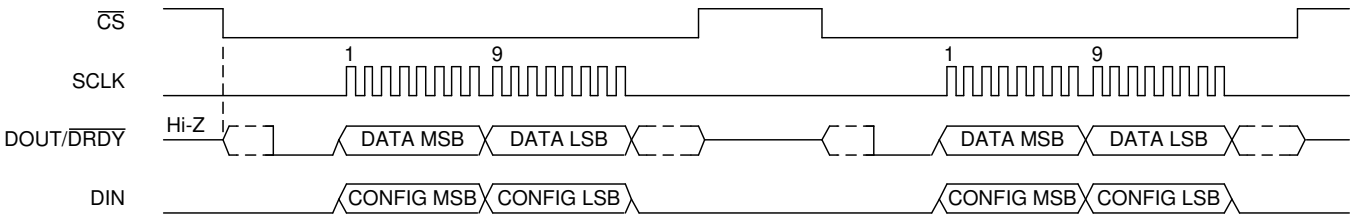


Figure 36. 16-Bit Data Transmission Cycle

9.6 Register Maps

The ADS1118-Q1 has two registers that are accessible through the SPI. The Conversion register contains the result of the last conversion. The Config register allows the user to change the ADS1118-Q1 operating modes and query the status of the devices.

9.6.1 Conversion Register [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary twos complement format. Following power up, the Conversion register is cleared to 0, and remains 0 until the first conversion is complete. The register format is shown in Figure 37.

Figure 37. Conversion Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

9.6.2 Config Register [reset = 058Bh]

The 16-bit Config register can be used to control the ADS1118-Q1 operating mode, input selection, data rate, full-scale range, and temperature sensor mode. The register format is shown in Figure 38.

Figure 38. Config Register

15	14	13	12	11	10	9	8
SS	MUX[2:0]			PGA[2:0]			MODE
R/W-0h	R/W-0h			R/W-2h			R/W-1h
7	6	5	4	3	2	1	0
DR[2:0]			TS_MODE	PULL_UP_EN	NOP[1:0]		Reserved
R/W-4h			R/W-0h	R/W-1h	R/W-1h		R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SS	R/W	0h	**Single-shot conversion start** This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0 = No effect 1 = Start a single conversion (when in power-down state) Always reads back as 0 (default).
14:12	MUX[2:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. 000 = AIN_P is AIN0 and AIN_N is AIN1 (default) 001 = AIN_P is AIN0 and AIN_N is AIN3 010 = AIN_P is AIN1 and AIN_N is AIN3 011 = AIN_P is AIN2 and AIN_N is AIN3 100 = AIN_P is AIN0 and AIN_N is GND 101 = AIN_P is AIN1 and AIN_N is GND 110 = AIN_P is AIN2 and AIN_N is GND 111 = AIN_P is AIN3 and AIN_N is GND

Table 7. Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	PGA[2:0]	R/W	2h	**Programmable gain amplifier configuration** These bits configure the programmable gain amplifier. 000 = FSR is ±6.144 V(1) 001 = FSR is ±4.096 V(1) 010 = FSR is ±2.048 V (default) 011 = FSR is ±1.024 V 100 = FSR is ±0.512 V 101 = FSR is ±0.256 V 110 = FSR is ±0.256 V 111 = FSR is ±0.256 V
8	MODE	R/W	1h	**Device operating mode** This bit controls the ADS1118-Q1 operating mode. 0 = Continuous-conversion mode 1 = Power-down and single-shot mode (default)
7:5	DR[2:0]	R/W	4h	**Data rate** These bits control the data-rate setting. 000 = 8 SPS 001 = 16 SPS 010 = 32 SPS 011 = 64 SPS 100 = 128 SPS (default) 101 = 250 SPS 110 = 475 SPS 111 = 860 SPS
4	TS_MODE	R/W	0h	**Temperature sensor mode** This bit configures the ADC to convert temperature or input signals. 0 = ADC mode (default) 1 = Temperature sensor mode
3	PULL_UP_EN	R/W	1h	**Pullup enable** This bit enables a weak internal pullup resistor on the DOUT/$\overline{\text{DRDY}}$ pin only when $\overline{\text{CS}}$ is high. When enabled, an internal 400-kΩ resistor connects the bus line to supply. When disabled, the DOUT/$\overline{\text{DRDY}}$ pin floats. 0 = Pullup resistor disabled on DOUT/$\overline{\text{DRDY}}$ pin 1 = Pullup resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin (default)
2:1	NOP[1:0]	R/W	1h	**No operation** The NOP[1:0] bits control whether data are written to the Config register or not. For data to be written to the Config register, the NOP[1:0] bits must be 01. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register. 00 = Invalid data; do not update the contents of the Config register 01 = Valid data; update the Config register (default) 10 = Invalid data; do not update the contents of the Config register 11 = Invalid data; do not update the contents of the Config register
0	Reserved	R	1h	**Reserved** Writing either 0 or 1 to this bit has no effect. Always reads back 1.

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS1118-Q1 is a precision, 16-bit ΔΣ ADC that offers many integrated features to ease the measurement of the most common sensor types including various type of temperature and bridge sensors. The following sections give example circuits and suggestions for using the ADS1118-Q1 in various situations.

10.1.1 Serial Interface Connections

The principle serial interface connections for the ADS1118-Q1 are shown in Figure 39.

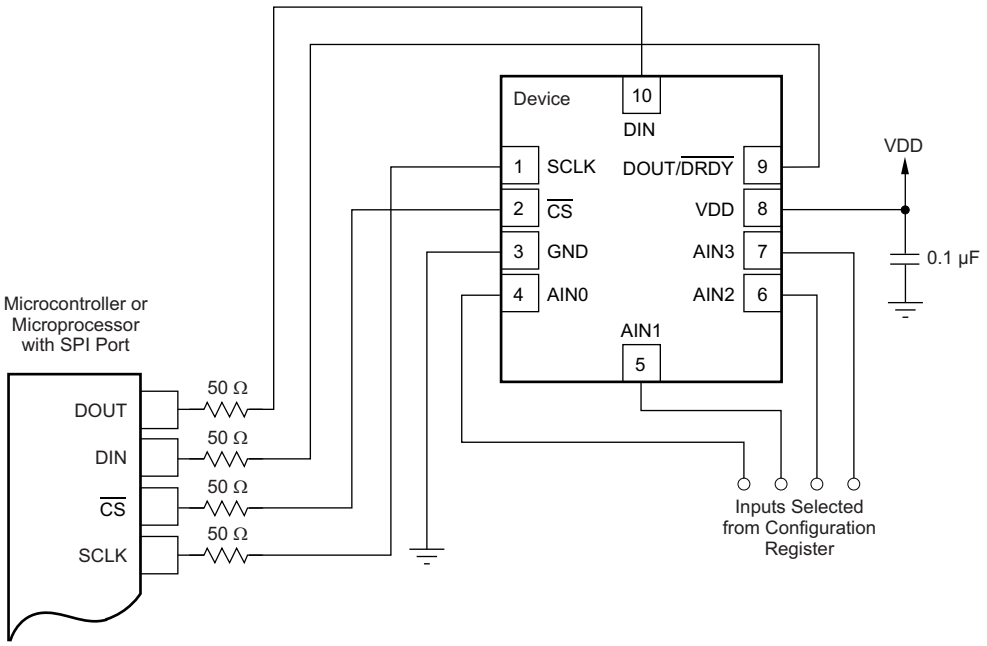


Figure 39. Typical Connections

Most microcontroller SPI peripherals operate with the ADS1118-Q1. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1, SCLK idles low, and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the ADS1118-Q1 can be found in the *Timing Requirements: Serial Interface* section.

It is a good practice to place 50-Ω resistors in the series path to each of the digital pins to provide some short-circuit protection. Take care to still meet all SPI timing requirements because these additional series resistors along with the bus parasitic capacitances present on the digital signal lines slews the signals.

The fully-differential input of the ADS1118-Q1 is ideal for connecting to differential sources (such as thermocouples and thermistors) with a moderately low source impedance. Although the ADS1118-Q1 can read fully-differential signals, the device cannot accept negative voltages on either of its inputs because of ESD protection diodes on each pin. When an input exceeds supply or drops below ground, these diodes turn on to prevent any ESD damage to the device.

Application Information (continued)

10.1.2 GPIO Ports for Communication

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADS1118-Q1 can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface requires only that the pins be configured as push or pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 30.8 ms, communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 30.8 ms between pulses.

10.1.3 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter repeats at multiples of the sampling frequency, also known as modulator frequency $f_{(MOD)}$, as shown in Figure 40. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

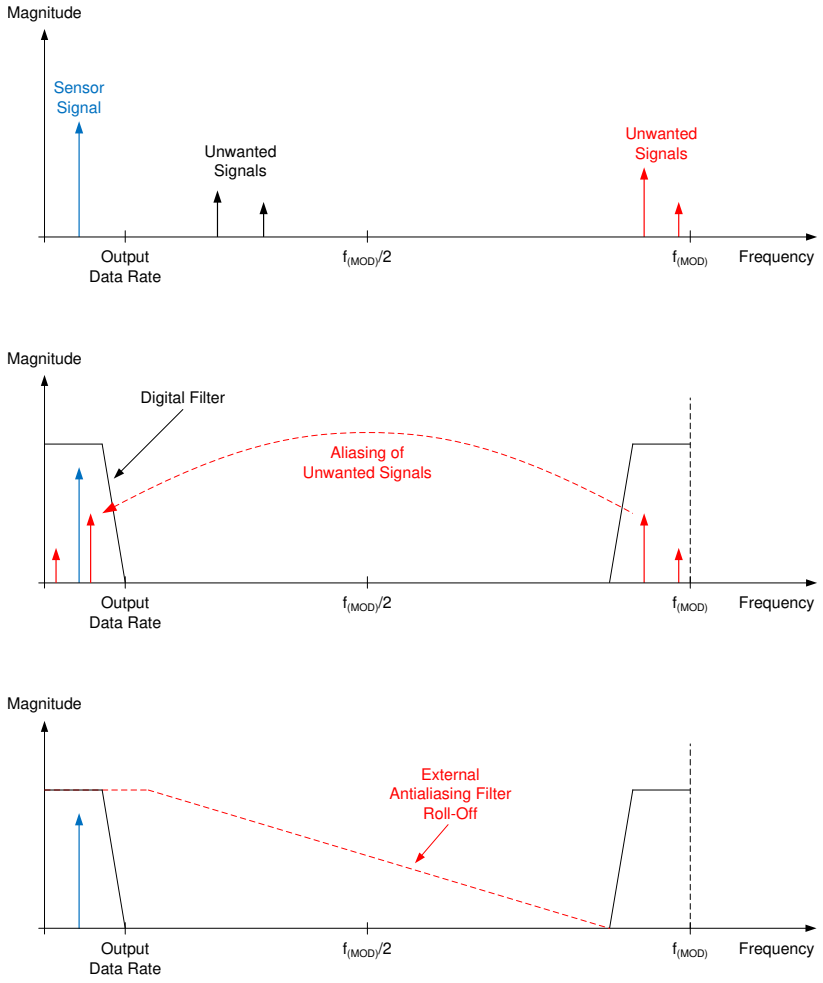


Figure 40. Effect of Aliasing

Application Information (continued)

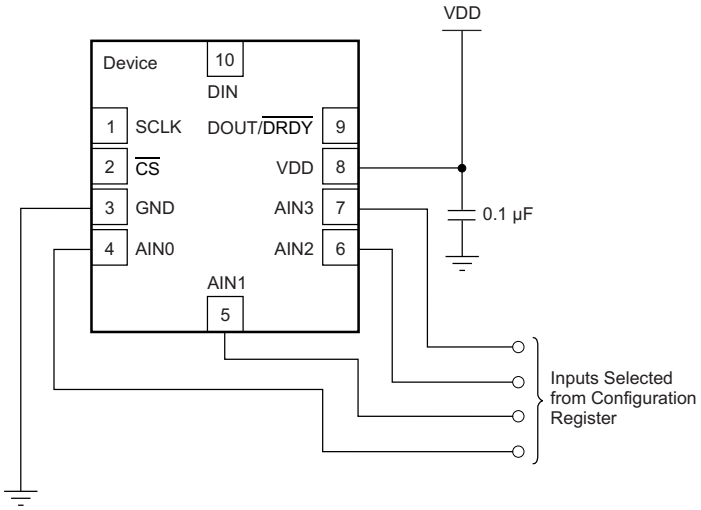
Many sensor signals are inherently band-limited; for example, the output of a thermocouple has a limited rate of change. In this case the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pickup along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed-circuit-board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order, resistor-capacitor (RC) filter is, in most cases, sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{(MOD)}$ / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1118-Q1 attenuates signals to a certain degree, as shown in Figure 28. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or ten times higher is generally a good starting point for a system design.

10.1.4 Single-Ended Inputs

Although the ADS1118-Q1 has two differential inputs, the device can measure four single-ended signals. Figure 41 shows a single-ended connection scheme. The ADS1118-Q1 is configured for single-ended measurement by configuring the mux to measure each channel with respect to ground. Data are then read out of one input based on the selection in the Config register. The single-ended signal can range from 0 V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to this circuit because the ADS1118-Q1 can only accept positive voltages with respect to ground. The ADS1118-Q1 does not lose linearity within the input range.

The ADS1118-Q1 offers a differential input voltage range of ±FS. The single-ended circuit shown in Figure 41, however, only uses the positive half of the ADS1118-Q1 FS input voltage range because differentially negative inputs are not produced. Because only half of the FS range is used, one bit of resolution is lost. For optimal noise performance, use differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.



NOTE: Digital pin connections omitted for clarity.

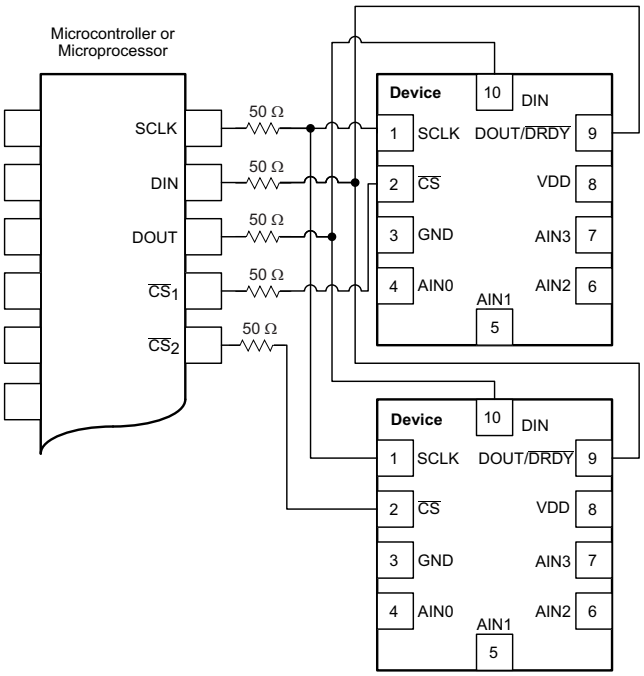
Figure 41. Measuring Single-Ended Inputs

The ADS1118-Q1 also allows AIN3 to serve as a common point for measurements by adjusting the mux configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the ADS1118-Q1 operates with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND < $V_{(AIN3)}$ < VDD; however, common-mode noise attenuation is not offered.

Application Information (continued)

10.1.5 Connecting Multiple Devices

When connecting multiple ADS1118-Q1 devices to a single SPI bus, SCLK, DIN, and DOUT/$\overline{\text{DRDY}}$ can be safely shared by using a dedicated chip-select ($\overline{\text{CS}}$) for each SPI-enabled device. By default, when $\overline{\text{CS}}$ goes high for the ADS1118-Q1, DOUT/$\overline{\text{DRDY}}$ is pulled up to VDD by a weak pullup resistor. This feature prevents DOUT/$\overline{\text{DRDY}}$ from floating near midrail and causing excess current leakage on a microcontroller input. If the PULL_UP_EN bit in the Config register is set to 0, the DOUT/$\overline{\text{DRDY}}$ pin enters a 3-state mode when $\overline{\text{CS}}$ transitions high. The ADS1118-Q1 cannot issue a data-ready pulse on DOUT/$\overline{\text{DRDY}}$ when $\overline{\text{CS}}$ is high. To evaluate when a new conversion is ready from the ADS1118-Q1 when using multiple devices, the master can periodically drop $\overline{\text{CS}}$ to the ADS1118-Q1. When $\overline{\text{CS}}$ goes low, the DOUT/$\overline{\text{DRDY}}$ pin immediately drives either high or low. If the DOUT/$\overline{\text{DRDY}}$ line drives low on a low $\overline{\text{CS}}$, new data are currently available for clocking out at any time. If the DOUT/$\overline{\text{DRDY}}$ line drives high, no new data are available and the ADS1118-Q1 returns the last read conversion result. Valid data can be retrieved from the ADS1118-Q1 at anytime without concern of data corruption. If a new conversion becomes available during data transmission, that conversion is not available for readback until a new SPI transmission is initiated.



NOTE: Power and input connections omitted for clarity.

Figure 42. Connecting Multiple ADS1118-Q1s

Application Information (continued)

10.1.6 Pseudo Code Example

The flow chart in Figure 43 shows a pseudo-code sequence with the required steps to set up communication between the device and a microcontroller to take subsequent readings from the ADS1118-Q1. As an example, the default Config register settings are changed to set up the device for FSR = ±0.512 V, continuous-conversion mode, and a 64-SPS data rate.

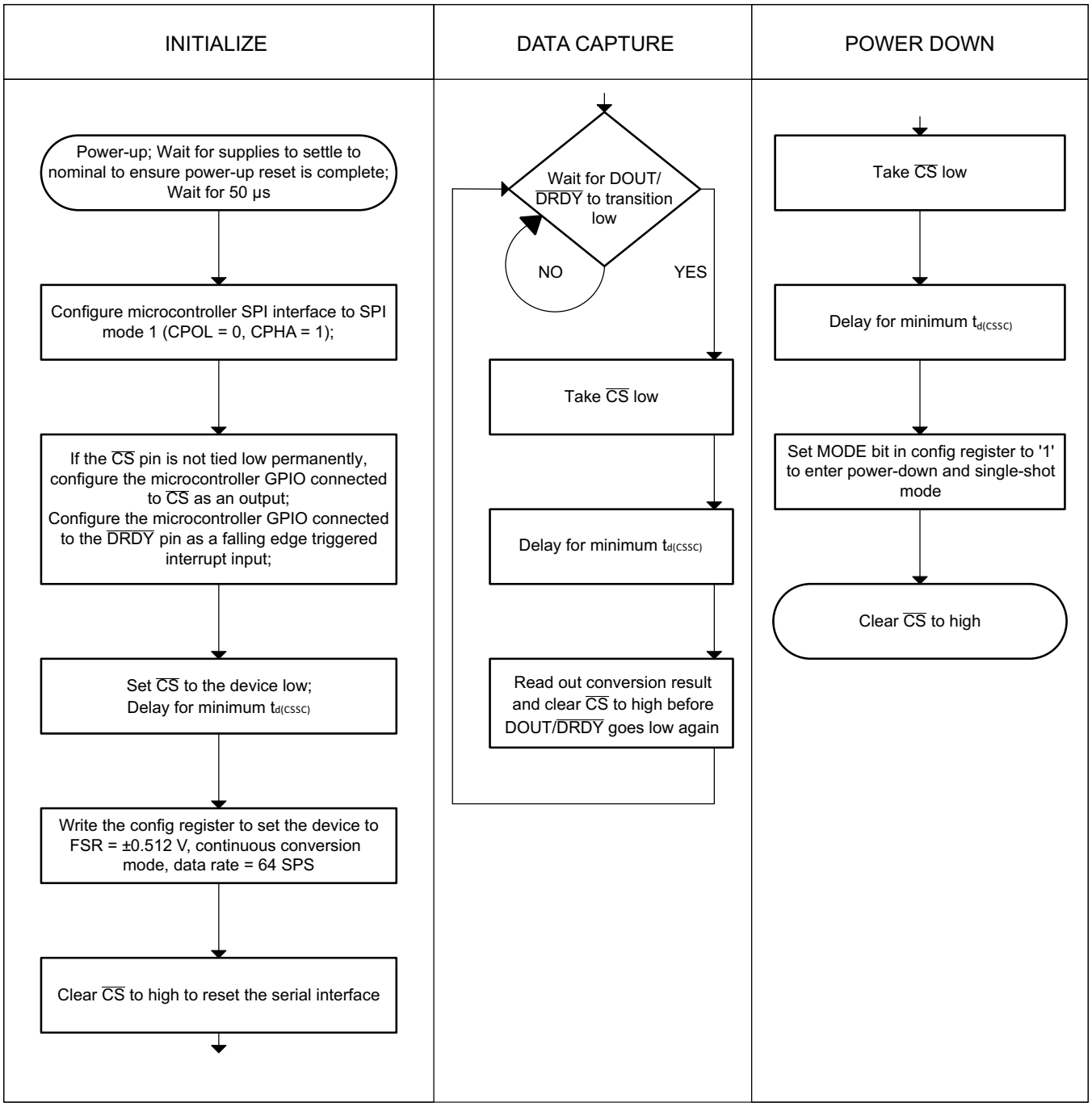


Figure 43. Pseudo-Code Example Flowchart

10.2 Typical Application

Figure 44 shows the basic connections for an independent, two-channel thermocouple measurement system when using the internal high-precision temperature sensor for cold-junction compensation. Apart from the thermocouples, the only external circuitry required are biasing resistors; first-order, low-pass, antialiasing filters; and a power-supply decoupling capacitor.

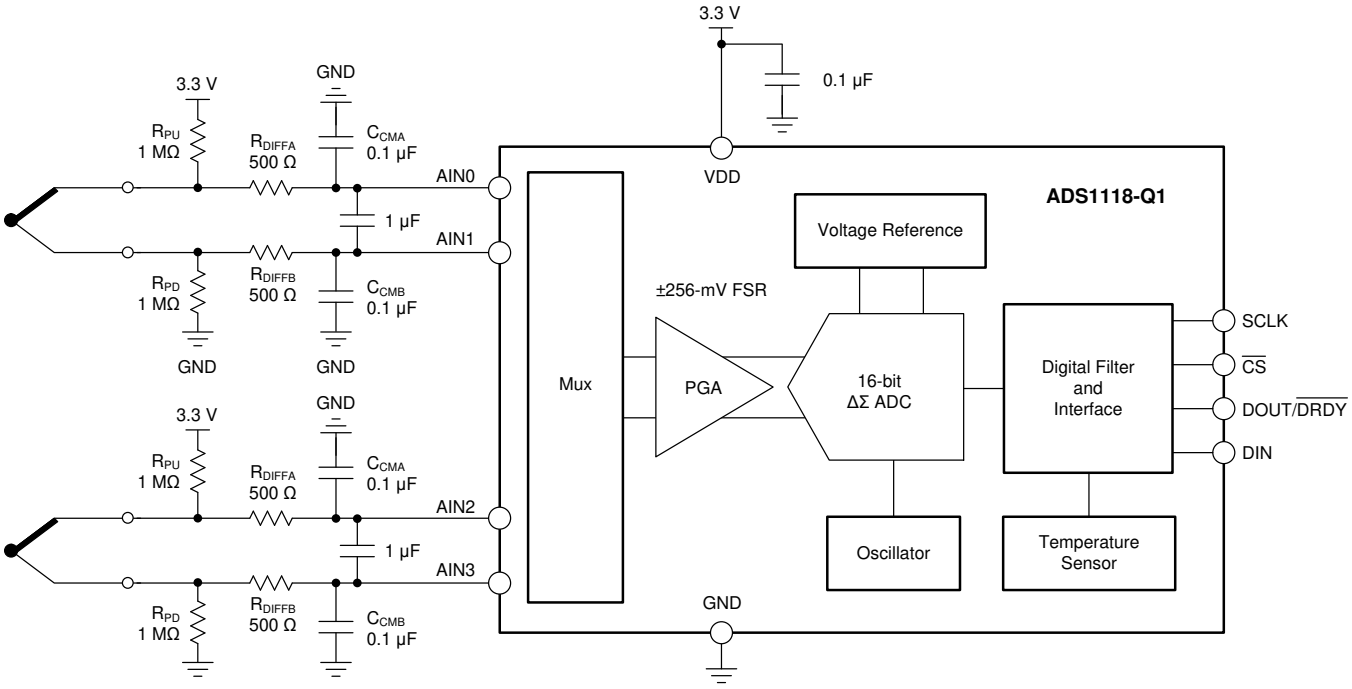


Figure 44. Two-Channel Thermocouple Measurement System

10.2.1 Design Requirements

Table 8 shows the design parameters for this application.

Table 8. Design Parameters

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V
Full-scale range	±0.256 V
Update rate	≥ 100 readings per second
Thermocouple type	K
Temperature measurement range	–200°C to +1250°C
Measurement accuracy at T_A = 25°C (1)	±1.2°C

(1) With offset calibration, and no gain calibration. Measurement does not account for thermocouple inaccuracy.

10.2.2 Detailed Design Procedure

The biasing resistors (R_{PU} and R_{PD}) serve two purposes. The first purpose is to set the common-mode voltage of the thermocouple to within the specified voltage range of the device. The second purpose is to offer a weak pullup and pulldown to detect an open thermocouple lead. When one of the thermocouple leads fails open, the positive input is pulled to VDD and the negative input is pulled to GND. The ADC consequently reads a full-scale value that is outside the normal measurement range of the thermocouple voltage to indicate this failure condition. When choosing the values of the biasing resistors, take care so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

Although the device digital filter attenuates high-frequency components of noise, provide a first-order, passive RC filter at the inputs to further improve performance. The differential RC filter formed by R_{DIFFA}, R_{DIFFB}, and the differential capacitor C_{DIFF} offers a cutoff frequency that is calculated using Equation 5. While the digital filter of the ADS1118-Q1 strongly attenuates high-frequency components of noise, provide a first-order, passive RC filter to further suppress high-frequency noise and avoid aliasing. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. Limit the filter resistor values to below 1 kΩ for best performance.

$$f_C = 1 / [2\pi \cdot (R_{DIFFA} + R_{DIFFB}) \cdot C_{DIFF}] \quad (5)$$

Two common-mode filter capacitors (C_{CMA} and C_{CMB}) are also added to offer attenuation of high-frequency, common-mode noise components. Differential capacitor C_{DIFF} must be at least an order of magnitude (10x) larger than these common-mode capacitors because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The highest measurement resolution is achieved when the largest potential input signal is slightly lower than the FSR of the ADC. From the design requirement, the maximum thermocouple voltage (V_{TC}) occurs at a thermocouple temperature (T_{TC}) of 1250°C. At this temperature, V_{TC} = 50.644 mV, as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature (T_{CJ}) of 0°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –40°C. A K-type thermocouple at T_{TC} = 1250°C produces an output voltage of V_{TC} = 50.644 mV – (–1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of T_{CJ} = –40°C. The device offers a full-scale range of ±0.256 V and that is what is used in this application example.

The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. The temperature sensor mode is enabled by setting bit TS_MODE = 1 in the Config register. The accuracy of the overall temperature sensor depends on how accurately the ADS1118-Q1 can measure the cold junction, and hence, careful component placement and PCB layout considerations must be employed for designing an accurate thermocouple system. The ADS1118 Evaluation Module provides a good starting point and offers an example to achieve good cold-junction compensation performance. The ADS1118 evaluation module uses the same schematic as shown in Figure 44, except with only one thermocouple channel connected. Refer to the *Precision Thermocouple Measurement With the ADS1118* application note for details on how to optimize your component placement and layout to achieve good cold-junction compensation performance.

The calculation procedure to achieve cold-junction compensation can be done in several ways. A typical way is to interleave readings between the thermocouple inputs and the temperature sensor. That is, acquire one on-chip temperature result, T_{CJ}, for every thermocouple ADC voltage measured, V_{TC}. To account for the cold junction, first convert the temperature sensor reading within the ADS1118-Q1 to a voltage (V_{CJ}) that is proportional to the thermocouple currently being used. This process is generally accomplished by performing a reverse lookup on the table used for the thermocouple voltage-to-temperature conversion. Adding these two voltages yields the thermocouple-compensated voltage (V_{Actual}), where $V_{Actual} = V_{CJ} + V_{TC}$. V_{Actual} is then converted to a temperature (T_{Actual}) using the same NIST lookup table. A block diagram showing this process is given in Figure 45. Refer to the *Precision Thermocouple Measurement With the ADS1118* application note for a detailed explanation of this method.

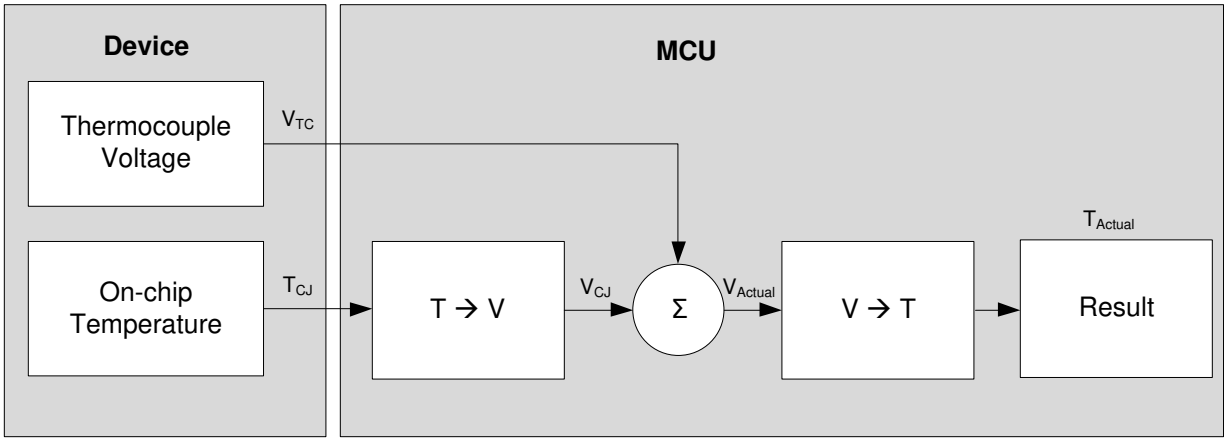


Figure 45. Software-Flow Block Diagram

Figure 46 and Figure 47 show the measurement results. The measurements are taken at $T_A = T_{CJ} = 25°C$. A system offset calibration is performed at $T_{TC} = 25°C$ that equates to $V_{TC} = 0$ V when $T_{CJ} = 25°C$. No gain calibration was performed during the measurements. The data in Figure 46 are taken using a precision voltage source as the input signal instead of a thermocouple. The solid black line in Figure 47 is the respective temperature measurement error and is calculated from the data in Figure 46 using the NIST tables. The solid black line in Figure 47 is the measurement error due to the ADC gain and nonlinearity error. The dashed blue lines in Figure 47 include the guard band for the temperature sensor inaccuracy (±1°C), in addition to the device gain and nonlinearity error. Note that the measurement results in Figure 46 and Figure 47 do not account for the thermocouple inaccuracy that must also be considered while designing a thermocouple measurement system.

10.2.3 Application Curves

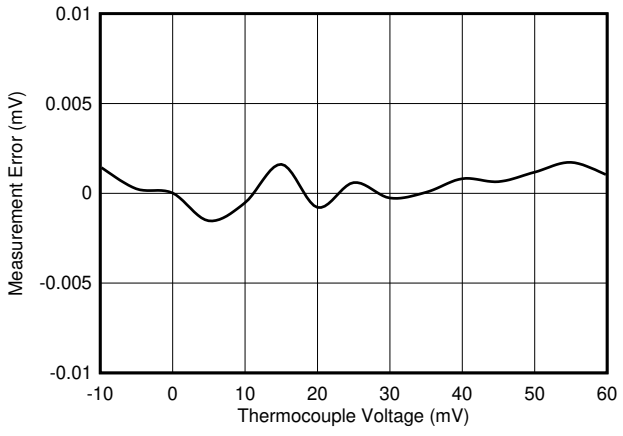


Figure 46. Voltage Measurement Error vs V_{TC}

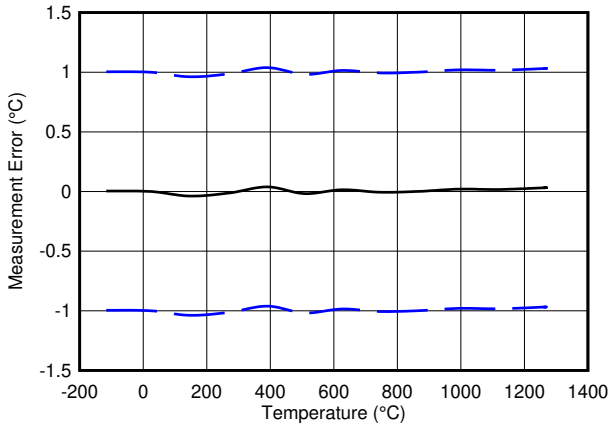


Figure 47. Temperature Measurement Error vs T_{TC}

11 Power Supply Recommendations

The device requires a single power supply, VDD, to power both the analog and digital circuitry of the device.

11.1 Power-Supply Sequencing

Wait approximately 50 µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

11.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. VDD must be decoupled with at least a 0.1-µF capacitor, as shown in Figure 48. The 0.1-µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the ADS1118-Q1 is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. For best performance, use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

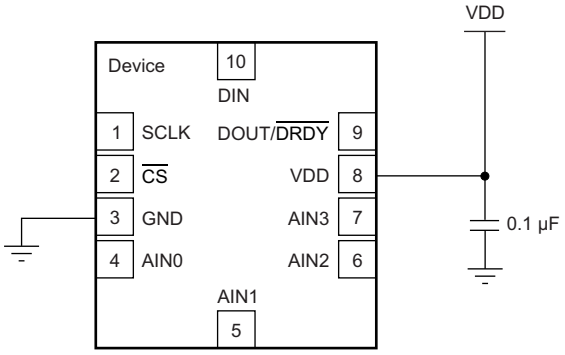


Figure 48. Power-Supply Decoupling

12 Layout

12.1 Layout Guidelines

Use best design practices when laying out a printed-circuit-board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog muxes] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 49. Although Figure 49 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

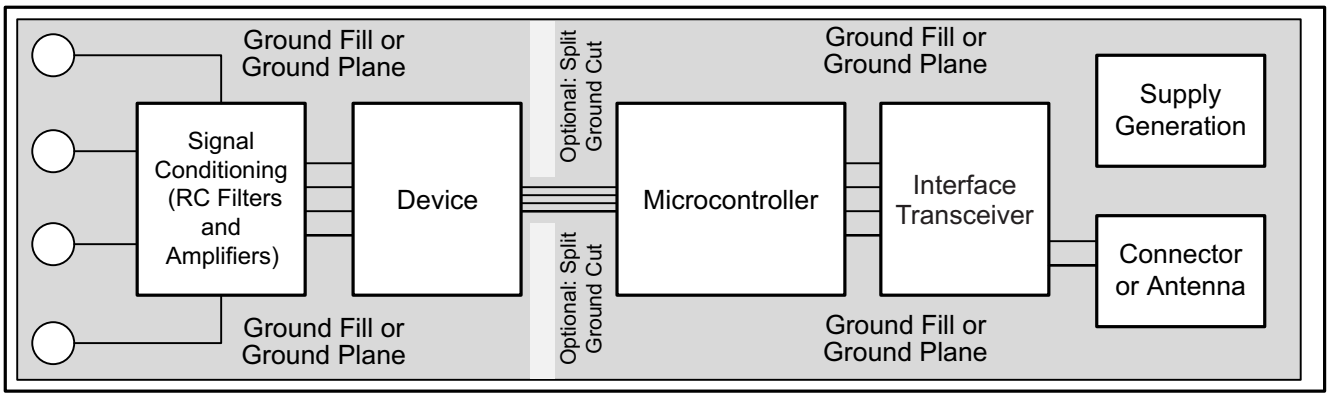


Figure 49. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the device as possible. A two-layer board is possible using common grounds for both analog and digital grounds. Additional layers can be added to simplify PCB trace routing. Ground fill may also reduce EMI and RFI issues.

For best system performance, keep digital components, especially RF portions, as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

Bypass supply pins to ground with a low-ESR ceramic capacitor. The optimum placement of the bypass capacitors is as close as possible to the supply pins. The ground-side connections of the bypass capacitors must be low-impedance connections for optimum performance. The supply current flows through the bypass capacitor terminal first and then to the supply pin to make the bypassing most effective.

Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Use high-quality differential capacitors. The best ceramic-chip capacitors are C0G (NPO), with stable properties and low-noise characteristics. Thermally isolate a copper region around the thermocouple input connections to create a thermally-stable cold junction. Obtaining acceptable performance with alternate layout schemes is possible as long as the above guidelines are followed.

12.2 Layout Example

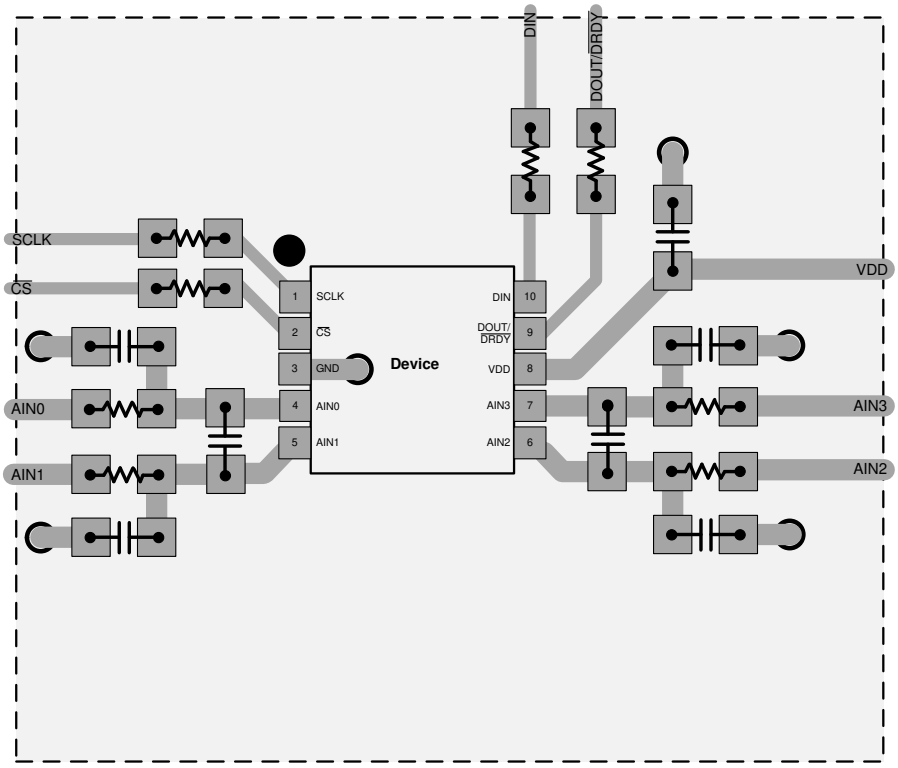


Figure 50. VSSOP Package

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Precision Thermocouple Measurement with the ADS1118* application report
- Texas Instruments, *ADS1118EVM User Guide and Software Tutorial* user guide
- Texas Instruments, *430BOOST-ADS1118 BoosterPack* user's guide
- Texas Instruments, *ADS1118 Boosterpack* quick start
- Texas Instruments, *A Glossary of Analog-to-Digital Specifications and Performance Characteristics* application report

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1118QDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZFPV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADS1118-Q1 :

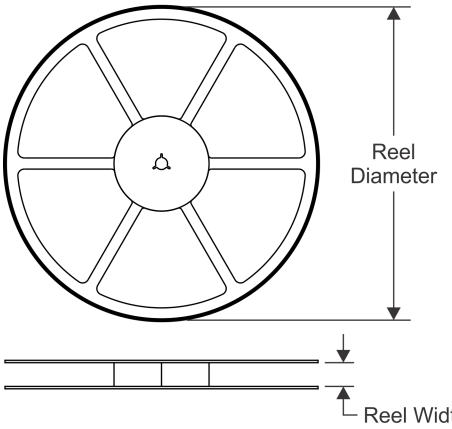
- Catalog: ADS1118

NOTE: Qualified Version Definitions:

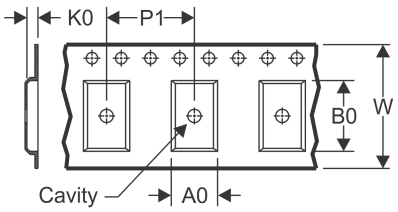
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

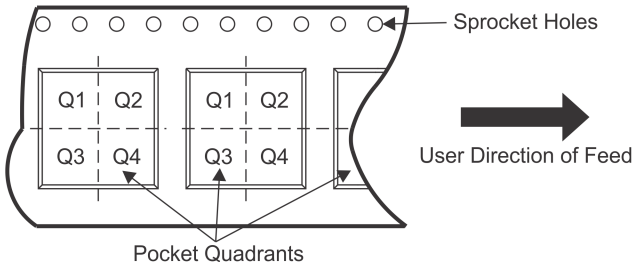


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



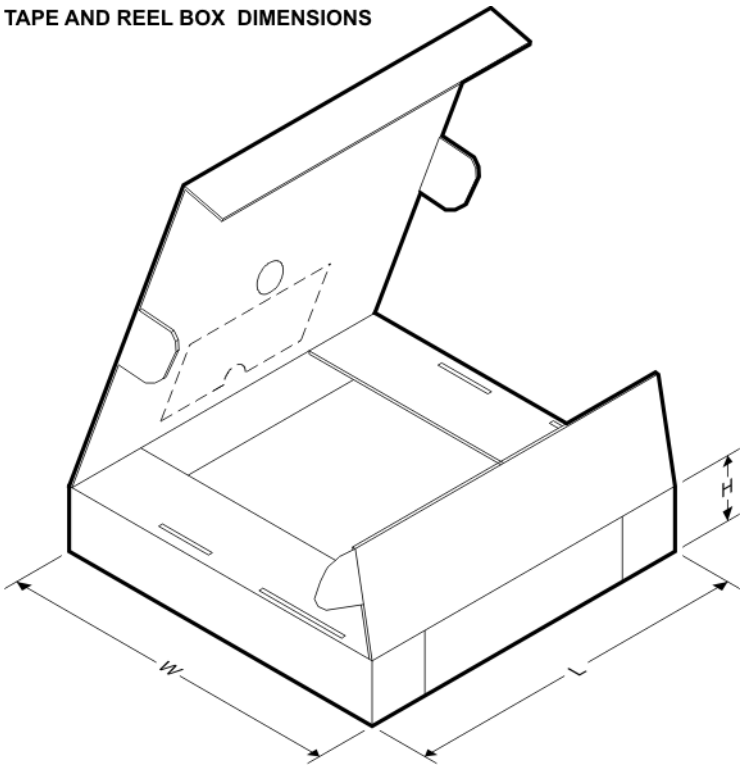
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1118QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

17-Jul-2020

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

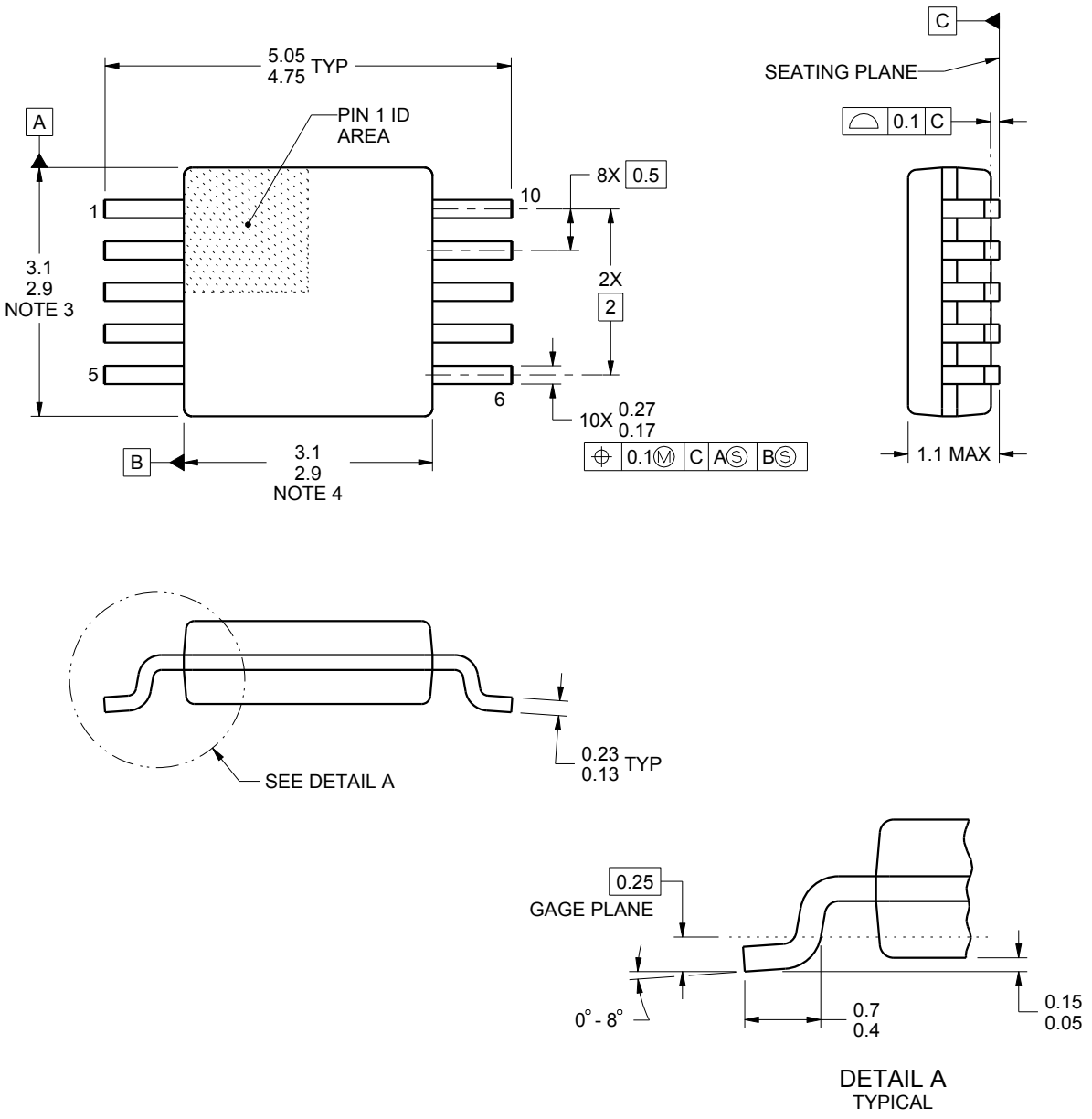
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1118QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

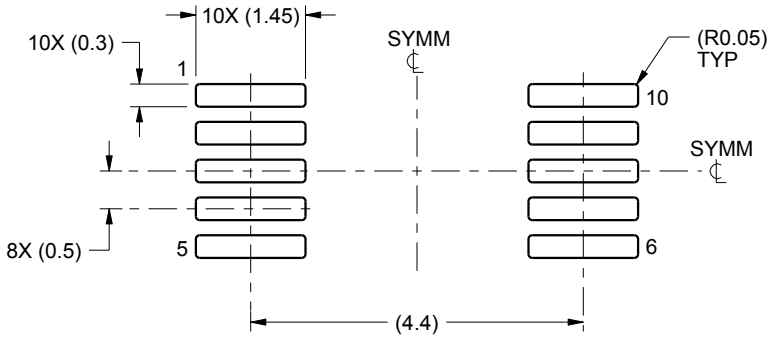
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

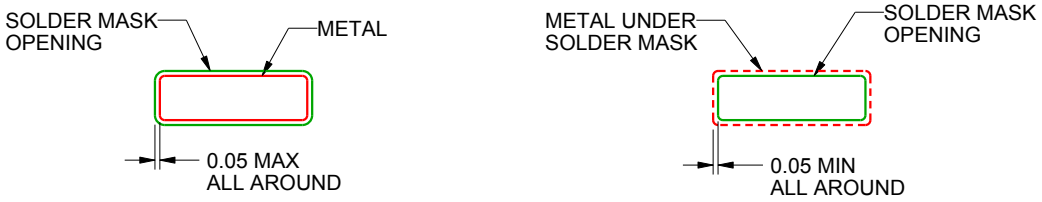
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

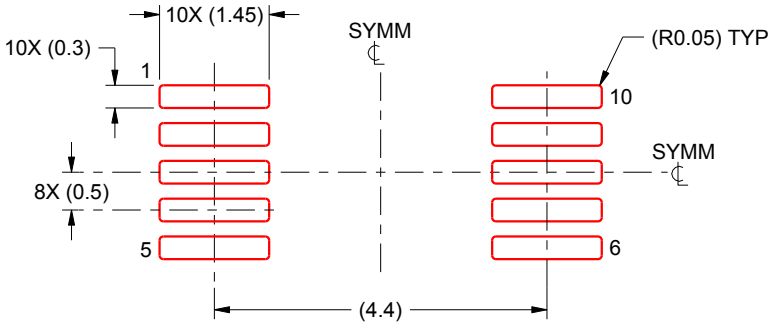
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.