SGM70276xQ
Automotive Camera PMIC with 4-Channel Output

GENERAL DESCRIPTION

The SGM70276xQ is a highly-integrated ultra-compact power management device. It incorporates three Buck converters and a high PSRR low-dropout (LDO) regulator. Every Buck converter operates in a forced fixed-frequency PWM mode. The high-voltage Buck converter operates in an input voltage range from 4V to 18.5V. And the two low-voltage Buck converters operate in an input voltage range from 2.7V to 5V.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM70276xQ is available in a Green TQFN-3×3-16GL package.

APPLICATIONS

Automotive Camera Modules
Front View Camera Modules (FVC)
Rear View Camera Modules (RVC)
Surround View Camera Modules (SVC)
Driver Monitor Camera Modules (DMS)
Occupant Monitoring System (OMS)
Camera Monitor System (CMS)
Power over Coax (POC) Camera Modules

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **HVBuck1**
  - **Input Voltage Range: 4V to 18.5V**
  - **2.7V to 5V Output Voltage Range**
  - **Output Current up to 1.5A**
- **LVBuck2**
  - **Input Voltage Range: 2.7V to 5V**
  - **Fixed Output Voltage Versions: 0.75V to 1.5V with 50mV/Step**
  - **Output Current up to 2A**
- **LVBuck3**
  - **Input Voltage Range: 2.7V to 5V**
  - **Fixed Output Voltage Versions: 1.7V to 1.9V with 100mV/Step**
  - **Output Current up to 750mA**
- **Low Dropout Regulator (LDO)**
  - **Input Voltage Range: 2.7V to 5V**
  - **Output Current up to 300mA**
  - **10 Flexible Output Voltage Settings via External Resistor**
  - **High PSRR:**
    72dB at 1kHz
    60dB at 100kHz
    39dB at 1MHz
- **Three Buck Converters:**
  - **Peak Current Mode PWM Operation**
  - **Fixed 2.1MHz Switching Frequency**
  - **Integrated Phase Shift and Frequency Dithering for EMI Suppression**
  - **Pins Related to LVBuck2/LVBuck3 Allowable Floating if Channel Unused**
- **10 Configurable Power Sequences via SEQ Pin**
- **SEQOUT for External Power IC Sequence Control (SGM70276AxQ)**
- **PG for Power Status Indication (SGM70276BxQ)**
- **Available in a Green TQFN-3×3-16GL Package**

代理商 威尔迈 www.vlswie.com 联系电话 138 2526 5270

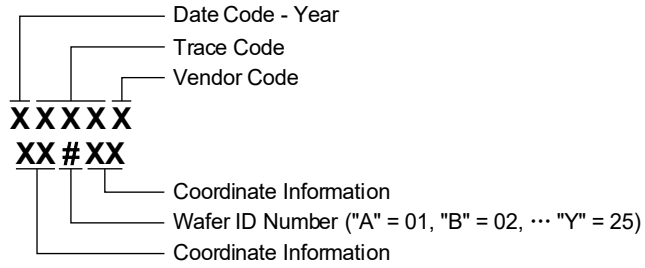
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM70276A-CBQ	TQFN-3×3-16GL	-40℃ to +125℃	SGM70276A-CBQTVH16G/TR	25VVH XXXXX XX#XX	Tape and Reel, 4000
SGM70276B-CBQ	TQFN-3×3-16GL	-40℃ to +125℃	SGM70276B-CBQTVH16G/TR	25WVH XXXXX XX#XX	Tape and Reel, 4000
SGM70276A-HBQ	TQFN-3×3-16GL	-40℃ to +125℃	SGM70276A-HBQTVH16G/TR	20JVH XXXXX XX#XX	Tape and Reel, 4000
SGM70276B-HBQ	TQFN-3×3-16GL	-40℃ to +125℃	SGM70276B-HBQTVH16G/TR	20KVH XXXXX XX#XX	Tape and Reel, 4000
SGM70276A-JBQ	TQFN-3×3-16GL	-40℃ to +125℃	SGM70276A-JBQTVH16G/TR	25XVH XXXXX XX#XX	Tape and Reel, 4000
SGM70276B-JBQ	TQFN-3×3-16GL	-40℃ to +125℃	SGM70276B-JBQTVH16G/TR	25YVH XXXXX XX#XX	Tape and Reel, 4000

NOTE: For more models not listed above, please contact your local SGMICRO sales representatives.

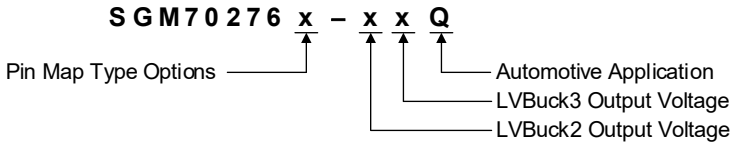
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

DEVICE NAMING DESCRIPTION



Pin Map Type Options															
A								B							
SEQOUT Pin Type								PG Pin Type							
LVBuck2 Output Voltage (V)															
A	B	C	D	E	F	G	H	N	J	K	L	M	P	R	S
0.75	0.8	0.85	0.9	0.95	1	1.05	1.1	1.15	1.2	1.25	1.3	1.35	1.4	1.45	1.5
LVBuck3 Output Voltage (V)															
A	B	C													
1.7	1.8	1.9													

ABSOLUTE MAXIMUM RATINGS

VIN to GND ..... -0.3V to 24V
SW1 to GND ..... -0.3V to 24V
BOOT to GND ..... -0.3V to SW + 5V
BOOT to SW1 ..... -0.3V to 5V
VOUT2, PVD23, VOUT3, SEQ, RSET, LDOOUT, LDOIN, FB1, PVCC, SEQOUT (SGM70276AxQ), PG (SGM70276BxQ) to GND ..... -0.3V to 6.5V
SW2, SW3 to GND ..... -0.3V to 6.5V
Package Thermal Resistance
TQFN-3×3-16GL, θ_{JA} ..... 39.1℃/W
TQFN-3×3-16GL, θ_{JB} ..... 13℃/W
TQFN-3×3-16GL, $\theta_{JC\ (TOP)}$ ..... 39.2℃/W
TQFN-3×3-16GL, $\theta_{JC\ (BOT)}$ ..... 5.2℃/W
Lead Temperature (Soldering, 10 sec.) ..... +260℃
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 4V to 18.5V
Supply Voltage, V_{PVD23}, V_{LDOIN} ..... 2.7V to 5V
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

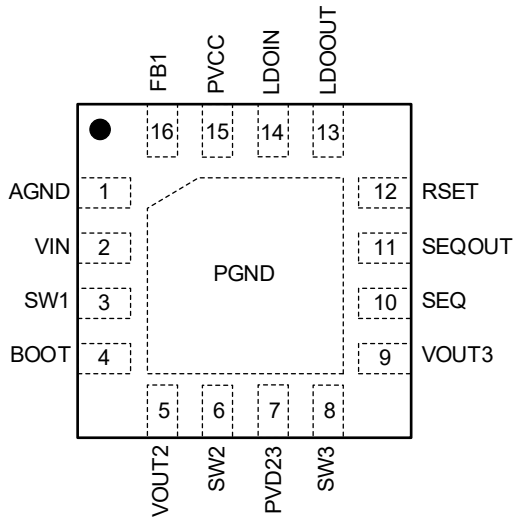
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

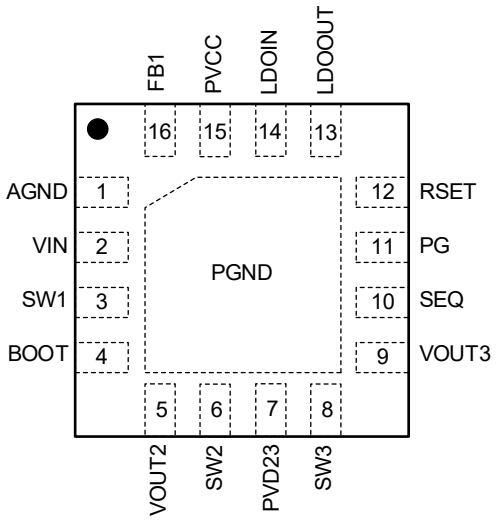
PIN CONFIGURATIONS

SGM70276AxQ (TOP VIEW)



TQFN-3×3-16GL

SGM70276BxQ (TOP VIEW)



TQFN-3×3-16GL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	AGND	P	Analog Ground.
2	VIN	P	HVBuck1 Supply Input. Place a 4.7μF ceramic capacitor from VIN pin to GND close to the device.
3	SW1	P	HVBuck1 Switch Node.
4	BOOT	P	BOOTCAP Pin for HVBuck1. Connect a 0.1μF bootstrap capacitor from this pin to SW1.
5	VOUT2	AI	LVBuck2 Output Voltage Feedback Input.
6	SW2	P	LVBuck2 Switch Node.
7	PVD23	P	LVBuck2 and LVBuck3 Input Voltage. Place a 4.7μF ceramic capacitor from PVD23 pin to GND as close as possible.
8	SW3	P	LVBuck3 Switch Node.
9	VOUT3	AI	LVBuck3 Output Voltage Feedback Input.
10	SEQ	AIO	Power-On Sequence Selection.
11	SEQOUT	AO	Sequence Control Output Pin (SGM70276AxQ). SEQOUT output is open-drain.
	PG	AO	Power Good Indication Pin for All Channels (SGM70276BxQ). PG output is open-drain.
12	RSET	AIO	Output Voltage Selection for LDO.
13	LDOOUT	P	LDO Output. Place a 2.2μF ceramic capacitor as close as possible for a better LDO performance. (2)
14	LDOIN	P	LDO Input Voltage. Place a 2.2μF ceramic capacitor from LDOIN pin to GND as close as possible.
15	PVCC	P	Internal Reference Voltage. Place a 1μF ceramic capacitor from PVCC pin to GND.
16	FB1	AI	HVBuck1 Feedback.
Exposed Pad	PGND	P	Device Thermal Pad and PGND Connection. Must be connected to main ground plane for proper operation.

NOTES:

1. P = power, AIO = analog input/output, AI = analog input, AO = analog output.

2. A larger capacitor will make impact on the soft-start time of LDO. It should be calculated cautiously.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, typical values are measured at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System						
Under-Voltage Lockout Threshold	V_{UVLO_H}	V_{IN} rising	3.6	3.8	4.1	V
	V_{UVLO_L}	V_{IN} falling	3.1	3.3	3.5	V
Input Over-Voltage Protection	V_{IN_OVP}		18.6	20	21.5	V
CH1 HVBuck1						
Input Voltage Range	V_{IN}		4		18.5	V
Output Voltage Range	V_{OUT_HV1}	Buck mode operation. Switching frequency, minimum on-time and minimum off-time need to be considered.	2.7		5	V
Output Feedback Voltage Accuracy	V_{FB1}		0.784	0.8	0.816	V
Switching Frequency	f_{SW_HV1}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{_HV1}$			6		%
Switching Minimum On-Time	$t_{ON_MIN_HV1}$				85	ns
Switching Minimum Off-Time	$t_{OFF_MIN_HV1}$				70	ns
High-side MOSFET On-Resistance	$R_{ON_HS_HV1}$	From VIN pin to SW1 pin (including estimating bond wire resistance)	90	190	325	mΩ
Low-side MOSFET On-Resistance	$R_{ON_LS_HV1}$	From SW1 pin to PGND pin (including estimating bond wire resistance)	80	160	235	mΩ
Inductor Peak Current-Limit	$I_{CL_PK_HV1}$		2.3	2.8	3.3	A
Inductor Valley Current-Limit	$I_{CL_VL_HV1}$			2		A
Negative Inductor Peak Current-Limit	$I_{CL_NPK_HV1}$		1	1.5	2	A
Output Discharge Resistor	R_{DIS_HV1}		130	220	310	Ω
Output Under-Voltage Falling Threshold	$UVP_{_F_HV1}$		40	50	60	%
Output Feedback Over-Voltage	$OVP_{_R_HV1}$	Rising threshold		112		%
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7		5	V
Output Voltage Range	V_{OUT_LV2}		0.75		1.5	V
Output Voltage Accuracy	$V_{OUT_ACC_LV2}$		-2		2	%
Switching Frequency	f_{SW_LV2}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{_LV2}$			6		%
Switching Minimum on-Time	$t_{ON_MIN_LV2}$				85	ns
High-side MOSFET On-Resistance	$R_{ON_HS_LV2}$	From PVD23 pin to SW2 pin (including estimated bondwires)	98	170	240	mΩ
Low-side MOSFET On-Resistance	$R_{ON_LS_LV2}$	From SW2 pin to PGND pin (including estimated bondwires)	45	74	102	mΩ
Inductor Peak Current-Limit	$I_{CL_PK_LV2}$		2.5	3.2	3.66	A
Inductor Valley Current-Limit	$I_{CL_VL_LV2}$			2.85		A
Negative Inductor Peak Current-Limit	$I_{CL_NPK_LV2}$		1	1.9	2.8	A
Output Discharge Resistor	R_{DIS_LV2}		4	7	11.5	Ω
Output Under-Voltage	$UVP_{_F_LV2}$	Falling threshold	40	50	60	%
Output Over-Voltage	$OVP_{_R_LV2}$	Rising threshold		120		%
	$OVP_{_F_LV2}$	Falling threshold		111		
Input Over-Voltage	$OVP_{_IN_R_LV2}$	Rising threshold	5.35	5.8	6.25	V
Input Over-Voltage Hysteresis	$OVP_{_IN_HYS_LV2}$	V_{IN_PVD23} falling		420		mV

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, typical values are measured at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7		5	V
Output Voltage Range	V_{OUT_LV3}		1.7		1.9	V
Output Voltage Accuracy	$V_{OUT_ACC_LV3}$		-2		2	%
Switching Frequency	f_{SW_LV3}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{_LV3}$			6		%
Switching Minimum On-Time	$t_{ON_MIN_LV3}$				85	ns
High-side MOSFET On-Resistance	$R_{ON_HS_LV3}$	From PVD23 pin to SW3 pin (including estimated bondwires)	175	320	468	mΩ
Low-side MOSFET On-Resistance	$R_{ON_LS_LV3}$	From SW3 pin to PGND pin (including estimated bondwires)	74	136	196	mΩ
Inductor Peak Current-Limit	$I_{CL_PK_LV3}$		1.1	1.6	2.2	A
Inductor Valley Current-Limit	$I_{CL_VL_LV3}$			1.3		A
Negative Inductor Peak Current-Limit	$I_{CL_NPK_LV3}$		0.9	1.45	2	A
Output Discharge Resistor	R_{DIS_LV3}		4	6.5	11	Ω
Output Under-Voltage	$UVP_{_F_LV3}$	Falling threshold	40	50	60	%
Output Over-Voltage	$OVP_{_R_LV3}$	Rising threshold		120		%
	$OVP_{_F_LV3}$	Falling threshold		111		
Input Over-Voltage	$OVP_{_IN_R_LV3}$	Rising threshold	5.35	5.8	6.25	V
Input Over-Voltage Hysteresis	$OVP_{_IN_HYS_LV3}$	V_{IN_PVD23} falling		420		mV
CH4 LDO (V_{IN_LDO} = 3.6V)						
Input Voltage Range	V_{IN_LDO}		2.7		5	V
Output Voltage Range	V_{OUT_LDO}	V_{OUT_LDO} setting via RSET	1.8		3.5	V
Output Voltage Accuracy	$V_{OUT_ACC_LDO}$	V_{IN_LDO} - V_{OUT_LDO} > 0.3V, I_{OUT_LDO} = 0mA to 300mA	-2		2	%
Maximum Output Current	$I_{OUT_MAX_LDO}$		300			mA
Dropout Voltage	$V_{DROP_300_LDO}$	I_{OUT_LDO} = 300mA (1)			200	mV
	$V_{DROP_150_LDO}$	I_{OUT_LDO} = 150mA (1)			100	
Output Current-Limit	I_{CL_LDO}		320	480	640	mA
Output Discharge Resistor	R_{DIS_LDO}		54	77	110	Ω
Output Under-Voltage	$UVP_{_F_LDO}$	Falling threshold	30	40	50	%
Output Over-Voltage	$OVP_{_R_LDO}$	Rising threshold		124		%
	$OVP_{_F_LDO}$	Falling threshold		109		
Input Over-Voltage	$OVP_{_IN_R_LDO}$	Rising threshold	5.35	5.8	6.25	V
Input Over-Voltage Hysteresis	$OVP_{_IN_HYS_LDO}$	V_{IN_LDO} falling		412		mV

NOTE:

1. Dropout voltage refers to the voltage variance between the input and output where the output voltage falls 100mV beneath its standard level.

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, typical values are measured at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PVCC (1)						
Internal Regulator Output Voltage	V_{OUT_PVCC}		4.235	4.485	4.735	V
Over-Current-Limit	I_{CL_PVCC}		90		200	mA
SEQOUT (SGM70276AxQ)						
Output Low Voltage		Current into SEQOUT pin equal to 2mA			200	mV
Input Leakage Current	I_{LEAK_SEQOUT}	1.8V applied on SEQOUT pin			1	μA
Power Good (SGM70276BxQ)						
Pull-Down Voltage	$V_{OUT_L_PG}$	Current into PG pin equal to 2mA			200	mV
Input Leakage Current	I_{LEAK_PG}	1.8V applied on PG pin			1	μA
Timing						
Soft-Start Time	t_{SS_HV1}	Time from V_{OUT_HV1} 0% rise to 90% of target value, no load	500	1000	1500	μs
	t_{SS_LV2}	Time from V_{OUT_LV2} 0% rise to 90% of target value, no load	500	1000	1500	
	t_{SS_LV3}	Time from V_{OUT_LV3} 0% rise to 90% of target value, no load	500	1000	1500	
	t_{SS_LDO}	Time from the previous turn on channel's output voltage reaching 90% of target value to V_{OUT_LDO} rise to 90% of target value.	200	600	1100	
PG Delay Time	t_{DLY_PG}	SGM70276BxQ	9	12	15	ms

NOTE:

1. PVCC serves as the initial output voltage for the pre-regulator, exclusively for internal circuits. It's prohibited to load externally on the PVCC pin.

SYSTEM CHARACTERISTICS

(T_A = +25℃, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
System							
Over-Temperature Protection	OTP				160		℃
Over-Temperature Protection Hysteresis	OTP_H				20		℃
CH1 HVBuck1							
Maximum Output Current	$I_{OUT_MAX_HV1}$			1.5			A
Load Regulation	$V_{LOAD_REG_HV1}$	I_{OUT_HV1} = 0A to 2A			0.025		%/A
Line Regulation	$V_{LINE_REG_HV1}$	V_{IN} = 5V to 18.5V, I_{OUT_HV1} = 2A			0.05		%
Load Transient	$V_{LOAD_TRAIN_HV1}$	I_{OUT_HV1} = 10mA to 500mA to 10mA, 1μs		-70		70	mV
Line Transient	$V_{LINE_TRAIN_HV1}$	V_{IN} = 5V to 18.5V to 5V, 100μs, I_{OUT_HV1} = 10mA/500mA		-60		60	mV
Output Ripple	V_{RIPPLE_HV1}	Peak to peak in one switching cycle			7		mVpp
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)							
Maximum Output Current	$I_{OUT_MAX_LV2}$			2			A
Load Regulation	$V_{LOAD_REG_LV2}$	I_{OUT_LV2} = 0A to 1.5A			0.03		%/A
Line Regulation	$V_{LINE_REG_LV2}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV2} = 1.5A			0.027		%
Load Transient	$V_{LOAD_TRAIN_LV2}$	I_{OUT_LV2} = 10mA to 500mA to 10mA, 1μs		-50		50	mV
Line Transient	$V_{LINE_TRAIN_LV2}$	V_{IN_PVD23} = 3V to 5V to 3V, 100μs, I_{OUT_LV2} = 10mA/1A		-10		10	mV
Output Ripple	V_{RIPPLE_LV2}	Peak to peak in one switching cycle			4		mVpp
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)							
Maximum Output Current	$I_{OUT_MAX_LV3}$			750			mA
Load Regulation	$V_{LOAD_REG_LV3}$	I_{OUT_LV3} = 0A to 750mA			0.02		%/A
Line Regulation	$V_{LINE_REG_LV3}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV3} = 750mA			0.065		%
Load Transient	$V_{LOAD_TRAIN_LV3}$	I_{OUT_LV3} = 10mA to 300mA to 10mA, 1μs		-40		40	mV
Line Transient	$V_{LINE_TRAIN_LV3}$	V_{IN_PVD23} = 3V to 5V to 3V, 100μs, I_{OUT_LV3} = 10mA/300mA		-15		15	mV
Output Ripple	V_{RIPPLE_LV3}	Peak to peak in one switching cycle			6		mVpp
CH4 LDO (V_{IN_LDO} = 3.6V)							
Power Supply Rejection Ratio	$PSRR_{LDO}$	I_{OUT_LDO} = 100mA, V_{OUT} = 3.3V	f = 1kHz		72		dB
			f = 100kHz		60		
			f = 1MHz		39		
Output Noise Voltage	$NOISE_{LDO}$	I_{OUT_LDO} = 100mA, f = 100Hz to 100kHz			71		μV
Load Transient	$V_{LOAD_TRAIN_LDO}$	I_{OUT_LDO} = 10mA to 200mA to 10mA, 1μs		-10		10	mV
Line Transient	$V_{LINE_TRAIN_LDO}$	V_{IN_LDO} step 600mV, LDO not in dropout condition, 10μs, I_{OUT_LDO} = 1mA/300mA		-5		5	mV

SYSTEM CHARACTERISTICS (continued)

(T_A = +25℃, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Component Requirement (1)						
Effective Input Capacitance	C_{IN_HV1}		1.5	4.7	10	μF
	C_{IN_PVD23}		1.5	4.7	10	
	C_{IN_LDO}		0.7	2.2	4	
Effective Output Capacitance	C_{OUT_HV1}		3.3	10	14	μF
	C_{OUT_LV2}		4.5	10	14	
	C_{OUT_LV3}		4.5	10	14	
	C_{OUT_LDO}		0.7	2.2	4	
Output Inductance	L_{HV1}		1	1.5	2	μH
	L_{LV2}		0.68	1	1.2	
	L_{LV3}		0.68	1	1.2	
Effective Boot Capacitance	C_{BOOT}		0.07	0.1	0.13	μF
Effective PVCC Capacitance	C_{PVCC}		0.3	1	1.4	μF

NOTE:

1. The device is not guaranteed to function outside its operating conditions.

TYPICAL APPLICATION CIRCUITS

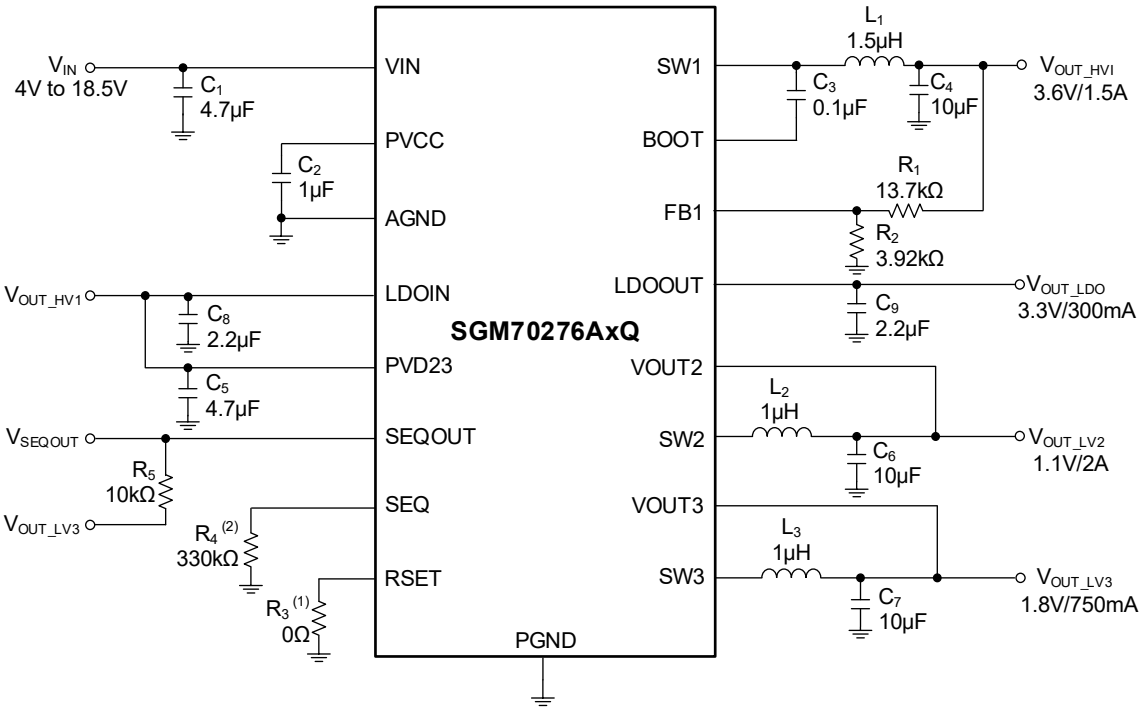


Figure 1. SGM70276AxQ Typical Application Circuit

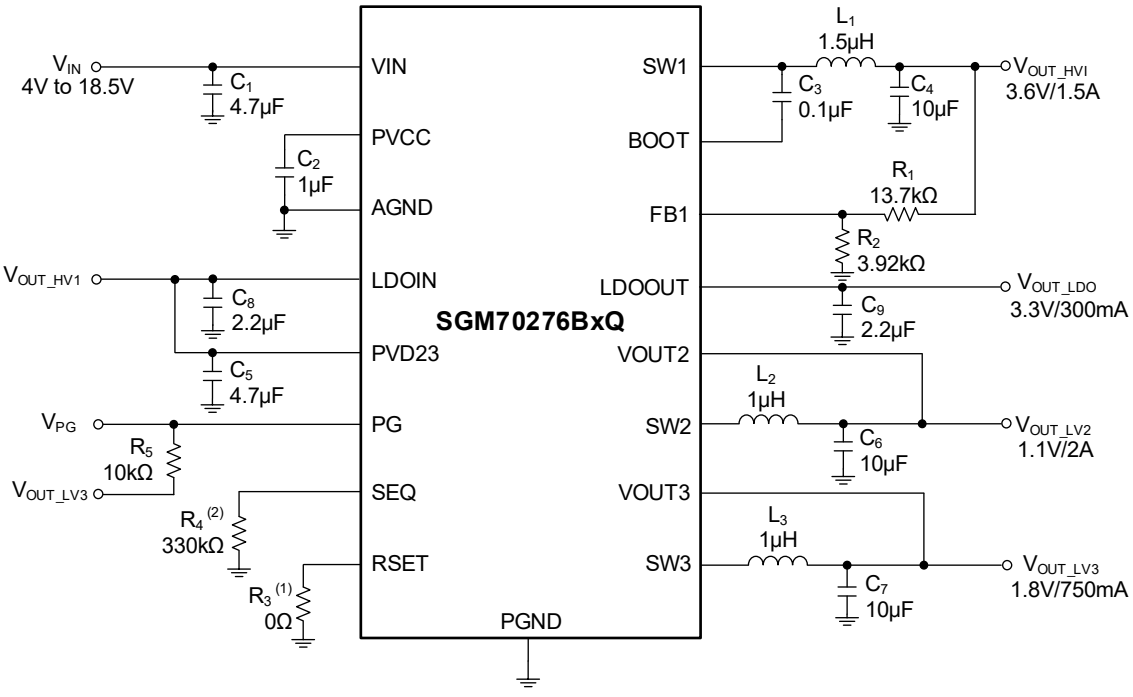


Figure 2. SGM70276BxQ Typical Application Circuit

NOTES:
1. The resistor is adjustable for different LDO output voltages.
2. The resistor is adjustable for different power-on sequences.

FUNCTIONAL BLOCK DIAGRAMS

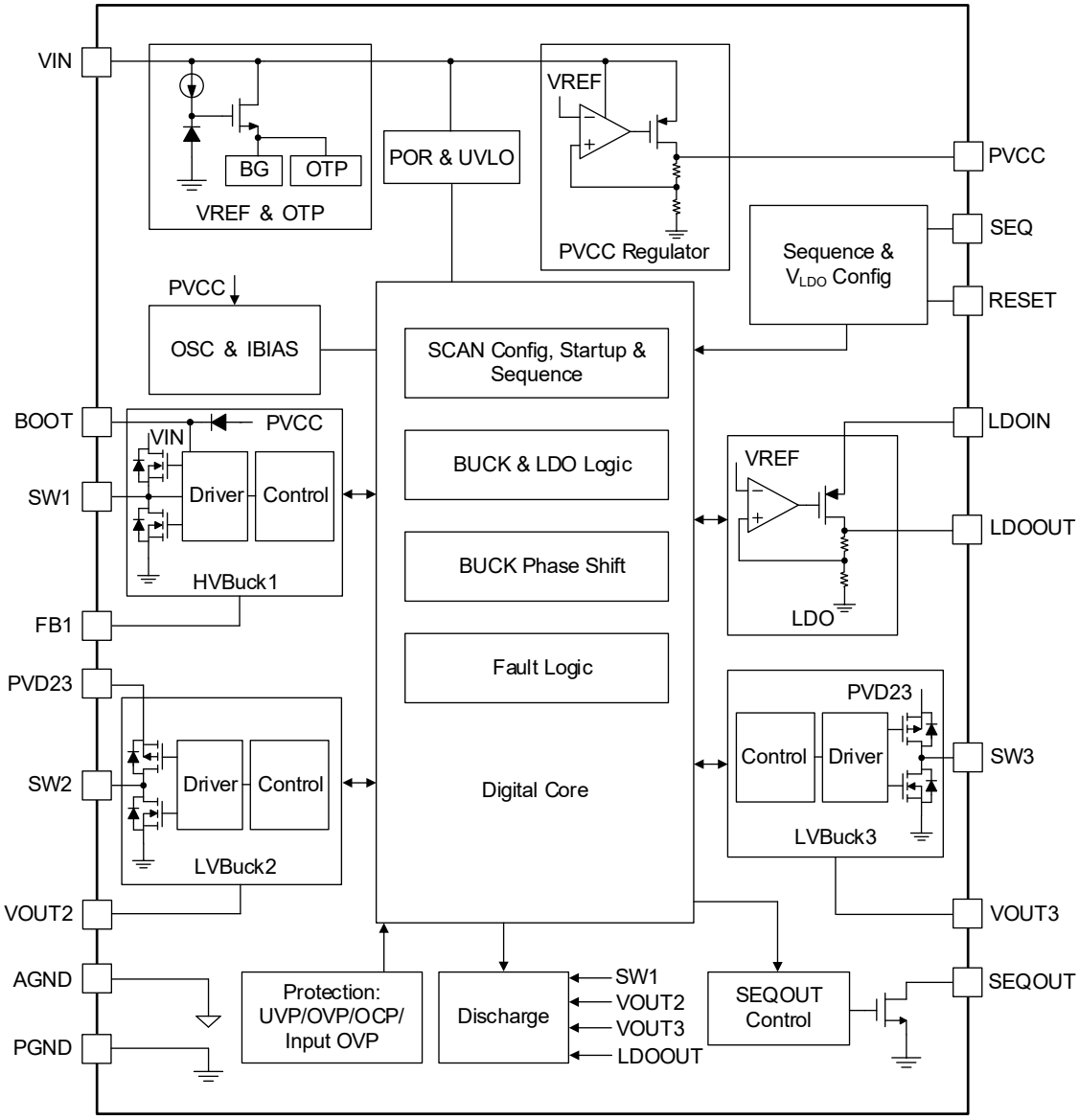


Figure 3. Block Diagram for SGM70276AxQ

FUNCTIONAL BLOCK DIAGRAMS (continued)

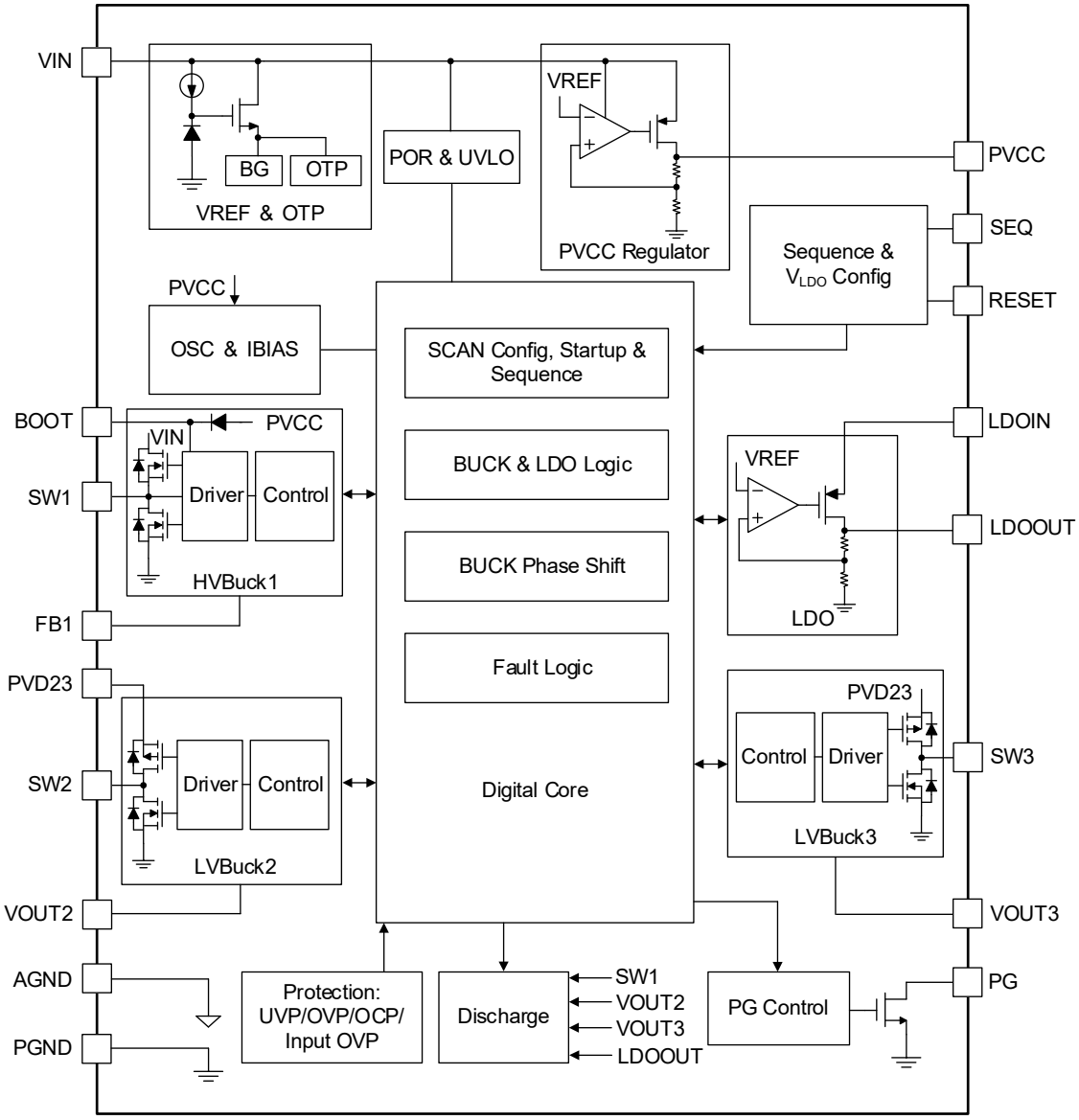
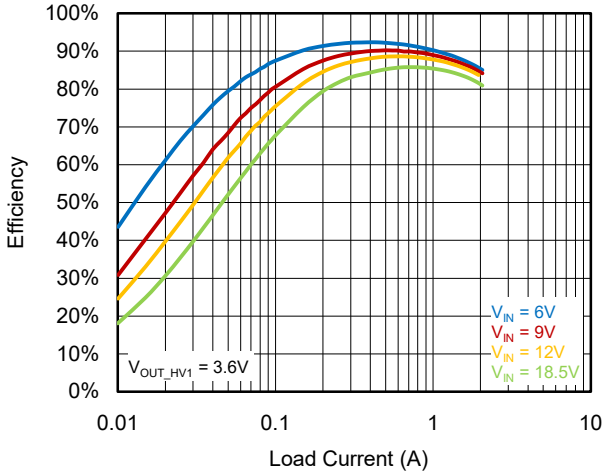


Figure 4. Block Diagram for SGM70276BxQ

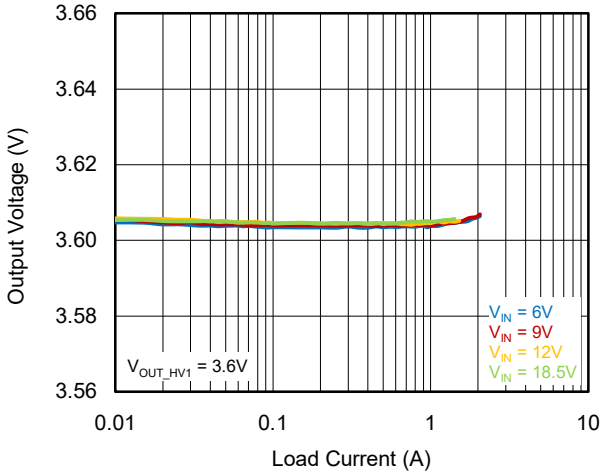
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise specified.

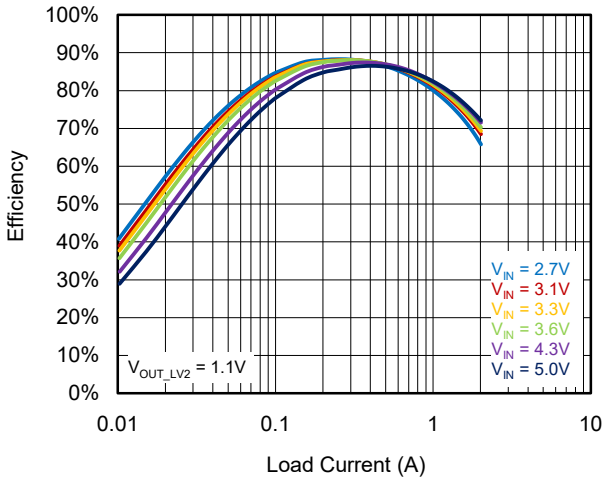
HVBuck1 Efficiency



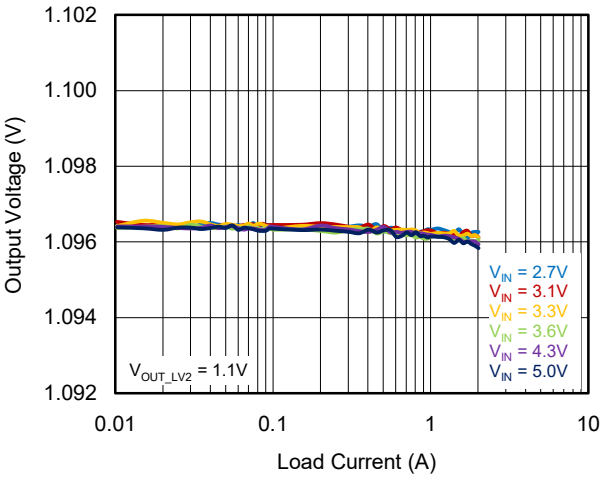
HVBuck1 Load Regulation



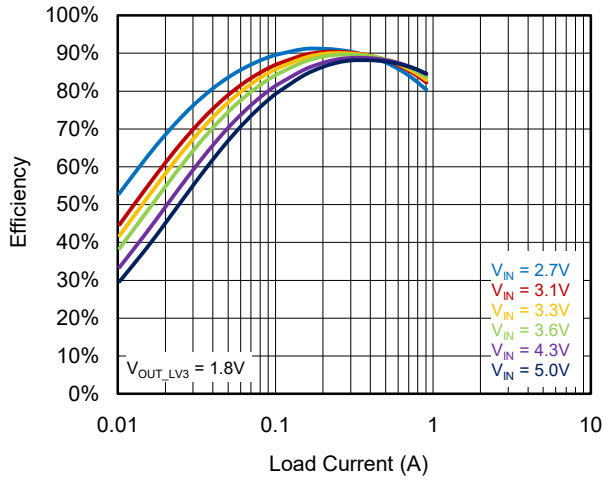
LVBuck2 Efficiency



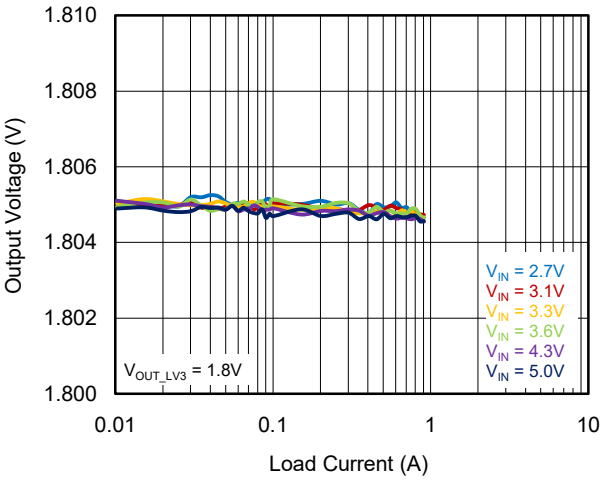
LVBuck2 Load Regulation



LVBuck3 Efficiency



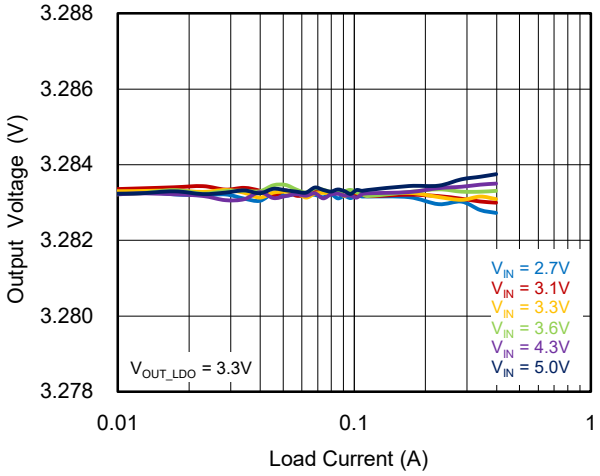
LVBuck3 Load Regulation



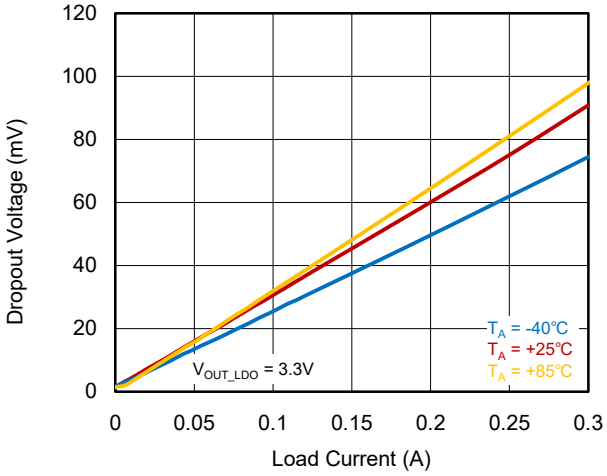
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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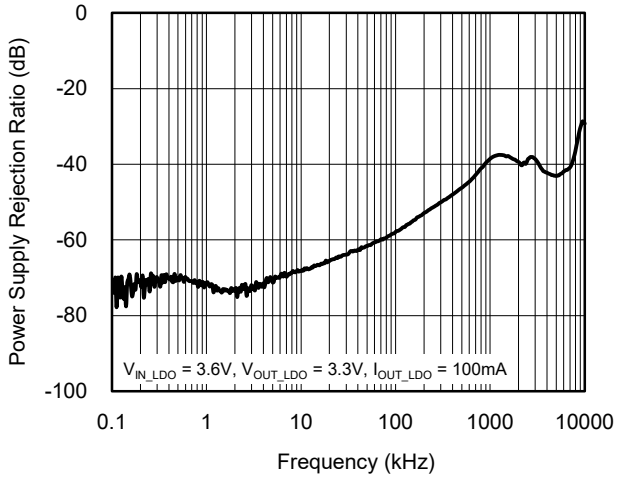
LDO Load Regulation



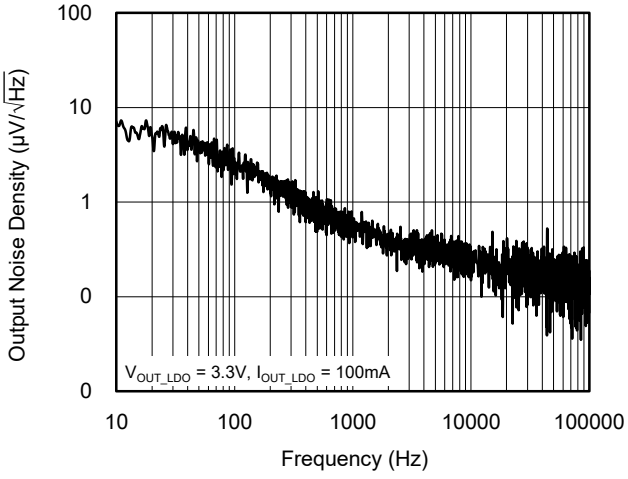
LDO Dropout Voltage vs. Output Current



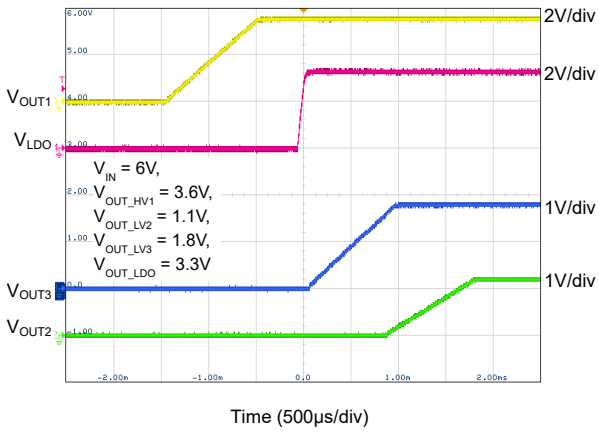
LDO PSRR



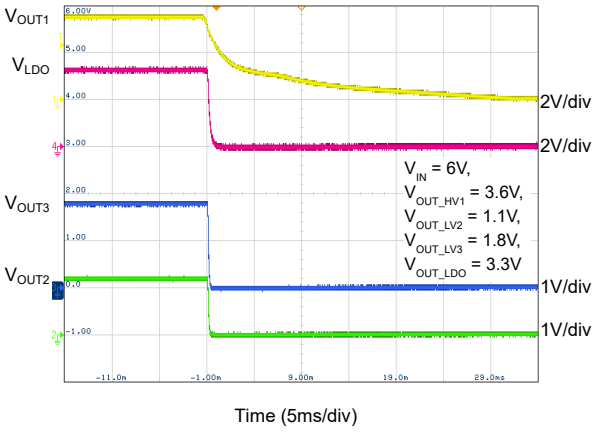
LDO Output Noise



SEQ0 Power-On



SEQ0 Power-Down



DETAILED DESCRIPTION

Power Management IC Overview

The SGM70276xQ is an automotive-grade power management IC (PMIC) that integrates three step-down converters - HVBuck1 (CH1), LVBuck2 (CH2), LVBuck3 (CH3) and one general-purpose regulator (LDO, CH4).

Under-Voltage and Over-Voltage Protection

The SGM70276xQ includes both input under-voltage lockout (UVLO) and input over-voltage protection (OVP) to ensure safe startup and operation.

UVLO

When V_{IN} falls below the V_{UVLO_L} threshold, the device shuts down. Operation automatically resumes once V_{IN} exceeds the V_{UVLO_H} threshold. The 500mV hysteresis between V_{UVLO_L} and V_{UVLO_H} prevents unstable conditions.

Input OVP

If V_{IN} exceeds the V_{OVP} threshold, all power rails (HVBuck1, LVBuck2, LVBuck3, and LDO) and the SEQOUT signal are immediately disabled. The device automatically recovers once the input voltage returns to the normal range. During an OVP condition, the power good (PG) signal is driven low (0V) to indicate a fault status.

Thermal Protection

An integrated over-temperature protection (OTP) circuit prevents thermal damage. When the junction temperature exceeds a typical value of +160℃, all outputs are disabled. The device automatically resumes normal operation once the temperature falls below the recovery threshold, ensuring reliable thermal cycling in automotive environments.

Internal Pre-Regulator

The IC incorporates a 4.45V linear regulator (PVCC) derived from VIN to power the internal control circuitry. The PVCC can also be used as the pull-up supply for the RSET and SEQ pins but must not power external loads or circuitry.

To minimize noise, a 1μF decoupling capacitor must be connected between the PVCC and AGND pins, and this capacitor should be positioned as close as possible to the PVCC pin.

Peak Current Mode Control

All three step-down converters operate on a peak current mode control architecture.

At the beginning of each switching cycle, an internal oscillator turns on the high-side MOSFET, allowing inductor current to ramp up. The peak inductor current is continuously compared against a control signal derived from the error amplifier, which regulates the output voltage by adjusting the duty cycle. Once the inductor current reaches the reference level, the high-side MOSFET turns off, and current flows through the low-side MOSFET. This process repeats every clock period, ensuring precise regulation of the inductor current, which determines the duty cycle and maintains the desired output voltage.

Spread-Spectrum Operation

To reduce electromagnetic interference (EMI) and meet automotive CISPR standards, the SGM70276xQ employs spread-spectrum frequency modulation.

This function applies a pseudo-random frequency variation of approximately 6% around the nominal switching frequency. By spreading the spectral energy across a wider frequency band, the converter significantly reduces peak EMI amplitudes and avoids interference with sensitive frequency bands such as the 1.8MHz AM radio range.

Phase-Shifted Operation

To further reduce simultaneous switching noise and overall radiated emissions, the SGM70276xQ supports phase-shifted operation between step-down converters. The internal clock system automatically distributes phase offsets among the converters.

For two-channel operation, the high-side MOSFETs are interleaved with a 180° phase shift. In three-channel operation, the converters operate with a 120° phase offset between phases.

This phase interleaving minimizes input ripple current and spreads the switching activity over time, improving both EMI performance and power supply stability.

DETAILED DESCRIPTION (continued)

Allowable Channel Floating

To simplify PCB layout and reduce component cost, unused converter channels (CH2 or CH3) are allowed to leave switching nodes (SW2/SW3) floating without any inductor or output capacitor. The PVD23 pin needs to be tied to a fixed voltage for floating detection, and no decoupling capacitor is required.

During startup, the device can automatically identify active and unused channels. Faults on unused channels do not affect the normal operation.

External Control Output (SGM70276AxQ)

The device integrates an open-drain external control output (SEQOUT) for sequencing or driving external circuits. A pull-up resistor should be connected from the SEQOUT pin to an external voltage supply. PVCC is forbidden from being used as the pull-up supply. Refer to the application tables for detailed timing and power-on sequence configurations.

Power Good Indication (SGM70276BxQ)

The SGM70276BxQ includes an open-drain power good (PG) output to indicate output status. Connect a pull-up resistor from PG to an external voltage source. PVCC is forbidden to be used as the pull-up supply.

When the last channel of power-on sequence reaches 90% of its target voltage, PG is asserted high after a 10ms delay. PG is pulled low when the device is disabled or a protection event occurs.

Channel Protection Features

The SGM70276xQ integrates multiple protections to prevent damages under abnormal conditions such as overload, short-circuit and assembly faults. All system and channel protection are listed in Table 1.

Under-Voltage Protection (UVP)

All Channels

If an under-voltage fault persists beyond the deglitch time on any converter or the LDO output, all channels shut down and device enters a latch-off state until supply power cycle occurs.

Over-Voltage Protection (OVP)

HVBuck1

When an over-voltage fault is detected at the feedback pin (FB1), both the high-side and low-side MOSFETs are immediately turned off. Operation resumes automatically once the voltage drops below the reset level.

LVBuck2, LVBuck3, and LDO

If an over-voltage fault condition persists beyond the deglitch time, all channels are disabled. Once the fault is cleared, all channels restart automatically in sequence.

Over-Current Protection (OCP)

HVBuck1, LVBuck2, and LVBuck3

Each converter employs a cycle-by-cycle peak current-limit to protect against excessive inductor current, including conditions where current exceeds inductor saturation level. During an over-current event, the controller immediately turns off the high-side MOSFET and turns on the low-side MOSFET to prevent further current rise. When the inductor current drops below the valley current-limit, normal operation resumes. Continuous faults beyond the deglitch time force all channels into latch-off mode. Recovery requires V_{IN} cycling.

LDO

When the load current reaches the LDO current-limit threshold, IC will report fault to digital core. If the fault persists beyond the deglitch time, all channels are disabled and the device enters latch-off mode until supply power cycle occurs.

Input Over-Voltage Protection (Input OVP)

LVBuck2, LVBuck3, and LDO

If input voltage exceeds the OVP threshold, all outputs are disabled. When the fault is cleared, the system automatically restarts in sequence.

DETAILED DESCRIPTION (continued)

Table 1. Protection

Type	Channel	Threshold (TYP)	Deglitch Time (TYP)	Protection	Reset and Threshold (TYP)
UVP	CH1	V_{FB1} ≤ 0.8V × 50%	5μs	All channels will be disabled and the device will latch off.	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	CH2	V_{OUT_LV2} ≤ 1.1V × 50%	5μs	All channels will be disabled and the device will latch off.	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	CH3	V_{OUT_LV3} ≤ 1.8V × 50%	5μs	All channels will be disabled and the device will latch off.	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	CH4	V_{OUT_LDO} ≤ V_{OUT_LDO} setting × 40%	5μs	All channels will be disabled and the device will latch off.	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
OVP	CH1	V_{FB1} ≥ 0.8V × 112%	NA	High/Low-side MOSFETs off, low-side MOSFET conditionally ON to charge the BOOT capacitor for driving high-side MOSFET.	V_{FB1} < 0.8V × 110%
	CH2	V_{OUT_LV2} ≥ 1.1V × 120%	5ms	Disable all channels	V_{OUT2} ≤ 1.1V × 111% with deglitch 5ms
	CH3	V_{OUT_LV3} ≥ 1.8V × 120%	5ms	Disable all channels	V_{OUT3} ≤ 1.8V × 111% with deglitch 5ms
	CH4	V_{OUT_LDO} ≥ V_{OUT_LDO} × 124%	5ms	Disable all channels	V_{OUT_LDO} ≤ V_{OUT_LDO} × 109% with deglitch 5ms
OCP	CH1	I_{L1_PEAK} ≥ $I_{CL_PK_HV1}$	10ms	Cycle-by-cycle detection if the condition keeps for 10ms, all channels will be disabled and the device will latch off.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	CH2	I_{L2_PEAK} ≥ $I_{CL_PK_LV2}$	10ms	Cycle-by-cycle detection if the condition keeps for 10ms, all channels will be disabled and the device will latch off.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	CH3	I_{L3_PEAK} ≥ $I_{CL_PK_LV3}$	10ms	Cycle-by-cycle detection if the condition keeps for 10ms, all channels will be disabled and the device will latch off.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	CH4	I_{OUT_LDO} ≥ 480mA	10ms	All channels will be disabled and the device will latch off.	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
Input OVP	CH1	V_{IN} ≥ 20V	5ms	Disable all channels	V_{IN} ≤ 19.2V, Auto-recovery
	CH2	V_{IN_PVD23} ≥ 5.8V	5μs	Disable all channels	V_{IN_PVD23} ≤ 5.38V with deglitch 5μs
	CH3	V_{IN_PVD23} ≥ 5.8V	5μs	Disable all channels	V_{IN_PVD23} ≤ 5.38V with deglitch 5μs
	CH4	V_{IN_LDO} ≥ 5.8V	5μs	Disable all channels	V_{IN_LDO} ≤ 5.38V with deglitch 5μs
OTP	System	T_J ≥ +160℃	5μs	Disable all channels	T_J ≤ +140℃, Auto-recovery
UVLO	System	V_{IN} ≤ 3.3V (after IC Operation)	32μs	Disable all channels	V_{IN} ≥ 3.8V

APPLICATION INFORMATION

Table 2. Power-On Sequence Control

SEQ No.		SEQ0	SEQ1	SEQ2	SEQ3	SEQ4	SEQ5	SEQ6	SEQ7	SEQ8	SEQ9
Sequence		CH1	CH1	CH1	CH1	CH1	CH1, CH2, CH3, CH4, SEQOUT	CH1	CH1	CH1	CH1
		CH4	CH2	CH2	SEQOUT	CH2, CH3, CH4, SEQOUT		CH3	CH3	SEQOUT	CH2
		CH3	CH3	SEQOUT	CH2			CH2	CH4	CH2	CH3
		CH2	SEQOUT	CH3	CH4			CH4	CH2	CH3	CH4
		SEQOUT	CH4	CH4	CH3			SEQOUT	SEQOUT	CH4	SEQOUT
Resistance on SEQ	MIN	1.07MΩ	319kΩ	164kΩ	81.6kΩ	45.4kΩ	26.1kΩ	14.5kΩ	7.78kΩ	Short to PVCC	Short to PGND
	TYP	1.1MΩ	330kΩ	169kΩ	84.5kΩ	47kΩ	27kΩ	15kΩ	8.06kΩ		
	MAX	1.13MΩ	341kΩ	174kΩ	87.4kΩ	48.6kΩ	27.9kΩ	15.5kΩ	8.34kΩ		

NOTES:

1. The SEQOUT output pin is only available in SGM70276AxQ. After SEQOUT output high state 1ms passed, the next channel continues the power on sequence.
2. For SGM70276BxQ, 1ms time interval will substitute the SEQOUT output. Below is the SEQ0 example.
   For SGM70276AxQ, CH1 → CH4 → CH3 → CH2 → SEQOUT.
   For SGM70276BxQ, CH1 → CH4 → CH3 → CH2 → 1ms → PG. (PG delay time = 10ms)

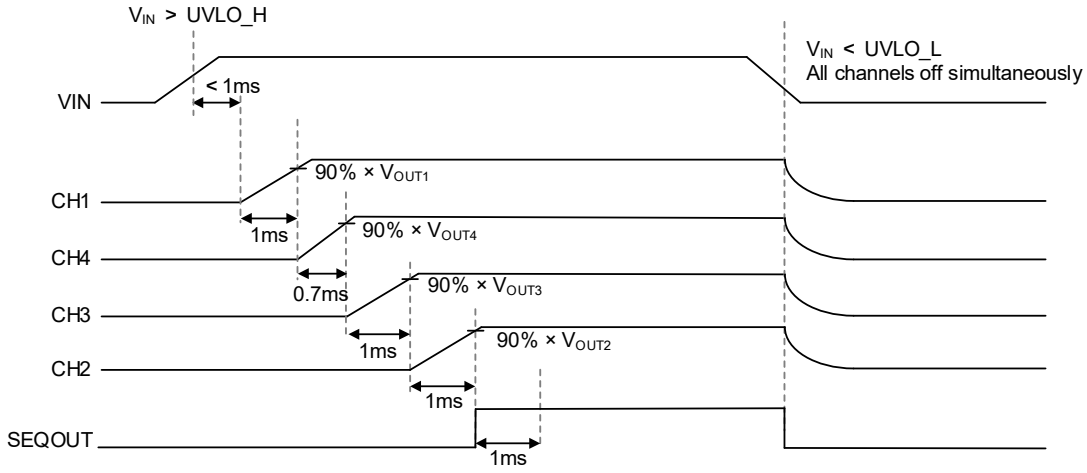


Figure 5 . Example SEQ0 for SGM70276AxQ

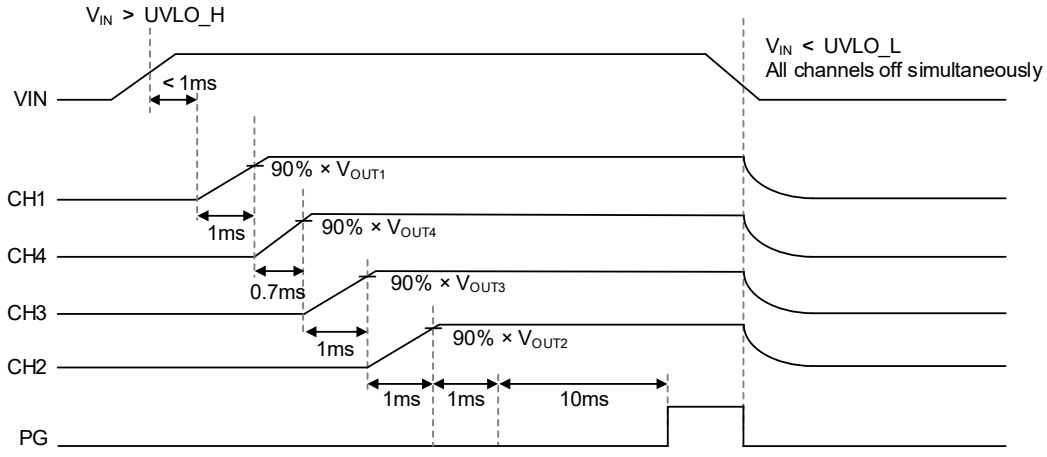


Figure 6. Example SEQ0 for SGM70276BxQ

APPLICATION INFORMATION (continued)

Power Sequence Control

The SGM70276xQ offers 10 distinct power-on sequences for the Buck converters and LDO, configurable via a dedicated resistor on the SEQ pin. The SEQ pin must never be left floating. Selecting a resistance outside the specified range will result in unpredictable power-up behavior. Note that all outputs are designed to power off simultaneously. The SEQ resistor value must be fixed before enabling the device, as any modifications during the power-on procedure may cause sequence errors. Detailed resistor values and their corresponding sequences are provided in the Table 2.

Output Voltage Setting

HVBuck1

The output voltage set by external feedback resistors is given by in the following equation.

$$V_{OUT_HV1} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB1} \quad (1)$$

where the reference voltage V_{FB1} is 0.8V (TYP).

The placement of the resistive divider should be as close as possible to the FB1 pin. For better output voltage accuracy, the divider resistors with ±1% tolerance or better should be used. The resistance ranges from a few kΩ to hundreds of kΩ is recommended.

LVBuck2 and LVBuck3

For SGM70276x-HBQ, the output voltage of LVBuck2 is fixed 1.1V. The output voltage of LVBuck3 is fixed 1.8V.

LDO

The LDO output voltage is controlled by setting the dedicated resistor on RSET pin. Operation of the RSET pin in a floating state is not allowable, and resistor values beyond the defined range do not guarantee proper output voltage. Real-time modification of output voltage is not recommended. The RSET resistor required to be set before the device is enabled.

Table 3. LDO Output Voltage

RSET No.	Voltage	Resistor on REST		
		MIN	TYP	MAX
RSET0	3.5V	1.07MΩ	1.1MΩ	1.13MΩ
RSET1	3.4V	319kΩ	330kΩ	341kΩ
RSET2	3.2V	164kΩ	169kΩ	174kΩ
RSET3	3.1V	81.6kΩ	84.5kΩ	87.4kΩ
RSET4	3.0V	45.4kΩ	47kΩ	48.6kΩ
RSET5	2.8V	26.1kΩ	27kΩ	27.9kΩ
RSET6	2.7V	14.5kΩ	15kΩ	15.5kΩ
RSET7	1.8V	7.78kΩ	8.06kΩ	8.34kΩ
RSET8	2.9V	Short to PVCC		
RSET9	3.3V	Short to PGND		

Input and Output Capacitor Selection

HVBuck1, LVBuck2 and LVBuck3

For step-down converters, it is recommended to use a minimum of a 4.7μF input capacitor and a 10μF output capacitor. Ripple voltage is a key parameter for output capacitor selection. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The formula for calculating output ripple is provided below:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (2)$$

where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) of capacitor.

LDO

Like all low dropout regulators, the SGM70276xQ requires careful selection of external capacitors to ensure regulator stability and performance. A 2.2μF capacitor is suitable for both the LDO input and output sides. Adding additional output capacitance help reduce output noise. However, it may also extend the LDO soft-start time, as the startup current is internally limited to 100mA.

APPLICATION INFORMATION (continued)

Layout Guidelines

Proper PCB layout is critical for the SGM70276xQ. High currents and fast switching nodes demand a well-designed layout to ensure system integrity. Improper layout can lead to instability, EMI problems, or inefficient power conversion. Adhering to the following guidelines is necessary to achieve the best possible performance and reliability:

Minimize Switching Node Area: Keep the trace between the switching node and the inductor as short as possible to reduce the switching loop area and mitigate EMI.

Capacitor Placement: Position input and output capacitors in close proximity to their respective pins to ensure effective filtering.

Power Trace Optimization: Ensure main power traces are wide and short to minimize parasitic resistance and inductance.

Grounding Strategy: Connect AGND and PGND to a robust ground plane to maximize thermal dissipation and provide superior noise immunity.

Feedback Sensing: Connect the feedback network directly to the output capacitor. This prevents signal "bouncing" or inaccuracies caused by the parasitic resistance and inductance of long PCB traces.

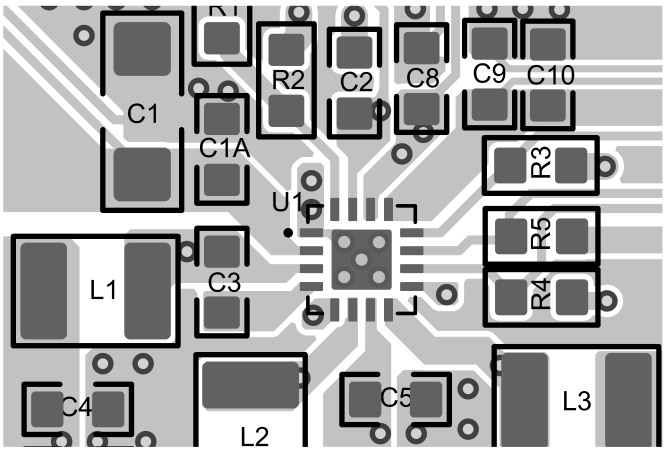


Figure 7. Layout Example for PCB Top Layer

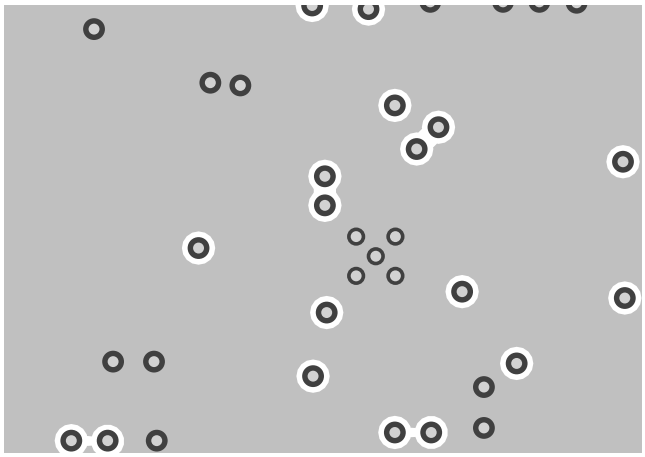


Figure 8. Layout Example for PCB Middle Layer 1

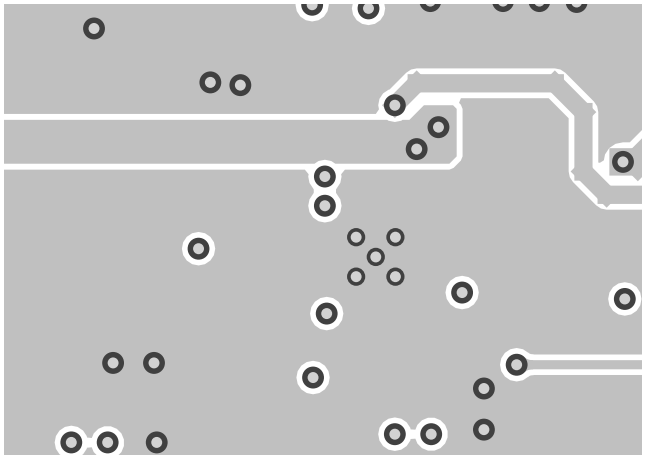


Figure 9. Layout Example for PCB Middle Layer 2

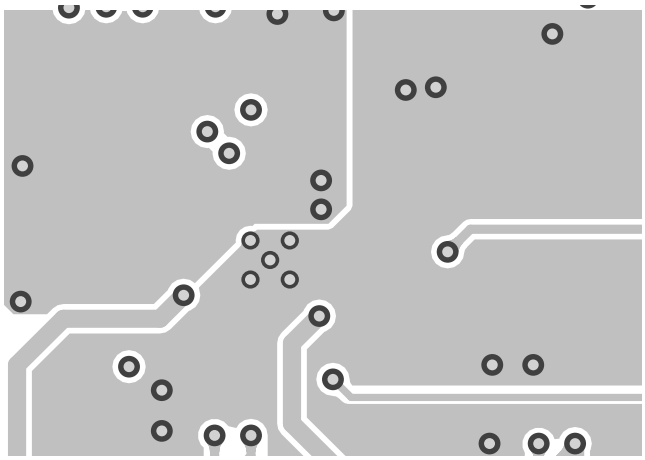


Figure 10. Layout Example for PCB Bottom Layer

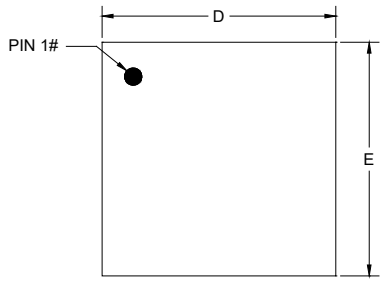
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

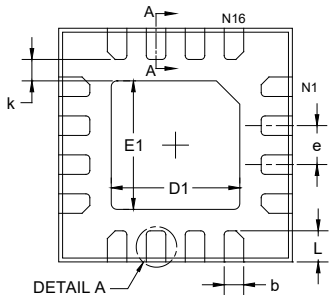
Changes from Original to REV.A (FEBRUARY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

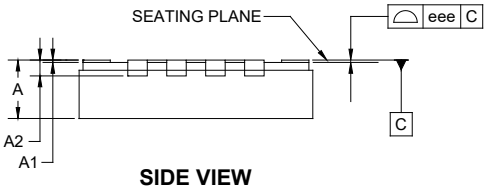
TQFN-3×3-16GL



TOP VIEW



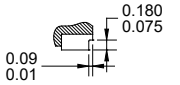
BOTTOM VIEW



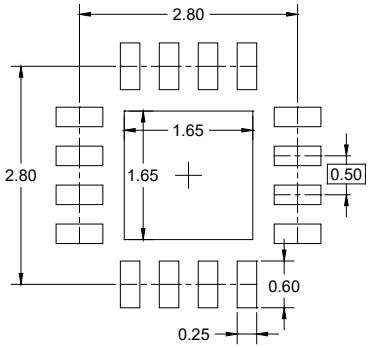
SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



SECTION A-A
TERMINAL CROSS SECTION



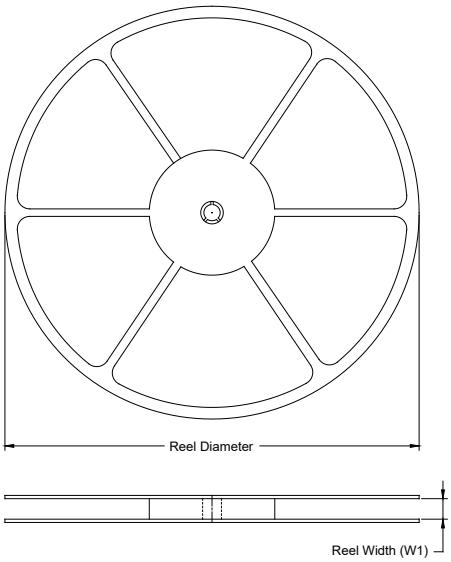
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	2.900	-	3.100
D1	1.600	-	1.800
E	2.900	-	3.100
E1	1.600	-	1.800
e		0.500 BSC	
L	0.300	-	0.500
k		0.275 REF	
eee		0.080	

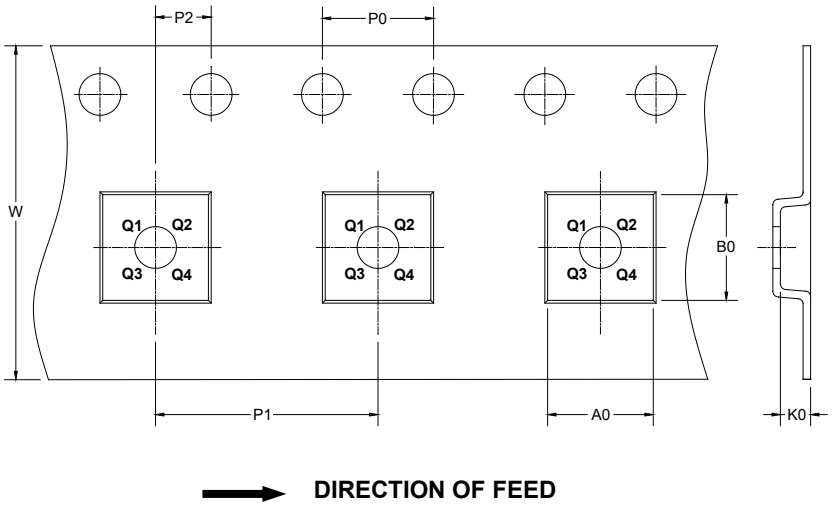
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



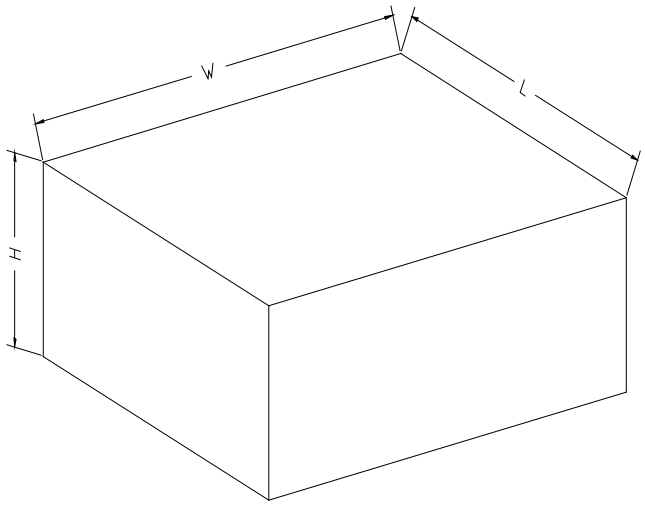
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16GL	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002