# SGM850xQ
# Precision Voltage Supervisor with Programmable Window Watchdog Timer for Automotive Applications

## GENERAL DESCRIPTION

The SGM850xQ has an exact windowed voltage supervisor with 1.4% accuracy for both over-voltage ($V_{IT+OV}$) and under-voltage ($V_{IT-UV}$) thresholds over the temperature from -40℃ to +125℃. It also possesses accurate hysteresis on both thresholds for some systems that need small tolerance. The device output (nRESET) delay can either be determined by factory default settings, or be determined by the external capacitor at CRST pin.

The SGM850xQ has an adjustable watchdog timer and a special watchdog output (nWDO). The nWDO can be used to locate the fault causes. The watchdog timeout period can either be determined by factory default settings, or be determined by the external capacitor at CWD pin. The watchdog function can be closed through SETx (x = 0, 1) pin to prevent some specific watchdog timeout events.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM850xQ is available in a Green TDFN-3×3-10BL package. It features wettable flanks for easy optical inspection.

## TYPICAL APPLICATION

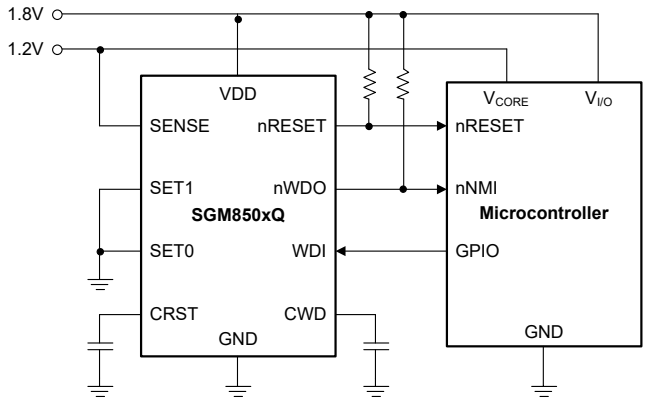



**Figure 1. Typical Application Circuit**

## FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  - **Device Temperature Grade 1**
  - **$T_A$ = -40℃ to +125℃**
- **Functional Safety**
  - **Available Documentation in the Design of Functional Safety Systems**
- **High Threshold Accuracy: 1.4% (MAX)**
- **Precision Over-Voltage and Under-Voltage Monitoring:**
  - **Voltage Rails from 0.4V to 5.0V**
  - **Fault Windows Threshold: ±4% for SGM850A-xQ and ±7% for SGM850B-xQ**
  - **0.7% Hysteresis**
- **Factory-Programmed Precision Watchdog and Reset Timers:**
  - **±15% Accurate Watchdog and Reset Delays**
- **Watchdog Disable Feature**
- **Adjustable Watchdog Timeout Period**
- **Adjustable Reset Delay**
- **Operating Voltage Range: 1.6V to 6.5V**
- **Low Supply Current: 9μA (TYP)**
- **Active-Low, Open-Drain Outputs**
- **Available in a Green Small TDFN-3×3-10BL Package**

## APPLICATIONS

Driver Monitoring
Automotive Telematics Control Unit
Digital Cockpit Processing Unit
On-board & Wireless Charger (OBC)
ADAS Domain Controller
Microcontrollers and DSPs

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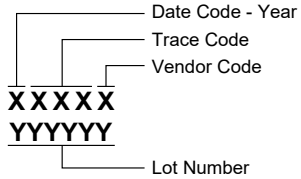
# PACKAGE/ORDERING INFORMATION

| MODEL | THRESHOLD VOLTAGE (V) | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|---|
| SGM850A-0.4Q | 0.4 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850A-0.4QTHS10G/TR | 10DTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850A-0.9Q | 0.9 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850A-0.9QTHS10G/TR | 10ETHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850A-1.2Q | 1.2 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850A-1.2QTHS10G/TR | 10FTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850A-1.8Q | 1.8 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850A-1.8QTHS10G/TR | 10GTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850A-2.5Q | 2.5 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850A-2.5QTHS10G/TR | 10HTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850A-3.0Q | 3.0 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850A-3.0QTHS10G/TR | 10JTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850A-3.3Q | 3.3 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850A-3.3QTHS10G/TR | 10KTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850A-5.0Q | 5.0 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850A-5.0QTHS10G/TR | 10LTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850B-0.4Q | 0.4 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850B-0.4QTHS10G/TR | 106THS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850B-0.9Q | 0.9 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850B-0.9QTHS10G/TR | 107THS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850B-1.2Q | 1.2 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850B-1.2QTHS10G/TR | 108THS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850B-1.8Q | 1.8 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850B-1.8QTHS10G/TR | 109THS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850B-2.5Q | 2.5 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850B-2.5QTHS10G/TR | 10ATHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850B-3.0Q | 3.0 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850B-3.0QTHS10G/TR | 10BTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850B-3.3Q | 3.3 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850B-3.3QTHS10G/TR | 104THS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |
| SGM850B-5.0Q | 5.0 | TDFN-3×3-10BL | -40℃ to +125℃ | SGM850B-5.0QTHS10G/TR | 10CTHS<br>XXXXX<br>YYYYYY | Tape and Reel, 4000 |

NOTE: Only SGM850B-0.4Q is under-voltage type (ADJ type), the other models are windowed ones (fixed sense thresholds).

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. YYYYYY = Lot Number.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

VDD Pin Supply Voltage Range ..... -0.3V to 7V
nRESET, nWDO Pin Output Voltage Range..... -0.3V to 7V
SET0, SET1, WDI, SENSE Pin Voltage Range... -0.3V to 7V
CWD, CRST Pin Voltage Range.....-0.3V to $V_{DD}$ + 0.3V (1)
nRESET, nWDO Pin Output Current .....±20mA
All Pins Input Current.....±20mA
Package Thermal Resistance
TDFN-3×3-10BL, $\theta_{JA}$ ..... 47.2℃/W
TDFN-3×3-10BL, $\theta_{JB}$ ..... 22.3℃/W
TDFN-3×3-10BL, $\theta_{JC\ (TOP)}$ ..... 48.3℃/W
TDFN-3×3-10BL, $\theta_{JC\ (BOT)}$ ..... 9.5℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (2) (3)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. The maximum value of CWD and CRST pin is $V_{DD}$ + 0.3V or 7V, whichever is smaller.

2. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

3. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

## RECOMMENDED OPERATING CONDITIONS

Supply Pin Voltage, $V_{DD}$.....1.6V to 6.5V
Input Pin Voltage, $V_{SENSE}$ .....0V to 6.5V
SET0 Pin Voltage, $V_{SET0}$ .....0V to 6.5V
SET1 Pin Voltage, $V_{SET1}$ .....0V to 6.5V
nRESET Delay Capacitor, $C_{CRST}$ .....0.1nF (1) to 1000nF (1)
Pull-up Resistor to VDD, $C_{RST}$.....9kΩ to 11kΩ (10kΩ, TYP)
Watchdog Timing Capacitor, $C_{CWD}$ .....0.1nF (2) to 1000nF (2)
Pull-up Resistor to VDD, CWD.....9kΩ to 11kΩ (10kΩ, TYP)
Pull-up Resistor, nRESET and nWDO, $R_{PU}$.....
.....1kΩ to 100kΩ (10kΩ, TYP)
nRESET Pin Current, $I_{RST}$..... 10mA (MAX)
Watchdog Output Current, $I_{nWDO}$ ..... 10mA (MAX)
Operating Junction Temperature, $T_J$ ..... -40℃ to +125℃

NOTES:

1. Taking $C_{CRST}$ from 0.1nF to 1000nF gives a reset delay from 0.82ms to 3.22s.

2. Taking $C_{CWD}$ from 0.1nF to 1000nF gives a $t_{WDU_TYP}$ from 62.74ms to 77.455s.

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

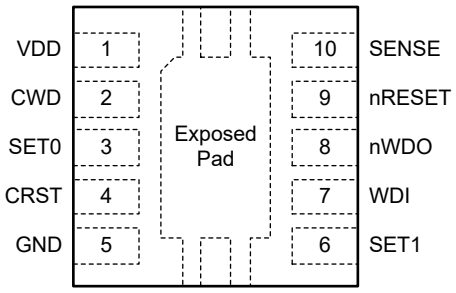
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




TDFN-3×3-10BL

## PIN DESCRIPTION

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1 | VDD | I | Supply Voltage Pin. Place a 0.1μF bypass capacitor under noisy conditions. |
| 2 | CWD | I | Programmable Watchdog Timeout Input. Watchdog timeout period can be programmed by the capacitor at this pin. For factory-set watchdog timeout options, connect this pin to VDD or leave it floating.<br>When using a capacitor, use $t_{WDU_TYP}$ (s) = 77.4 × $C_{CWD}$ (μF) + 0.055 (s) to determine the window watchdog upper boundary. And the SETx pins can set the lower watchdog boundary. |
| 3 | SET0 | I | Logic Input. SET0 along with SET1 and CWD determines the watchdog ratio, timeout period and disable function. |
| 4 | CRST | I | Programmable Reset Timeout Pin. The reset timeout period can be programmed by the capacitor at this pin. For factory-set reset timeout options, please connect this pin to VDD or leave it floating.<br>When using an external capacitor, use $t_{RST_TYP}$ (s) = 3.22 × $C_{CRST}$ (μF) + 0.0005 (s) to determine the reset timeout period. |
| 5 | GND | G | Ground Pin. |
| 6 | SET1 | I | Logic Input. SET1 along with SET0 and CWD determines the watchdog ratio, timeout period and disable function. |
| 7 | WDI | I | Watchdog Input. A falling edge at WDI pin between the maximum lower watchdog window boundary ($t_{WDL_MAX}$) and the minimum upper watchdog window boundary ($t_{WDU_MIN}$) ensures nWDO unasserted.<br>Use SETx pins to close the watchdog function once the watchdog is unasserted. When the watchdog function is closed, as well as nRESET or nWDO is low, no signals at WDI is effective. Note that the WDI pin must be connected to VDD or GND once the watchdog function is closed. |
| 8 | nWDO | O | Watchdog Output. The pull-up resistor for nWDO is recommended to select from 1kΩ to 100kΩ. When the watchdog timeout period ends, nWDO asserts low for the nRESET timeout delay ($t_{RST}$). Note that nWDO can only be asserted low when nRESET is high. When nRESET goes low, nWDO is in a high-impedance state. |
| 9 | nRESET | O | Reset output. The pull-up resistor for nRESET is recommended to select from 1kΩ to 100kΩ. When the SENSE pin voltage is lower than the under-voltage threshold ($V_{IT - (UV)}$) or above the over-voltage threshold ($V_{IT + (OV)}$), nRESET becomes low. When the SENSE pin voltage falls into the normal monitoring range, the reset timer starts to count and nRESET turns high after the timer completion. In the power-on process, the state of nRESET is undefined when VDD is still below the power-on reset voltage ($V_{POR}$). Above $V_{POR}$, nRESET goes low and remains low until the SENSE pin voltage is within the operating range (between $V_{IT - (UV)}$ and $V_{IT + (OV)}$). |
| 10 | SENSE | I | SENSE Input to Monitor the Voltage Rail. |
| Exposed Pad | — | — | Exposed Pad. Connect this pad to GND. |

NOTE: I = input, O = output, G = ground

# ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 1.6V to 6.5V, $R_{PULL}$ = 10kΩ, $T_A$ = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **General Characteristics** | | | | | | |
| Supply Voltage | $V_{DD}$ (1) (2) (3) | | 1.6 | | 6.5 | V |
| Supply Current | $I_{DD}$ | | | 9 | 19 | μA |
| **Reset Function** | | | | | | |
| Power-On Reset Voltage | $V_{POR}$ (2) | $I_{nRESET}$ = 15μA, $V_{OL_MAX}$ = 0.25V | | | 0.8 | V |
| Under-Voltage Lockout Voltage | $V_{UVLO}$ (1) | | | 1.37 | | V |
| Over-Voltage SENSE Threshold Accuracy, Entering nRESET | $V_{IT+\,OV}$ | | $V_{IT+\,NOM}$ - 1.4% | | $V_{IT+\,NOM}$ + 1.4% | V |
| Under-Voltage SENSE Threshold Accuracy, Entering nRESET | $V_{IT-\,UV}$ | | $V_{IT+\,NOM}$ - 1.4% | | $V_{IT+\,NOM}$ + 1.4% | V |
| Falling SENSE Threshold Voltage, Adjustable Version Only | $V_{IT_ADJ}$ | | 0.3944 | 0.4 | 0.4056 | V |
| Hysteresis Voltage | $V_{HYST}$ | | 0.2 | 0.7 | 1.4 | % |
| CRST Pin Charge Current | $I_{CRST}$ | CRST = 0.5V | 320 | 375 | 430 | nA |
| CRST Pin Threshold Voltage | $V_{CRST}$ | | 1.185 | 1.21 | 1.235 | V |
| **Window Watchdog Function** | | | | | | |
| CWD Pin Charge Current | $I_{CWD}$ | CWD = 0.5V | 335 | 375 | 415 | nA |
| CWD Pin Threshold Voltage | $V_{CWD}$ | | 1.185 | 1.21 | 1.235 | V |
| nRESET, nWDO Output Low | $V_{OL}$ | $V_{DD}$ = 5V, $I_{SINK}$ = 3mA | | | 0.4 | V |
| nRESET, nWDO Output Leakage Current | $I_D$ | $V_{DD}$ = 1.6V, $V_{nRESET}$ = $V_{nWDO}$ = 6.5V | | | 1 | μA |
| SET0, SET1 Low-Level Input Voltage | $V_{IL}$ | | | | 0.25 | V |
| SET0, SET1 High-Level Input Voltage | $V_{IH}$ | | 0.8 | | | V |
| WDI Low-Level Input Voltage | $V_{IL_WDI}$ | | | | 0.3 × $V_{DD}$ | V |
| WDI High-Level Input Voltage | $V_{IH_WDI}$ | | 0.8 × $V_{DD}$ | | | V |
| SENSE Pin Idle Current | $I_{SENSE}$ | All models, $V_{SENSE}$ = 5.0V, $V_{DD}$ = 3.3V | | 1.85 | 2.5 | μA |
| | | SGM850B-0.4Q only, $V_{SENSE}$ = 5.0V, $V_{DD}$ = 3.3V | -50 | | 50 | nA |
| **General Characteristics** | | | | | | |
| CWD Pin Evaluation Period | $t_{INIT_CWD}$ | | | 2.3 | | ms |
| CRST Pin Evaluation Period | $t_{INIT_CRST}$ | | | 500 | | μs |
| Time Required between Changing the SET0 and SET1 Pins | $t_{SET}$ | | | 550 | | μs |
| SET0, SET1 Pin Setup Time | | | | 1 | | μs |
| Startup Delay (3) | $t_{SD}$ | | | 370 | | μs |
| **Reset Function** | | | | | | |
| Reset Timeout Period | $t_{RST}$ | CRST = NC | 170 | 200 | 230 | ms |
| | | CRST = 10kΩ to VDD | 8.5 | 10 | 11.5 | ms |
| $V_{SENSE}$ to nRESET Delay | $t_{RST-DEL}$ | $V_{DD}$ = 5V, $V_{SENSE}$ = $V_{IT+\,OV}$ + 2.5% | | 50 | | μs |
| | | $V_{DD}$ = 5V, $V_{SENSE}$ = $V_{IT-\,UV}$ - 2.5% | | 25 | | |

NOTES:
1. Once $V_{DD}$ is lower than $V_{UVLO}$, nRESET turns low.
2. Once $V_{DD}$ is lower than $V_{POR}$, nRESET and nWDO are both undefined.
3. During power-on, $V_{DD}$ must keep a minimum value of 1.6V for at least 370μs before the output corresponds to the SENSE voltage.

## TIMING REQUIREMENTS

($V_{DD}$ = 1.6V to 6.5V, $R_{PULL}$ = 10kΩ, $T_A$ = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

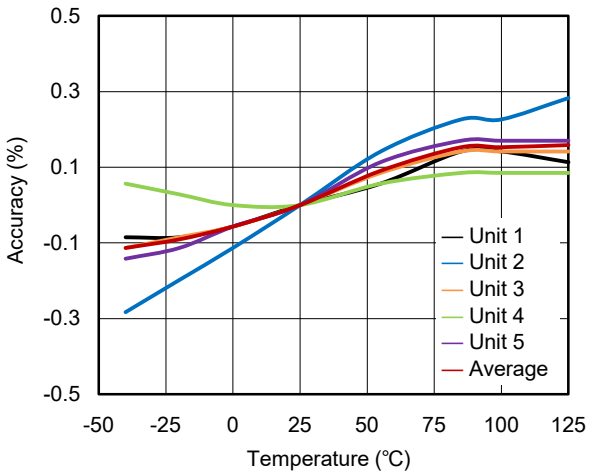
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Window Watchdog Function** | | | | | | |
| Window Watchdog Ratio of Lower Boundary to Upper Boundary | WD ratio | CWD = programmable, SET0 = 0, SET1 = 0 (1) | | 1/8 | | |
| | | CWD = programmable, SET0 = 1, SET1 = 1 (1) | | 1/2 | | |
| | | CWD = programmable, SET0 = 0, SET1 = 1 (1) (2) | | 3/4 | | |
| Window Watchdog Lower Boundary | $t_{WDL}$ | CWD = NC, SET0 = 0, SET1 = 0 | 19.1 | 22.5 | 25.9 | ms |
| | | CWD = NC, SET0 = 0, SET1 = 1 | 1.50 | 1.88 | 2.26 | ms |
| | | CWD = NC, SET0 = 1, SET1 = 0 | Watchdog disabled | | | |
| | | CWD = NC, SET0 = 1, SET1 = 1 | 680 | 800 | 920 | ms |
| | | CWD = 10kΩ to VDD, SET0 = 0, SET1 = 0 | 7.43 | 8.8 | 10.07 | ms |
| | | CWD = 10kΩ to VDD, SET0 = 0, SET1 = 1 | 7.43 | 8.8 | 10.07 | ms |
| | | CWD = 10kΩ to VDD, SET0 = 1, SET1 = 0 | Watchdog disabled | | | |
| | | CWD = 10kΩ to VDD, SET0 = 1, SET1 = 1 | 1.50 | 1.88 | 2.26 | ms |
| Window Watchdog Upper Boundary | $t_{WDU}$ | CWD = NC, SET0 = 0, SET1 = 0 | 46.7 | 55.0 | 63.3 | ms |
| | | CWD = NC, SET0 = 0, SET1 = 1 | 23.3 | 27.5 | 31.7 | ms |
| | | CWD = NC, SET0 = 1, SET1 = 0 | Watchdog disabled | | | |
| | | CWD = NC, SET0 = 1, SET1 = 1 | 1360 | 1600 | 1840 | ms |
| | | CWD = 10kΩ to VDD, SET0 = 0, SET1 = 0 | 93.5 | 110.0 | 126.5 | ms |
| | | CWD = 10kΩ to VDD, SET0 = 0, SET1 = 1 | 165.7 | 195.0 | 224.3 | ms |
| | | CWD = 10kΩ to VDD, SET0 = 1, SET1 = 0 | Watchdog disabled | | | |
| | | CWD = 10kΩ to VDD, SET0 = 1, SET1 = 1 | 9.56 | 11.3 | 12.94 | ms |
| Setup Time Required for the Device to Respond to Changes on WDI after Being Enabled | $t_{WD-SETUP}$ | | | 120 | | μs |
| Minimum WDI Pulse Duration | | | | 100 | | ns |
| WDI to nWDO Delay | $t_{WD-DEL}$ | | | 120 | | ns |

NOTES:
1. 0 refers to $V_{SET} \le V_{IL}$, 1 refers to $V_{SET} \ge V_{IH}$.
2. If this watchdog ratio is used, then $t_{WDL_MAX}$ can overlap $t_{WDU_MIN}$.

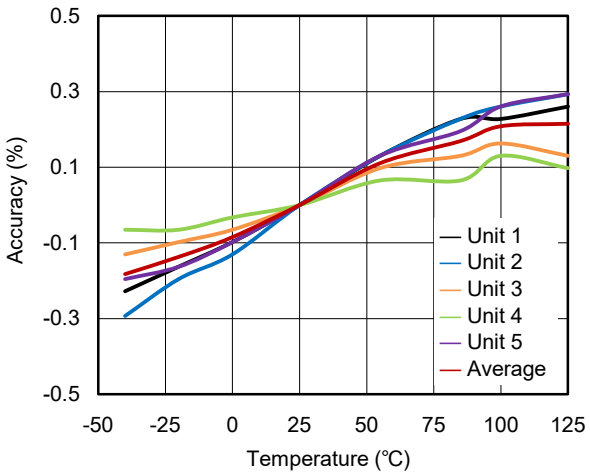
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = +25℃, $V_{DD}$ = 1.6V to 6.5V unless otherwise noted.

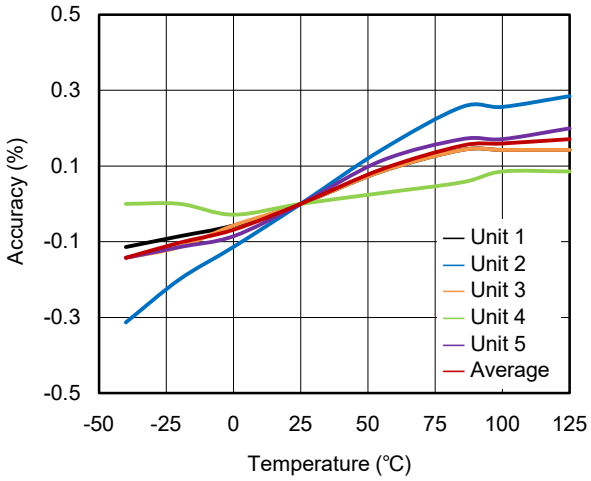
$V_{IT+OV}$ Accuracy vs. Temperature



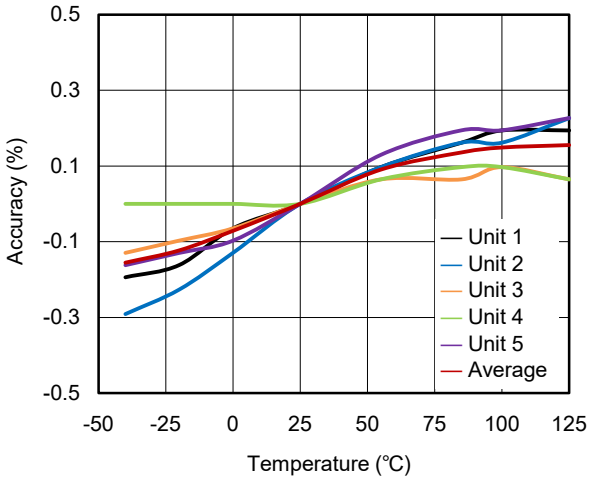

$V_{IT-UV}$ Accuracy vs. Temperature



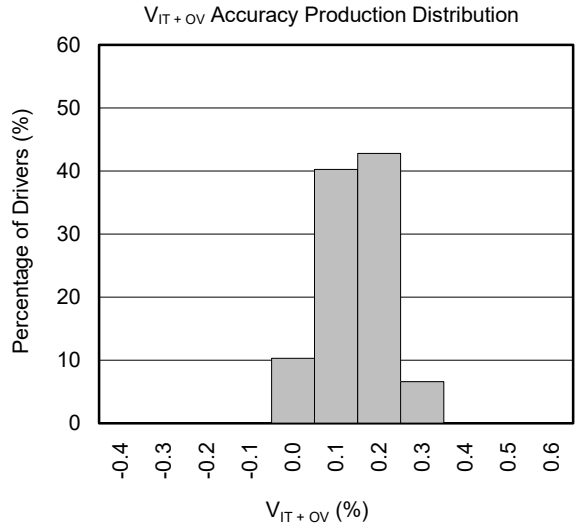

$V_{IT-OV}$ Accuracy vs. Temperature



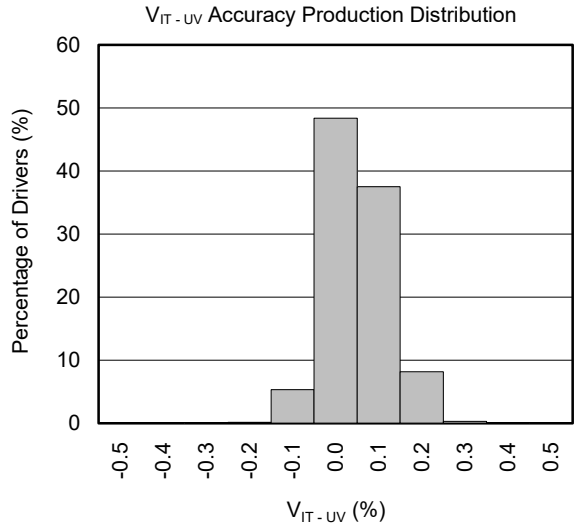

$V_{IT+UV}$ Accuracy vs. Temperature




$V_{IT+OV}$ Accuracy Production Distribution



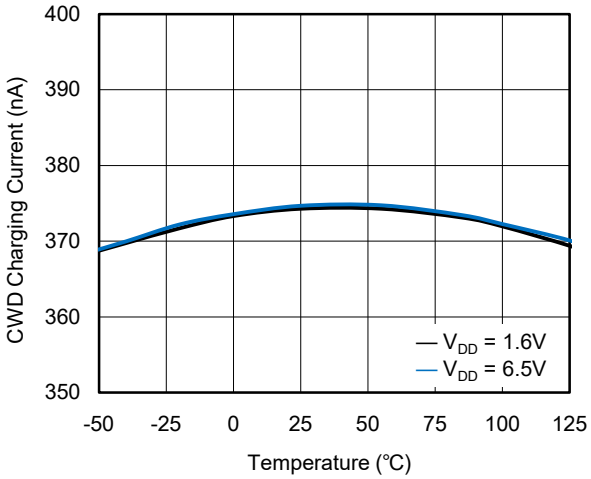

$V_{IT-UV}$ Accuracy Production Distribution



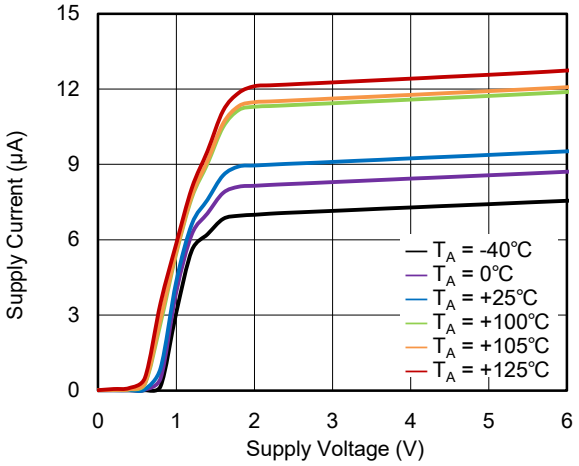
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{DD}$ = 1.6V to 6.5V unless otherwise noted.

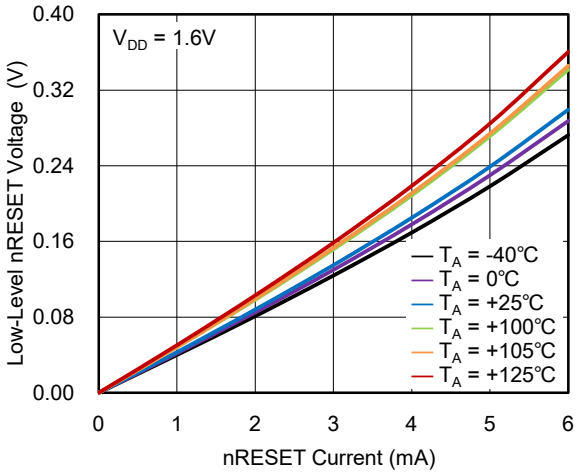
CWD Charging Current vs. Temperature



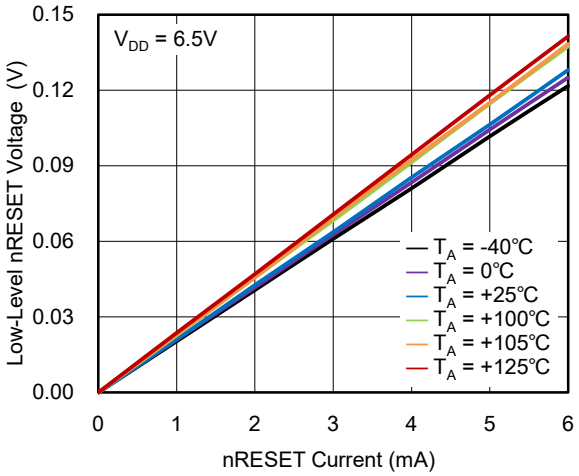

Supply Current vs. Supply Voltage



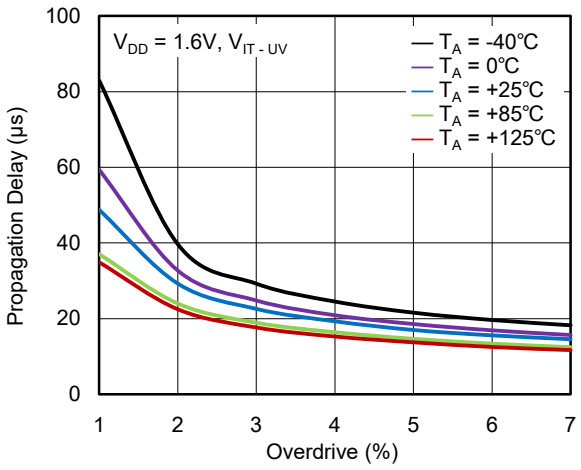

Low-Level nRESET Voltage vs. nRESET Current



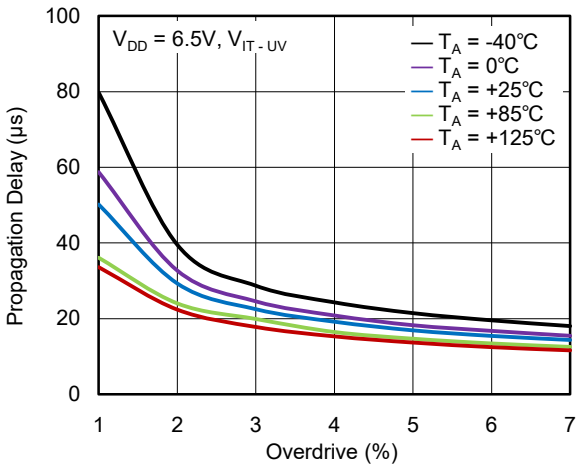

Low-Level nRESET Voltage vs. nRESET Current




Propagation Delay vs. Overdrive



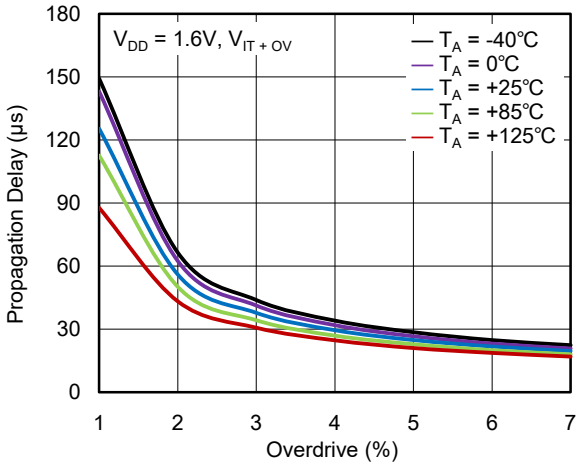

Propagation Delay vs. Overdrive



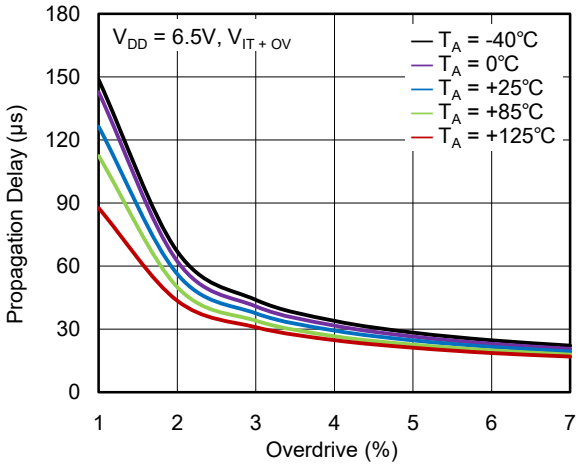
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{DD}$ = 1.6V to 6.5V unless otherwise noted.

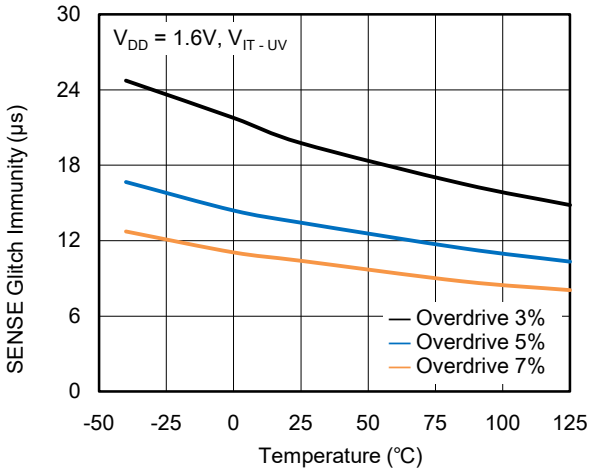
Propagation Delay vs. Overdrive



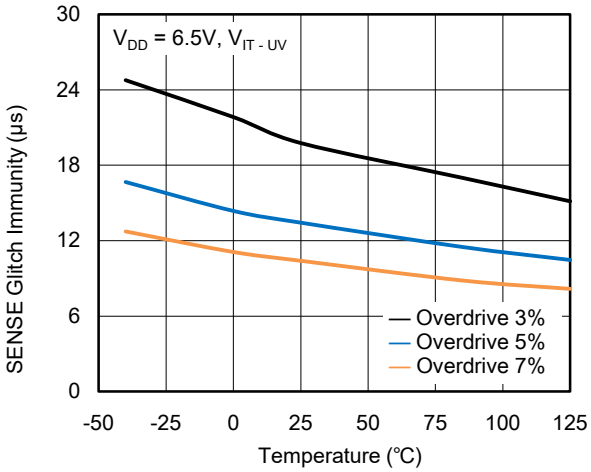

Propagation Delay vs. Overdrive



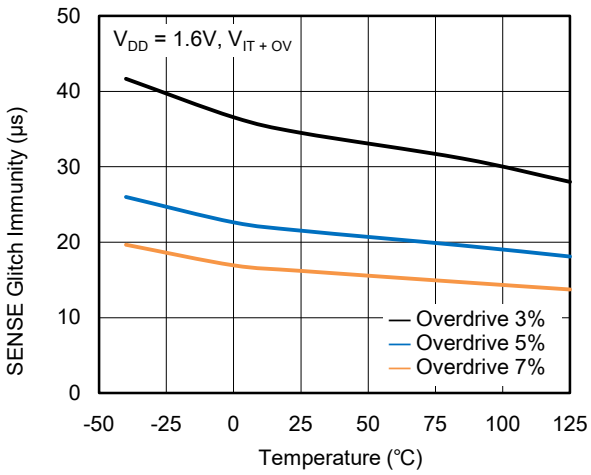

SENSE Glitch Immunity vs. Temperature



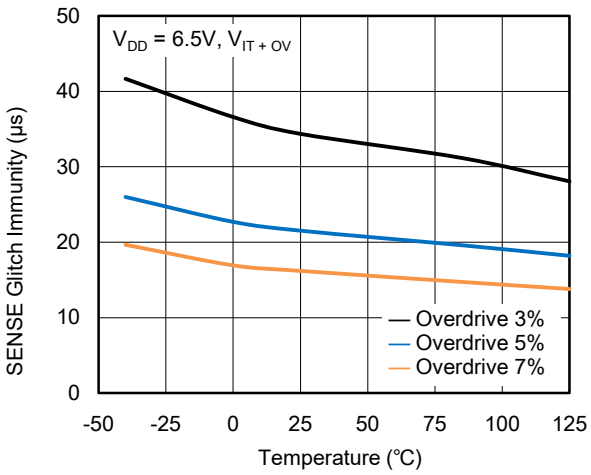

SENSE Glitch Immunity vs. Temperature



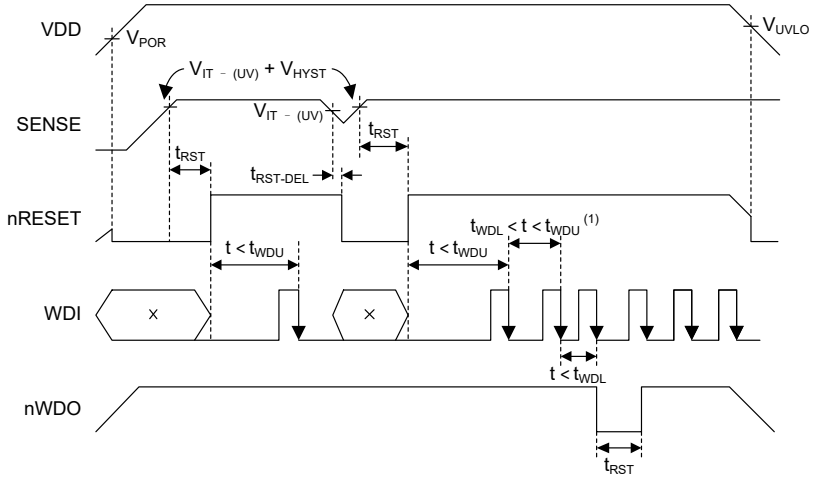

SENSE Glitch Immunity vs. Temperature




SENSE Glitch Immunity vs. Temperature



## TIMING REQUIREMENTS (continued)




NOTE: 1. See Figure 3 for WDI timing requirements.

**Figure 2. Timing Diagram**

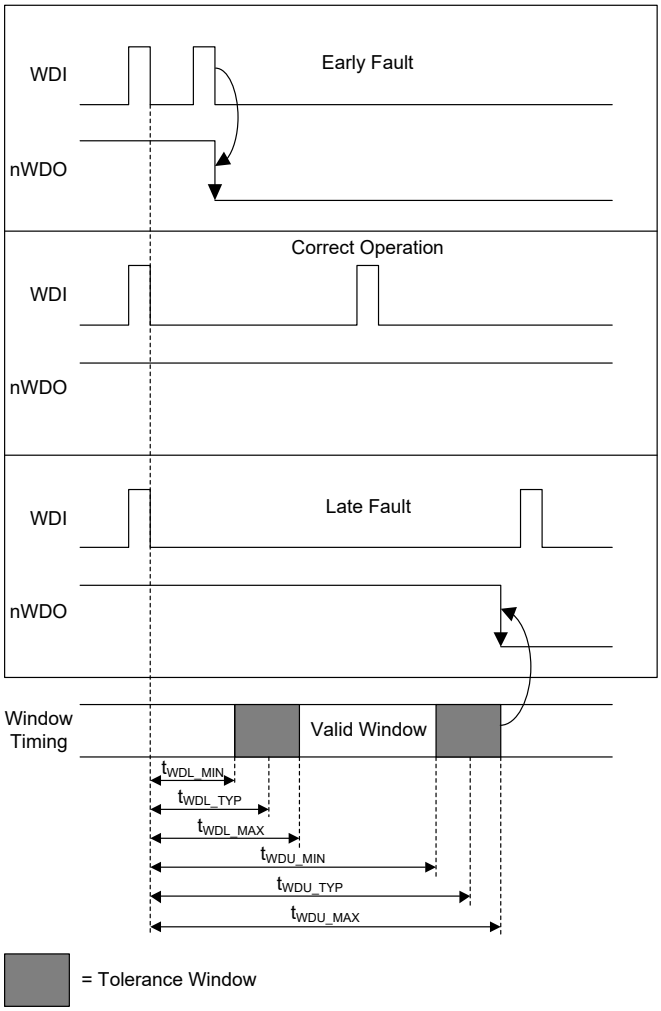
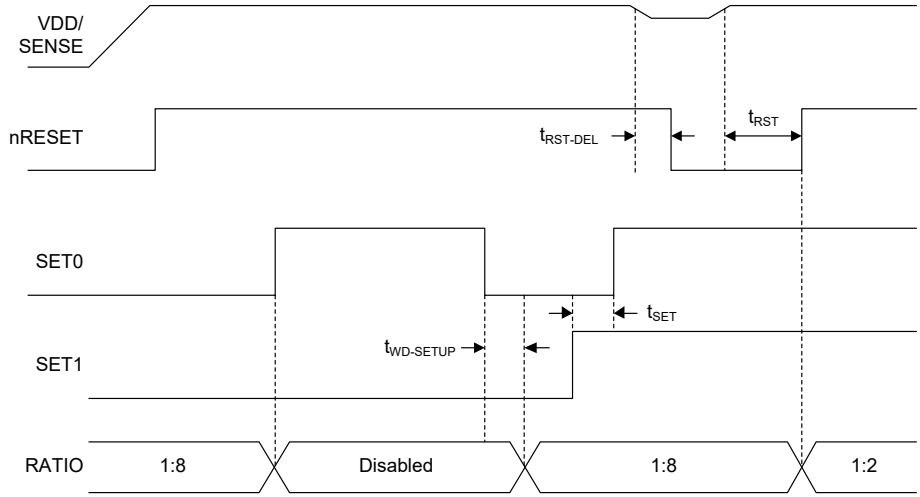



**Figure 3. SGM850xQ Window Watchdog Timing**

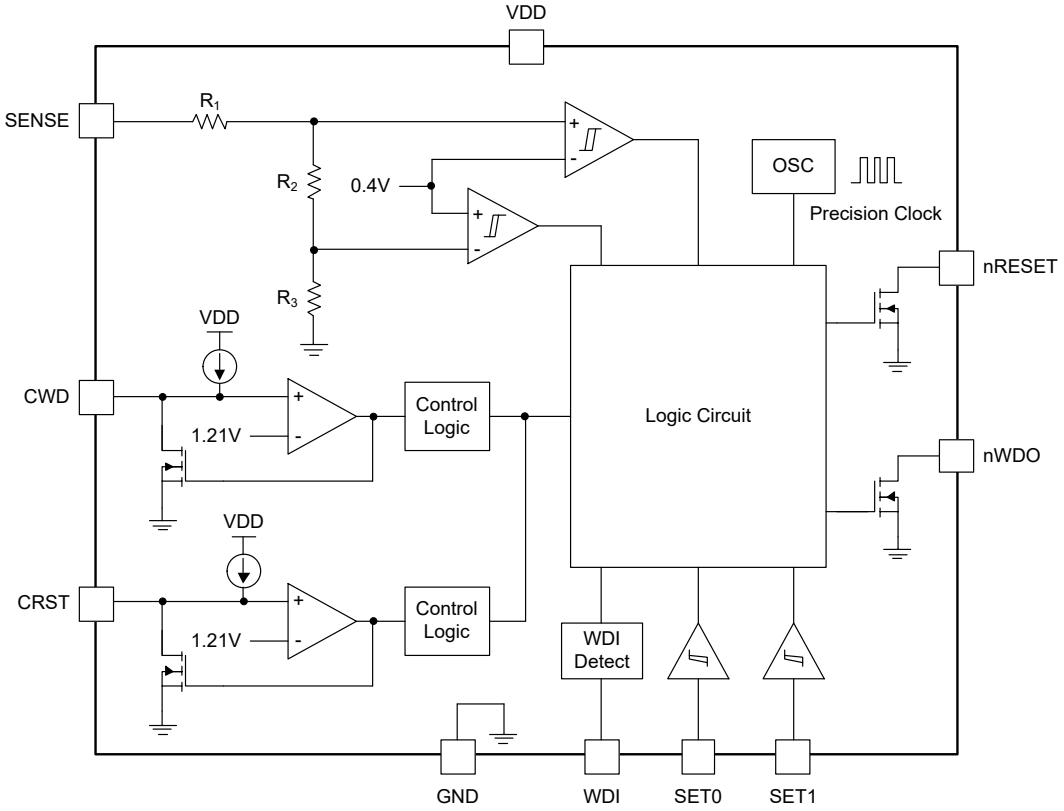
## TIMING REQUIREMENTS (continued)




NOTE: 1. The state of SET0 and SET1 should be the same before and after the watchdog disable event.

**Figure 4. Changing SET0 and SET1 Pins**

# FUNCTIONAL BLOCK DIAGRAMS




NOTE: $R_{TOTAL} = R_1 + R_2 + R_3 = 2.7M\Omega$.

**Figure 5. Fixed Version Block Diagram**

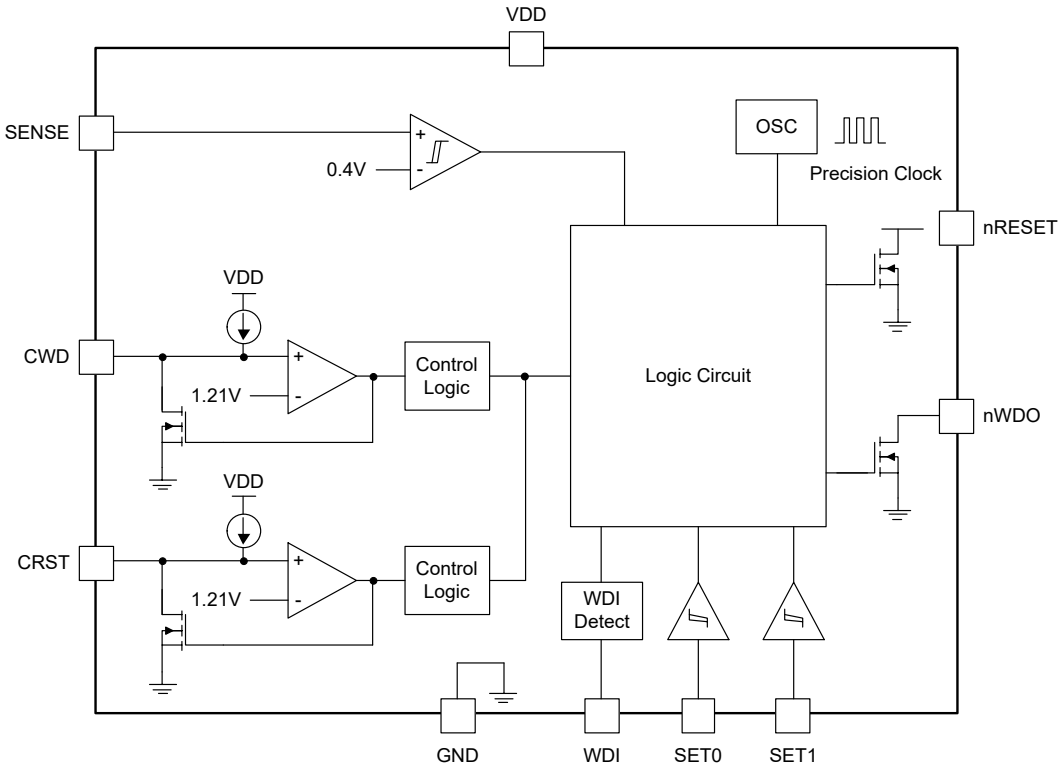



**Figure 6. Adjustable Version Block Diagram**

# DETAILED DESCRIPTION

The SGM850xQ has an exact windowed voltage supervisor with 1.4% accuracy for both over-voltage ($V_{IT+OV}$) and under-voltage ($V_{IT-UV}$) thresholds over the temperature from -40℃ to +125℃. It also possesses accurate hysteresis on both thresholds ($V_{IT+OV}$ and $V_{IT-UV}$) for systems that need small tolerance like microcontroller unit (MCU). Moreover, the device has an internal windowed watchdog to avoid the run out problem, especially under safety critical applications.

## CRST

The CRST pin gives user the option to adopt the preset reset delay by connecting the CRST pin to VDD (CRST = VDD) or leave it floating (CRST = NC), or take the user-programmed reset delay by connecting the CRST pin to an external capacitor (CRST = CAP). Once the SENSE voltage falls into the valid window ($V_{IT-UV}$ < $V_{SENSE}$ < $V_{IT+OV}$), the CRST pin state is detected in 500μs ($t_{INIT_CRST}$) with the built-in state machine. When the CRST pin is connected to VDD, a pull-up resistor of 10kΩ is advised.

## nRESET

The nRESET pin is an open-drain output. There must be a pull-up resistor to pull up the nRESET voltage to the demanded voltage level. The determination of this resistor should take low-level output voltage ($V_{OL}$), capacitance between the nRESET and GND, and nRESET pin leakage current into consideration. Usually, a pull-up resistor ranging from 1kΩ to 100kΩ is accepted.

## Over- and Under-Voltage Fault Detection

The SGM850xQ incorporates an OV detector and a UV detector, as well as a precise voltage reference. Besides, it has a built-in divider resistor network for the SENSE pin to reduce the overall component number and improve the detection accuracy as well. Both the OV detector and UV detector adopt precise hysteresis in order to give noise suppression and deglitch capability. When the SENSE pin voltage ($V_{SENSE}$) enters the valid threshold window, nRESET maintains low for $t_{RST}$ and then goes high. Note that $t_{RST}$ is determined by the configuration at the CRST pin. On the contrary, when $V_{SENSE}$ is lower than $V_{IT-UV}$ or higher than $V_{IT+OV}$, nRESET goes low after $t_{RST-DEL}$, as shown in Figure 7.

Considering the maximum voltage of the SENSE pin is 6.5V, it is recommended placing a capacitor ranging from 1nF to 10nF at the SENSE pin to suppress the possible spike voltages under noisy environments.

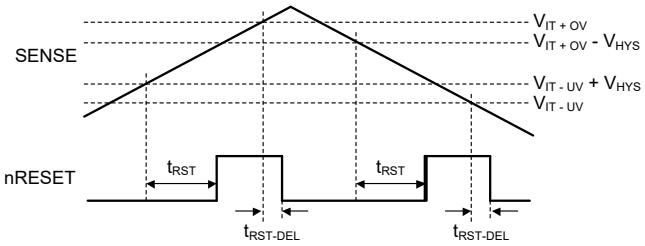



**Figure 7. Timing Diagram of SENSE and nRESET**

## Adjustable Operation Using the SGM850B-0.4Q

The SENSE pin threshold of SGM850B-0.4Q is fixed at 0.4V and can be used to monitor voltages higher than 0.4V with the circuit depicted in Figure 8. Note that these two models have only UV threshold comparator. Hence, the monitored signal ($V_{MON}$) threshold can be calculated as described in Equation 1 and Equation 2, respectively:

$$V_{MON} = V_{IT_ADJ} \times (1 + R_1/R_2) \quad (1)$$

$$R_{TOTAL} = R_1 + R_2 \quad (2)$$

Note that using large resistors helps reduce the current flowing into the SENSE pin. However, it has negative effect on the detection accuracy due to smaller bias current. Consequently, $R_{TOTAL}$ should be limited to ensure that the current flowing through the SENSE pin resistor divider is not larger than 100 × $I_{SENSE}$ (SENSE pin idle current).

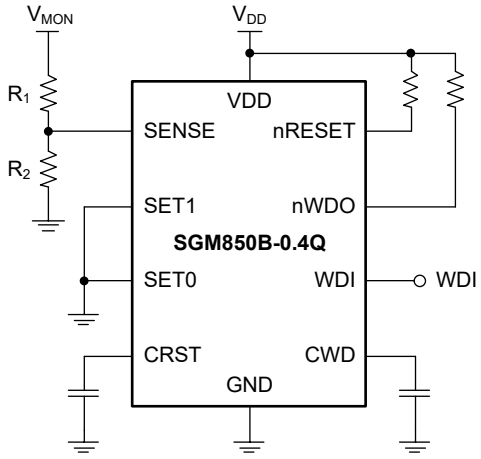



**Figure 8. Adjustable Voltage Monitor**

# DETAILED DESCRIPTION (continued)

## Window Watchdog

### SET0 and SET1

The combination of SET0 and SET1 pins can be used to either disable the watchdog or change the ratio between the watchdog upper boundary and lower boundary. The first condition of disabling the watchdog is activated at once, while the latter one can only be activated with the occurrence of a rising edge for nRESET.

#### *Enabling the Window Watchdog*

The SGM850xQ possesses the watchdog disable function by setting SET0 = 1 and SET0 = 0. Due to this feature, the user can jump over the possible error caused by the watchdog in the initialization process or in shutdown mode. The device responds at once from the watchdog enable mode to the watchdog disable mode. However, it takes 120μs ($t_{WD-SETUP}$) to change from the watchdog disable mode to the watchdog enable mode (see Figure 9). Note that the SGM850xQ does not recognize any WDI signal during $t_{WD-SETUP}$.

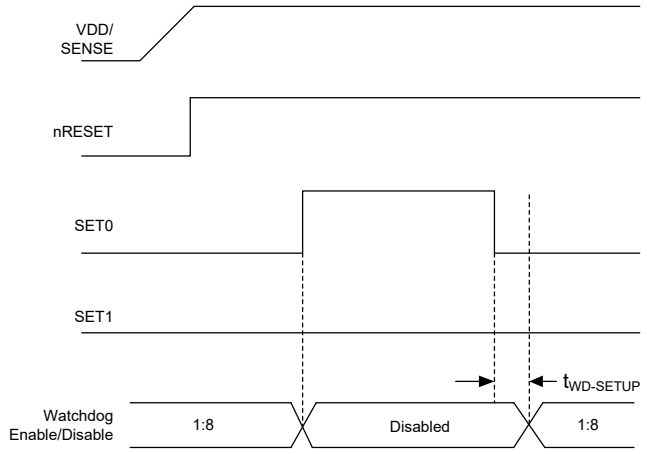
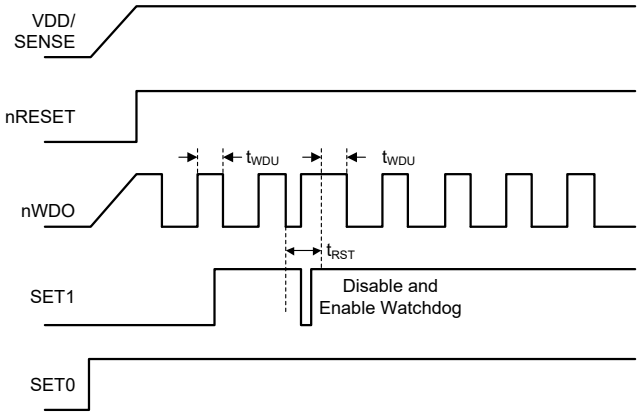



**Figure 9. Enable the Watchdog**

#### *Disabling the Watchdog Timer when Using the CRST Capacitor*

When the device watchdog changes from disable mode to enable mode, nWDO behaves differently between fixed configuration (CRST = NC or CRST = VDD) and adjustable configuration (CRST = CAP). To be more explicit, for fixed configuration of CRST, the watchdog timer is activated immediately once the watchdog is reenabled. However, for adjustable configuration of CRST, the watchdog timer will not be activated unless the period of $t_{RST}$ is terminated after the watchdog is reenabled.




NOTE: No WDI signal, WDI is always at GND.

**Figure 10. Enable and Disable the Watchdog Timer during an nWDO Reset Event**

#### *SET0 and SET1 During Normal Watchdog Operation*

The combination of SET0/1 can be used to configure the watchdog ratio from the upper boundary ($t_{WDU}$) to the lower boundary ($t_{WDL}$). Aside from the set of watchdog disable function for SET0/1, three sets of watchdog ratio are available: 1:8, 3:4 and 1:2. See Table 6 for more details. Usually, SET0 and SET1 are not allowed to change at the same time and a delay of 550μs ($t_{SET}$) is advised between the SET0 state change and SET1 state change. To change the watchdog ratio, it is not sufficient to change the state of SET0/1. That means, a reset event must take place to renew the timing option saved in the SGM850xQ. Details can be seen in Figure 11.

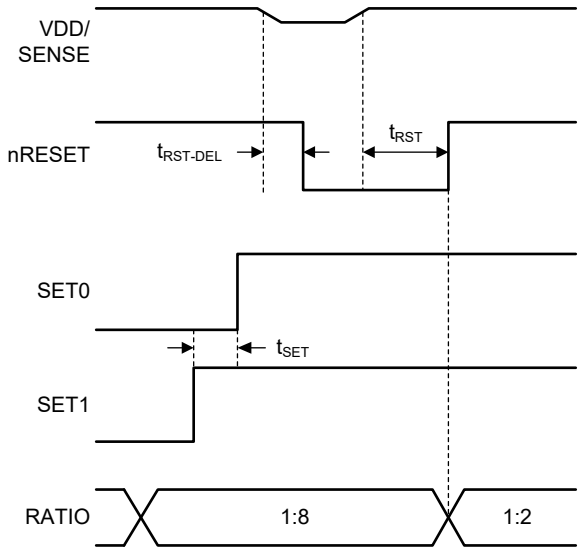



**Figure 11. Changing SET0 and SET1 Pins**

# DETAILED DESCRIPTION (continued)

## Window Watchdog Timer

The SGM850xQ contains a windowed watchdog, which is specially designed for the purpose of safety critical applications. For the conventional watchdog, the watchdog timer will release an asserted signal to pull down the nWDO pin if an effective WDI edge is not detected within the timeout time. Differently, the windowed watchdog timer will release an asserted signal when no effective WDI edge is detected within the window consisting of ($t_{WDL_MAX}$, $t_{WDU_MIN}$). Note that $t_{WDU}$ is determined by the CWD pin while $t_{WDL}$ is determined by the combination of CWD and SET0/1 pins. Figure 12 illustrates how the windowed watchdog works with different WDI pattern.

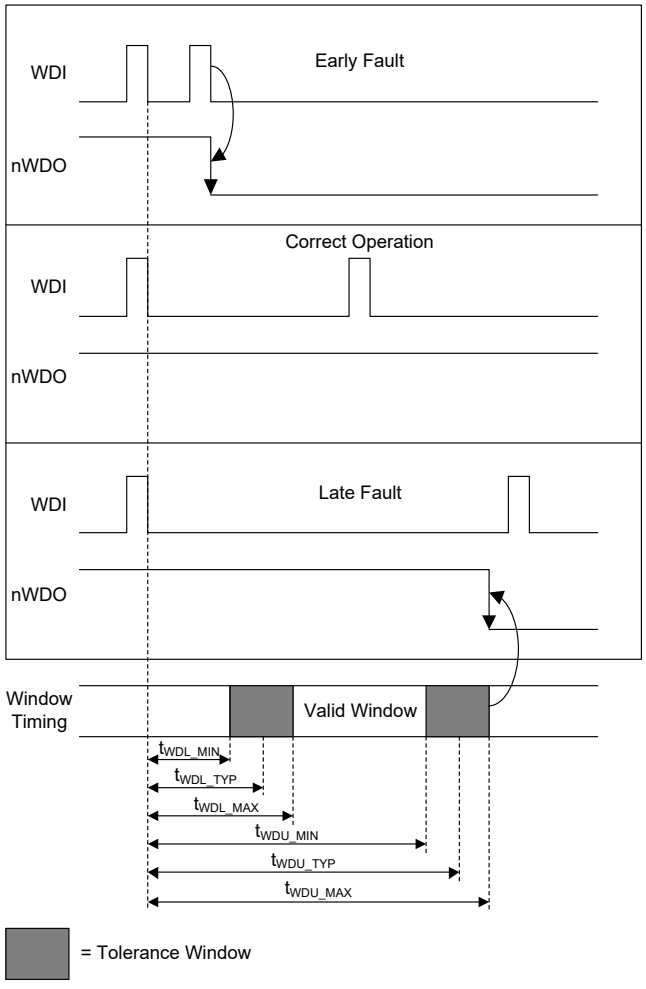



**Figure 12. SGM850xQ Window Watchdog Timing**

## CWD

Through the CWD pin, users can obtain a high-precision and preset watchdog timing in factory or a programmed one. There are three options of the SGM850xQ to configure the watchdog timer. Keep CWD pin floating or pull up a 10kΩ resistor to the VDD pin to set two different factory-programmed timers. Connect a capacitor between the CWD pin and GND to achieve an adjustable timer. Every time when $V_{DD}$ enters the valid threshold window ($V_{IT\,-\,UV}$ < $V_{SENSE}$ < $V_{IT\,+\,OV}$), the device checks the CWD configuration state within $t_{INIT_CWD}$ (about 2.3ms, TYP). During this time, an internal state machine is used to check the CWD pin state and lock it out until nRESET is asserted or powered off.

## WDI Functionality

The WDI pin is the falling-edge triggered watchdog timer input pin. The WDI pulse should be sent out within the window of ($t_{WDL_MAX}$, $t_{WDU_MIN}$), and the pulse of WDI should be at least larger than 100ns to ensure that the pulse can be detected by the device. However, the first pulse should be released before $t_{WDU_MIN}$. If a valid WDI is received, the nWDO remains deasserted. If not, the nWDO is asserted to be low. The WDI is a logic input pin and it cannot be left floating. Users should drive WDI to either VDD or GND to avoid the increasing current of the supply current. When nRESET is asserted, the watchdog function is disabled and any signals at WDI cannot be recognized by the device. When nRESET is deasserted, the device operates normally and the WDI signals can be recognized.

## nWDO Functionality

The nWDO is an independent watchdog output pin, and it can issue a fault flag in the watchdog timing with no need to trigger an nRESET signal, which is always used to reset the whole system. When nRESET is logic high, the nWDO keeps normal operation and it asserts to be low for $t_{RST}$ if no valid WDI is triggered within the valid watchdog timing region. And when the nRESET signal is asserted low for some other reason, the nWDO pin goes high if a resistor is connected to the VDD pin or another voltage rail. When the nRESET signal is deasserted again, the watchdog timer turns back to normal operation as soon as possible.

# DETAILED DESCRIPTION (continued)

## Device Functional Modes

Table 1 summarizes the functional modes of the SGM850xQ.

**Table 1. Device Functional Modes**

| VDD | WDI | nWDO | SENSE | nRESET |
|---|---|---|---|---|
| $V_{DD} < V_{POR}$ | — | — | — | Undefined |
| $V_{POR} \le V_{DD} < V_{UVLO}$ | Ignored | High | — | Low |
| $VDD \ge V_{DD_MIN}$ | Ignored | High | $V_{SENSE} < V_{IT+UV}$ (1) | Low |
| | Ignored | High | $V_{SENSE} > V_{IT-OV}$ (1) | Low |
| | $t_{WDL_MAX} \le t_{PULSE}$ (3) $\le t_{WDU_MIN}$ | High | $V_{IT-UV} < V_{SENSE} < V_{IT+OV}$ (2) | High |
| | $tWDL_{_MAX} > t_{PULSE}$ (3) | Low | $V_{IT-UV} < V_{SENSE} < V_{IT+OV}$ (2) | High |
| | $tWDU_{_MIN} < t_{PULSE}$ (3) | Low | $V_{IT-UV} < V_{SENSE} < V_{IT+OV}$ (2) | High |

NOTES:

1. When $V_{SENSE}$ has not entered the valid window.
2. When $V_{SENSE}$ is in the valid window.
3. Where $t_{PULSE}$ is the time between falling edges on WDI.

### $V_{DD}$ is below $V_{POR}$ ($V_{DD} < V_{POR}$)

When $V_{DD} < V_{POR}$, nRESET signal is undefined and is not to be relied upon for proper device function.

### Above Power-On Reset but Less than UVLO ($V_{POR} \le V_{DD} < V_{UVLO}$)

When $V_{POR} < V_{DD} <$ UVLO, the nRESET pin maintains low no matter what the SENSE pin voltage is. Note that nWDO turns high once nRESET is asserted low and no WDI signal is accepted into the SGM850xQ.

### Above UVLO but Less than $V_{DD_MIN}$ ($V_{UVLO} \le V_{DD} < V_{DD_MIN}$)

When $V_{DD} > V_{UVLO}$ but $V_{DD} < V_{DD_MIN}$, nRESET state is determined by $V_{SENSE}$ like in normal operation but accuracy is not guaranteed.

### Normal Operation ($V_{DD} \ge V_{DD_MIN}$)

When $V_{DD} > V_{DD_MIN}$ continues longer than $t_{SD}$, the nRESET output state is determined by the SENSE pin voltage. When the SENSE pin voltage is within the valid window ($V_{IT-UV} < V_{SENSE} < V_{IT+OV}$), nRESET turns high. When the SENSE pin voltage goes outside of the valid window ($V_{SENSE} < V_{IT-UV}$ or $V_{SENSE} > V_{IT+OV}$), nRESET turns low. Note that nWDO turns high once nRESET is asserted low.

# APPLICATION INFORMATION

According to the eventual application requirements, the way to properly implement the device will be described in detail below.

## CRST Delay

The CRST pin gives user three options to adopt the preset reset delay by connecting CRST to VDD or leaving it floating, or taking the user-programmed reset delay by connecting CRST to an external capacitor. The nRESET delay time is determined by the CRST configuration. Figure 13 shows the three configurations of CRST. Once nRESET is asserted, the CRST pin state is detected in 500μs with the built-in state machine.

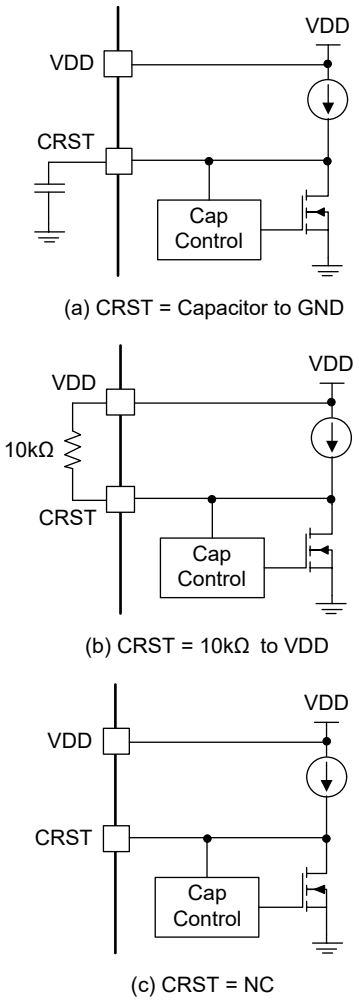



**Figure 13. CRST Configuration Circuit**

## Factory-Programmed Reset Delay Timing

Table 2 illustrates the fixed option of CRST for $t_{RST}$ when CRST = VDD or CRST = NC. Note that the SGM850xQ achieves an accuracy of 15% for $t_{RST}$.

**Table 2. Reset Delay Time for Factory-Programmed Reset Delay Timing**

| CRST | $t_{RST}$ (MIN) | $t_{RST}$ (TYP) | $t_{RST}$ (MAX) |
|---|---|---|---|
| NC | 170ms | 200ms | 230ms |
| 10kΩ to VDD | 8.5ms | 10ms | 11.5ms |

## Programmable Reset Delay-Timing

The SGM850xQ charges the capacitor at the CRST pin with current ($I_{CRST}$) of 375nA. The recommended CRST capacitor ranges from 100pF ($t_{RST}$ = 800μs) to 1μF ($t_{RST}$ = 3.22s). The typical $t_{RST}$ under different $C_{CRST}$ can be described as Equation 3:

$$t_{RST}\ (s) = 3.22 \times C_{CRST}\ (\mu F) + 0.0005\ (s) \quad (3)$$

When the parameter variation of $I_{CRST}$ and $V_{CRST}$ are taken into consideration, $t_{RST_MIN}$ and $t_{RST_MAX}$ can be calculated as Equation 4 and Equation 5, respectively.

$$t_{RST_MIN}\ (s) = 2.7558 \times C_{CRST}\ (\mu F) + 0.00045\ (s) \quad (4)$$

$$t_{RST_MAX}\ (s) = 3.8594 \times C_{CRST}\ (\mu F) + 0.00057\ (s) \quad (5)$$

The constant values of 0.00045 and 0.00057 are guaranteed by design.

When the VDD voltage is higher than $V_{DD_MIN}$ and SENSE voltage falls into the valid region ($V_{IT\ -\ UV} < V_{SENSE} < V_{IT\ +\ OV}$), the SGM850xQ begins to charge $C_{CRST}$ until $V_{CRST}$ = 1.21V. Once $V_{CRST}$ = 1.21V, $C_{CRST}$ is discharged by the internal resistor and soon nRESET is released. In order to obtain a precise $t_{RST}$, choosing high quality ceramic capacitor like C0G, X5R, X7R and placing the CRST capacitor close to the chip are both highly recommended. Table 3 presents the examples between $t_{RST}$ and ideal $C_{CRST}$.

**Table 3. Reset Delay Time for Common Ideal Capacitor Values**

| $C_{CRST}$ | $t_{RST}$ (MIN) | $t_{RST}$ (TYP) | $t_{RST}$ (MAX) |
|---|---|---|---|
| 100pF | 0.72ms | 0.82ms | 0.95ms |
| 1nF | 3.21ms | 3.72ms | 4.43ms |
| 10nF | 28ms | 32.7ms | 39ms |
| 100nF | 276ms | 323ms | 386ms |
| 1μF | 2756ms | 3220ms | 3860ms |

NOTE: Minimum and maximum values are calculated using ideal capacitors.

# APPLICATION INFORMATION (continued)

## CWD Functionality

Figure 14 shows the schematic circuits of three options of the SGM850xQ to configure the watchdog timer.

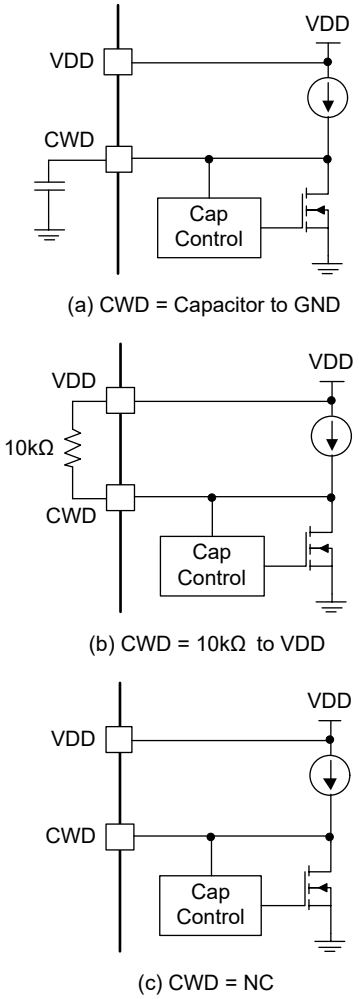



**Figure 14. CWD Configuration Circuit**

If connecting a 10kΩ pull-up resistor between the CWD pin and the VDD pin or leaving CWD pin floating (CWD = NC) is adopted, the factory-set watchdog timeouts are enabled (see Timing Requirements table). Connect a capacitor between the CWD pin and GND to set watchdog timing period using Equation 6.

### Adjustable Capacitor Timing

The windowed watchdog timing can be user-defined by connecting a capacitor to the CWD pin, then a constant current source of 375nA (TYP) begins to charge $C_{CWD}$ until $V_{CWD}$ = 1.21V (TYP). The watchdog upper boundary ($t_{WDU}$) of SGM850xQ can be calculated as Equation 6.

$$t_{WDU_TYP}\ (s) = 77.4 \times C_{CWD}\ (\mu F) + 0.055\ (s) \quad (6)$$

The capacitor $C_{CWD}$ used for the SGM850xQ is recommended to be between 100pF ($t_{WDU}$ = 62.74ms) and 1μF ($t_{WDU}$ = 77.455s). Note that Equation 6 is only accurate for ideal capacitors. Once the capacitor tolerances are considered, the obtained watchdog timeout may vary from the pre-set value. It is recommended using C0G ceramic capacitors to achieve higher accuracy. Once $t_{WDU}$ is decided by the $C_{CWD}$ capacitor, use SET0/1 to set $t_{WDL}$. Table 6 gives examples of $t_{WDU}$ under different $C_{CWD}$.

### Factory-Programmed Timing Options

Connecting a 10kΩ pull-up resistor between the CWD pin and the VDD pin or leaving CWD pin floating results in a fixed factory-set watchdog timing pattern, which is presented in detail in Table 4.

**Table 4. Factory-Programmed Watchdog Timing**

| Input | | | Watchdog Lower Boundary, $t_{WDL}$ | | | Watchdog Upper Boundary, $t_{WDU}$ | | |
|---|---|---|---|---|---|---|---|---|
| CWD | SET0 | SET1 | MIN | TYP | MAX | MIN | TYP | MAX |
| Floating | 0 | 0 | 19.1ms | 22.5ms | 25.9ms | 46.7ms | 55.0ms | 63.3ms |
| | 0 | 1 | 1.50ms | 1.88ms | 2.26ms | 23.3ms | 27.5ms | 31.7ms |
| | 1 | 0 | Watchdog disabled | | | Watchdog disabled | | |
| | 1 | 1 | 680ms | 800ms | 920ms | 1360ms | 1600ms | 1840ms |
| 10kΩ to VDD | 0 | 0 | 7.43ms | 8.8ms | 10.07ms | 93.5ms | 110.0ms | 126.5ms |
| | 0 | 1 | 7.43ms | 8.8ms | 10.07ms | 165.7ms | 195.0ms | 224.3ms |
| | 1 | 0 | Watchdog disabled | | | Watchdog disabled | | |
| | 1 | 1 | 1.50ms | 1.88ms | 2.26ms | 9.56ms | 11.3ms | 12.94ms |

# APPLICATION INFORMATION (continued)

**Table 5. $t_{WDU}$ Values for Common Ideal Capacitor Values**

| $C_{CRST}$ | $t_{WDU}$ (MIN) | $t_{WDU}$ (TYP) | $t_{WDU}$ (MAX) |
|---|---|---|---|
| 100pF | 55.5ms | 62.74ms | 71.65ms |
| 1nF | 117.2ms | 132.4ms | 151.2ms |
| 10nF | 734ms | 829ms | 947ms |
| 100nF | 6898ms | 7795ms | 8902ms |
| 1μF | 68547ms | 77455ms | 88453ms |

NOTE: Minimum and maximum values are calculated using ideal capacitors.

**Table 6. Programmable CWD Timing**

| Input | | | Watchdog Lower Boundary, $t_{WDL}$ (s) | | | Watchdog Upper Boundary, $t_{WDU}$ (s) | | |
|---|---|---|---|---|---|---|---|---|
| CWD | SET0 | SET1 | MIN | TYP | MAX | MIN (2) | TYP (1) | MAX (2) |
| $C_{CWD}$ | 0 | 0 | $t_{WDU_MIN}$ × 0.125 | $t_{WDU}$ × 0.125 | $t_{WDU_MAX}$ × 0.125 | 0.885 × $t_{WDU_TYP}$ | $t_{WDU_TYP}$ | 1.142 × $t_{WDU_TYP}$ |
| | 0 | 1 | $t_{WDU_MIN}$ × 0.75 | $t_{WDU}$ × 0.75 | $t_{WDU_MAX}$ × 0.75 | 0.885 × $t_{WDU_TYP}$ | $t_{WDU_TYP}$ | 1.142 × $t_{WDU_TYP}$ |
| | 1 | 0 | Watchdog disabled | | | Watchdog disabled | | |
| | 1 | 1 | $t_{WDU_MIN}$ × 0.5 | $t_{WDU}$ × 0.5 | $t_{WDU_MAX}$ × 0.5 | 0.885 × $t_{WDU_TYP}$ | $t_{WDU_TYP}$ | 1.142 × $t_{WDU_TYP}$ |

NOTES:

1. Calculated from Equation 6 using ideal capacitors.
2. The $t_{WDU_MIN}$ and $t_{WDU_MAX}$ include $I_{CWD}$ and $V_{CWD}$ minimum to maximum variation

## Adjustable SENSE Configuration

When no variant of the SGM850xQ meets the user threshold requirements, the practice that placing an external resistor divider outside the SENSE pin for SGM850B-0.4Q is a good choice. Table 7 presents how to use different combinations of resistors to achieve the needed threshold voltage. Note that a larger resistor value for the outside resistor divider helps reduce the overall current consumption at the cost of worse detection accuracy. Hence, a tradeoff is made that the current flowing through $R_2$ is 100 times larger than that flowing into the device. The relationship between the divider resistor and the monitor voltage is described in Equation 7 and the structure pattern for user-defined threshold voltage is illustrated in Figure 15.

$$V_{MON} = V_{IT_ADJ} \times (1 + R_1/R_2) \quad (7)$$

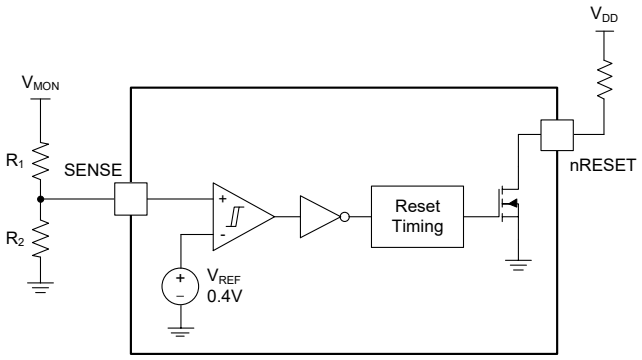



**Figure 15. Adjustable Voltage Divider**

**Table 7. SENSE Resistor Divider Values**

| Input Voltage (V) | 4% Threshold | | | 10% Threshold | | |
|---|---|---|---|---|---|---|
| | $R_1$ (kΩ) | $R_2$ (kΩ) | Threshold Voltage (V) | $R_1$ (kΩ) | $R_2$ (kΩ) | Threshold Voltage (V) |
| 0.5 | 16.2 | 80.6 | 0.48 | 10 | 80.6 | 0.45 |
| 0.8 | 75 | 80.6 | 0.77 | 64.9 | 80.6 | 0.72 |
| 0.9 | 93.1 | 80.6 | 0.86 | 82.5 | 80.6 | 0.81 |
| 1.2 | 150 | 80.6 | 1.14 | 137 | 80.6 | 1.08 |
| 1.8 | 267 | 80.6 | 1.73 | 249 | 80.6 | 1.64 |
| 2.5 | 402 | 80.6 | 2.40 | 374 | 80.6 | 2.26 |
| 3 | 499 | 80.6 | 2.88 | 464 | 80.6 | 2.70 |
| 3.3 | 562 | 80.6 | 3.19 | 523 | 80.6 | 2.99 |
| 5 | 887 | 80.6 | 4.80 | 825 | 80.6 | 4.49 |
| 12 | 2260 | 80.6 | 11.62 | 2100 | 80.6 | 10.82 |

# APPLICATION INFORMATION (continued)

### Overdrive on the SENSE Pin

The SGM850xQ can suppress short spikes or glitches on the SENSE pin. The immunity ability is decided by the duration time and overdrive voltage.

When $V_{SENSE}$ is lower than the trip point for a long time, then the nRESET is asserted and the output is pulled low. When $V_{SENSE}$ is just a few nanoseconds lower than the trip point, the nRESET does not assert and the output continues to be high. Alter the time length that asserts the nRESET by increasing the proportion where $V_{SENSE}$ is lower than the trip point. For example, when $V_{SENSE}$ is 10% lower than the trip point, the comparator responds much faster and the nRESET is asserted much quicker than when just below the trip point voltage. Calculation of the overdrive percentage is shown in Equation 8.

$$\text{Overdrive} = |(V_{SENSE}/V_{ITx} - 1) \times 100\%| \quad (8)$$

In Equation 8, $V_{ITx}$ can be the OV threshold of $V_{IT+OV}$ or UV threshold of $V_{IT-UV}$. In Figure 16, $t_1$ and $t_2$ denote the maximum time that nRESET holds its state and does not respond to the OV/UV overdrive.

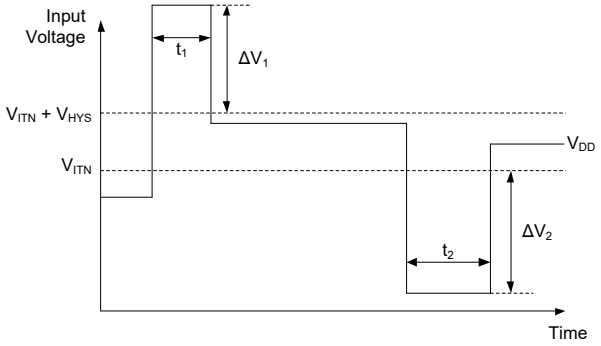



**Figure 16. Overdrive Voltage on the SENSE Pin**

## Monitoring a 1.2V Rail with Factory-Programmable Watchdog Timing

Figure 17 illustrates how the SGM850A-1.2Q is used to supervise the $V_{CORE}$ voltage of 1.2V for the MCU.

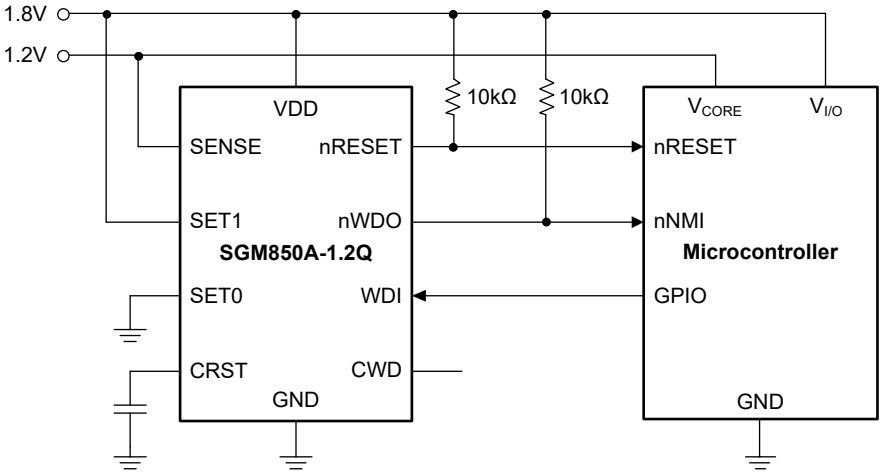



**Figure 17. Monitoring Supply Voltage and Watchdog Supervision of a Microcontroller**

### Design Requirements

**Table 8. Design Parameters**

| Parameter | Design Requirement | Design Result |
|---|---|---|
| Reset Delay | $t_{RST} \geq 250ms$ | $t_{RST_MIN} = 260ms$, $t_{RST_TYP} = 322ms$ |
| Watchdog Window | Functions with a 200Hz pulse-width modulation (PWM) signal with a 50% duty cycle | $t_{WDU_MIN} = 23.3ms$ and $t_{WDL_MAX} = 2.26ms$ under the condition that CWD = NC, SET0 = 0 and SET1 = 1 |
| Output Logic Voltage | 1.8V CMOS | 1.8V CMOS |
| Monitored Rail | 1.2V within ±5.5% | $V_{IT+OV_MAX} = 1.2648V$ (5.4%) |
| | | $V_{IT-UV_MIN} = 1.1352V$ (-5.4%) |
| Maximum Device Current Consumption | $I_{DD} \leq 200\mu A$ | $I_{DD_TYP} = 10\mu A$ and $I_{DD_MAX} = 190\mu A$ when nWDO or nRESET is asserted |

# APPLICATION INFORMATION (continued)

## Detailed Design Procedure

### *Monitoring the 1.2V Rail*

Considering 1.2V is one of the threshold variants and ±5.5% tolerance is usually needed for the MCU power rail, choose SGM850A-1.2Q is suitable. Furthermore, when the device detection accuracy is taken into consideration, maximum OV threshold ($V_{IT+\ (OV\text{-}Worst\ Case)}$) and minimum UV threshold ($V_{IT-\ (UV\text{-}Worst\ Case)}$) can be calculated as:

$$V_{IT+\ (OV\text{-}Worst\ Case)} = V_{IT+\ OV\ (TYP)} \times 1.054$$
$$= 1.2 \times 1.054 = 1.2648V \quad (9)$$

$$V_{IT-\ (UV\text{-}Worst\ Case)} = V_{IT-\ UV\ (TYP)} \times 0.946$$
$$= 1.2 \times 0.946 = 1.1352V \quad (10)$$

### *Meeting the Minimum Reset Delay*

Note that $t_{RST}$ under CRST = NC or CRST = VDD of the SGM850A-1.2Q does not meet the minimum reset delay requirements. As a consequence, taking a capacitor at the CRST pin to employ the needed $t_{RST}$ is necessary. The ideal minimum $C_{CRST}$ can be obtained by solving Equation 11 with ambient temperature from -40℃ to +125℃ considered:

$$C_{CRST_MIN_IDEAL}(\mu F) = \frac{t_{CRST_MIN} - 0.00045}{2.7558}$$
$$= \frac{0.25 - 0.00045}{2.7558} = 0.091\mu F \quad (11)$$

With Equation 11 listed above, the ideal $C_{CRST_MIN}$ can be calculated as 0.091μF. When the capacitor variation of ±10% is taken into account, then $C_{CRST_MIN}$ can be deduced as in Equation 12:

$$C_{CRST_MIN} = \frac{t_{CRST_MIN_IDEAL}}{1 - C_{TOLERANCE}} = \frac{0.091\mu F}{1 - 0.1} = 0.101\mu F \quad (12)$$

With Equation 12 listed above, $C_{CRST_MIN}$ can be calculated as 0.101μF. After that, the calculated $C_{CRST}$ should be rounded to a real capacitance. For example, a 0.1μF capacitor is advisable. It should be paid attention to that the DC characteristics and temperature characteristics of a capacitor have some influence to the final value.

### *Setting the Watchdog Window*

The basic rule to select the suitable $t_{WDU_MIN}$ and $t_{WDL_MAX}$ is to choose the appropriate combination of CWD, SET0 and SET1. The first step is to choose $t_{WDU_MIN}$ larger than the PWM period of 5ms (between two falling edges). Usually, a factory-set $t_{WDU_MIN}$ with CWD = NC or CWD = VDD is more popular because of less external components used. Here, CWD = NC with SET0 = 0 and SET1 = 1 is employed. As a result, $t_{WDL_MAX}$ = 2.26ms and $t_{WDU_MIN}$ = 23.3ms is yielded.

### *Calculating the nRESET and nWDO Pull-up Resistor*

The nRESET and nWDO pin are both open-drain outputs, as shown in Figure 18. How to choose an appropriate pull-up resistor has been described in detail in nRESET section. A tradeoff is made between the low level output voltage $V_{OL}$ and the current flowing into the nRESET and nWDO pin ($I_{RST}$ and $I_{WDO}$). The constraint for $V_{OL}$ is lower than 0.4V and for $I_{RST}$ and $I_{WDO}$ is lower than 10mA. Note that every time only one of nRESET and nWDO will be pulled low. Thus, only the current flowing through one pull-up resistor should be considered. For example, when the power rail pulled up to is 1.8V, the pull-up resistor should be less than 9.47kΩ. Take the pull-up resistor as 10kΩ, the obtained maximum total current consumption is 190μA.

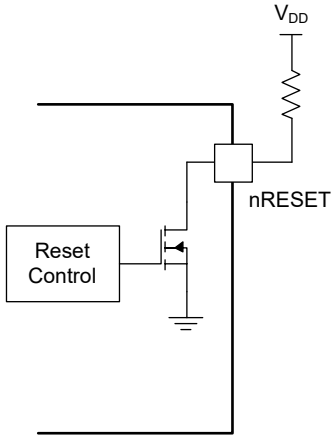


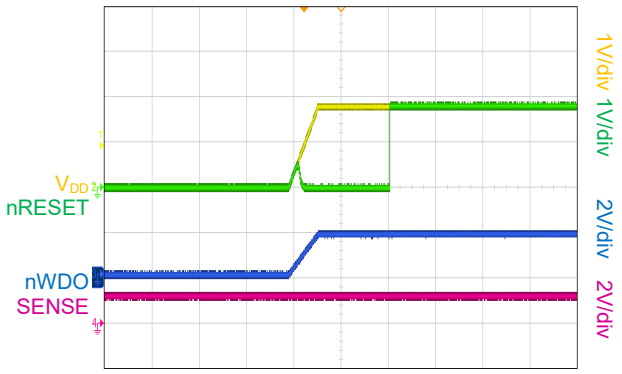

**Figure 18. Open-Drain nRESET Configuration**

# APPLICATION INFORMATION (continued)

## Application Curves

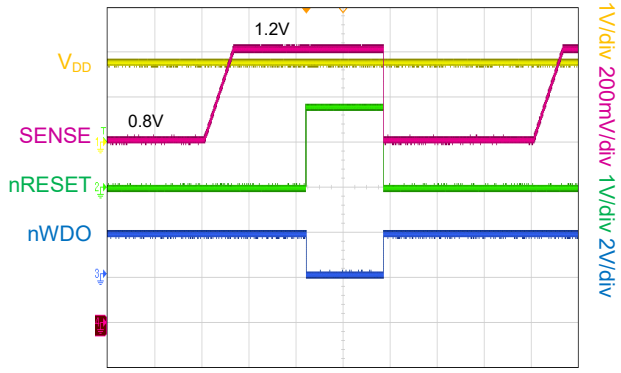
$T_A$ = +25℃, unless otherwise noted.

Startup Waveform



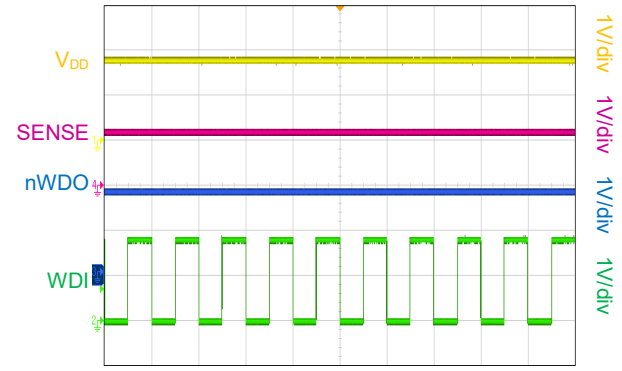

Time (200ms/div)

Window Comparator Thresholds Entering a Valid Window



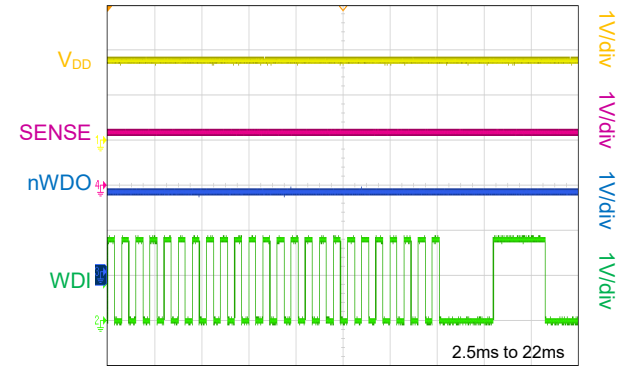

Time (200ms/div)

200Hz WDI Pulse



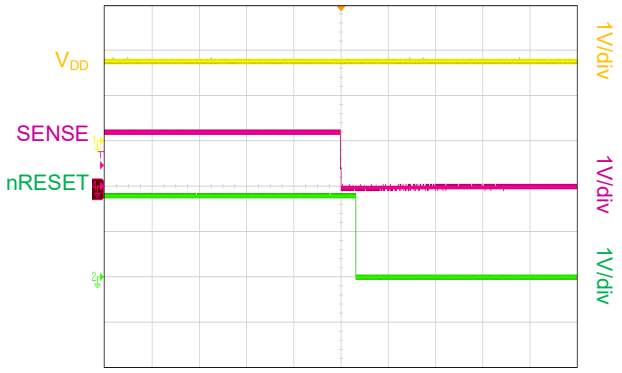

Time (5ms/div)

Window Watchdog Timing




Time (10ms/div)

Typical nRESET Delay Timing




Time (20μs/div)

# APPLICATION INFORMATION (continued)

## Using SGM850B-0.4Q to monitor a 0.7V Rail with an Adjustable Window Watchdog Timing

A typical application for the SGM850B-0.4Q is shown in Figure 19.

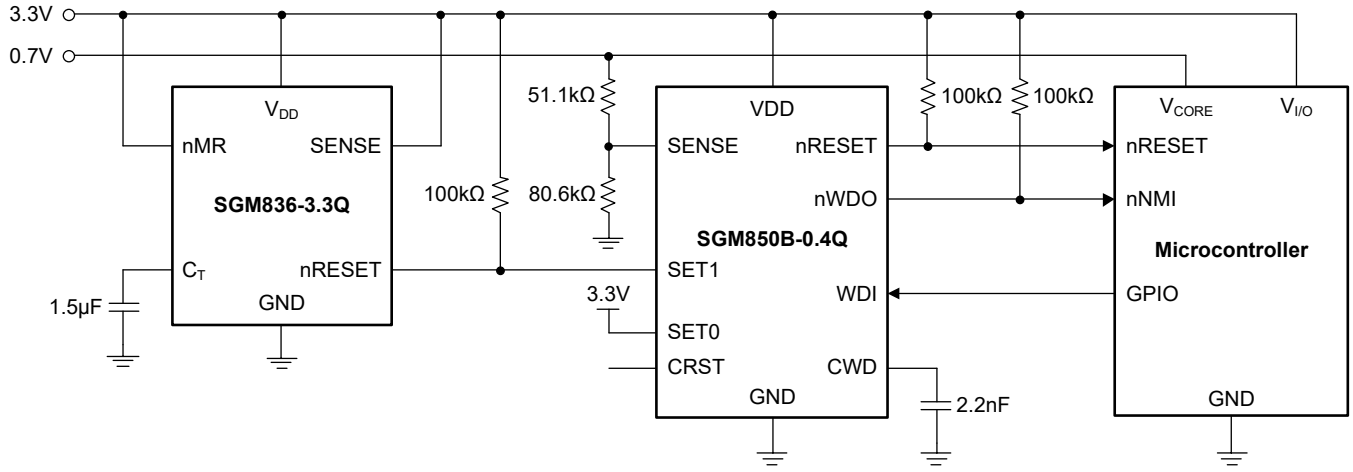



**Figure 19. Monitoring Supply Voltage and Watchdog Supervision of a Microcontroller**

## Design Requirements

**Table 9. Design Parameters**

| Parameter | Design Requirement | Design Result |
|---|---|---|
| Reset Delay | Minimum reset delay of 150ms | Minimum reset delay of 170ms |
| Watchdog Disable for Initialization Period | Watchdog must remain disabled for 7s until logic enables the watchdog timer | 7.87s (TYP) |
| Watchdog Window | 250ms, maximum | $t_{WDL_MAX}$ = 128.63ms, $t_{WDU_MIN}$ = 199.37ms |
| Output Logic Voltage | 3.3V CMOS | 3.3V CMOS |
| Monitored Rail | 0.7V, with 7% threshold | $V_{ITN_MAX}$ 0.67V (-4.7%) |
| | | $V_{ITN_TYP}$ 0.65V (-6.6%) |
| | | $V_{ITN_MIN}$ 0.641V (-8.5%) |
| Maximum Device Current Consumption | 50μA | 10μA of current consumption typical, worst-case of 52μA when WDO or nRESET is asserted (1) |

NOTE: 1. Only includes the current consumption of the SGM850xQ.

## Detailed Design Procedure

### *Meeting the Minimum Reset Delay*

Note that $t_{RST}$ under CRST = NC of the SGM850B-0.4Q just meets the minimum reset delay requirement. As a consequence, taking a floating state at the CRST pin benefits the user for less outside components.

### *Setting the Window Watchdog*

It has been described in Figure 14 that three configurations can be employed for the CWD pin. Considering that only a maximum window of 250ms is required, a user-defined $t_{WDU_MIN}$ and $t_{WDL_MAX}$ is more suitable. With known $t_{WDU_MIN}$ in mind, the ideal $C_{CWD}$ can be calculated with Equation 13.

$$C_{CWD_IDEAL}(\mu F) = \frac{t_{WDU} - 0.055}{77.4}$$
$$= \frac{0.25 - 0.055}{77.4} = 0.0025\mu F \quad (13)$$

Then round the obtained $C_{CWD}$ to 2.2nF. After that, calculate $t_{WDU_MIN}$ and $t_{WDL_MAX}$ based on Table 5.

$$t_{WDU_MIN}\,(ms) = 0.885 \times t_{WDU_TYP}\,(ms) =$$
$$0.885 \times (77.4 \times 2.2 \times 10^{-3} + 0.055) = 199.37ms \quad (14)$$

$$t_{WDL_MAX}\,(ms) = 0.5 \times 1.142 \times t_{WDU_MAX}\,(ms) =$$
$$0.5 \times 1.142 \times \left(1.05 \times 77.4 \times 2.2 \times 10^{-3} + 0.055\right)$$
$$= 128.63ms \quad (15)$$

## APPLICATION INFORMATION (continued)

It should be noted that capacitance variation, DC characteristics and temperature characteristics of $C_{CWD}$ have effect on the final performance. As for the capacitor dielectric, the C0G ceramic capacitor is highly recommended.

***Watchdog Disabled during the Initialization Period***

Usually, the watchdog is disabled in the initialization process of an MCU to avoid undesired errors. It has been mentioned above that the watchdog is disabled under SET0 = 1 and SET1 = 0. In this application, SET0 is connected to the VDD pin of the SGM850B-0.4Q and the SGM836-3.3Q is adopted to pull down the SET1 pin for a period over 7s. To realize the reset delay time of 7s for the SGM836-3.3Q, a 1.5μF $C_T$ capacitor is adopted, resulting in a delay time of 7.87s. Relative waveforms for the circuit depicted in Figure 19.

***Calculating the Sense Resistor***

With the known SENSE pin voltage threshold ($V_{IT_ADJ}$) and SENSE pin idle current ($I_{SENSE}$) kept in mind, one can calculate the resistor divider value as follows. Note that larger resistor value for the outside resistor divider helps reduce the overall current consumption at the cost of worse detection accuracy. Hence, a tradeoff is made that the current flowing through $R_2$ is 100 times larger than that flowing into the device. Given that 80.6kΩ of $R_2$ yields a 5μA current consumption. Hence, the supervised voltage falling threshold can be calculated as:

$$V_{ITN} = V_{IT_ADJ} + R_1 \times \frac{V_{IT_ADJ}}{R_2} \quad (16)$$

where:

$V_{ITN}$ is the monitored falling threshold voltage and $V_{IT_ADJ}$ = 0.4V is the threshold voltage on the SENSE pin.

Substituting $V_{ITN}$ = 0.65V into Equation 16 yields $R_1$ = 51.1kΩ.

Take the variation of resistor, threshold voltage and current flowing into the SENSE pin, $V_{ITN_MIN}$ and $V_{ITN_MAX}$ can be calculated as:

$$V_{ITN_MIN} = V_{IT_ADJ_MIN} + R_{1_MIN} \times \left( \frac{V_{IT_ADJ_MIN}}{R_{2_MAX}} + I_{SENSE_MIN} \right) = 0.641V \quad (17)$$

$$V_{ITN_MAX} = V_{IT_ADJ_MAX} + R_{1_MAX} \times \left( \frac{V_{IT_ADJ_MAX}}{R_{2_MIN}} + I_{SENSE_MAX} \right) = 0.67V \quad (18)$$

where:

$V_{ITN}$ is the falling monitored threshold voltage

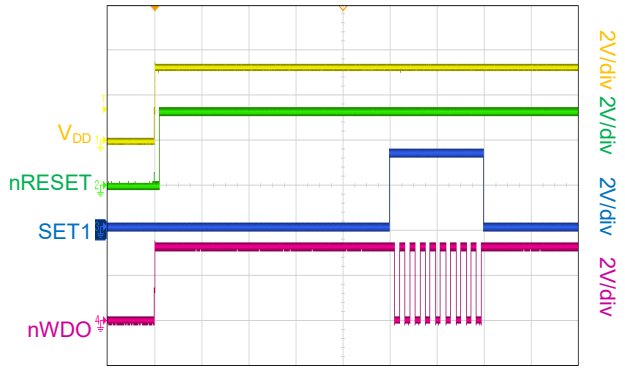
$V_{IT_ADJ}$ is the sense voltage threshold and

$I_{SENSE}$ is the sense pin current

The calculated tolerance on $R_1$ and $R_2$ is 1%.

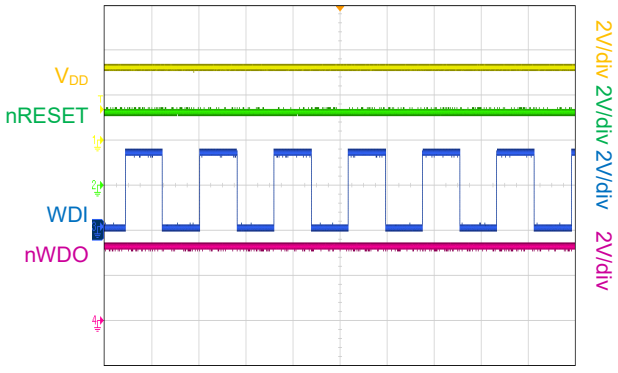
### Application Curves

Startup without a WDI Signal




Time (2s/div)

Typical WDI Signal




Time (10ms/div)

# APPLICATION INFORMATION (continued)

## Power Supply Recommendations

This device is configured to function normally with an input voltage ranging from 1.6V to 6.5V. Note that incorporating a capacitor ranging from 0.1μF to 1μF between the VDD and GND pins is advisable, depending on the noise characteristics of the input voltage supply.

## Layout Guidelines

Though not mandatory, placing a 0.1μF ceramic capacitor close to the VDD pin is recommended to suppress the noise or transient spikes.

Place $C_{CRST}$ or the pull-up resistor as close as possible to the CRST pin. If a capacitor is not connected to the CRST pin, then reducing parasitic capacitance on this pin leads to a more accurate nRESET delay time.

Place $C_{CWD}$ or the pull-up resistor as close as possible to the CWD pin.

Place the pull-up resistors for nRESET and nWDO pins as close to the corresponding pin as possible.

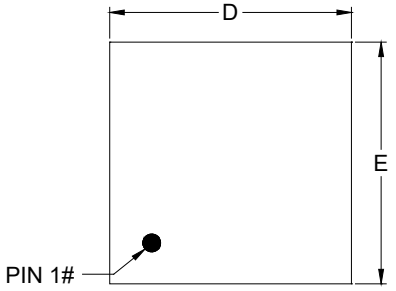
# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

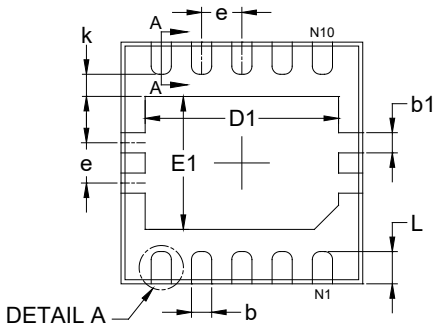
| Changes from Original (DECEMBER 2024) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

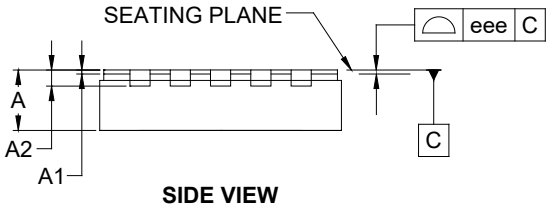
## TDFN-3×3-10BL



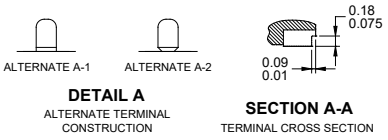

TOP VIEW




BOTTOM VIEW

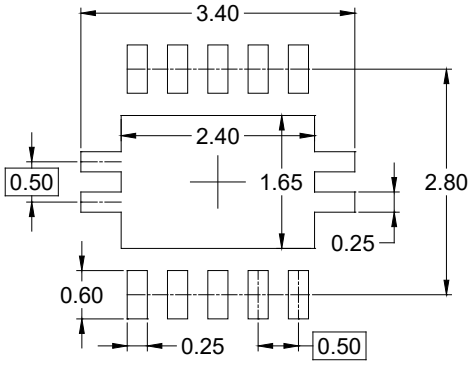



SIDE VIEW




**DETAIL A**
ALTERNATE TERMINAL CONSTRUCTION

**SECTION A-A**
TERMINAL CROSS SECTION



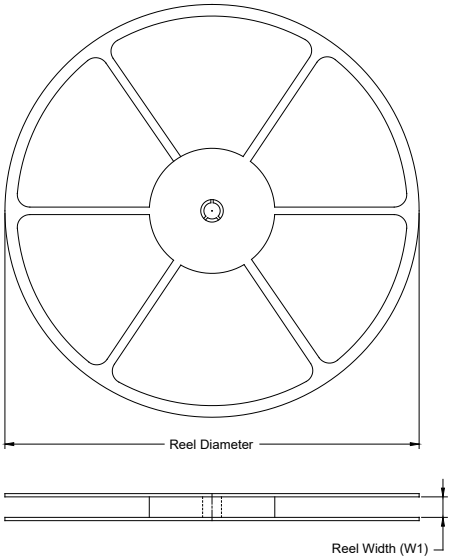

**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.700 | - | 0.800 |
| A1 | 0.000 | - | 0.050 |
| A2 | | 0.203 REF | |
| b | 0.200 | - | 0.300 |
| b1 | | 0.250 REF | |
| D | 2.900 | - | 3.100 |
| D1 | 2.300 | - | 2.500 |
| E | 2.900 | - | 3.100 |
| E1 | 1.550 | - | 1.750 |
| e | | 0.500 BSC | |
| k | | 0.275 REF | |
| L | 0.300 | - | 0.500 |
| eee | | 0.080 | |

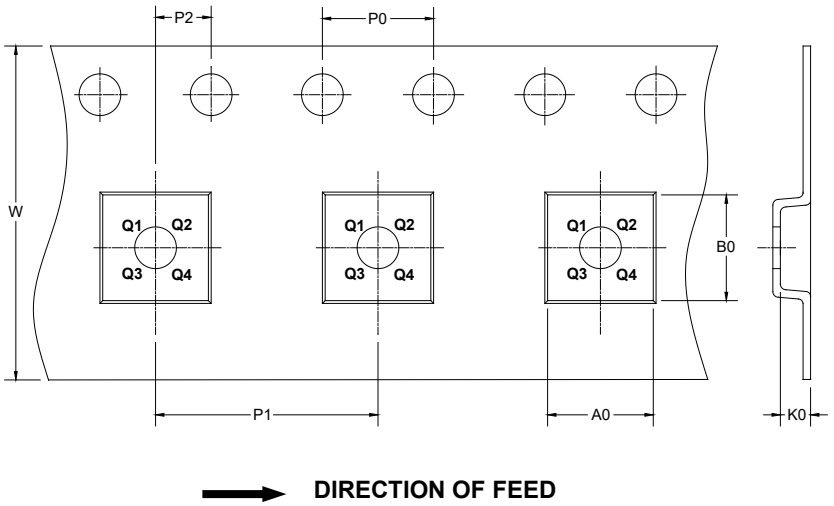
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



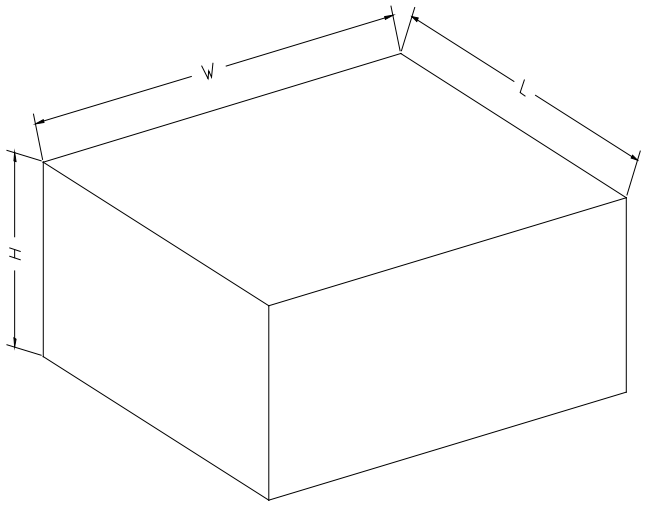

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TDFN-3×3-10BL | 13" | 12.4 | 3.35 | 3.35 | 1.13 | 4.0 | 8.0 | 2.0 | 12.0 | Q2 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

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