SGM61451AQ/SGM61451BQ
Automotive
40V, 5A Buck Converter with 47μA I_Q

GENERAL DESCRIPTION

The SGM61451xQ is a frequency programmable, internally compensated, Buck regulator with an integrated high-side MOSFET. It provides up to 5A output current capability over a wide input range from 4V to 40V, which accommodates a variety of Buck applications in an automotive input environment. Only 47μA (TYP) sleep-mode quiescent current makes the SGM61451xQ suitable for battery powered systems. An ultra-low 2.1μA (TYP) shutdown current can further prolong battery life.

The SGM61451xQ uses peak-current mode control with constant switching frequency to provide optimal output voltage accuracy and fast loop response. Switching frequency is widely adjustable, which enables optimization of either efficiency or solution size. Internal loop compensation makes it easy to use and eliminates many external components. Frequency spread spectrum version (SGM61451BQ) is also available for reducing EMI.

The SGM61451xQ employs adjustable soft-start time to prevent high start-up inrush current. An enable pin is provided for simplification of on/off control and system power sequencing. Protection features include thermal shutdown, input under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The device is available in Green TDFN-4×4-10AL and SOIC-8 (Exposed Pad) packages.

APPLICATIONS

General Purpose Automotive Battery Regulation
Automotive ADAS or Surround View
Cluster and Infotainment
Telematics Control Unit

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Wide Input Voltage Range: 4V to 40V**
- **High Continuous Output Current: Up to 5A**
- **Ultra-Low Quiescent Current: 47μA (TYP)**
- **Ultra-Low Shutdown Current: 2.1μA (TYP)**
- **Integrated High-side MOSFET:**
  - **TDFN Package: 90mΩ**
  - **SOIC Package: 80mΩ**
- **Adjustable Switching Frequency: 200kHz to 2.5MHz**
- **Frequency Synchronization for External Clock**
- **Reduced EMI Spread Spectrum Options:**
  - **SGM61451AQ: No Spread Spectrum**
  - **SGM61451BQ: Spread Spectrum**
- **Peak Current Mode Control**
- **Internal Compensation for Ease of Use**
- **Support High Duty Cycle Operation**
- **Precision Enable Input**
- **Adjustable Soft-Start Time**
- **Available in Green TDFN-4×4-10AL and SOIC-8 (Exposed Pad) Packages**

TYPICAL APPLICATION

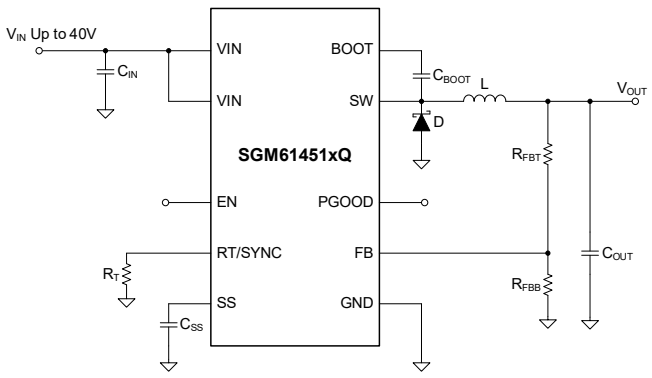


Figure 1. Typical Application Circuit

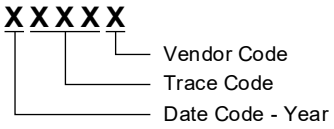
代理商 威尔迈 www.viswic.com 联系电话 138 2526 5270

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61451AQ	TDFN-4×4-10AL	-40℃ to +125℃	SGM61451AQTHH10G/TR	0GCTHH10 XXXXX	Tape and Reel, 3000
	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61451AQPS8G/TR	0G8PS8 XXXXX	Tape and Reel, 4000
SGM61451BQ	TDFN-4×4-10AL	-40℃ to +125℃	SGM61451BQTHH10G/TR	0GKTHH10 XXXXX	Tape and Reel, 3000
	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61451BQPS8G/TR	0GDPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- VIN, EN to GND ..... -0.3V to 44V
- BOOT to GND ..... -0.3V to 49V
- SS to GND ..... -0.3V to 5V
- FB to GND ..... -0.3V to 6V
- RT/SYNC to GND ..... -0.3V to 3.6V
- PGOOD to GND ..... -0.3V to 6V

Output Voltage
- BOOT to SW 6V
- SW to GND ..... -3V to 44V

Package Thermal Resistance
- TDFN-4×4-10L, θ_{JA} ..... 31.4℃/W
- TDFN-4×4-10L, θ_{JB} ..... 10.8℃/W
- TDFN-4×4-10L, $\theta_{JC\ (TOP)}$ ..... 24.9℃/W
- TDFN-4×4-10L, $\theta_{JC\ (BOT)}$ ..... 2.8℃/W
- SOIC-8 (Exposed Pad), θ_{JA} ..... 38.9℃/W
- SOIC-8 (Exposed Pad), θ_{JB} ..... 12.3℃/W
- SOIC-8 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 46.9℃/W
- SOIC-8 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 1.5℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

RECOMMENDED OPERATING CONDITIONS

Buck Regulator
- VIN ..... 4V to 40V
- VOUT ..... 0.8V to 28V
- BOOT 45V
- SW ..... -1V to 40V
- FB ..... 0V to 5V

Control
- EN ..... 0 to 40V
- RT/SYNC ..... 0V to 3.3V
- SS ..... 0V to 3V
- PGOOD to GND ..... 0V to 5V

Switching Frequency Range
- RT Mode ..... 200kHz to 2500kHz
- SYNC Mode ..... 250kHz to 2300kHz

Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

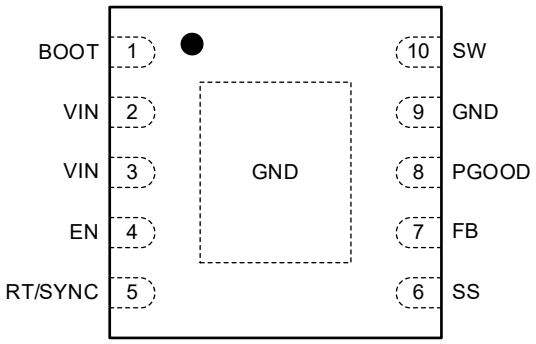
SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

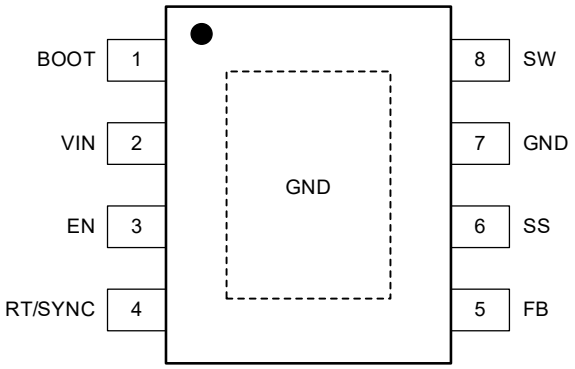
PIN CONFIGURATIONS

(TOP VIEW)



TDFN-4×4-10AL

(TOP VIEW)



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
TDFN	SOIC			
1	1	BOOT	P	Bootstrap Supply Voltage for Internal High-side Driver. Connect a high-quality 100nF capacitor as close as possible to the IC between this pin and the SW pin.
2, 3	2	VIN	P	Input Supply to Regulator. Connect to a 4V to 40V power source.
4	3	EN	A	Enable Input to Regulator. Pull this pin below the low threshold to shut the chip down. Pull it above the high threshold or float enables the chip. This pin can be connected to VIN pin via a resistor if the shutdown feature is not required or to a resistor divider to adjust UVLO threshold.
5	4	RT/SYNC	A	Resistor Timing or External Clock Input. Connect an external resistor between this pin and the ground to set the switching frequency or connect the pin to a synchronization clock.
6	6	SS	A	Soft-Start Control Pin. Connect a capacitor to this pin to set soft-start time.
7	5	FB	A	Feedback Input to Regulator. Connect to tap point of feedback voltage divider. Do not float. Do not ground.
8	—	PGOOD	A	Open-Drain Power Good Flag Output. Connect to suitable voltage supply through a 10kΩ to 100kΩ resistor. Can be left open when not used.
9	7	GND	G	Power and Analog Ground Terminal. Ground reference for internal references, logic and regulated output voltage. For the reason, care must be taken in PCB layout.
10	8	SW	P	Switching Output of The Regulator. A high-side power MOSFET is internally connected to this pin. Connect to power inductor and bootstrap capacitor.
Exposed Pad		GND	G	Thermal Exposed Pad. Connected this pin to ground plane on PCB. It is the main thermal relief path for the die.

NOTE: A = Analog, P = Power, G = Ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 4V to 40V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_{IN} = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply (VIN Pin)							
Operating Input Voltage	V_{IN}			4		40	V
Under-Voltage Lockout Threshold	V_{UVLO}	Rising threshold		3.5	3.7	4	V
Under-Voltage Lockout Threshold Hysteresis	V_{UVLO_HYS}				320		mV
Shutdown Supply Current	I_{SD}	V_{EN} = 0V, T_J = +25℃, V_{IN} = 4V to 40V			2.1	5	μA
Operating Quiescent Current (Non-Switching)	I_Q	V_{FB} = 1V		25	47	65	μA
Enable (EN Pin)							
Enable Threshold Voltage	V_{EN_TH}	V_{EN} rising		1.11	1.20	1.38	V
Enable Hysteresis Threshold Voltage	V_{EN_HYS}	Hysteresis voltage			80		mV
Enable Pin Current	I_{EN_PIN}	Enable rising threshold +50mV			-4.4		μA
		Enable falling threshold -50mV			-0.9		
Enable Hysteresis Current	I_{EN_HYS}	Rising threshold			-3.5		μA
External Soft-Start (SS Pin)							
SS Pin Current	I_{SS}	T_J = +25℃			-3		μA
Power Good (PGOOD Pin) (1)							
Power Good Flag Under-Voltage Tripping Threshold	V_{PG_UV}	% of V_{REF}	Power good		94		%
			Power bad		91		
Power Good Flag Over-Voltage Tripping Threshold	V_{PG_OV}	% of V_{REF}	Power bad		109		%
			Power good		105		
Power Good Flag Recovery Hysteresis	V_{PG_HYS}	Under-voltage			3		%
		Over-voltage			4		
PGOOD Leakage Current at High Level Output	I_{PG}	V_{PULL_UP} = 5V			10	200	nA
PGOOD Low Level Output Voltage	V_{PG_LOW}	I_{PULL_UP} = 1mA			0.1		V
Minimum V_{IN} for Valid PGOOD Output	$V_{IN_PG_MIN}$	V_{PULL_UP} < 5V at I_{PULL_UP} = 100μA			1	1.5	V
Voltage Reference (FB Pin)							
Reference Voltage	V_{REF}	T_J = +25℃		0.740	0.750	0.768	V
		T_J = -40℃ to +125℃		0.735	0.750	0.772	
High-side MOSFET							
On-Resistance	R_{DSON}	V_{IN} = 12V, BOOT to SW = 5V, TDFN package			90	160	mΩ
		V_{IN} = 12V, BOOT to SW = 5V, SOIC package			80	150	
High-side MOSFET Current Limit							
Current Limit	I_{LIM}	T_J = +25℃, close loop, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 300kHz, L = 8.2μH		6.6	7.4	8.1	A
Thermal Performance							
Thermal Shutdown Threshold	T_{SD}				173		℃
Thermal Shutdown Hysteresis	T_{HYS}				15		℃

NOTE:

1. Valid for TDFN package only.

SWITCHING CHARACTERISTICS

(V_{IN} = 4V to 40V, T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	f_{SW}	R_T = 11.5kΩ	1860	1990	2120	kHz
Switching Frequency Range at SYNC Mode			250		2300	
Switching Frequency Dithering (1) (2)	f_{DITHER}	Spread spectrum option, frequency dithering over center frequency		±6%		
SYNC Clock High Level Threshold	V_{SYNC_H}		1.7			V
SYNC Clock Low Level Threshold	V_{SYNC_L}				0.5	V
Minimum SYNC Input Pulse Width (2)	t_{SYNC_MIN}	Measured at 500kHz, V_{SYNC_H} > 3V, $V_{SYNC\ L}$ < 0.3V		30		ns
PLL Lock in Time (2)	t_{LOCK_IN}	Measured at 500kHz		100		μs
Minimum Controllable On Time (2)	t_{ON_MIN}	V_{IN} = 26V, V_{OUT} = 5V, f_{SW} = 2.2MHz, I_{OUT} = 5A		95		ns
Maximum Duty Cycle (2)	D_{MAX}			98		%

NOTE:

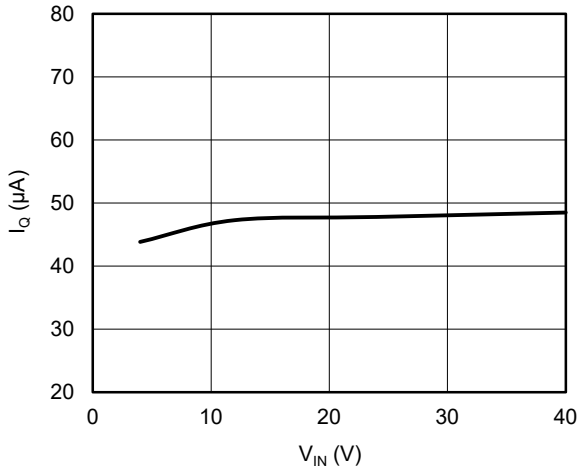
1. Valid for SGM61451BQ only.

2. Guaranteed by design, not tested in production.

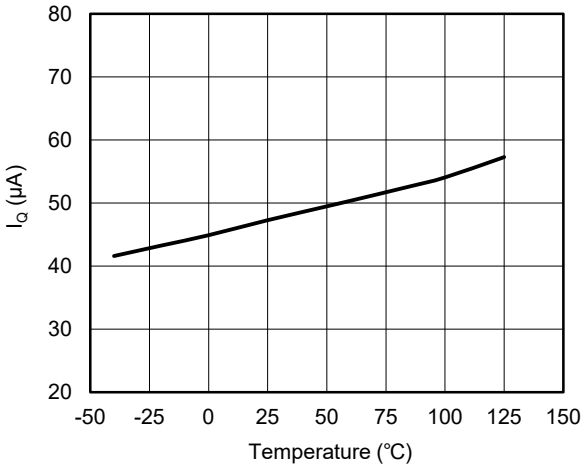
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 300kHz, L = 8.2μH, C_{OUT} = 47μF × 2, unless otherwise noted.

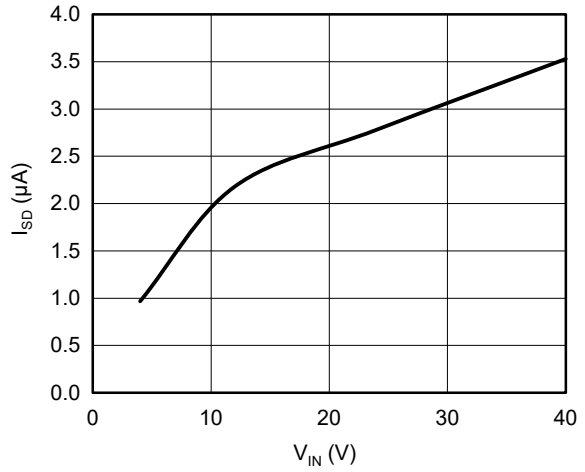
I_Q vs. V_{IN}



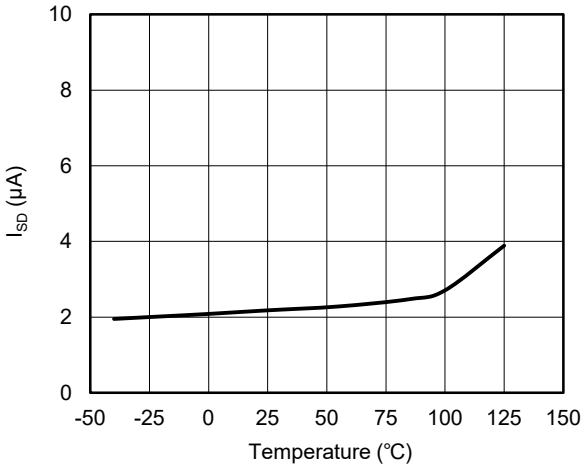
I_Q vs. Temperature



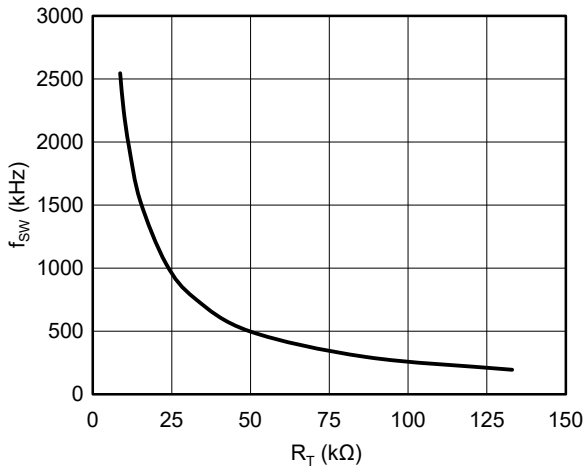
I_{SD} vs. V_{IN}



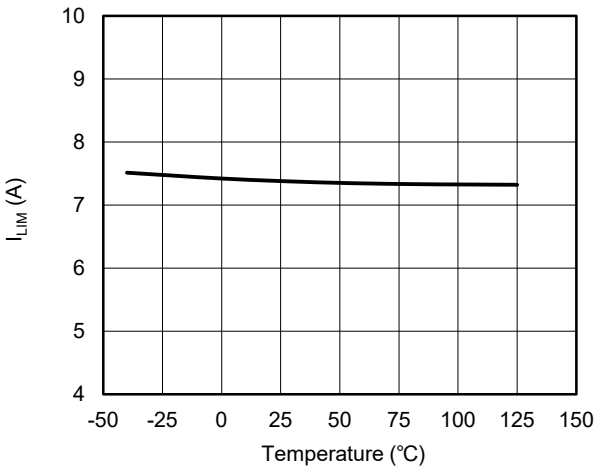
I_{SD} vs. Temperature



f_{SW} vs. R_T



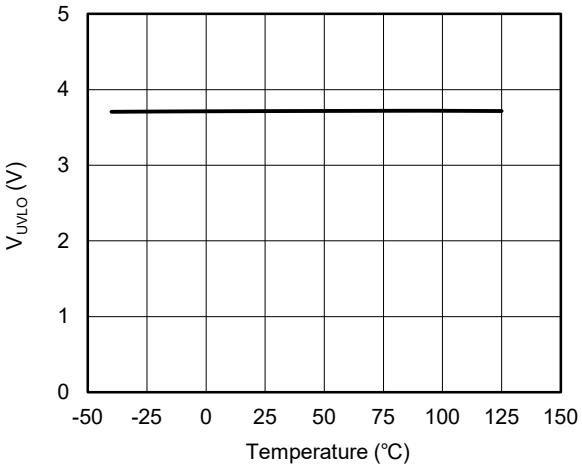
I_{LIM} vs. Temperature



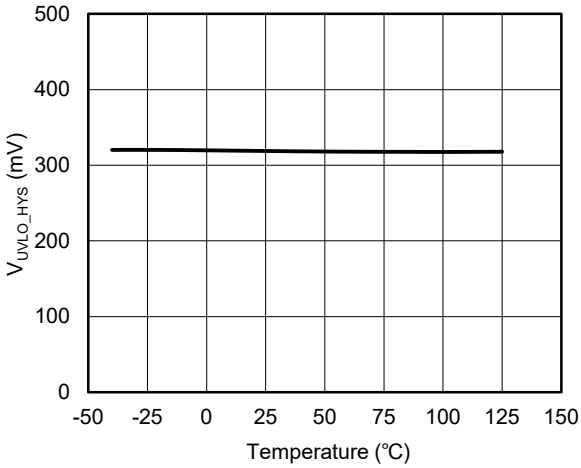
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 300kHz, L = 8.2μH, DCR = 10mΩ, C_{OUT} = 47μF × 2, unless otherwise noted.

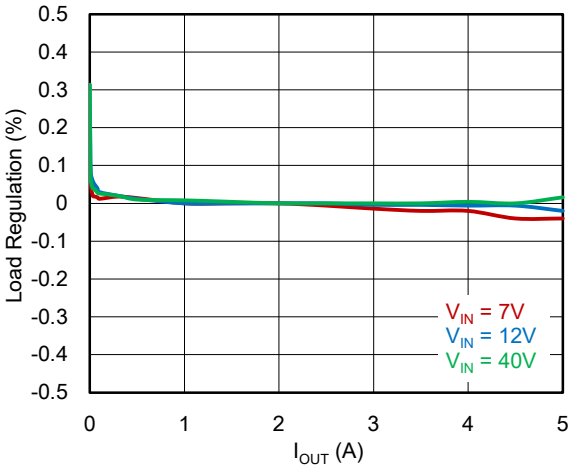
V_{UVLO} vs. Temperature



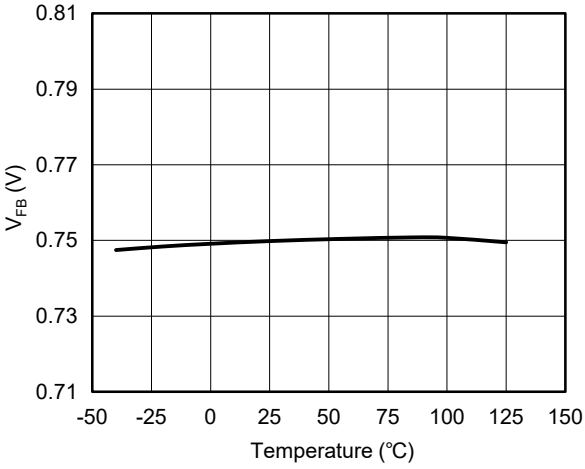
V_{UVLO_HYS} vs. Temperature



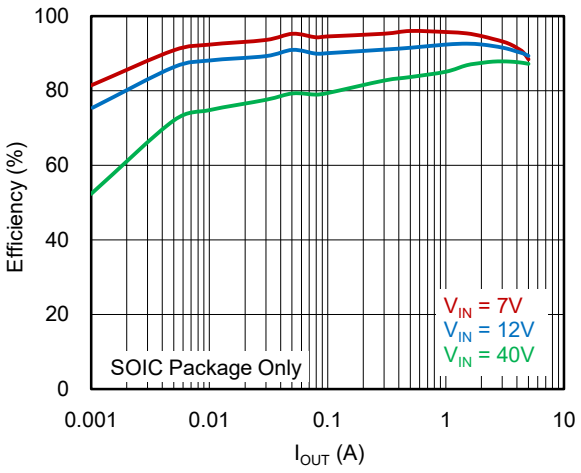
Load Regulation



V_{FB} vs. Temperature



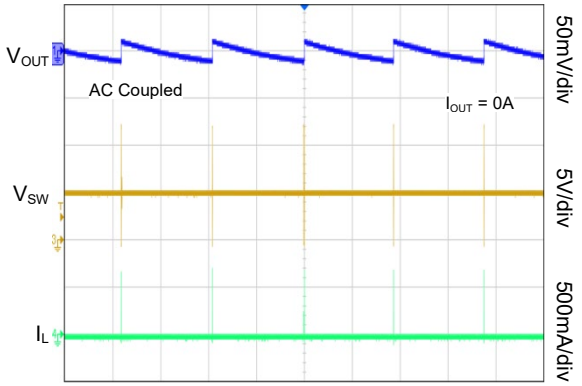
Efficiency vs. I_{OUT}



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

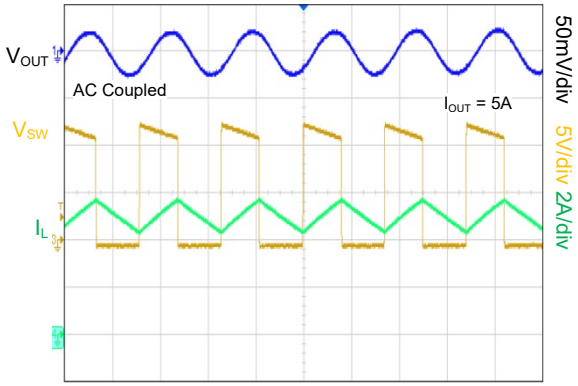
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 300kHz, L = 8.2μH, C_{OUT} = 47μF × 2, unless otherwise noted.

Steady State, PSM Mode



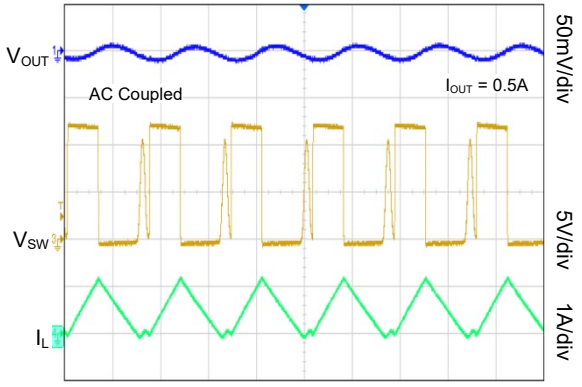
Time (5ms/div)

Steady State, CCM Mode



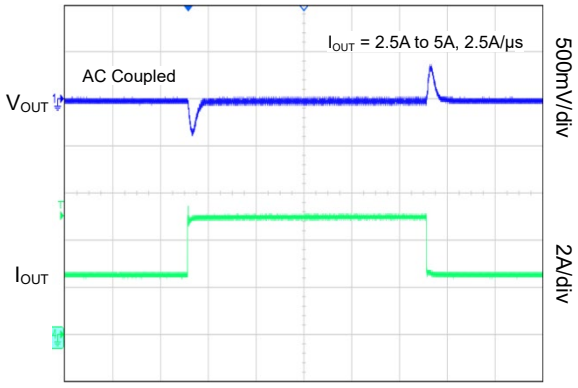
Time (2μs/div)

Steady State, DCM Mode



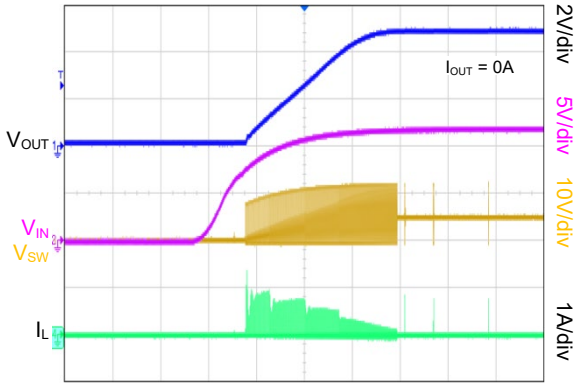
Time (2μs/div)

Load Transient



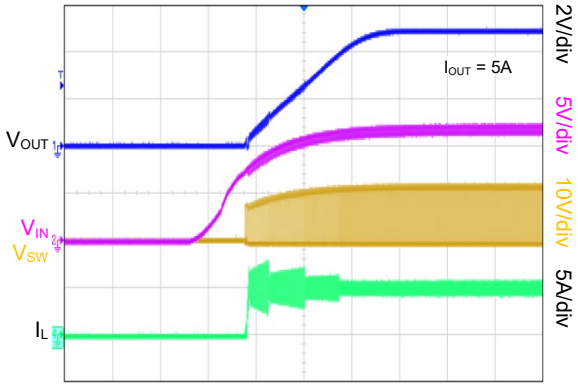
Time (100μs/div)

Start by VIN



Time (2ms/div)

Start by VIN

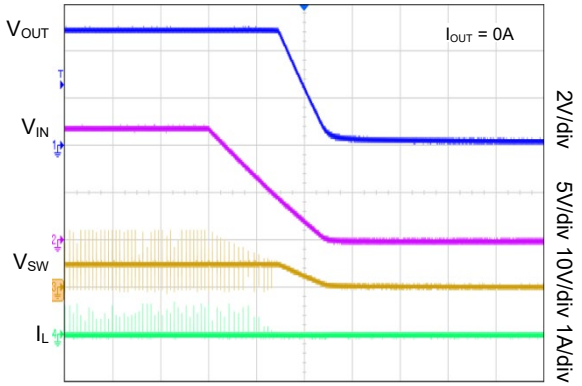


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

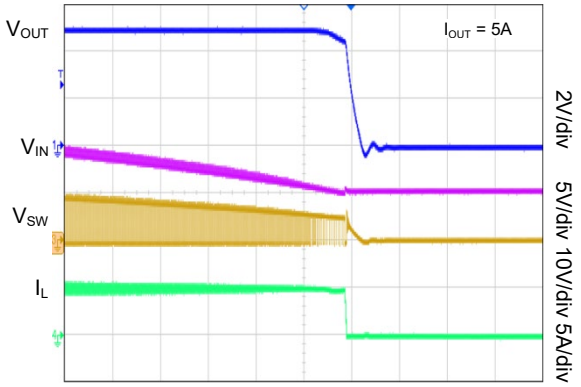
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 300kHz, L = 8.2μH, C_{OUT} = 47μF × 2, unless otherwise noted.

Shutdown by VIN



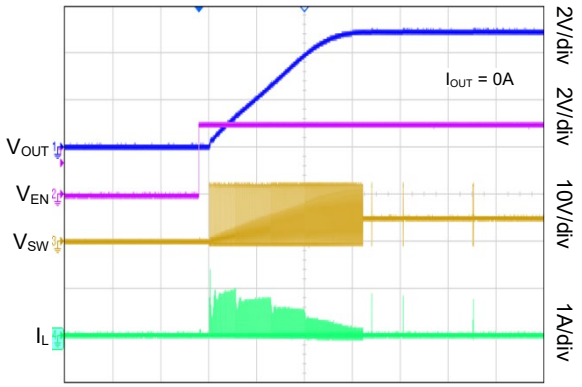
Time (100ms/div)

Shutdown by VIN



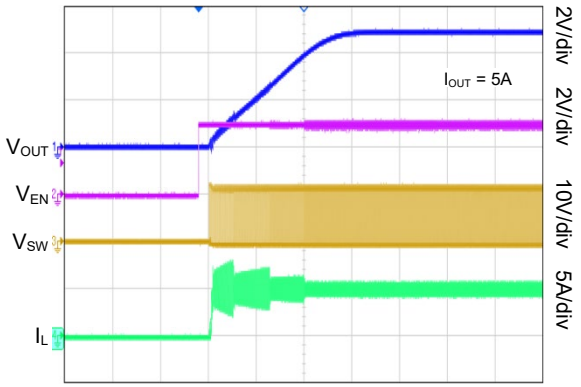
Time (200μs/div)

Start by EN



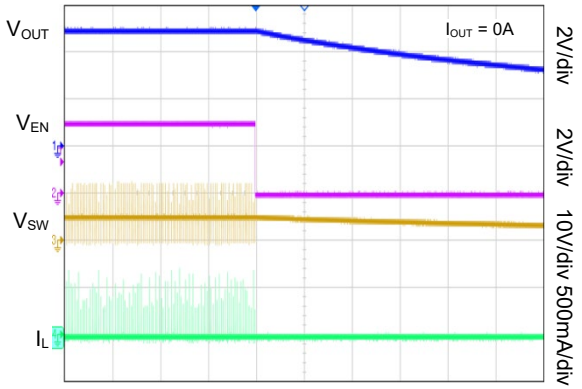
Time (2ms/div)

Start by EN



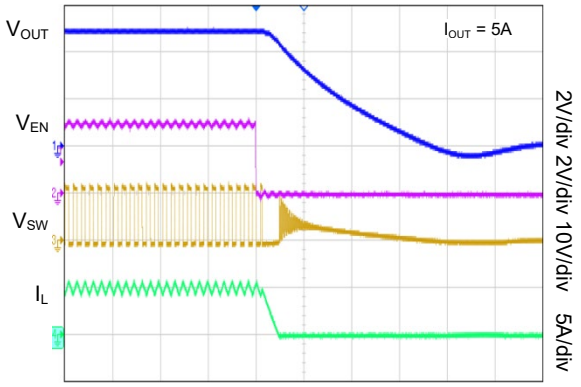
Time (2ms/div)

Shutdown by EN



Time (200ms/div)

Shutdown by EN

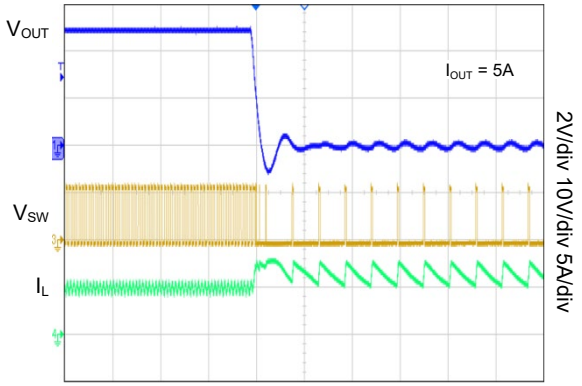


Time (20μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

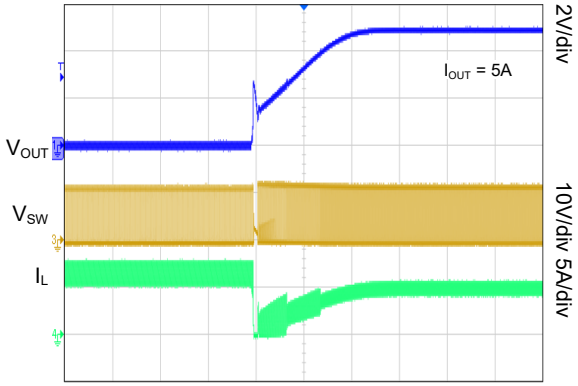
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 300kHz, L = 8.2μH, C_{OUT} = 47μF × 2, unless otherwise noted.

SCP Entry



Time (50μs/div)

SCP Recovery



Time (2ms/div)

FUNCTIONAL BLOCK DIAGRAM

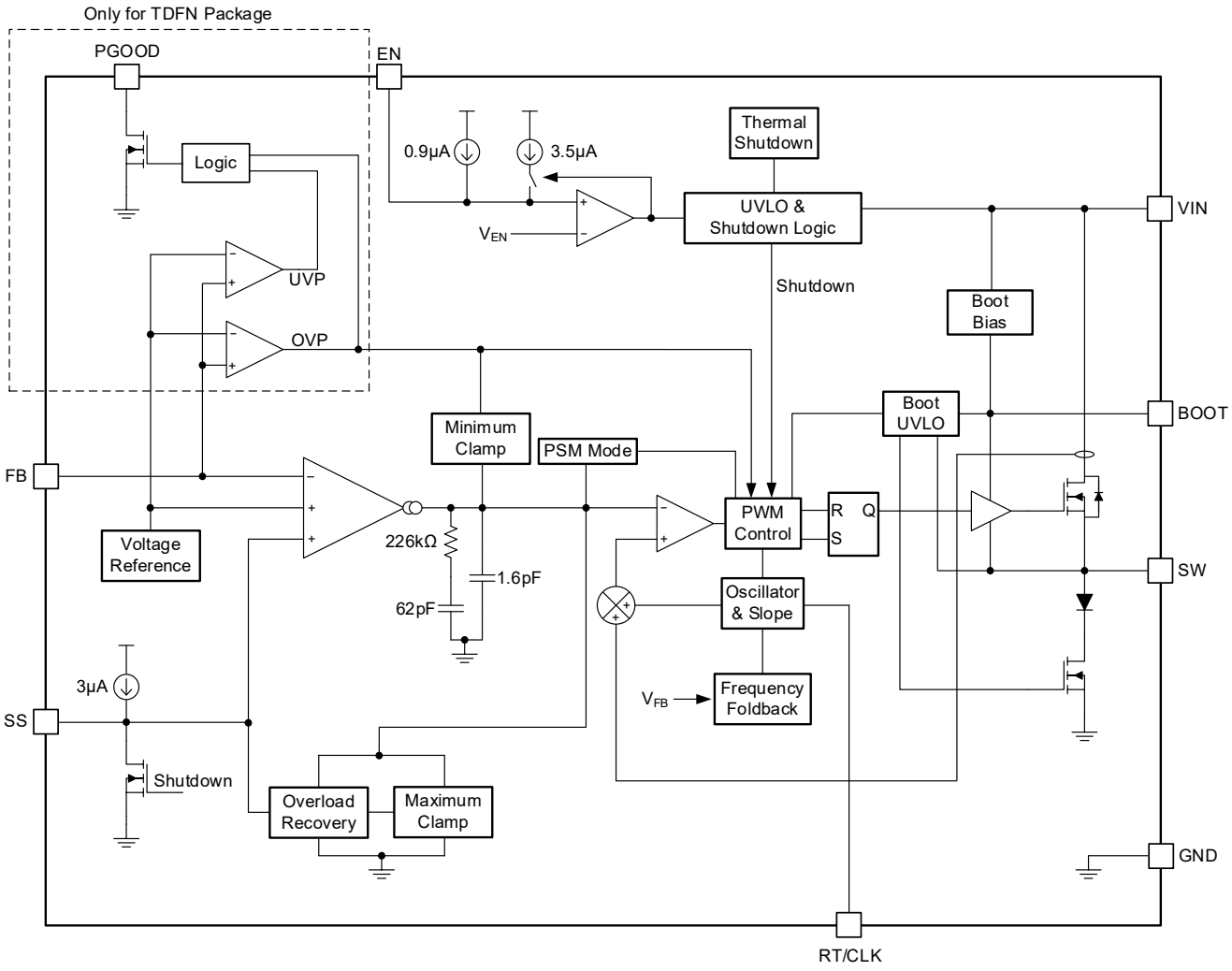


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61451xQ is a 40V Buck converter with an integrated N-MOSFET power switch and 5A continuous output current capability. Using peak current mode control, this device provides good line and load transient responses with reduced output capacitance. Light load efficiency is enhanced by a special power-save mode.

The minimum operating input voltage of the device is 4V and its nominal frequency is 300kHz. The quiescent current is 47μA. It reduces to 2.1μA if the device is disabled. The low R_{DSON} high-side switch (80mΩ for SOIC package, 90mΩ for TDFN package) allows high operating efficiency.

The EN pin is internally pulled up by a current source that can keep the device enabled if EN is floating. It can also be used to increase the input UVLO threshold using a resistor divider.

The bootstrap diode is integrated and only a small capacitor between BOOT and SW pins (C_{BOOT}) is needed for the MOSFET gate driving bias. A separate UVLO circuit monitors C_{BOOT} voltage and turns the switch off if this voltage falls below a preset threshold.

The switching frequency is adjusted by using a resistor to ground which is connected to the RT/SYNC pin. It is also can be synchronized to an external clock signal.

The SS pin internal current source allows soft-start time adjustments with a small external capacitor. This feature provides more flexibility in output filter design.

During startup and over-current, the frequency is reduced (frequency fold-back) to allow easy maintenance of low inductor current.

Additional features such as thermal shutdown, over-voltage protection and short-circuit protection (cycle-by-cycle current limit) are also provided.

Minimum Input Voltage (4V) and UVLO

The recommended minimum operating input voltage is 4V. It may operate with lower voltages that are above the V_{IN} rising UVLO threshold (3.7V TYP). If V_{IN} falls below its falling UVLO threshold, the device will stop switching.

Enable Input and UVLO Adjustment

An internal current source pull-up keeps the EN pin voltage at high state by default. The device will enable if the EN pin voltage exceeds the enable threshold of 1.2V and V_{IN} exceeds its UVLO threshold. The device will disable if the EN voltage is externally pulled low or the VIN pin voltage falls below its UVLO threshold.

If an application requires a higher input UVLO threshold, an external input UVLO adjustment circuit is recommended in Figure 3. Figure 3 shows how UVLO and hysteresis are increased using R_{EN1} and R_{EN2}. A 3.5μA additional current is injected to the divider when EN pin voltage exceeds V_{EN_TH} (1.2V) to provide hysteresis and it will be removed when EN pin voltage is below V_{EN_TH} - V_{EN_HYS}. Use Equations 1 and 2 to calculate these resistors. V_{START} is the input start (turn-on) threshold voltage and V_{STOP} is the input stop (turn-off) threshold voltage.

$$R_{EN1} = \frac{V_{START}\left(\frac{V_{EN_TH} - V_{EN_HYS}}{V_{EN_TH}}\right) - V_{STOP}}{3.5\mu A + 0.9\mu A \times \left(1 - \frac{V_{EN_TH} - V_{EN_HYS}}{V_{EN_TH}}\right)} \quad (1)$$

$$R_{EN2} = \frac{V_{EN_TH} \times R_{EN1}}{0.9\mu A \times R_{EN1} + V_{START} - V_{EN_TH}} \quad (2)$$

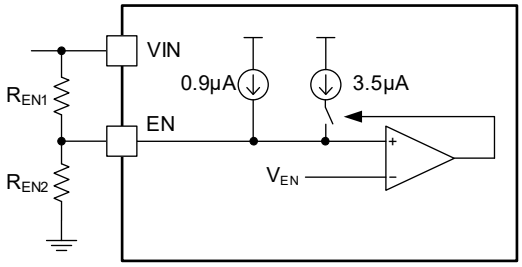


Figure 3. Input UVLO Adjustment

Low Dropout Operation and Bootstrap Gate Driving (BOOT Pin)

An internal regulator provides the bias voltage for gate driver using a 0.1μF ceramic capacitor. X5R or better dielectric types are recommended. The capacitor must have a 10V or higher voltage rating.

The SGM61451xQ operates at maximum duty cycle when input voltage is closed to output voltage as long as the bootstrap voltage (V_{BOOT} - V_{SW}) is greater than its UVLO threshold. When the bootstrap voltage falls below its UVLO, the high-side switch is turned off, and the integrated low-side switch is turned on to recharge the BOOT capacitor. After the recharge, the high-side switch is turned on again to regulate the output.

DETAILED DESCRIPTION (continued)

SS Pin and Soft-Start Adjustment

It is recommended to add a soft-start capacitor (C_{SS}) between the SS and GND pins to set the soft-start time from 1ms to 10ms for a proper startup. The lower of the SS pin voltage V_{SS} and V_{REF} is applied to the error amplifier to regulate the output. The internal I_{SS} = 3μA current charges C_{SS} and provides a linear voltage ramp on the SS pin. Use Equation 3 to calculate the soft-start time.

$$t_{SS}\ (ms) = \frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)} \quad (3)$$

Slope Compensation

Without implementing some slope compensation, the PWM pulse widths will be unstable and oscillatory at duty cycles above 50%. To avoid sub-harmonic oscillations in this device, an internal compensation ramp is added to the measured switch current before comparing it with the control signal by the PWM comparator.

Power-Save Mode

At light loads, the SGM61451xQ enters pulse-skipping power-save mode (PSM) to keep its high efficiency by lowering the number of switching pulses. When the EA output voltage (V_{COMP}) is lower than the internal PSM threshold. The device will enter PSM in such conditions.

After entering PSM for a delay time, some modules are shut down to minimum input current, and the device draws only 47μA (TYP) input quiescent current. The device can exit PSM if V_{COMP} rises above the internal PSM threshold. During PSM operation, the actual load current (DC) threshold for PSM will depend on the output filter.

Synchronization to RT/SYNC Pin

The internal oscillator can synchronize to an external logic clock applied to the RT/SYNC pin (see Figure 4) in the 250kHz to 2300kHz range. The SW rising edge (switch turn-on) is synchronized with the CLK falling edge. The CLK low and high levels must be less than 0.5V (TYP) and more than 1.7V (TYP) and have a pulse width larger than 30ns. So, when the CLK source is off, the DC resistance (R_T) between RT/SYNC and GND pins determines the default switching frequency.

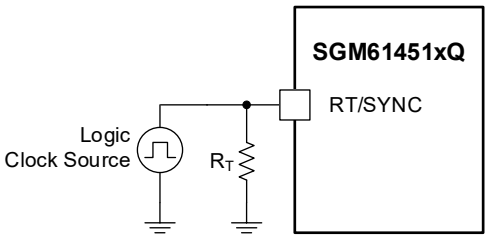


Figure 4. Synchronization to External Clock

Switching Frequency and Timing Resistor (RT/SYNC Pin)

The switching frequency can be set from 200kHz to 2500kHz by a timing resistor (R_T) placed between the RT/SYNC and GND pins. There is an internal bias voltage on the RT/SYNC pin during the RT mode and must have a resistor to ground to set the switching frequency. Use Equation 4 to find the R_T resistance for any desired switching frequency (f_{SW}).

$$R_T\ (k\Omega) = 42904 \times f_{SW}\ (kHz)^{-1.088} \quad (4)$$

Power Good (PGOOD)

The SGM61451xQ with TDFN package has a power good (PGOOD) pin for indicating the output voltage in the desired level. The PGOOD pin is an open-drain output that requires 10kΩ to 100kΩ resistor pulled up to a suitable voltage supply.

As shown in Figure 5, when the FB voltage is within the power good range, the PGOOD switch is turned off and the PGOOD pin is pulled up to high. When the FB voltage is outside the power good range, the PGOOD switch is turned on and the PGOOD pin is pulled down to low.

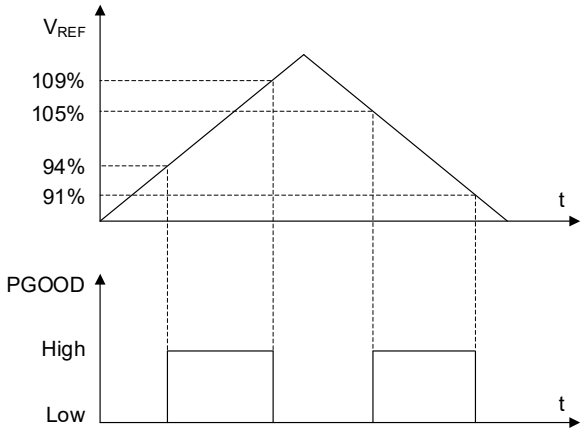


Figure 5. PGOOD Flag

DETAILED DESCRIPTION (continued)

Over-Current Protection and Frequency Fold-back

Over-current protection (OCP) is naturally provided by current mode control. In each cycle, the high-side current sensing starts a short time (blanking time) after the high-side switch is turned on. The sensed high-side switch current is continuously compared with the EA output (V_{COMP}) when the high-side current reaches to that threshold, the high-side switch is turned off. If the output is overload, the peak current of high-side switch is limited by a maximum peak current I_{LIM}.

The natural OCP of the peak current mode control may not be able to provide a complete protection when an output short-circuit occurs and an extra protection mechanism for short-circuit is needed. During an output short, inductor current may runaway above over-current limits because of the high input voltage and the minimum controllable on-time. In these conditions, current can saturate the inductor and the current may even increase higher until the device is damaged. In the SGM61451xQ, this problem is effectively solved through increasing the off-time during short-circuit by reducing the switching frequency (frequency fold-back).

In a short or overload condition, if the peak current limit is triggered 6 times consecutively, the switching frequency will be divided by 2 immediately, as the FB voltage drops, the frequency will be divided by 4 (V_{FB} = 0.4V) and 8 (V_{FB} = 0.2V). In conclusion, if the sensed high-side switch current reached to peak current-limit I_{LIM}, the HS is turned off, the HS switch is turned on at the next clock. On the contrary, when the output short-circuit is removed or V_{IN} start-up, the switching frequency increase with the FB voltage at V_{FB} = 0.2V, 0.4V, 0.6V respectively. Finally the SGM61451AQ working at the switching frequency set by R_T.

Over-Voltage Transient Protection

When an overload or an output fault condition is removed, large overshoots may occur on the output. The SGM61451xQ includes over-voltage protection (OVP) circuit to reduce such over-voltage transients. If V_{FB} voltage exceeds 109% of the V_{REF} threshold, the MOSFET is turned off. When it returns below 105% of the V_{REF} threshold, the MOSFET is released again.

Spread Spectrum Switching (SGM61451BQ Only)

Spread spectrum technique is used in the SGM61451BQ to flatten the generated EMI spectrum and reduce the large EMI peaks. The switching frequency is periodically varied between -6% and +6% of the nominal value.

Thermal Shutdown (TSD)

If the junction temperature (T_J) exceeds +173℃, the TSD protection circuit will stop switching to protect the device from overheating. The device will automatically restart with a power up sequence when the junction temperature drops below +158℃.

APPLICATION INFORMATION

A typical application circuit for the SGM61451xQ as a Buck converter is shown in Figure 6. It is used for converting a 7V to 40V supply voltage to a lower voltage level supply voltage (5V) suitable for the system.

The external components are designed based on the application requirements and device stability. Some suitable parameters for different output voltages are provided in Table 1 to simplify the selection of components. The C_{OUT} values in Table 1 are actual derating values. Higher nominal values are used for ceramic capacitors.

Typical Application

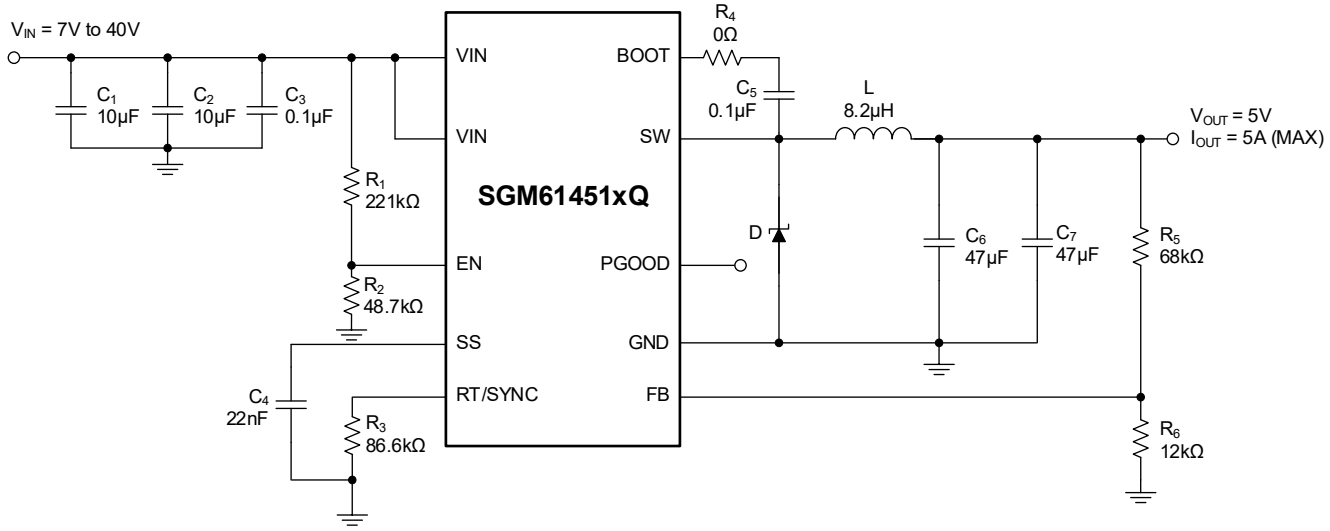


Figure 6. 5V Output SGM61451xQ Design Example

Table 1. Some Typical L and C_{OUT} Values for Stable Operation

f_{SW} (kHz)	V_{OUT} (V)	L (μH)	C_{OUT} (μF)	R_5 (kΩ)	R_6 (kΩ)
300	3.3	5.5	100	68	20
300	5	8.2	68	68	12
300	12	15	47	150	10
300	24	22	22	316.2	10.2
2200	5	1	10	68	12

Design Requirements

The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage	12V (TYP), 7V to 40V
Start Input Voltage (Rising V_{IN})	6.42V
Stop Input Voltage (Falling V_{IN})	5.21V
Output Voltage	5V
Output Voltage Ripple	50mV, 1% of V_{OUT}
Output Current Rating	5A
Transient Response 2.5A to 5A Load Step	250mV, 5% of V_{OUT}
Operation Frequency	300kHz

Switching Frequency Selection

Several parameters such as losses, inductor and capacitors sizes and response time are considered in selection of the switching frequency. Higher frequency increases the switching and gate charge losses, and lower frequency requires larger inductance and capacitances, which results in larger overall physical size and higher cost. Therefore, a tradeoff is needed between losses and component size. If the application is noise-sensitive to a frequency range, the frequency should be selected out of that range.

For this design, a lower switching frequency of 300kHz is chosen and a 86.6kΩ resistor can be chosen for R_3 according to Equation 4.

APPLICATION INFORMATION (continued)

Input Capacitor Design

High frequency decoupling on the input supply pins is necessary for the device. A bulk capacitor may also be needed in some applications. Typically, 10μF to 22μF high quality ceramic capacitor (X5R, X7R or better) with voltage rating twice the maximum input voltage is recommended for decoupling capacitor. If the source is away from the device (> 5cm) some bulk capacitance is also needed to damp the voltage spikes caused by the wiring or PCB trace parasitic inductances. For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. Therefore, 2×10μF/50V/X7R capacitors and a 0.1μF ceramic capacitor placed right beside the device VIN and GND pins for very high-frequency filtering are used. This ripple can be calculated from Equation 5.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (5)$$

Inductor Design

Equation 6 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions, especially if a hard-saturation core type inductor (such as ferrite) is chosen. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 20% to 40% ripple is selected (K_{IND} = 0.2 ~ 0.4). Choosing a higher K_{IND} value reduces the selected inductance, however, a too high K_{IND} factor may result in insufficient slope compensation.

$$L = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (6)$$

In this example, the calculated inductance will be 7.29μH with K_{IND} = 0.4, so the nearest larger inductance of 8.2μH is selected. The ripple, RMS and peak inductor current calculations are summarized in Equations 7, 8 and 9 respectively.

$$\Delta I_L = \frac{V_{IN_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (7)$$

$$I_{L_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (8)$$

$$I_{L_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (9)$$

Note that during startup, load transients or under fault conditions, the peak inductor current may exceed the calculated I_{L_PEAK}. Therefore, it is always safer to choose the inductor saturation current higher than the switch current limit.

External Diode

An external power diode between the SW and GND pins is needed for the SGM61451xQ to complete the converter. This diode must tolerate the application's absolute maximum ratings. The reverse blocking voltage must be higher than V_{IN_MAX} and its peak current must be above the maximum inductor current. Choose a diode with small forward voltage drop for higher efficiency. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 50V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SGM61451xQ.

Output Capacitor

Three primary criteria must be considered for design of the output capacitor (C_{OUT}):

1. The converter pole location.
2. The output voltage ripple.
3. The transient response to a large change in load current.

APPLICATION INFORMATION (continued)

The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually a more stringent criterion in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step).

Equation 10 can be used to calculate the minimum output capacitance that is needed to supply a current step (ΔI_{OUT}) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (10)$$

where:
ΔI_{OUT} is the change in output current.
ΔV_{OUT} is the allowable change in the output voltage.

For example, if the acceptable transient from 2.5A to 5A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V and ΔI_{OUT} = 2.5A, the minimum required capacitance will be 66.67μF. Note that the impact of output capacitor ESR on the transient is not taken into account in Equation 10. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient. However, for aluminum electrolytic and tantalum capacitors, or high current power supplies, the ESR contribution to ΔV_{OUT} must be considered.

When the load steps down, the excess inductor current will charge the capacitor and the output voltage will overshoot. So C_{OUT} must be large enough as given in Equation 11 to absorb the excess inductor energy with limited over-voltage. Equation 11 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT_H}^2 - I_{OUT_L}^2}{(V_{OUT} + \Delta V_{OUT})^2 - V_{OUT}^2} \quad (11)$$

where:
I_{OUT_H} is the high level of the current step.
I_{OUT_L} is the low level of the current step.

For example, if the acceptable transient from 5A to 2.5A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V, the minimum required capacitance will be 60μF.

Equation 12 can be used for the output voltage ripple criteria and finding the minimum output capacitance needed. V_{OUT_RIPPLE} is the maximum acceptable ripple.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT_RIPPLE}} \quad (12)$$

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 13. For a specific output capacitance value, use Equation 13 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{COUT} < \frac{V_{OUT_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (13)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, 2 × 47μF/25V X5R ceramic capacitors with 5mΩ of ESR are used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 14 calculates the RMS current that the output capacitor must support. In this example, it is 513mA.

$$I_{COUT_RMS} = \frac{V_{OUT} \times (V_{IN_MAX} - V_{OUT})}{\sqrt{12} \times V_{IN_MAX} \times L \times f_{SW}} \quad (14)$$

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor (C_5). A 5Ω to 10Ω resistor (R_4) can be added in series with C_5 to slow down switch-on speed of the high-side switch and reduce EMI if needed. Too high values for R_4 may cause insufficient C_5 charging in high duty-cycle applications. Slower switch-on speed will also increase switch losses and reduce efficiency.

APPLICATION INFORMATION (continued)

UVLO Setting

The Input UVLO can be programmed using an external voltage divider on the EN pin of the SGM61451xQ. In this design R_1 is connected between VIN pin and EN pin and R_2 is connected between EN pin and GND (see Figure 6). The UVLO has two thresholds, one for power-up (turn-on) when the input voltage is rising and one for power-down (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 6.42V (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input falls below 5.21V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_1 = 221kΩ and R_2 = 48.7kΩ.

Feedback Resistors Setting

Use an external resistor divider (R_5 and R_6) to set the output voltage using Equations 15 and 16.

$$R_5 = R_6 \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}} \right) \quad (15)$$

$$V_{OUT} = V_{REF} \times \left(\frac{R_5}{R_6} + 1 \right) \quad (16)$$

For this example, the selected values are R_5 = 68kΩ, R_6 = 12kΩ, resulting in a 5V output voltage.

Layout Considerations

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. Following the guidelines provided here are necessary to design a good layout:

- Bypass the VIN pin to GND pin (where it connects to the anode pin of the power diode) with low-ESR ceramic capacitors (X5R/X7R or better) and place them as close as possible.
- Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections, SW pin and the catch diode.
- Connect the device GND pin directly to the exposed pad (Power Pad) copper area under the IC device.
- Stitch the exposed pad to the internal ground planes and the back side of the PCB directly under the IC using multiple thermal vias.
- Use a short and wide path for routing the SW pin to the cathode of the catch diode on the same layer and to the output inductor.
- Keep the SW area minimal and away from sensitive signals like FB input and divider resistors or RT/SYNC to avoid capacitive noise coupling.
- Top side GND plane that is connected to the exposed pad provides the best heat removal path for the IC. It should be large enough for designs that operate with full rated loads. Thicker copper planes can improve heat dissipation.
- Place the RT resistor (R_3) as close as possible to the RT/SYNC pin with short routes.

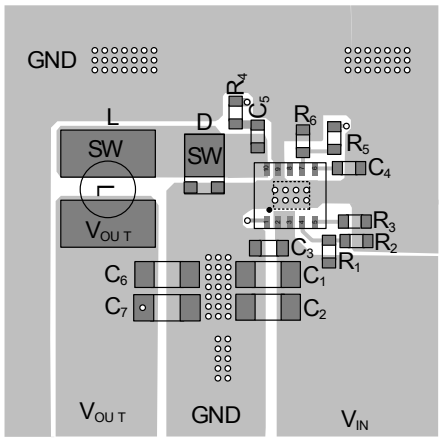


Figure 7. Top Layer (TDFN Package)

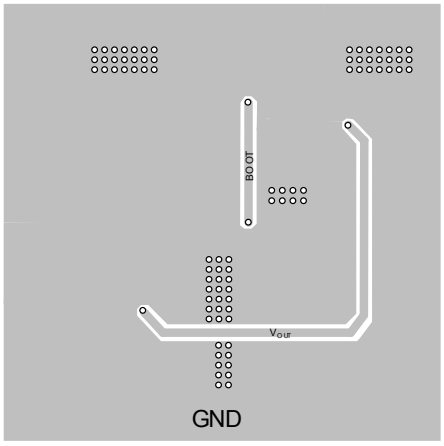


Figure 8. Bottom Layer (TDFN Package)

APPLICATION INFORMATION (continued)

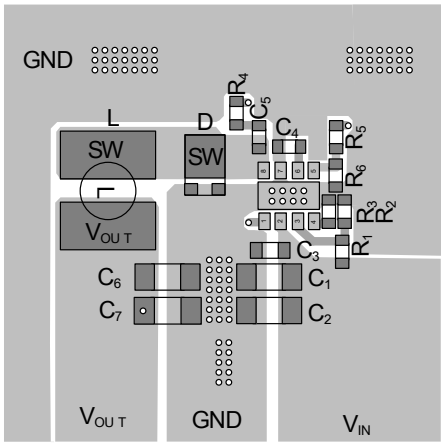


Figure 9. Top Layer (SOIC Package)

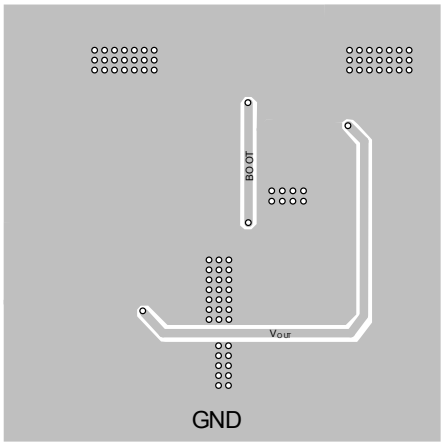


Figure 10. Bottom Layer (SOIC Package)

REVISION HISTORY

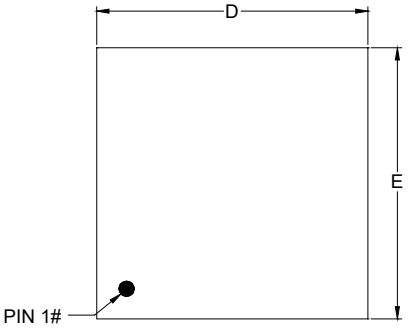
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2025 – REV.A to REV.A.1	Page
Added SGM61451BQ and SOIC Package	All

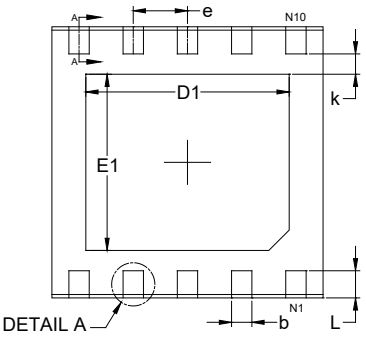
Changes from Original (MARCH 2025) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

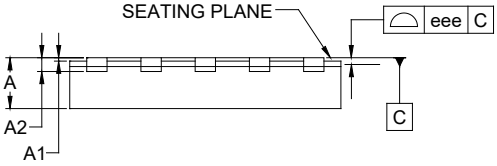
TDFN-4×4-10AL



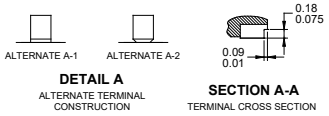
TOP VIEW



BOTTOM VIEW

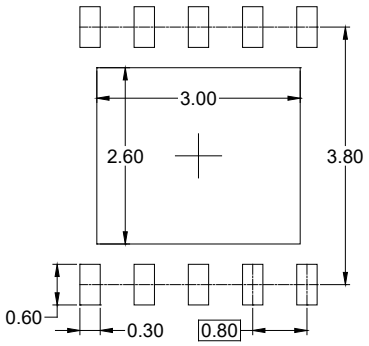


SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

SECTION A-A
TERMINAL CROSS SECTION



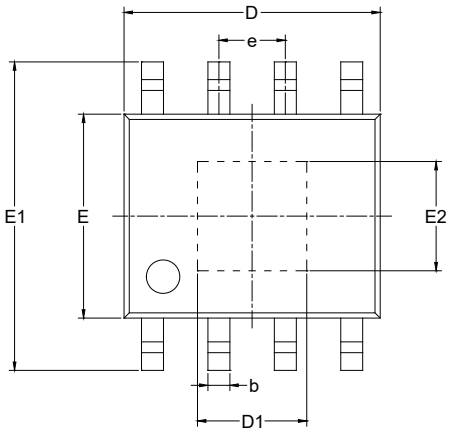
RECOMMENDED LAND PATTERN (Unit: mm)

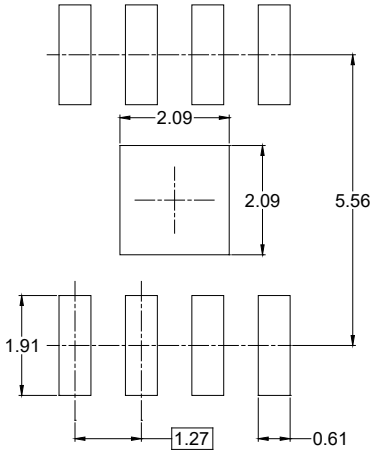
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.250	-	0.350
D	3.900	-	4.100
D1	2.900	-	3.100
E	3.900	-	4.100
E1	2.500	-	2.700
e		0.800 BSC	
k		0.300 REF	
L	0.300	-	0.500
eee		0.080	

NOTE: This drawing is subject to change without notice.

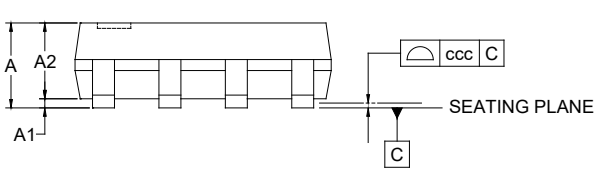
PACKAGE OUTLINE DIMENSIONS

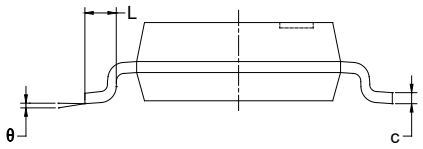
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)



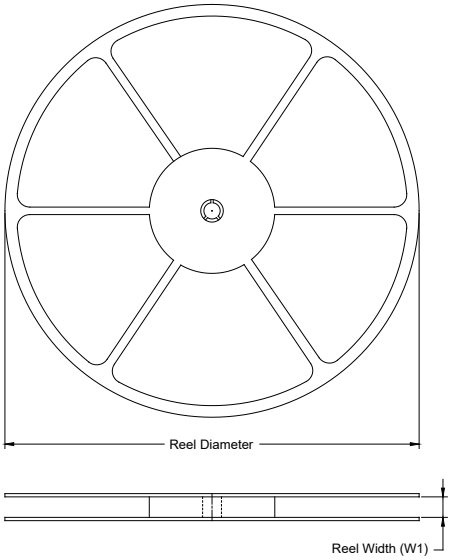


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	1.890	-	2.290
E	3.800	-	4.000
E1	5.800	-	6.200
E2	1.890	-	2.290
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

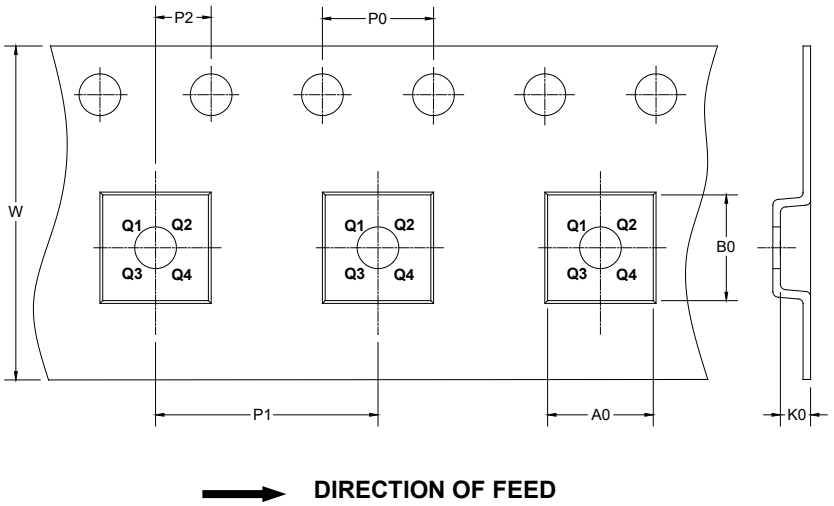
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



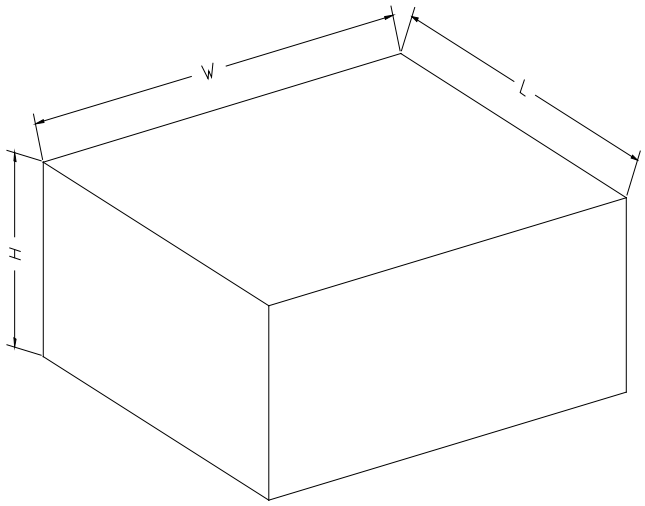
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-4×4-10AL	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002