SGM61101Q
Automotive 3V to 17V, 0.6A Synchronous Buck Converter with AHP-COT Control

GENERAL DESCRIPTION

The SGM61101Q is a high-frequency, synchronous Buck converter optimized for simple and quick application to high density designs. High output voltage accuracy and fast transient response along with small LC output filter elements are easily achievable with the 2.1MHz (TYP) switching frequency and the AHP-COT control.

The 3V to 17V input voltage range makes this device a suitable choice for both 12V input power rails and the battery powered applications including Li-Ion batteries. It supports 100% duty cycle operation and can provide 0.6A continuous current to its adjustable or fixed output voltage versions. The enable input (EN) and power-good output (PG) pins provide power sequencing capability.

In power-save mode (PSM), the VIN quiescent current is reduced to 22μA (TYP). Operation mode is seamlessly changed between PWM and PSM to keep the efficiency high in entire load range. Mode changing is automatically decided based on the load current at the DCM/CCM changeover level.

In the shutdown mode, the device is completely turned off and the current consumption drops to 1.2μA (TYP).

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

SGM61101Q is available in a Green TDFN-2×2-8AL package.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **AHP-COT Control**
- **3V to 17V Input Voltage Range**
- **Support 0.6A Output Current**
- **0.9V to 5.5V Adjustable Output Voltage**
- **Fixed Output Voltage Version: 3.3V**
- **Internal Compensation**
- **170μs (TYP) Soft-Start Time**
- **Pre-biased Function during Soft Startup**
- **Power-Save Mode with Seamless Transition**
- **22μA (TYP) Quiescent Current**
- **Power-Good Output**
- **100% Duty Cycle Mode**
- **Under-Voltage Lockout (UVLO)**
- **Thermal Shutdown Protection**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Available in a Green TDFN-2×2-8AL Package**

APPLICATIONS

Automotive Cameras
Advanced Driver Assistance Systems (ADAS)
Automotive Infotainment and Cluster
Vehicle Body Electronics and Lighting

TYPICAL APPLICATION

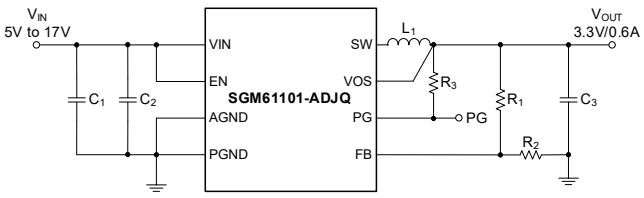
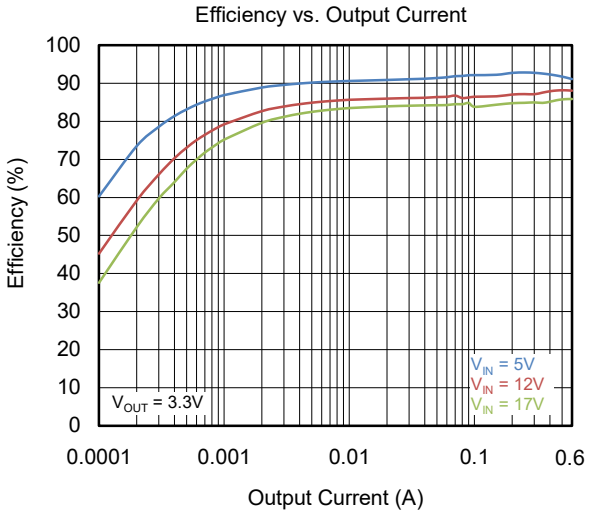


Figure 1. Typical Application Circuit



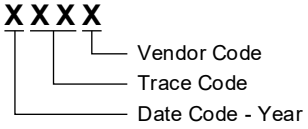
代理商 威尔边 www.vsvie.com 联系电话 138 2526 5270

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61101-ADJQ	TDFN-2×2-8AL	-40℃ to +125℃	SGM61101-ADJQTDE8G/TR	0TS XXXX	Tape and Reel, 3000
SGM61101-3.3Q	TDFN-2×2-8AL	-40℃ to +125℃	SGM61101-3.3QTDE8G/TR	0TT XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Pin Voltage Range
VIN ..... -0.3V to 20V
EN, SW ..... -0.3V to V_{IN} + 0.3V
FB, PG, VOS ..... -0.3V to 6V
Power Good Sink Current, PG 10mA
Package Thermal Resistance
TDFN-2×2-8AL, θ_{JA} ..... 56.7℃/W
TDFN-2×2-8AL, θ_{JB} ..... 24.8℃/W
TDFN-2×2-8AL, $\theta_{JC\ (TOP)}$ ..... 79℃/W
TDFN-2×2-8AL, $\theta_{JC\ (BOT)}$ ..... 6.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±2000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 3V to 17V
Output Voltage Range, V_{OUT} ..... 0.9V to 5.5V
Operating Junction Temperature, T_J ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

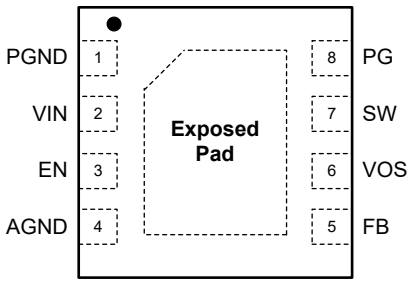
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-8AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	PGND	G	Power Ground.
2	VIN	P	Supply Voltage.
3	EN	I	Enable Input. Pull up to a logic-high voltage to enable the device, pull down to disable it.
4	AGND	G	Analog Ground.
5	FB	I	Output Voltage Feedback Input (in the Adjustable Version). Connect a resistor divider from the output to this pin to set the output voltage. In the fixed output versions, an internal resistor connects this pin to ground and it is recommended to short the FB pin to AGND to improve the thermal performance.
6	VOS	I	Output Voltage Sense Pin. Connect this pin to sense the output ripple that is needed for the internal control loop.
7	SW	P	Switch Node. Connect this pin to the internal MOSFET switches. Connect inductor between SW and output capacitor.
8	PG	O	Power-Good Output. Indicate readiness when high (V_{OUT} ready) and indicate V_{OUT} below nominal regulation when low. Open-drain, a pull-up resistor is necessary, and it becomes high-impedance state when the device is switched off.
Exposed Pad	AGND	G	Ground. Must be connected to AGND and soldered to achieve good-power dissipation and mechanical reliability.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are measured at V_{IN} = 12V and T_A = +25℃, unless otherwise noted.)

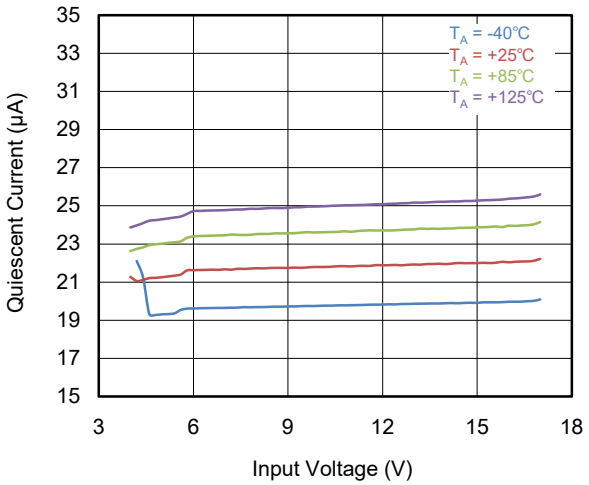
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Input Voltage Range (1)	V_{IN}		3		17	V
Operating Quiescent Current	I_Q	V_{IN} = 12V, EN = high, I_{OUT} = 0mA, device not switching		22	32	μA
Shutdown Current	I_{SD}	EN = low		1.2	2.8	μA
Under-Voltage Lockout Threshold	V_{UVLO}	Falling input voltage	2.6	2.73	2.85	V
		Hysteresis		160		mV
Thermal Shutdown Temperature	T_{SD}	T_J rising		160		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		
Control (EN, PG)						
High Level Input Voltage (EN)	V_{EN_H}		0.9			V
Low Level Input Voltage (EN)	V_{EN_L}				0.3	V
Input Leakage Current (EN)	I_{LKG_EN}	EN = V_{IN} or GND		0.01	0.5	μA
Power-Good Threshold Voltage	V_{TH_PG}	V_{PG} rising, V_{FB} referenced to V_{REF}	91	95	98	%
		V_{PG} falling, V_{FB} referenced to V_{REF}	85	89	92	
Power-Good Output Low	V_{OL_PG}	I_{SINK} = 2mA		0.12	0.3	V
Input Leakage Current (PG)	I_{LKG_PG}	V_{PG} = 1.8V		1	100	nA
Power Switch						
High-side MOSFET On-Resistance	R_{DSON}	V_{IN} ≥ 6V		255	450	mΩ
		V_{IN} = 3V		305		
Low-side MOSFET On-Resistance		V_{IN} ≥ 6V		115	200	mΩ
		V_{IN} = 3V		165		
High-side MOSFET DC Current Limit	I_{LIM}	V_{IN} = 12V	1.5	1.8	2	A
Low-side MOSFET DC Current Limit		V_{IN} = 12V	0.7	0.9	1.2	A
Output						
Soft-Start Time	t_{SS}	V_{IN} = 12V, from start switching to 90%V_{OUT} nominal		170		μs
Internal Reference Voltage	V_{REF}		0.782	0.8	0.818	V
FB Input Leakage Current	I_{LKG_FB}	SGM61101Q-ADJ, V_{FB} = 1.2V		1	100	nA
Output Voltage Range	V_{OUT}	SGM61101Q-ADJ, V_{IN} ≥ V_{OUT}	0.9		5.5	V
Feedback Voltage Accuracy (2)		PWM mode operation, V_{IN} ≥ V_{OUT} + 1V	-3		3	%
		Power-save mode operation, C_{OUT} = 2 × 22μF	-3		4	
Output Voltage Load Regulation (2)	$\Delta V_{OUT}/I_{OUT}$	PWM mode operation, V_{IN} = 12V, V_{OUT} = 3.3V		0.1		%/A
Output Voltage Line Regulation (2)	$\Delta V_{OUT}/V_{IN}$	PWM mode operation, 4V ≤ V_{IN} ≤ 17V, V_{OUT} = 3.3V, I_{OUT} = 0.5A		0.02		%/V

NOTE:

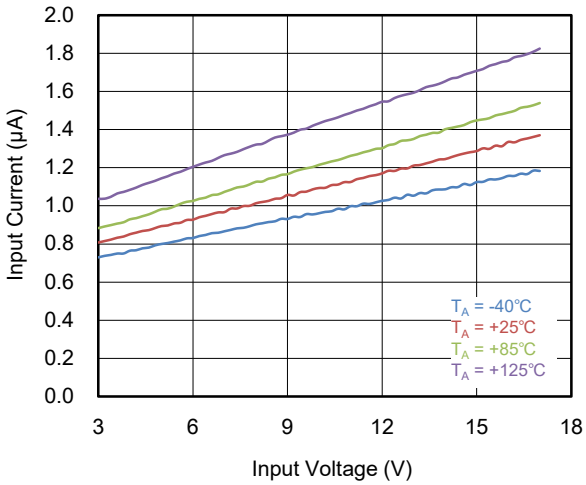
1. The device remains operational even during under-voltage lockout conditions.
2. Close loop test.

TYPICAL PERFORMANCE CHARACTERISTICS

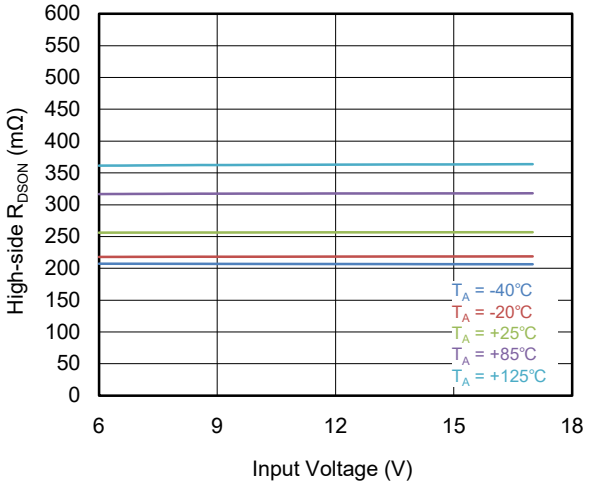
Quiescent Current vs. Input Voltage



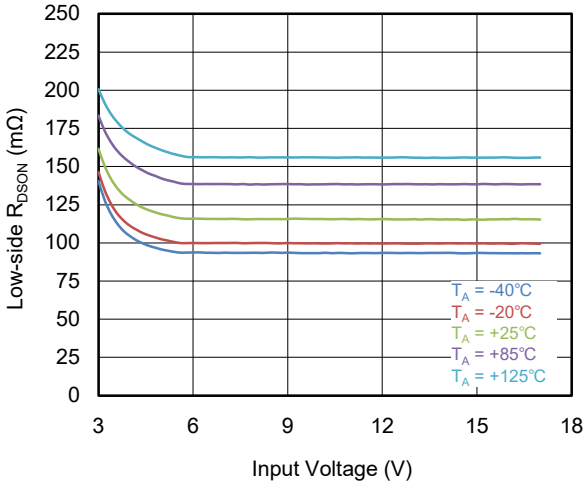
Shutdown Current vs. Input Voltage



High-side R_{DSON} vs. Input Voltage



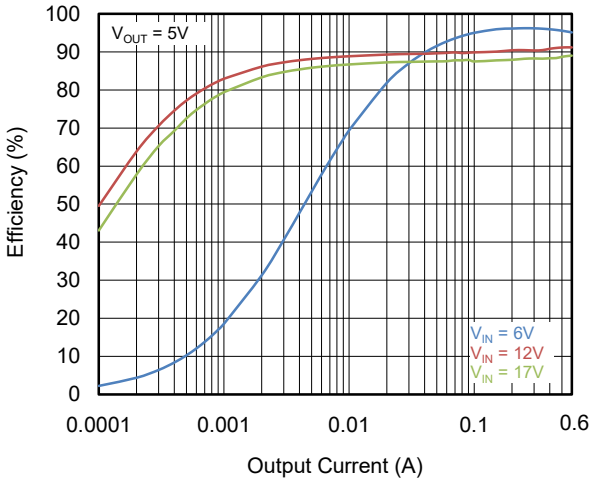
Low-side R_{DSON} vs. Input Voltage



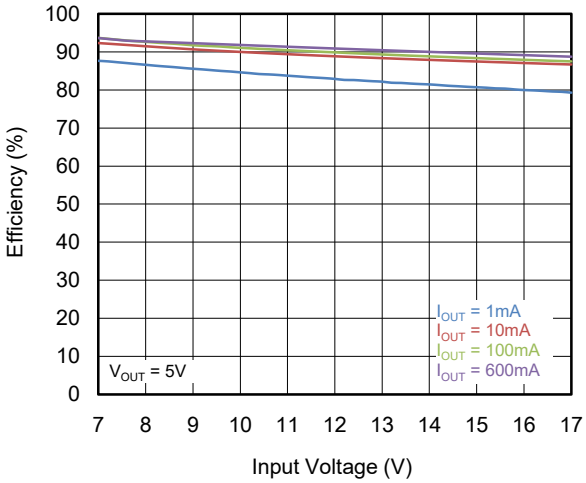
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH and DCR_{TYP} = 57mΩ, unless otherwise noted.

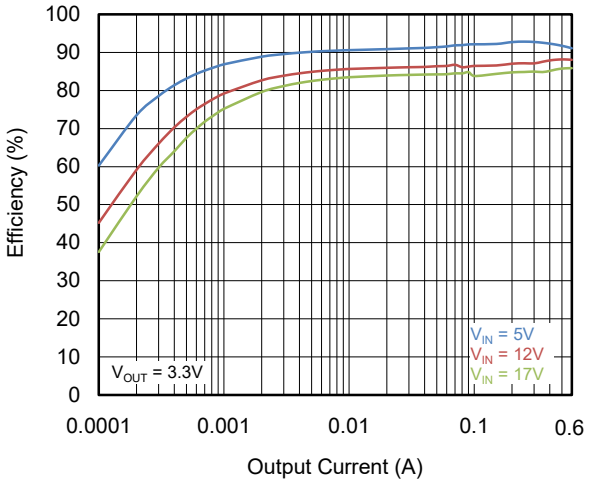
Efficiency vs. Output Current



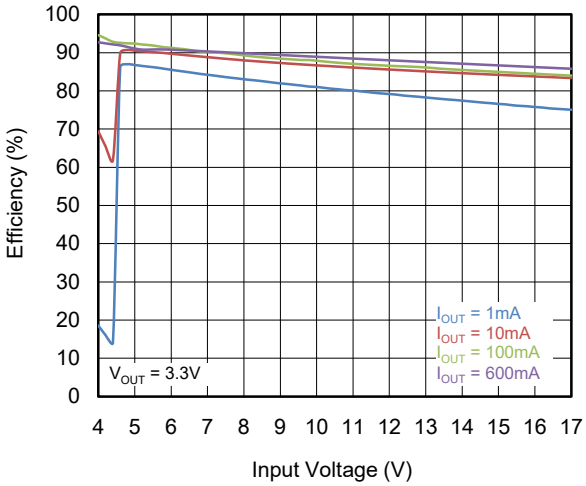
Efficiency vs. Input Voltage



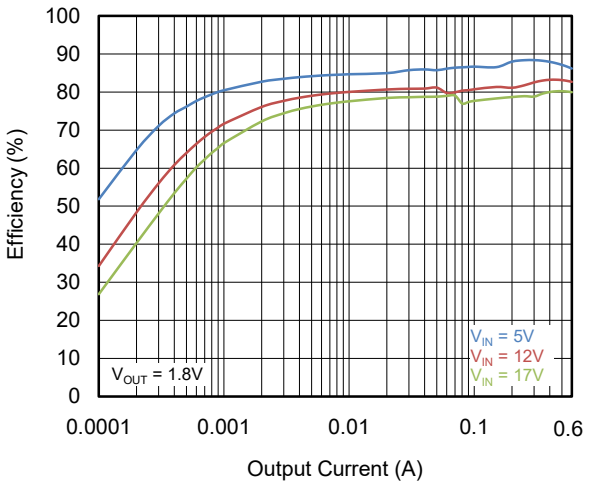
Efficiency vs. Output Current



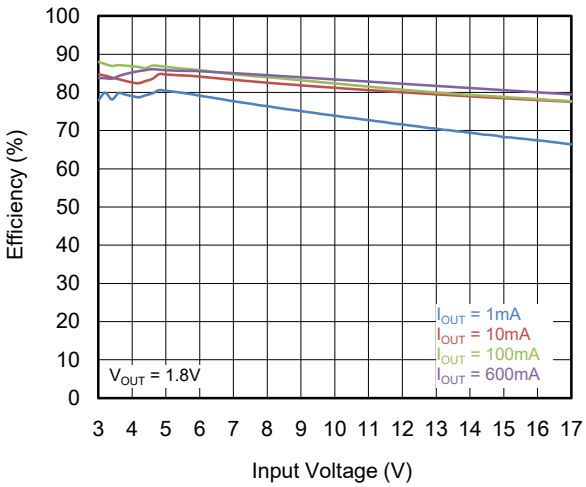
Efficiency vs. Input Voltage



Efficiency vs. Output Current



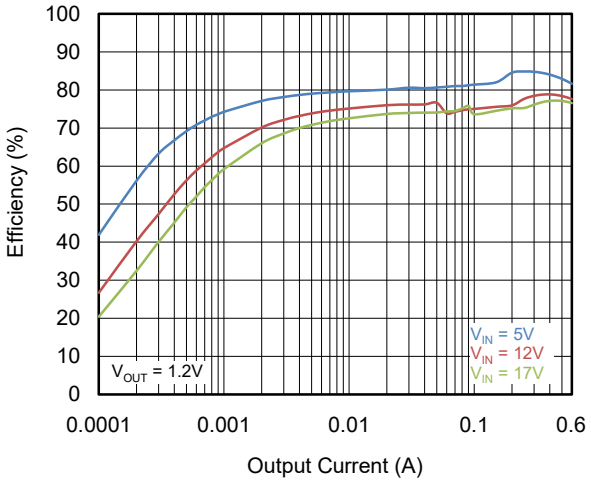
Efficiency vs. Input Voltage



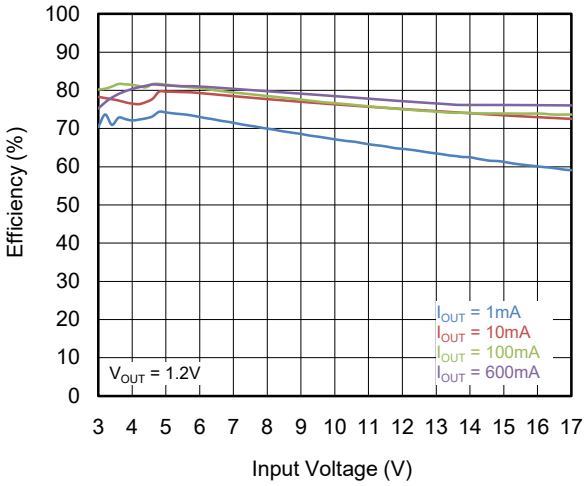
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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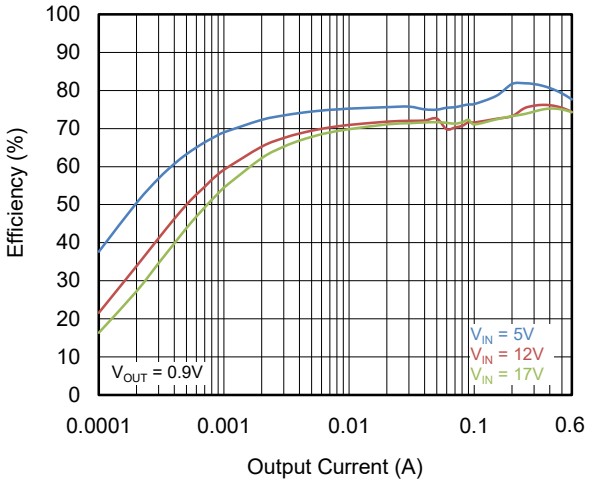
Efficiency vs. Output Current



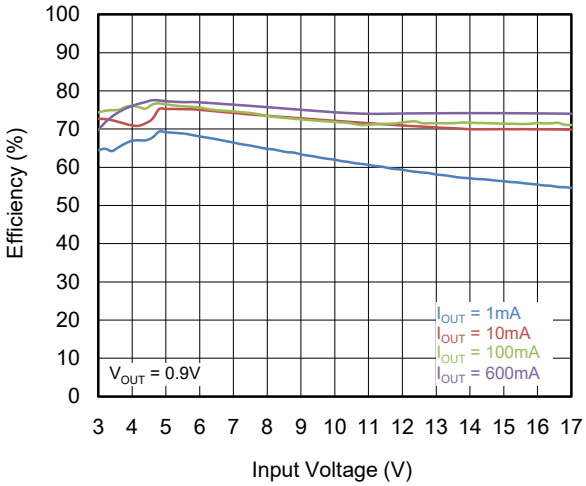
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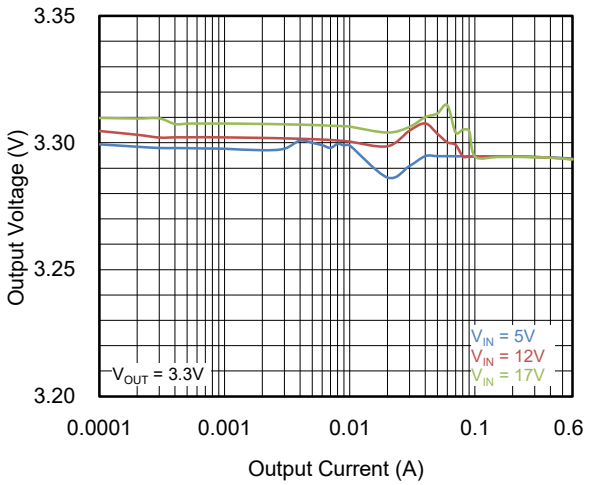
Efficiency vs. Output Current



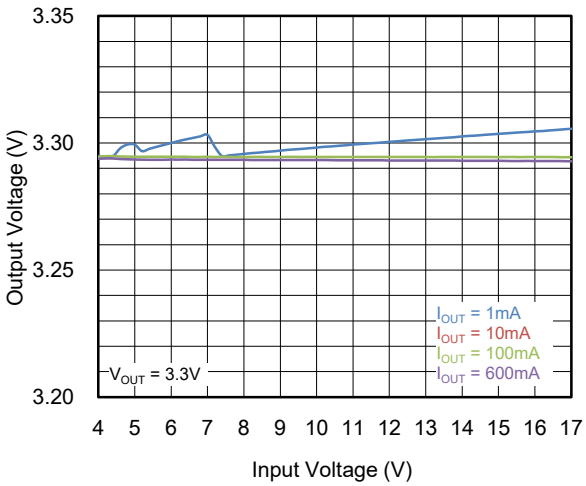
Efficiency vs. Input Voltage



Load Regulation



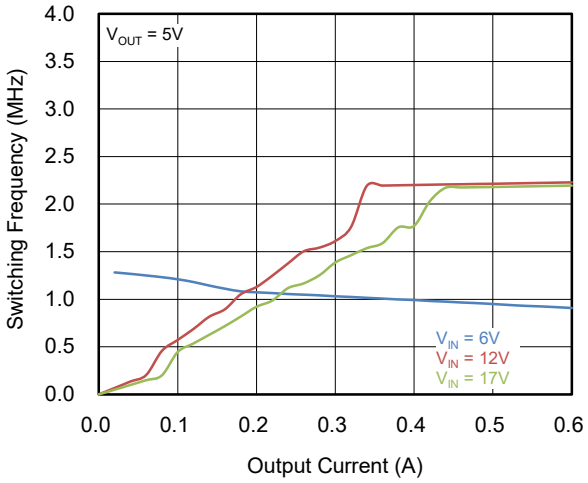
Line Regulation



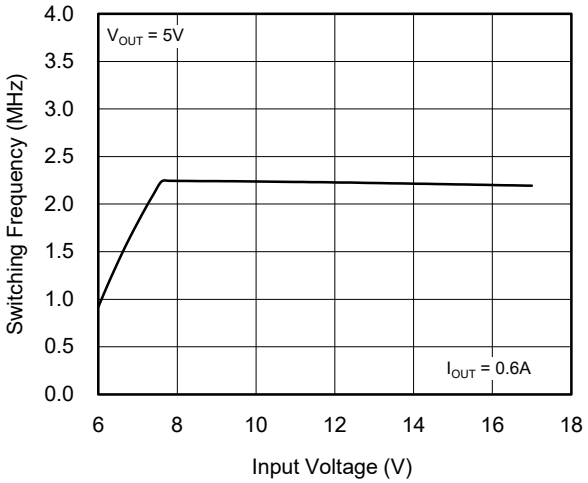
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH and DCR_{TYP} = 57mΩ, unless otherwise noted.

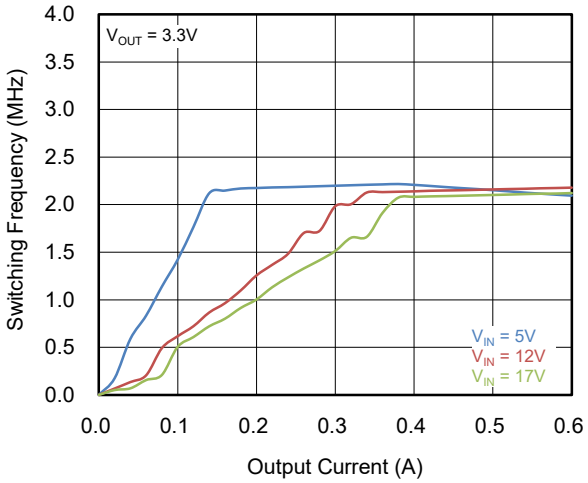
Switching Frequency vs. Output Current



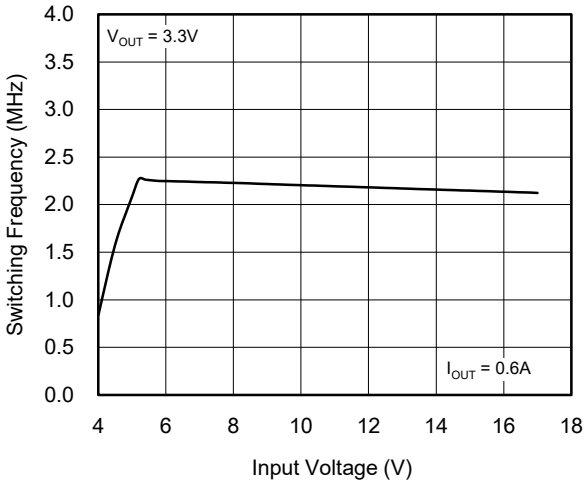
Switching Frequency vs. Input Voltage



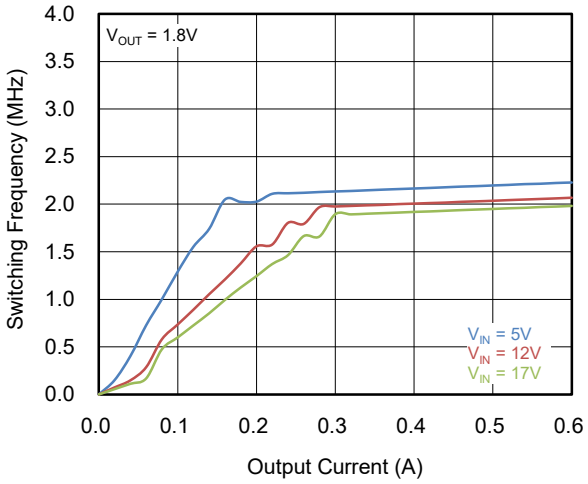
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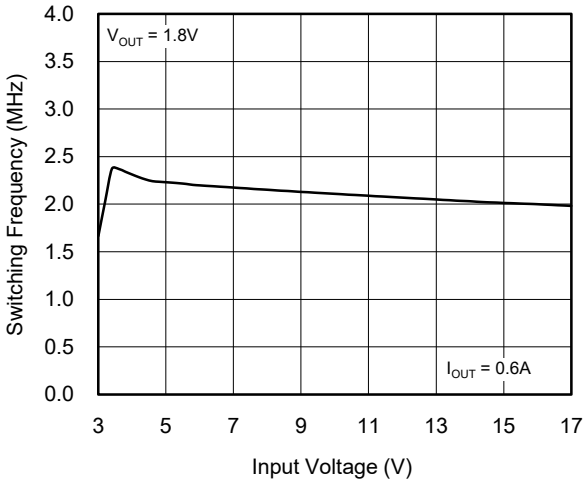
Switching Frequency vs. Input Voltage



Switching Frequency vs. Output Current



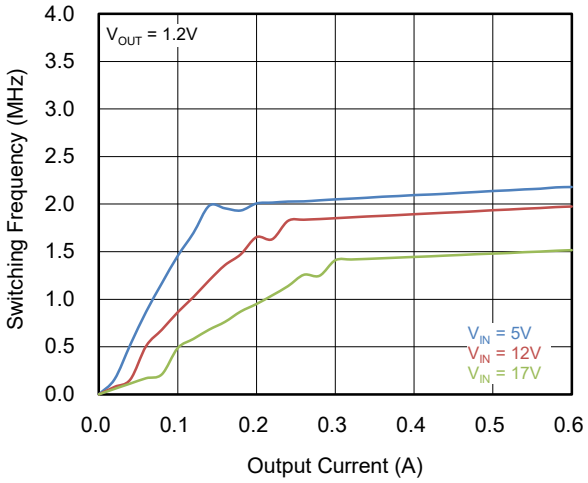
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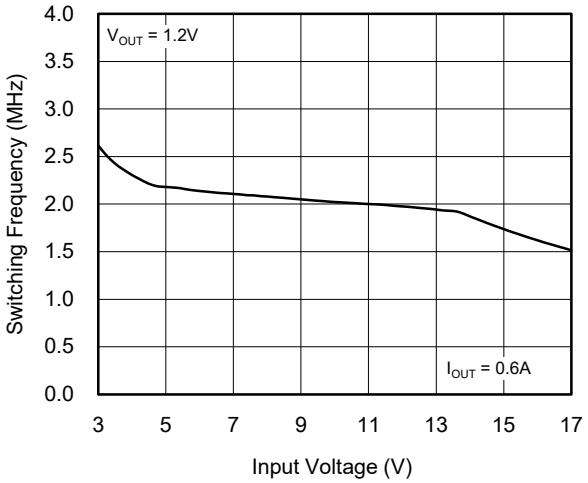
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH and DCR_{TYP} = 57mΩ, unless otherwise noted.

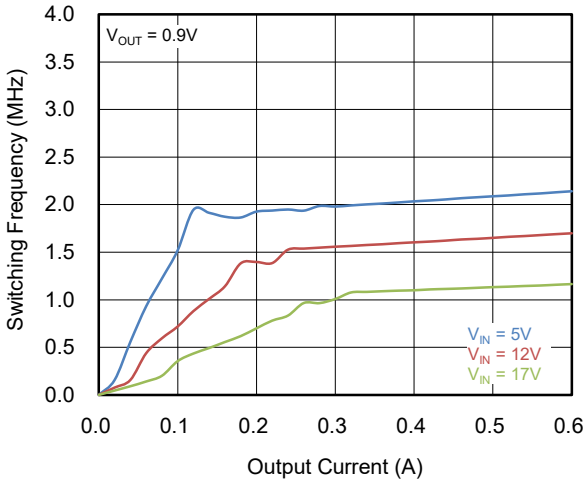
Switching Frequency vs. Output Current



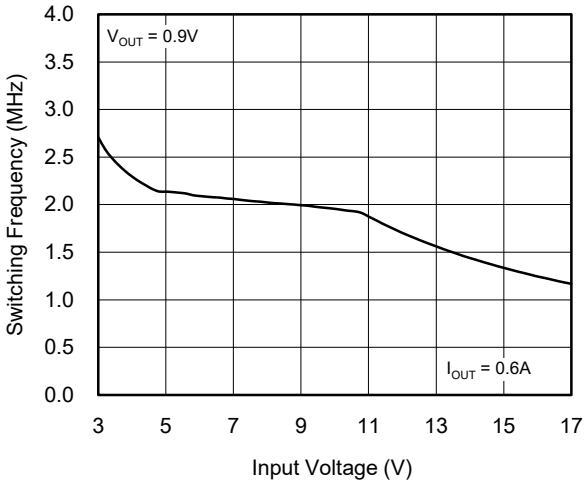
Switching Frequency vs. Input Voltage



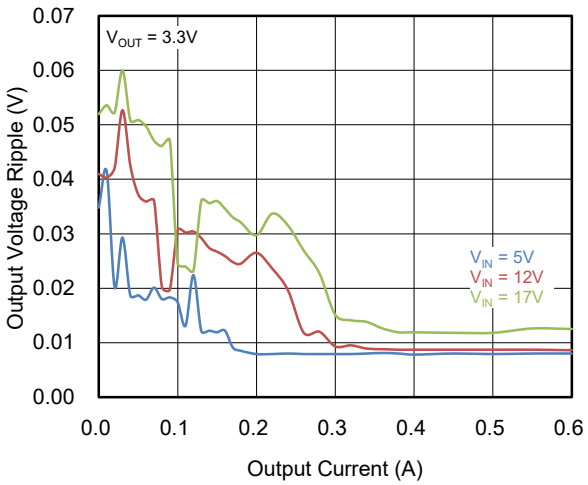
Switching Frequency vs. Output Current



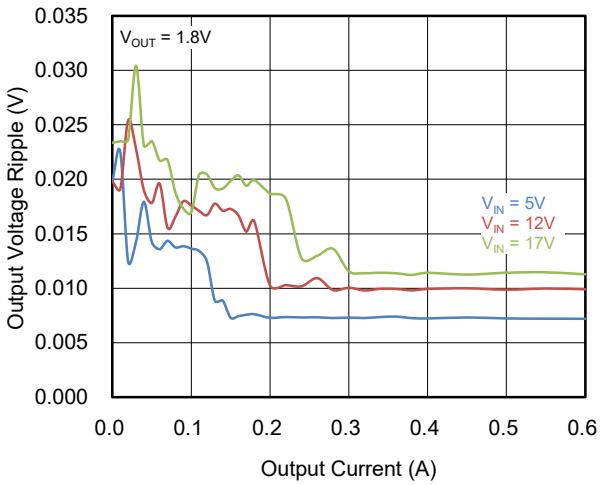
Switching Frequency vs. Input Voltage



Output Voltage Ripple vs. Output Current



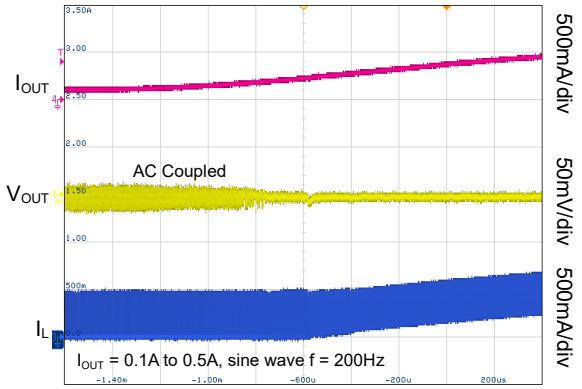
Output Voltage Ripple vs. Output Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

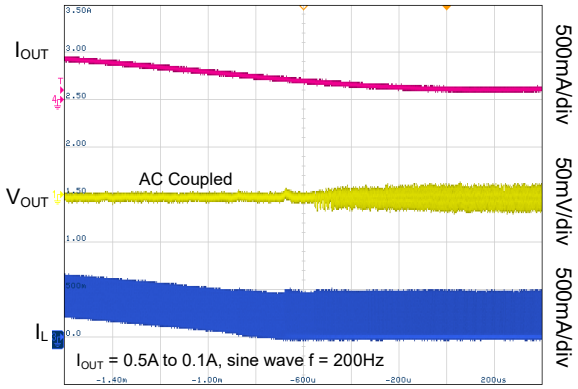
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH and DCR_{TYP} = 57mΩ, unless otherwise noted.

DCM to CCM Mode Transition



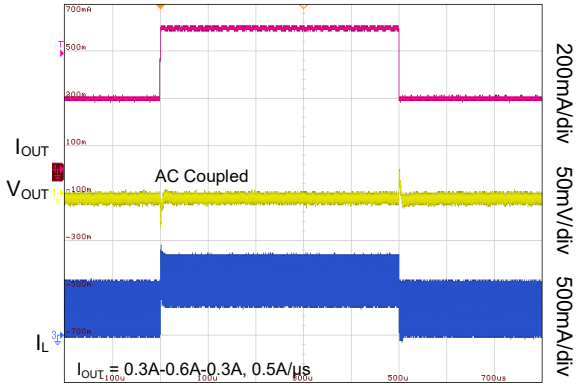
Time (200μs/div)

CCM to DCM Mode Transition



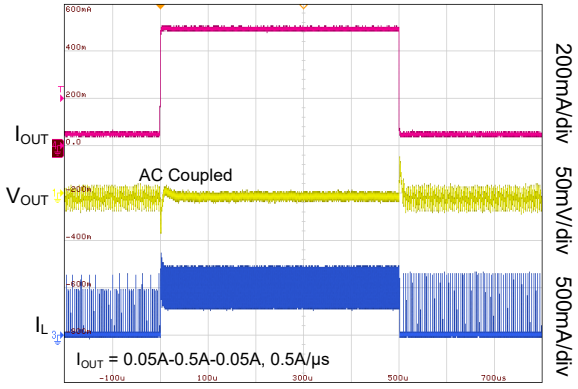
Time (200μs/div)

Load Transient Response in CCM



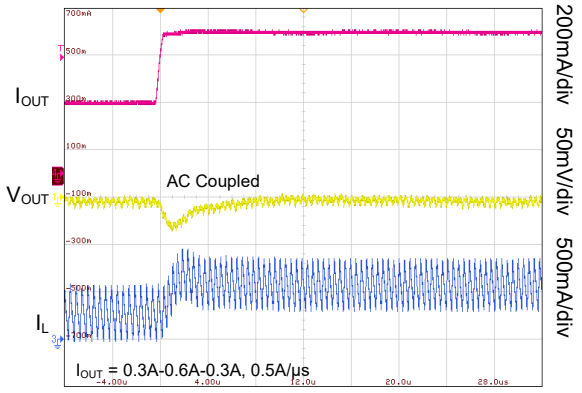
Time (100μs/div)

Load Transient Response from DCM to CCM



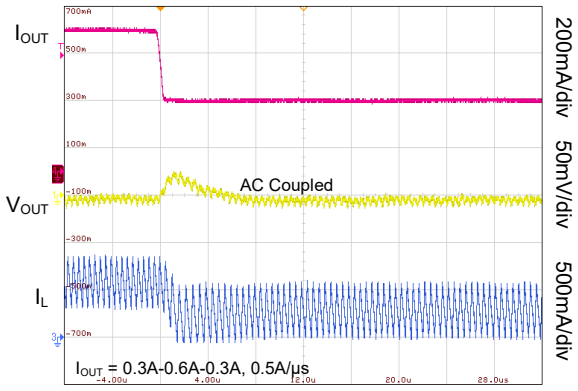
Time (100μs/div)

Load Transient Response in CCM, Rising Edge



Time (4μs/div)

Load Transient Response in CCM, Falling Edge

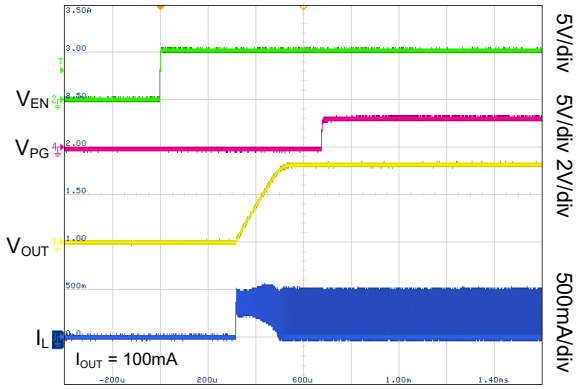


Time (4μs/div)

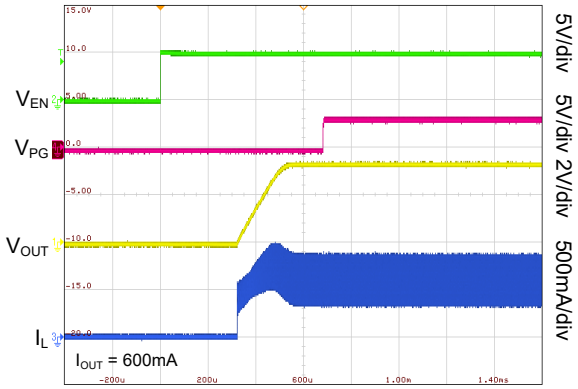
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH and DCR_{TYP} = 57mΩ, unless otherwise noted.

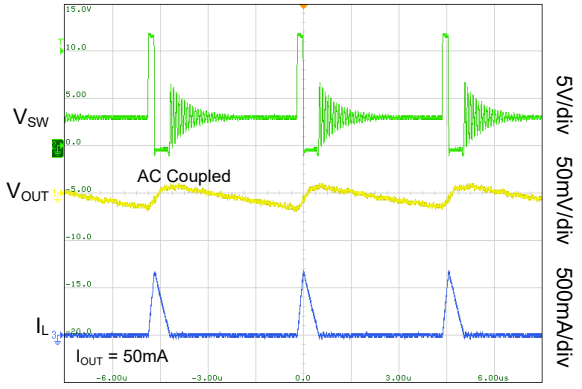
Startup with 100mA



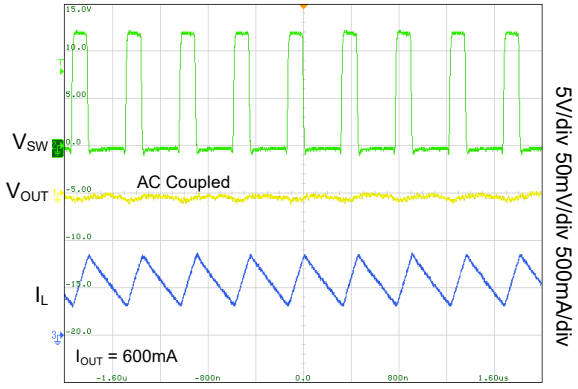
Startup with 600mA



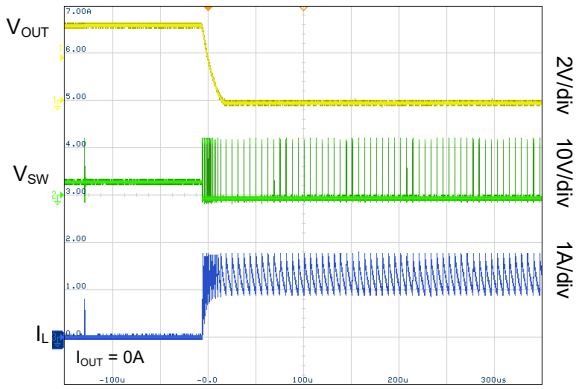
Typical Operation in Power-Save Mode



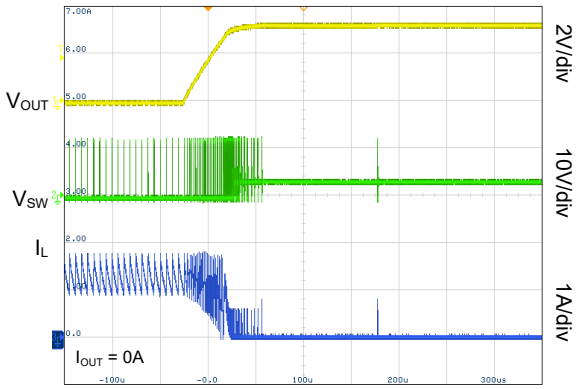
Typical Operation in PWM Mode



Current Limit with Output Short



Recover form Output Short



FUNCTIONAL BLOCK DIAGRAM

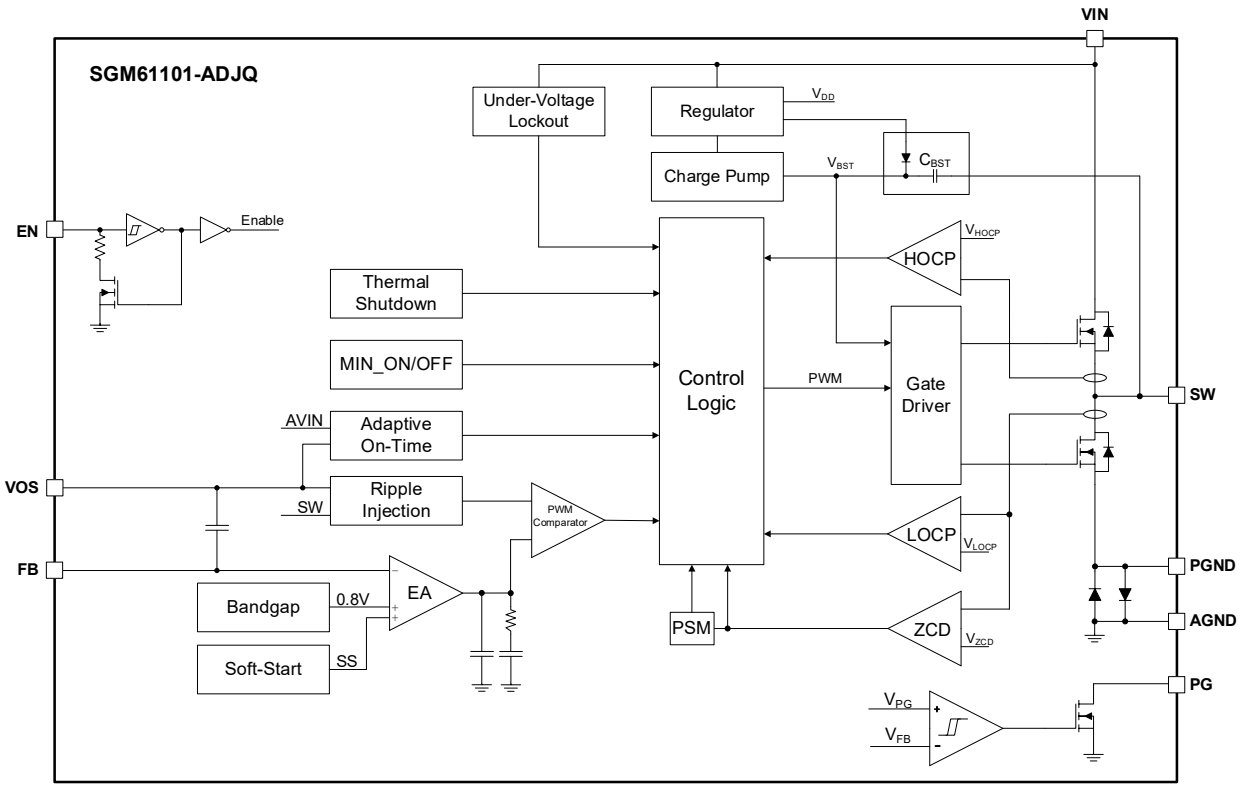


Figure 2. Block Diagram (Adjustable Output Voltage)

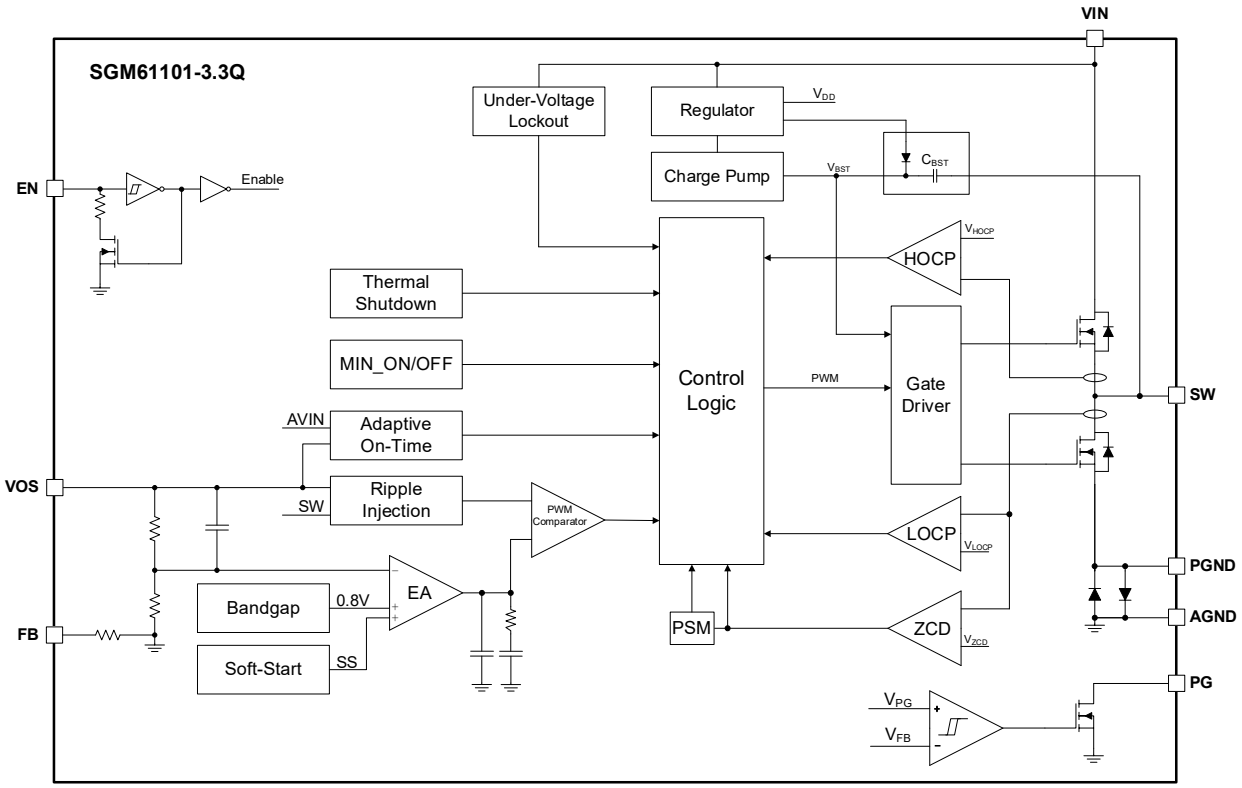


Figure 3. Block Diagram (Fixed Output Voltage)

DETAILED DESCRIPTION

Overview

SGM61101Q is a series of high-frequency, synchronous Buck converter with AHP-COT architecture and advanced regulation topology. The device works in pulse width modulation (PWM) mode at medium to heavy loads. When the load current falls, it goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current. Operation mode is seamlessly changed between PWM and PSM to keep the efficiency high in entire load range. In PWM mode, the device operates at typical 2.1MHz switching frequency.

Under-Voltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, under-voltage lockout is implemented to shut down the device when input voltage is lower than V_{UVLO} (when V_{IN} voltage falls). When the input voltage is higher than V_{UVLO}, the device will recover to normal operation with a 160mV hysteresis.

Device Enable and Disable (EN)

The SGM61101Q is enabled by setting the EN pin input to high. It is disabled when EN pin falls low. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the setting point voltage. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off to reduce the device current to 1.2μA. The EN pin is connected with a pull-down resistor to ensure that it remains at the appropriate level. When the EN is connected to a high level, the pull-down circuit is disconnected. If it keeps floating after a low level is connected, the internal pull-down resistance will remain low until the pin is connected to a high level. So the EN pin must be reliably connected to a high or low level.

Soft-Start and Pre-biased Output

A 170μs internal soft-start circuit is included to prevent input inrush current and input voltage drops during startup. This circuit slowly ramps up to the error amplifier reference voltage (V_{REF} = 0.8V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61101Q is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turning on, a bias on the output is likely to exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output voltage cannot drop too much during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device cannot be able to start up properly. During the pre-biased start, when the internal set ramp voltage is higher than the pre-biased voltage, the switch is allowed to operate, and then start normally until the output voltage reaches the given value.

Power Good (PG)

The device has PG function inside. PG is an open-drain output with a maximum sinking capacity of 2mA. Connect the pin to GND or keep it floating when it is not in use, otherwise this pin should be pulled to a logical high rail not exceeding 5.5V with an external resistor. For the SGM61101Q, the PG pin is driven to a low level, when the device is started until the output voltage reaches 95% of the set value, otherwise it is in a high impedance state. Table 1 respectively shows the PG state changes of SGM61101Q under different conditions. By connecting the PG signal to the EN pins of other converters, it can be used for sequencing of multiple tracks.

Table 1. PG Output State in Different Conditions

Device Information		PG State	
		High-Z	Low
Enable (EN = High)	$V_{FB} \geq V_{TH_PG}$	√	
	$V_{FB} \leq V_{TH_PG}$		√
Shutdown by EN (EN = Low)		√	
Thermal Shutdown	$T_J > T_{SD}$	√	
UVLO	$0.7V < V_{IN} < V_{UVLO}$	√	
Power Supply Removal	$V_{IN} < 0.7V$	√	

DETAILED DESCRIPTION (continued)

Pulse Width Modulation (PWM) Operation

In the condition of continuous conduction mode (CCM) which occurs at medium to heavy load, the device works in pulse width modulation (PWM) operation. Then a fixed on-time architecture is activated. The device operates at a nominal switching frequency of 2.1MHz (TYP).

Power-Save Mode (PSM)

As the load current decreases, the inductor current will change from continuous mode (CCM) to discontinuous mode (DCM). At this time, the on-time t_{ON} of the switch in COT mode is unchanged, and the turn-off time becomes longer, so the switching frequency decreases. When the load current is further reduced, the SGM61101Q series will enter the power saving mode (PSM). The device then maintains high efficiency by reducing the switching frequency and operating at a minimum static current. In PSM mode, the inductor current is discontinuous and the output voltage is slightly higher than the nominal output voltage. This effect can be mitigated by a larger output capacitance. The switching frequency is greatly reduced as the load current decreases in PSM mode.

When the duty cycle is small, the minimum on-time is set to limit the switching loss, in which case the circuit frequency is below the nominal value. When the input and output voltages are close, the device will remain in PWM mode, no matter how the load changes, and no longer enter PSM mode.

100% Duty Cycle

When the input voltage gradually drops to the regulation output voltage, the device can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN_MIN} = V_{OUT} + I_{OUT_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

V_{IN_MIN} is the minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is the maximum output current.

R_{DSON} is high-side MOSFET on-resistance.

R_L is inductor DC resistance (DCR).

Switch Current Limits and Short-Circuit Protection

Limiting switch current protects the switch itself and also prevents over-current sources and the inductor. When the high-side (HS) switch current exceeds the high-side switch threshold, the HS switch is off and the low-side (LS) switch is on to reduce the inductive current and limit the peak current. The switch on the high-side (HS) can be turned on again only when the switch current on the low-side (LS) is lower than the low switch threshold.

Thermal Protection and Shutdown

Thermal protection is included to protect the die against overheating damage. If the junction temperature exceeds T_{SD} threshold, the switching is stopped and the device is shut down. An automatic recovery with a soft-start begins when the junction cools down for 20℃ below the T_{SD} limit.

APPLICATION INFORMATION

In this section, power supply design with the SGM61101Q synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

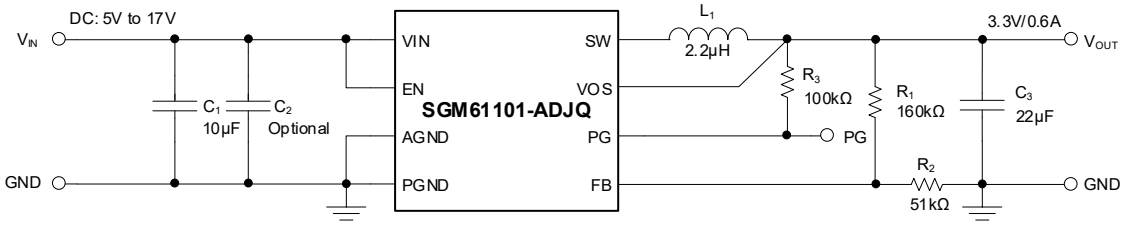


Figure 4. 3.3V Output Voltage Application of SGM61101-ADJQ

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 4. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage (SGM61101Q)	5V to 17V
Output Voltage	3.3V
Maximum Output Current	0.6A

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1	10μF,Ceramic Capacitor, 25V, Size0805	Standard
C_2	0.1μF, Ceramic Capacitor, 25V, Size 0603	Standard
C_3	22μF, Ceramic Capacitor, 6.3V, Size 0805	Standard
L_1	2.2μH, Power Inductor, DCR_{TYP} = 57mΩ, I_{SAT} = 3.2A, I_{RMS} = 2.3A	Sunlord
R_1	160kΩ, Chip Resistor,1/16W, 1%, Size 0603	Standard
R_2	51kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_3	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard

Input Capacitor Selection (C_{IN})

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. In most cases, a 10μF input capacitor is recommended, a larger value reduces input voltage ripple and improves system stability. Usually a 0.1μF low ESR ceramic capacitor is recommended to be connected between the VIN and PGND pins as closely as possible.

Inductor Selection

The important factors for inductor selection are inductance (L), saturation current (I_{SAT}), RMS rating (I_{RMS}), DC resistance (DCR) and dimensions. Use Equation 2 to find the inductor peak current (I_{L_MAX}) and peak-to-peak ripple current (ΔI_L) in static conditions:

$$I_{L_MAX} = I_{OUT_MAX} + \frac{\Delta I_L}{2}$$
$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

where:

I_{OUT_MAX} is the maximum output DC current.

ΔI_L is the inductor current ripple (peak-to-peak).

f_{SW} is switching frequency (MHz).

L is the inductance value (μH).

Usually, the peak-to-peak inductor current is selected between 10% and 40% of the maximum output current. However, under COT control, when the input voltage is high and the load is extremely low, the larger inductance value is conducive to reduce the output voltage ripple. Saturation current of the recommended inductance is higher than 120% × I_{L_MAX}. The inductor initial tolerance can be as high as -20% to +20% of the nominal value and proper current derating is usually required. More generally, choosing the saturation current above high-side limit is enough. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. Larger inductance values reduce the ripple current but lead to sluggish transient response. 2.2μH is the recommended value for the typical application.

APPLICATION INFORMATION (continued)

Output Capacitor Selection (C_{OUT})

The architecture of the SGM61101Q allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors are recommended due to the low output voltage ripple. To keep the resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. The bias voltage can cause the capacitance of the ceramic capacitor to decrease significantly, and the degree of decrease depends on the specification of the capacitor (size, nominal voltage, temperature standard).

The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value. C_{OUT} = 22μF is the recommended values for the typical application. If the switching frequency is seriously reduced due to the decrease of the input voltage, it is recommended to increase the output capacitance to ensure system stability.

Output Voltage Adjustment

Use Equation 3 for selecting the feedback resistors (R_1 and R_2) in Figure 4 to set the desired output voltage. There is a 10pF capacitance between the VOS pin and the FB pin inside the device. It forms a set of zero-pole pair with R_1 and R_2. The position of the zero-pole pair will affect the dynamic characteristics and stability of the system. Therefore, for different output voltages, please refer to the R_1/R_2 values of similar output voltages in Figure 4 to Figure 8.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R_2 \times \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (3)$$

Various Output Voltages

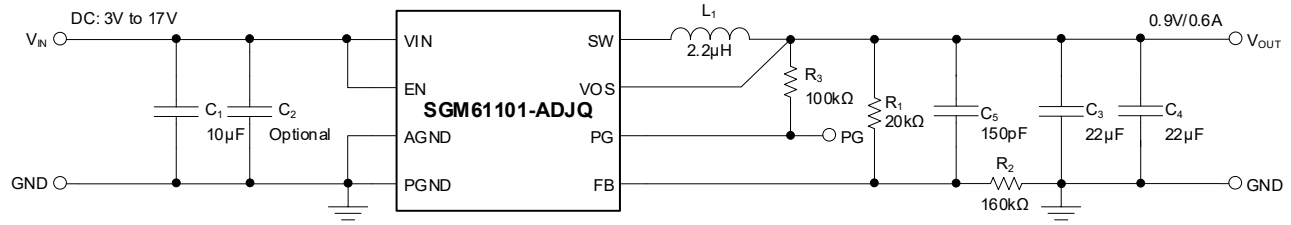


Figure 5. 0.9V Output Voltage Application of SGM61101-ADJQ

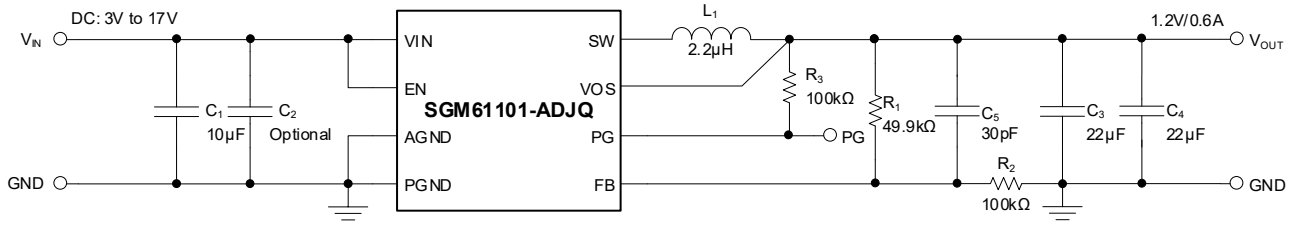


Figure 6. 1.2V Output Voltage Application of SGM61101-ADJQ

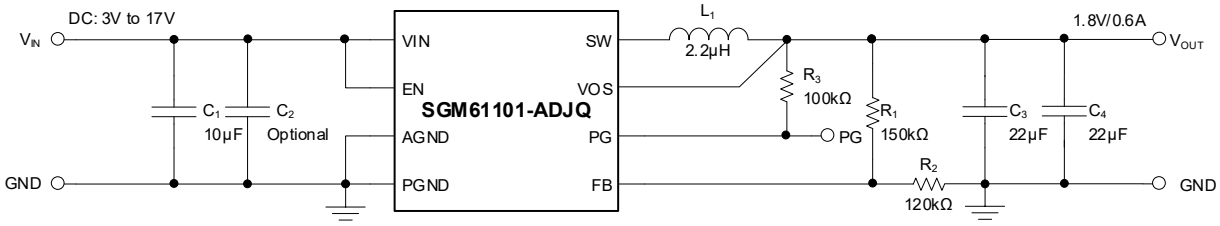


Figure 7. 1.8V Output Voltage Application of SGM61101-ADJQ

APPLICATION INFORMATION (continued)

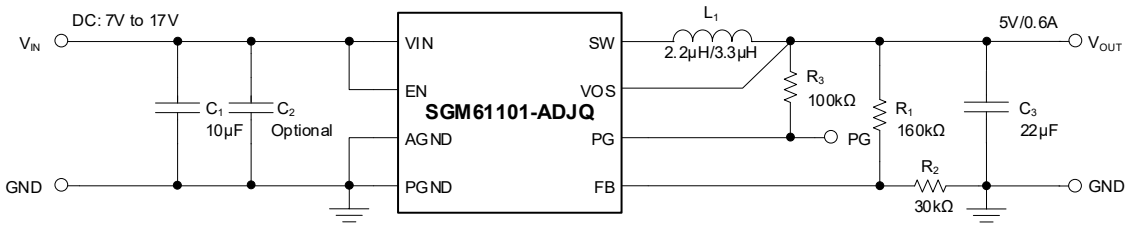


Figure 8. 5V Output Voltage Application of SGM61101-ADJQ

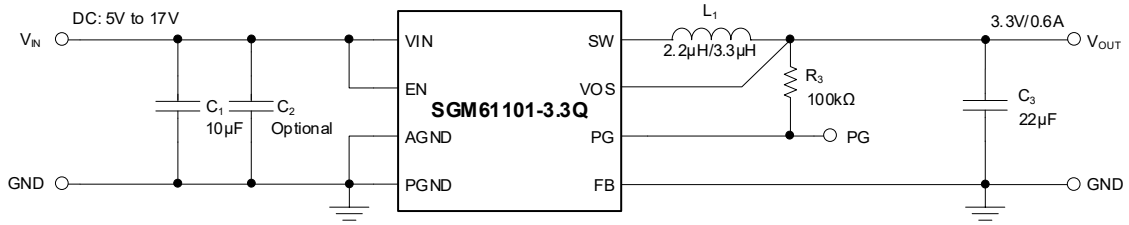


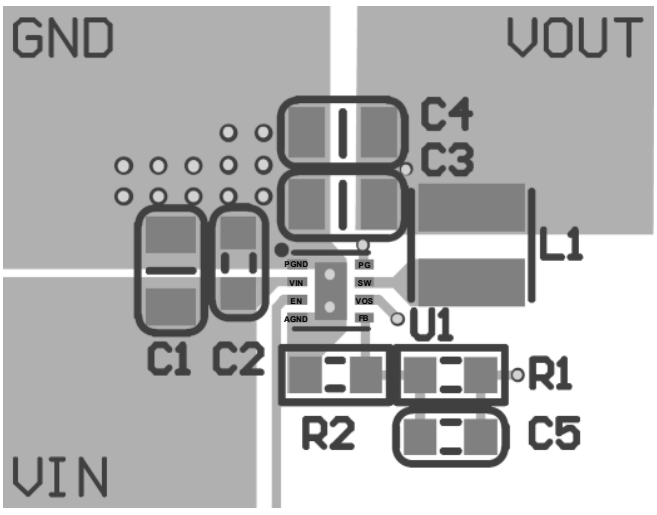
Figure 9. Application of SGM61101-3.3Q

Layout Guidelines

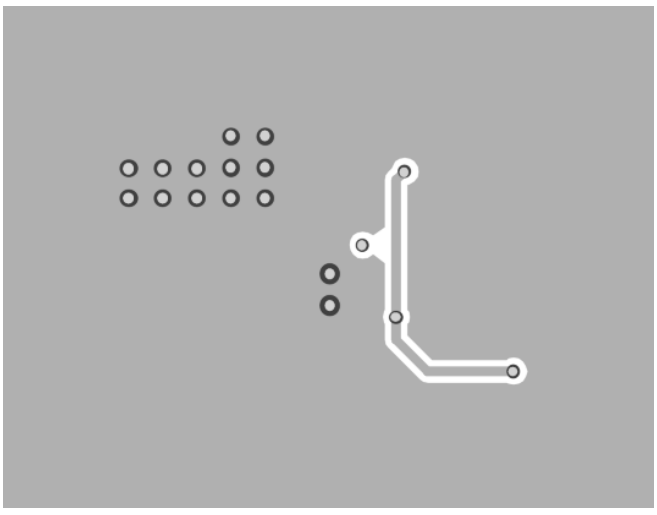
A good printed-circuit-board (PCB) layout is a critical element of any high-performance design. Follow the guidelines below for designing a good layout for the SGM61101Q.

- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device PGND pin to minimize the AC current loops.
- Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep signal traces such as FB and VOS sensing lines away from SW or other noise sources. Both of them need to be connected to VOUT by the shortest path and near the output capacitor.
- Divider resistors are placed close to the IC and connect to the AGND and FB pins directly.
- AGND pin and PGND pin need to be connected through the exposed pad for single-point grounding. In order to ensure mechanical reliability and good heat dissipation, the exposed pad must be fully welded to the circuit board.
- Use GND planes in middle layers (if used) for shielding and minimizing the ground potential drifts.

Refer to Figure 10 for a recommended PCB layout.



Top Layer



Bottom Layer

Figure 10. PCB Layout

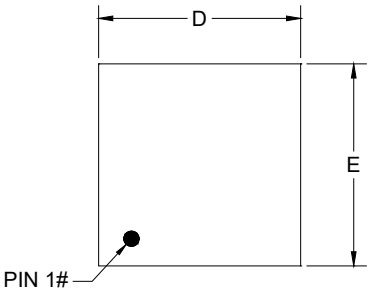
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

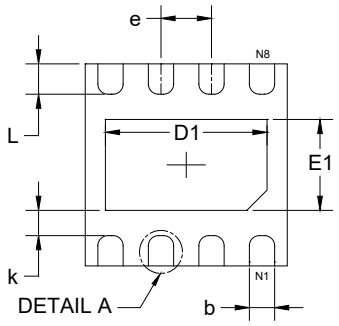
Changes from Original (NOVEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

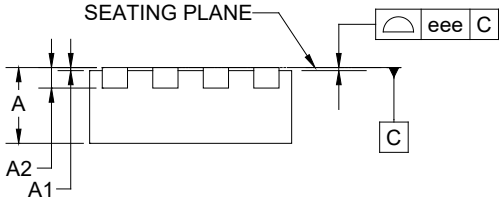
TDFN-2×2-8AL



TOP VIEW



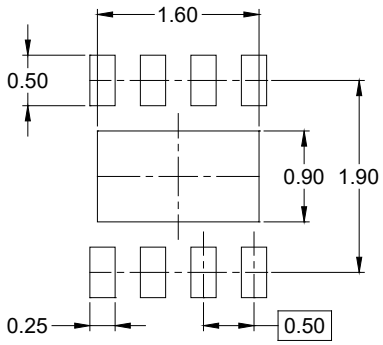
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



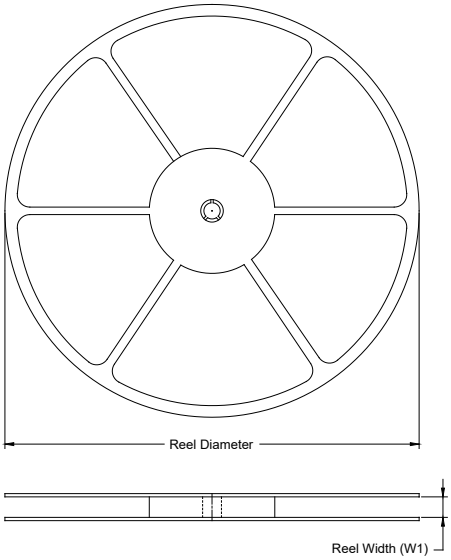
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	1.900	-	2.100
D1	1.450	-	1.700
E	1.900	-	2.100
E1	0.750	-	1.000
k	0.200	-	-
e	0.500 BSC		
L	0.200	-	0.400
eee	0.080		

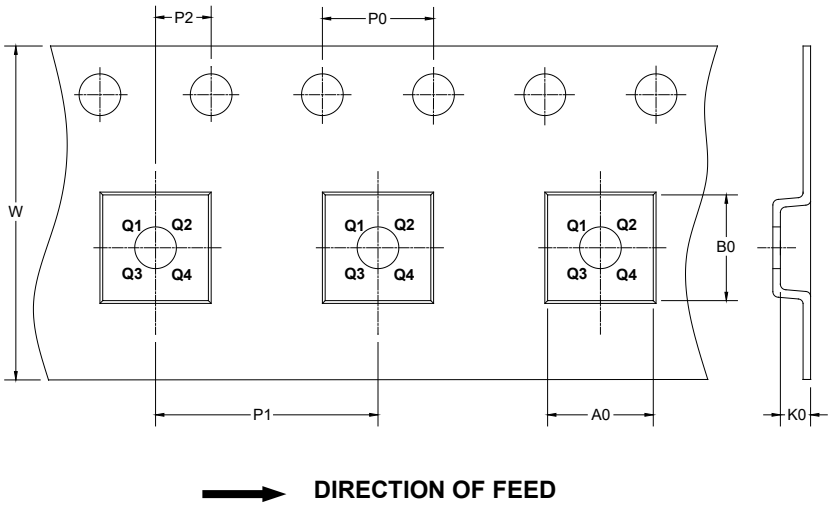
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



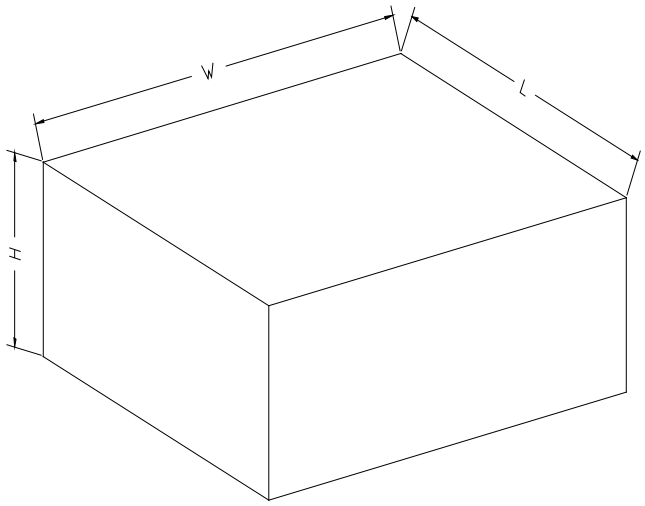
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002