MAX16141/ MAX16141A

3.5V to 36V Ideal Diode Controllers with Voltage and Current Circuit Breaker

General Description

The MAX16141/MAX16141A ideal diode controllers provide system protection against a variety of system faults, such as reverse current, reverse voltage, overcurrent, input overvoltage/undervoltage, and overtemperature conditions. The wide operating voltage range of 3.5V to 36V, combined with 5µA (typ) of shutdown current, make the MAX16141/MAX16141A ideal for automotive applications. An integrated charge pump drives the gate of the back-to-back external nFETs 9V (typ) above the source connection, minimizing power loss between the source and the load.

A fast-acting comparator allows the MAX16141/MAX16141A to block reverse-current flow within 1µs (max) of the input falling below the output voltage. An external current-sense resistor between RS and OUT provides overload monitoring capability. Two input pins, OVSET and UVSET, provide set points to protect against input overvoltage and undervoltage events using a simple resistive-divider.

During startup, the MAX16141/MAX16141A monitor the voltage drop across the external nFETs (V_{IN} - V_{OUT}) and the load current for overcurrent fault to ensure V_{OUT} is greater than 0.9 x V_{IN}. Once the startup event is complete, the MAX16141/MAX16141A are ready to protect against systems faults. During normal operation, some systems experience brownouts or short interruptions of power. To ensure smooth system recovery from these interruptions, the MAX16141/MAX16141A include a secondary power input (V_{CC}) to keep critical circuits alive. When the main input power recovers, the MAX16141/MAX16141A enable the gate in fast mode (70µs, max) to charge the output capacitor.

Both devices feature a low-power mode that is enabled with a logic input. In low-power mode the devices allow limited current flow from source to the load. For the MAX16141, the low-power mode is enabled using an active-low logic input, $\overline{SLEEP}$. For the MAX16141A, the low-power mode is activated using an active-high logic input (SLEEP).

Additional features include an internal switch that isolates the monitoring from the UVSET and OVSET resistive network in shutdown mode to help minimize system power loss.

The MAX16141/MAX16141A are available in a 4mm x 4mm x 0.75mm, 16-pin TQFN package and operate over the automotive temperature range of -40°C to +125°C.

Applications

- Automotive Power Systems
- Network/Telecom Power Systems
- RAID Systems
- Servers
- PoE Systems

Benefits and Features

- Wide Voltage Range
  - 3.5V to 36V Operating Voltage Range
  - -36V to +60V Input Protection Voltage Range
- Eliminates Discrete Diode Power Dissipation
- 5µA (typ) Shutdown Mode Current Reduces Battery Drain
- Sleep Mode Provides up to 400µA Load Current
- TERM Switch Reduces Power Consumption
- Isolates Failed Supply from Load
  - Bidirectional Current Blocking on Open
  - Bidirectional Voltage Blocking on Open
- Current Protection
  - Factory-Adjustable Overcurrent Trip Thresholds
  - Factory-Adjustable Reverse-Current Trip Thresholds
- Resistor Adjustable Overvoltage and Undervoltage Trip Thresholds
- Automotive Qualified
  - Operates down to +3.5V, Riding out Cold-Crank Conditions
  - -40°C to +125°C Operating Temperature Range
- N-Channel MOSFET Gate Driver of V_{IN} + 9V
- Fault Output
  - UVLO, OVLO, Overcurrent, Reverse-Current, Battery Reversal, and Thermal Shutdown
  - AEC-Q100 Qualified MAX16141AAF/V+T

Ordering Information appears at end of data sheet.

19-100342; Rev 9; 4/22

Typical Application Circuit

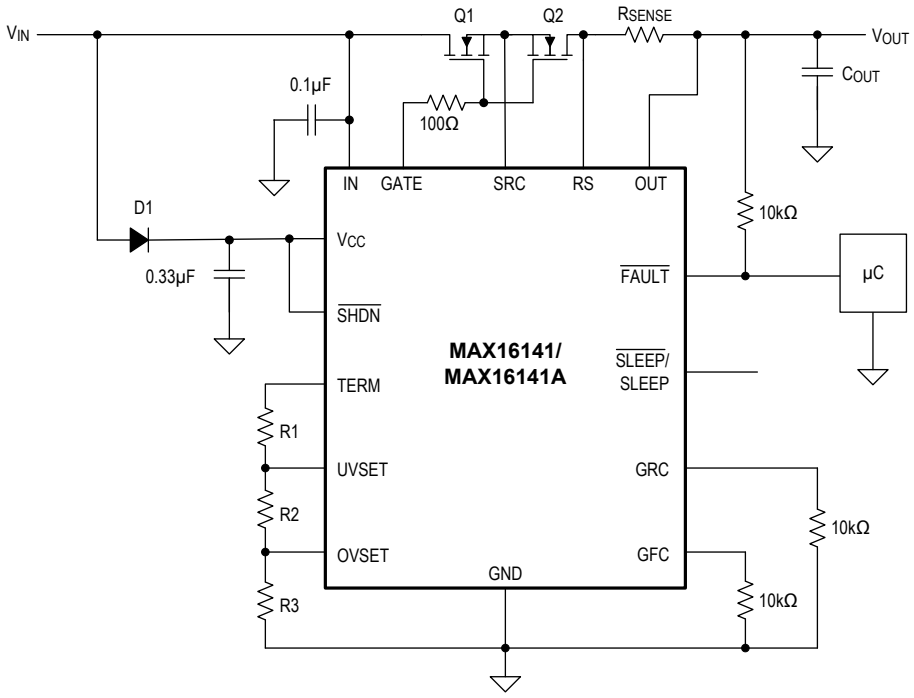


TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Typical Application Circuit . . . 2
Absolute Maximum Ratings . . . 6
Package Information . . . 6
16-TQFN . . . 6
16-TQFN . . . 6
Electrical Characteristics . . . 6
Typical Operating Characteristics . . . 10
Pin Configuration . . . 12
Pin Configuration . . . 12
Pin Descriptions . . . 12
Functional Diagram . . . 14
Detailed Description . . . 15
Device Operation . . . 15
Power-Up . . . 15
Undervoltage Protection . . . 15
Overvoltage Protection . . . 15
Overvoltage/Undervoltage Threshold Hysteresis . . . 15
Overcurrent Protection . . . 15
Ideal Diode Reverse-Current Protection . . . 16
Reverse-Voltage Protection . . . 16
Thermal Shutdown Protection . . . 16
GATE Ramp-Up Control . . . 16
GATE Ramp-Down Control . . . 16
Sleep Mode . . . 16
Gate Charge Pump . . . 17
TERM Connection . . . 17
FAULT Output . . . 17
Auto-Retry . . . 18
Applications Information . . . 19
Setting Overvoltage/Undervoltage Threshold . . . 19
Reverse-Voltage Protection . . . 20
Ovecurrent Threshold Setting . . . 22
Short Power Interruptions . . . 22
Gate Rise Time Control . . . 23
MOSFET Selection . . . 24
MOSFET Power Dissipation . . . 24

TABLE OF CONTENTS (CONTINUED)

Selector Guide 25
Typical Application Circuit 26
Typical Automotive Application Circuit 26
Ordering Information 26
Revision History 27

LIST OF FIGURES

Figure 1. Sleep Mode Operation 17
Figure 2. UVSET and OVSET Threshold Setting 20
Figure 3. Reverse-Voltage Fault 21
Figure 4. Recommended Reverse-Voltage Protection Circuit 22
Figure 5. Short Power Interruption and Recover 23
Figure 6. Gate Voltage Slow to Fast-Mode Transition 24
Figure 7. Selector Guide 25

Absolute Maximum Ratings

V_{IN} to GND ..... -36V to +60V
V_{CC}, SHDN, FAULT, RS OUT to GND ..... -0.3V to +60V
RS, OUT to GND ..... -0.3V to +60V
V_{IN} to V_{CC}, V_{IN} to SHDN, V_{IN} to TERM ..... -45V to +60V
SRC, GATE to GND ..... -36V to +50V
SRC to GATE, RS to OUT ..... -36V to +36V
V_{IN} to V_{OUT} ..... -60V to +60V
TERM to V_{CC} ..... -60V to +1V
SLEEP, OVSET, UVSET, GRC, GFC, to GND ..... -0.3V to +6V

Continuous Sink/Source Current (all pins except FAULT) ..... ±20mA
FAULT Continuous Sink/Source Current ..... ±5mA
Continuous Power Dissipation (TQFN 16-Pin derate 25mW/°C above +70°C.) ..... to 2000mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16-TQFN

Package Code	T1644+4A
Outline Number	21-0139
Land Pattern Number	90-0070
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	59.30°C/W
Junction to Case (θ_{JC})	6°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	40
Junction to Case (θ_{JC})	6

16-TQFN

Package Code	T1644Y+4
Outline Number	21-100267
Land Pattern Number	90-0070
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	40°C/W
Junction to Case (θ_{JC})	6°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 12V, $C_{GATE-SRC}$ = 7nF, C_{VCC} = 0.33µF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All specs are subject to change.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		V_{IN} and V_{CC}	Operating range	3.5		36	V

Electrical Characteristics (continued)

(V_{IN} = 12V, $C_{GATE-SRC}$ = 7nF, C_{VCC} = 0.33µF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All specs are subject to change.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Protection Voltage Range	V_{IN}		-36		+60	V
INPUT SUPPLY CURRENT						
Input Supply Current	I_{IN}	V_{SHDN} = high, V_{IN} = V_{SRC} = V_{OUT} = 12V		2.0	3.8	mA
		V_{SHDN} = high, V_{IN} = V_{SRC} = V_{OUT} = 36V		2.1	4.0	
		V_{SHDN} = low, V_{IN} = 12V		5	10	µA
		V_{SHDN} = low, V_{IN} = 36V		6	15	
Sleep Mode Supply Current	I_{SLEEP}	Internal PFET on, charge pump off		10	15	µA
SRC Input Current	I_{SRC}	V_{IN} = 12V, $\overline{SHDN}$ = high		1	2	mA
Undervoltage Lockout	UVLO	V_{IN} rising			3.3	V
OVSET/UVSET Input Current					1.5	µA
OVSET/UVSET Threshold		V_{IN} rising	0.485	0.5	0.515	V
OVSET Threshold Hysteresis	V_{OV_HYS}	MAX16141AAF, MAX16141AAAF, MAX16141ADF/V, MAX16141BAF/V		0.05 x V_{OV_TH}		V
UVSET Threshold Hysteresis	V_{UV_HYS}	MAX16141AAF, MAX16141AAAF, MAX16141ADF/V, MAX16141BAF/V		0.2 x V_{UV_TH}		V
TERM On-Resistance	R_{TERM}			0.7	1.3	kΩ
Startup Response Time	t_{SU}			450		µs
OVSET to GATE Prop Delay		V_{OVSET} rising from (V_{TH_OV} - 100mV) to (V_{TH_OV} + 100mV)		10		µs
UVSET to GATE Prop Delay		V_{UVSET} falling from (V_{UV_TH} + 100mV) to (V_{UV_TH} - 100mV)		20		µs
OVSET to $\overline{FAULT}$ Prop Delay	t_{OV}	V_{OVSET} rising from (V_{OV_TH} - 100mV) to (V_{OV_TH} + 100mV)		0.3		µs
GATE OUTPUT VOLTAGE						
GATE Output Voltage High Above V_{SRC}	V_{GS}	V_{IN} = V_{SRC} = V_{OUT} = 3.5V, I_{GATE} = -1µA	5	6.3	8	V
		V_{IN} = V_{SRC} = V_{OUT} = 12V, I_{GATE} = -1µA	8	9	11	
		V_{IN} = V_{SRC} = V_{OUT} = 24V, I_{GATE} = -1µA	7	8.5	11	
		V_{IN} = V_{SRC} = V_{OUT} = 36V, I_{GATE} = -1µA	6.25	8	11	
GATE Charge Pump Current	I_{GATE}	V_{IN} = V_{GATE} = V_{SRC} = 12V		1200		µA
$\overline{SHDN}$, $\overline{SLEEP}$ Logic-High Input Voltage	V_{IH}		1.4			V
$\overline{SHDN}$, $\overline{SLEEP}$ Logic-Low Input Voltage	V_{IL}				0.4	V
$\overline{SHDN}$ Input Pulse Width	t_{PW_SHDN}		6			µs
$\overline{SHDN}$ Input Pulldown Current	I_{SPD}			0.1	1.2	µA

Electrical Characteristics (continued)

(V_{IN} = 12V, $C_{GATE-SRC}$ = 7nF, C_{VCC} = 0.33µF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All specs are subject to change.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{FAULT}$ Ouput Voltage Low	V_{OL}	$\overline{FAULT}$ sinking 1mA				0.4	V
$\overline{FAULT}$ Leakage Current	I_{IL}	$V_{\overline{FAULT}}$ = 12V				0.5	µA
OUT Input Resistance	R_{OUT}				4		MΩ
REVERSE-CURRENT THRESHOLD							
Reverse-Current Threshold Voltage	V_{REV}	V_{IN} < V_{OUT} (MAX16141AAF, MAX16141AAAF, MAX16141BAF/V)		7	10	14	mV
		V_{IN} < V_{OUT} (MAX16141ADF/V)		30	40	52	
Reverse Current-Blocking Response Time	t_{REV}	Overdrive threshold voltage = 40mV			0.3	1	µs
Fast Reverse Recovery Turn-On Time (*Note 2*)	t_{REV_FAST}	Gate rise from GND to V_{SRC} + 3.5V, C_{GS} = 7nF (*Note 1*)	100Ω from GATE to gate of the MOSFETs			70	µs
OVERCURRENT THRESHOLDS							
Overcurrent Threshold (*Note 2*)	$V_{(RS-OUT)}$	MAX16141(A)A__		22.5	25	27.5	mV
		MAX16141(A)B__		45	50	55	
		MAX16141(A)C__		67.5	75	82.5	
		MAX16141(A)D__		90	100	110	
Overcurrent Response Time		Comparator overdrive = 40mV, response time is measured from overcurrent event to $\overline{FAULT}$ pulling low				0.5	µs
Thermal Shutdown	TH_{SHDN}				+145		°C
Thermal Shutdown Hysteresis	TH_{SHDN_HYS}				15		°C
Power-OK Threshold		V_{OUT} rising			0.9 x V_{IN}		V
Power-OK Threshold		V_{OUT} falling			0.87 x V_{IN}		V
GATE RAMP RATE CONTROL CURRENT							
Gate Rise Time		R_{GRC} = 10kΩ, gate rising from ground to SRC + 3.5V			10		ms
		R_{GRC} = 20kΩ, gate rising from ground to SRC + 3.5V			20		
		R_{GRC} = 40kΩ, gate rising from ground to SRC + 3.5V			40		
GATE RAMP DOWN							
Gate Fall Time		R_{GFC} = 20kΩ, GATE is falling from (V_{SRC} + 8V) to V_{SRC}		200			µs
		R_{GFC} = 10kΩ, GATE falling from (V_{SRC} + 8V) to V_{SRC}		100			
GATE Pulldown Current		Active during reverse bias detection to achieve 1µs (max) response time			0.280		A

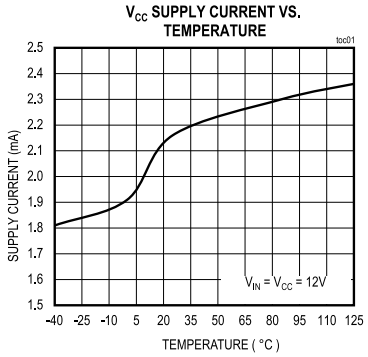
Note 1: Tested with MOSFETs, NVD6824NL.

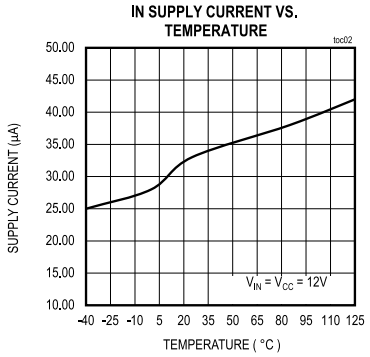
Note 2: Guaranteed by design and bench characterization.

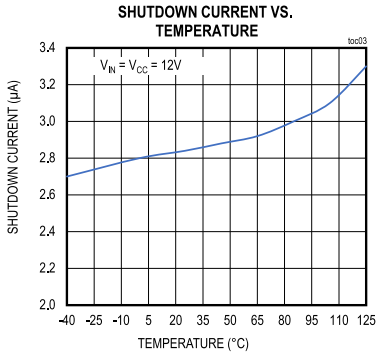
Note 3: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

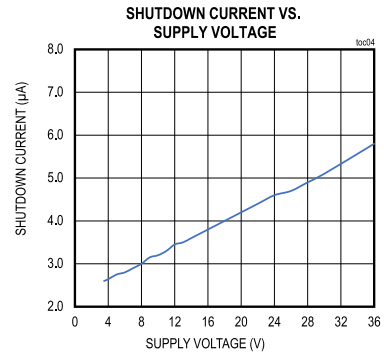
Typical Operating Characteristics

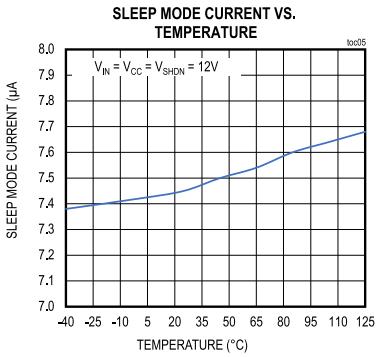
(V_{IN} = V_{CC} = 12V, C_{VCC} = 0.33µF, T_A = -40°C to +125°C, unless otherwise noted.)

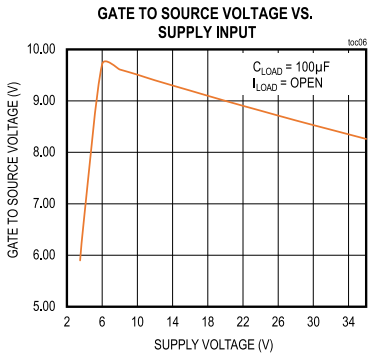


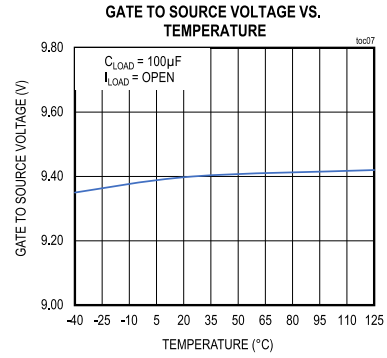


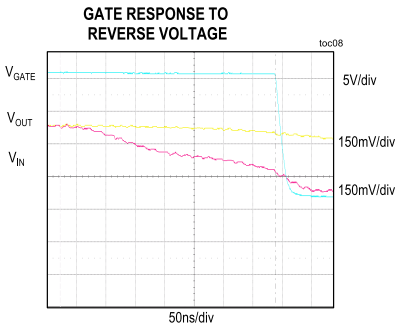


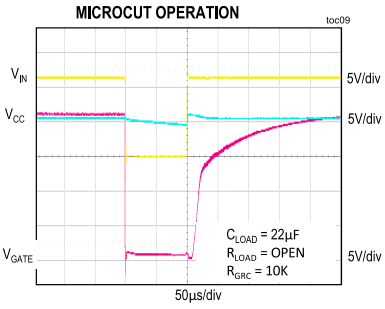








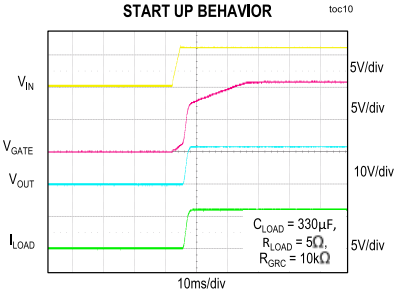




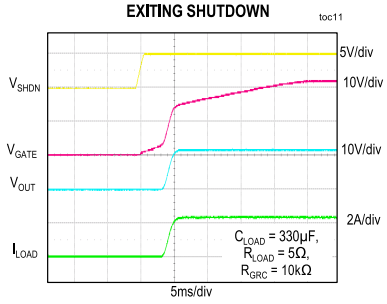
Typical Operating Characteristics (continued)

(V_{IN} = V_{CC} = 12V, C_{VCC} = 0.33µF, T_A = -40°C to +125°C, unless otherwise noted.)

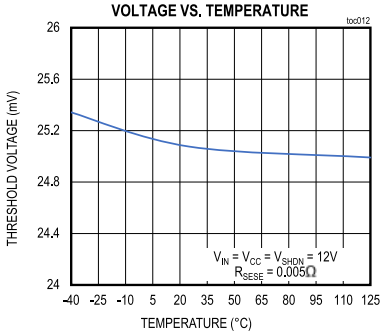
START UP BEHAVIOR



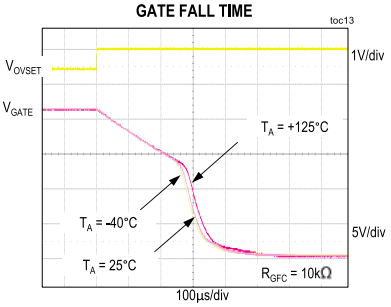
EXITING SHUTDOWN



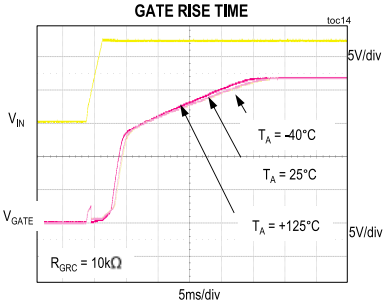
CURRENT-SENSE THRESHOLD VOLTAGE VS. TEMPERATURE



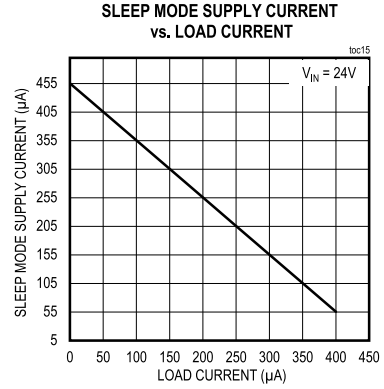
GATE FALL TIME



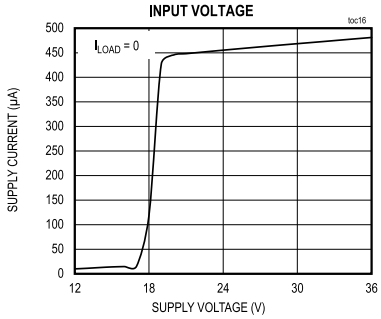
GATE RISE TIME



SLEEP MODE SUPPLY CURRENT vs. LOAD CURRENT

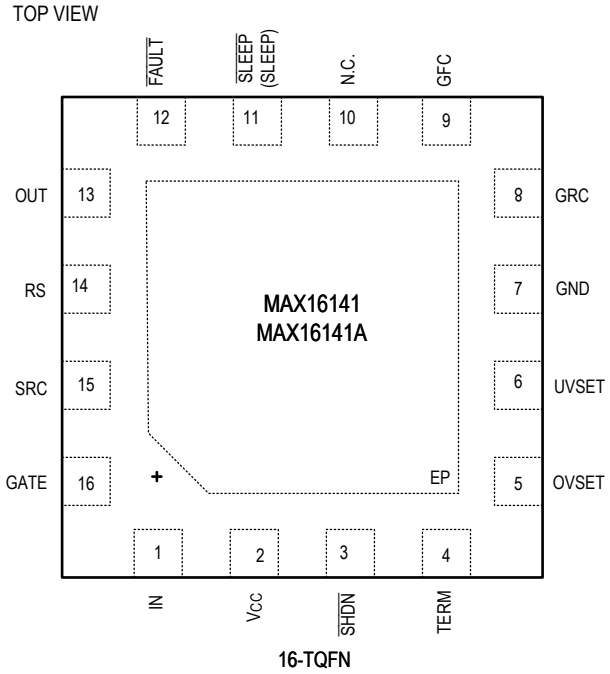


SLEEP MODE CURRENT vs. INPUT VOLTAGE



Pin Configuration

Pin Configuration



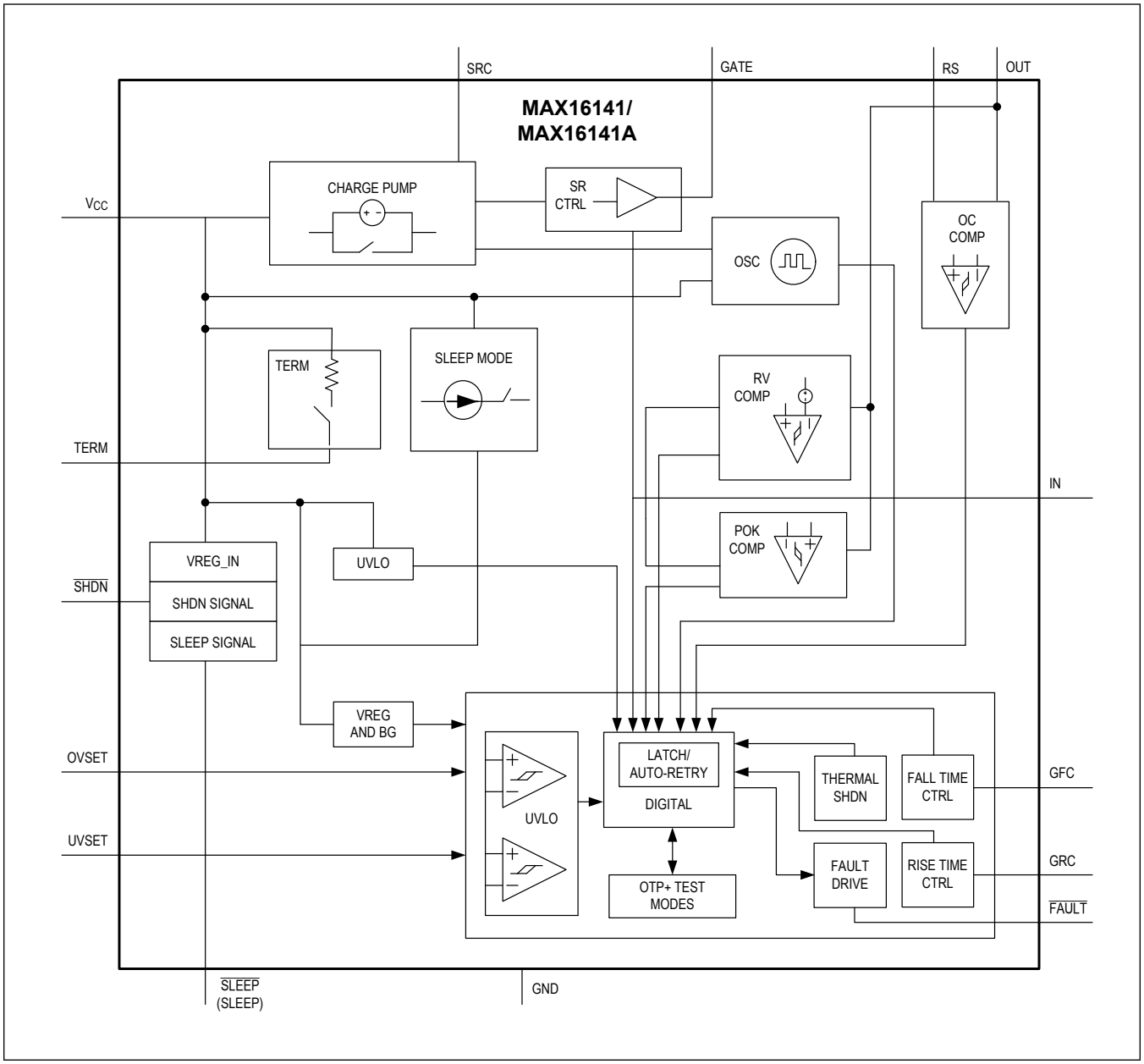
Pin Descriptions

PIN	NAME	FUNCTION
1	IN	Sense Input. Bypass IN with a 0.1µF ceramic capacitor to GND.
2	V_{CC}	Auxiliary Power Input. V_{CC} provides power to the MAX16141/MAX16141A during a short interruption of power at IN. Connect V_{CC} to IN through a diode and 0.33µF bypass capacitor to ground.
3	$\overline{SHDN}$	Active-Low Shutdown Input. Drive $\overline{SHDN}$ low to drive GATE low and TERM to high-impedance state. Drive $\overline{SHDN}$ high for normal operation.
4	TERM	UVSET/OVSET Voltage-Divider Termination Output. TERM is internally connected to V_{CC} through a switch. Connect TERM to the high-side of the UVSET/OVSET resistive-divider network for undervoltage and overvoltage settings. TERM remains off during sleep mode.
5	OVSET	Overvoltage Threshold Adjustment Input. Connect a resistive-divider from TERM to OVSET and GND to set the overvoltage threshold.
6	UVSET	Undervoltage Threshold Adjustment Input. Connect a resistive-divider from TERM to UVSET and GND to set the undervoltage threshold.
7	GND	Ground
8	GRC	Gate Rise Control Input. Connect a resistor from GRC to ground to set the gate rise time. See the *Electrical Characteristics* table for appropriate resistor values.
9	GFC	Gate Fall Control Input. A resistor from GFC to ground allows the MAX16141/MAX16141A to disable the gate slower in the event of an overvoltage fault. See the *Electrical Characteristics* table for appropriate resistor values.
10	N.C.	No Connect. Connect to ground.

Pin Descriptions (continued)

PIN	NAME	FUNCTION
11	$\overline{SLEEP}$/SLEEP	Sleep Mode input. In sleep mode, the gate drive and TERM switch are disabled. Power to the load flows through an internal low-power switch, SRC, and body diode of Q2. In the MAX16141, sleep mode input is active low ($\overline{SLEEP}$) and in the MAX16141A, sleep mode input is active high (SLEEP). See Figure 1 for more detail.
12	$\overline{FAULT}$	Active-Low, Open-Drain Fault Output. $\overline{FAULT}$ requires a pullup resistor.
13	OUT	Load Current/Output Voltage Sense Input. OUT is internally connected to a current-sense comparator input and a voltage comparator. During normal operation, the MAX16141/MAX16141A monitor the overcurrent conditions using a sense resistor between RS and OUT. During the reverse-voltage condition, the MAX16141/MAX16141A enter a fault mode when the voltage between OUT and IN exceeds the set threshold. For accurate overcurrent monitoring, use a Kelvin connection from R_{SENSE} to OUT.
14	RS	Current-Sense Positive Input. RS is internally connected to the positive input of a current-sense resistor. Connect a sense resistor between RS and OUT to set the overload threshold. For accurate overcurrent monitoring, use a Kelvin connection from R_{SENSE} to RS.
15	SRC	Source Input. Connect SRC to the common source connection of the external n-channel MOSFETs. An external zener diode between SRC and GATE protects the gates of the external MOSFETs.
16	GATE	Gate-Driver Output. Connect GATE to the gates of the external n-channel MOSFETs. GATE is the charge-pump output during normal operation. GATE is quickly pulled low during a fault condition or when $\overline{SHDN}$ is pulled low.
—	EP	Exposed Pad. Connect EP to a contiguous ground plane.

Functional Diagram



Detailed Description

Device Operation

The MAX16141/MAX16141A are ideal diode controllers featuring several system-level protections, such as reverse-current, overcurrent, overvoltage, undervoltage, and overtemperature faults. The MAX16141/MAX16141A consume only 5µA (typ) in shutdown mode. During a reverse-voltage condition, $V_{OUT} > V_{IN}$, the MAX16141/MAX16141A disable the gate within 1µs (max) of V_{IN} falling below V_{OUT} by the factory-set threshold.

An internal charge pump drives the gate 9V (typ) above the source voltage to fully turn on two external back-to-back N-channel FETs, minimizing power dissipation and voltage drop across the FETs. The MAX16141/MAX16141A monitor the load current using a sense resistor between between RS and OUT and protect against reverse current flow when V_{IN} fall below V_{OUT}. These devices feature gate ramp rate control to provide correct operation in a variety of situations. For example, the ramp-up during power-up can be adjusted to avoid excessive inrush current. In the case of an overvoltage fault, the ramp down rate is slow enough to avoid large inductive transients when interrupting high fault currents. On the other hand, the gate drive responds quickly to transient shorts of the input to ground, thereby preventing discharge of the load-side capacitance. When the input recovers, the gate drive ramps up quickly enough to provide power to the load before the load voltage can drop excessively.

Power-Up

At power-up, the MAX16141/MAX16141A enable the gate drive 450µs (t_{SU}) after the input voltage crosses the undervoltage threshold. During power-up, the gate's rise time is determined by value of resistor connected between GRC and GND while $\overline{FAULT}$ remains low and goes high-impedance when the output voltage is greater than 90% of V_{IN} if no fault condition is present.

Undervoltage Protection

The MAX16141/MAX16141A monitor the input voltage for undervoltage fault. An external resistive divider connected between TERM, UVSET, and GND sets the undervoltage threshold. (TERM is connected to V_{CC} through a switch when $\overline{SHDN}$ is high.) When the input voltage falls below the undervoltage threshold ($V_{CC} = V_{IN} < V_{UVTH} - V_{HYS}$), the MAX16141/MAX16141A pull the gate voltage low, turning off the external MOSFETs, and $\overline{FAULT}$ asserts. When the input voltage rises above the undervoltage threshold ($V_{CC} = V_{IN} > V_{UVTH}$), GATE goes high after a 450µs startup delay (typ).

Overvoltage Protection

The MAX16141/MAX16141A detect overvoltage conditions using an external resistive divider connected between TERM, OVSET, and GND. (TERM is connected to V_{CC} through a switch when $\overline{SHDN}$ is high.) When the input voltage exceeds the programmed overvoltage threshold, the MAX16141/MAX16141A pull GATE to ground and isolate the load from the source voltage. The falling ramp rate of the gate voltage is determined by the value of the resistor connected between GFC and ground. See the *Electrical Characteristics* table for GATE's fall times vs. resistor values. During the overvoltage fault condition, GATE latches low and $\overline{FAULT}$ stays asserted.

Overvoltage/Undervoltage Threshold Hysteresis

The MAX16141/MAX16141A offer six factory-set overvoltage/undervoltage threshold hysteresis options. See Figure 7 for available options.

Overcurrent Protection

The MAX16141/MAX16141A detect an overcurrent fault condition using a sense resistor between RS and OUT. When the load current exceeds the factory-set threshold, the MAX16141/MAX16141A isolate the load from the input and disable GATE low with a slow falling ramp rate, as selected by the resistor value between GFC and ground. See the *Electrical Characteristics* table for GATE's fall times vs. resistor values. During the overcurrent fault condition, GATE enters the 300ms (typ) auto-retry mode while $\overline{FAULT}$ stays asserted. Upon on the termination of an overcurrent fault condition, the MAX16141/MAX16141A pull the gate voltage high and allow $\overline{FAULT}$ to deassert.

The MAX16141/MAX16141A offer four factory-set overcurrent threshold options. See Figure 7 for available options.

Ideal Diode Reverse-Current Protection

The MAX16141/MAX16141A detect reverse-current conditions using a comparator that monitors the differential voltage between IN and OUT. When V_{IN} falls below V_{OUT} by the factor-set thresholds, the MAX16141/MAX16141A disable the gate drive within 1µs (max) to minimize load discharge into the source. The gate drive is enabled once the input rises above the output voltage by 50mV. The MAX16141/MAX16141A offer four factory-set reverse-current thresholds. See Figure 7 for available options.

Reverse-Voltage Protection

The MAX16141/MAX16141A offer reverse-voltage protection to prevent damage to the downstream circuitry caused by battery reversal or negative transients at the input. The input voltage (IN) withstands reverse voltage down to -36V below ground. When V_{IN} is forced below ground, an internal circuit blocks the current flow from GND to IN to protect the MAX16141/MAX16141A during negative transients events. During a reverse-voltage condition, the gate drive is disabled within 1µs (max) to isolate the load from the source.

Note: *GATE is internally connected to SRC through a 15MΩ resistor. Connecting GATE to lower input impedance nodes forms a resistive divider between IN, GATE, and GND and keeps the external FETs on.*

Thermal Shutdown Protection

The MAX16141/MAX16141A include thermal shutdown protection that turns off the external MOSFETs if the internal die temperature exceeds +145°C (T_J). By ensuring good thermal coupling between the MOSFETs and the MAX16141/MAX16141A, the thermal shutdown can turn off the MOSFETs if they overheat. When the junction temperature exceeds T_J = +145°C (typ), the internal thermal sensor signals the shutdown logic, pulling the GATE voltage low and allowing the device to cool. The MAX16141/MAX16141A isolate the load from the input by pulling the gate to ground with a slow falling ramp rate to prevent transient overshoots beyond the input protection voltage and assert $\overline{FAULT}$. When T_J drops by 15°C (typ), GATE goes high with a slow rising ramp rate and the MOSFETs turn back on. Do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

GATE Ramp-Up Control

To ensure proper power-up, the MAX16141/MAX16141A offer three different gate rise times set with a resistor connected from GRC to GND. See the *Electrical Characteristics* table for more detail. The gate's controlled rise time ensures soft-start with limited inrush current and is active during power-up, when exiting shutdown, recovering from undervoltage, overvoltage, and thermal faults.

Note: *The values in the Electrical Characteristics table are determined based on a 7nF gate-to-source capacitance. Depending on the gate-to-source capacitance, the rise time of the gate will be different.*

GATE Ramp-Down Control

The MAX16141/MAX16141A control the gate fall time using a resistor from GFC to ground. See the *Electrical Characteristics* table for allowed resistor values. The gate's fall-time control remains active during overvoltage, overcurrent, and thermal shutdown faults.

Sleep Mode

Sleep mode is a low-power mode that allows the MAX16141/MAX16141A to deliver power to the load using an internal low power MOSFET. In sleep mode, the MAX16141/MAX16141A deliver up to 400µA of current to the load while consuming only 10µA (typ). Load currents higher than 400µA force the MAX16141/MAX16141A to go into constant current mode and cause the output voltage to droop. During sleep mode, the charge pump and TERM switch are disabled. The load current flows through the internal MOSFET, SRC, and body diode of Q2. See Figure 1 for more detail. The MAX16141 features an active-low logic input ($\overline{SLEEP}$), and the MAX16141A features an active-high logic input (SLEEP).

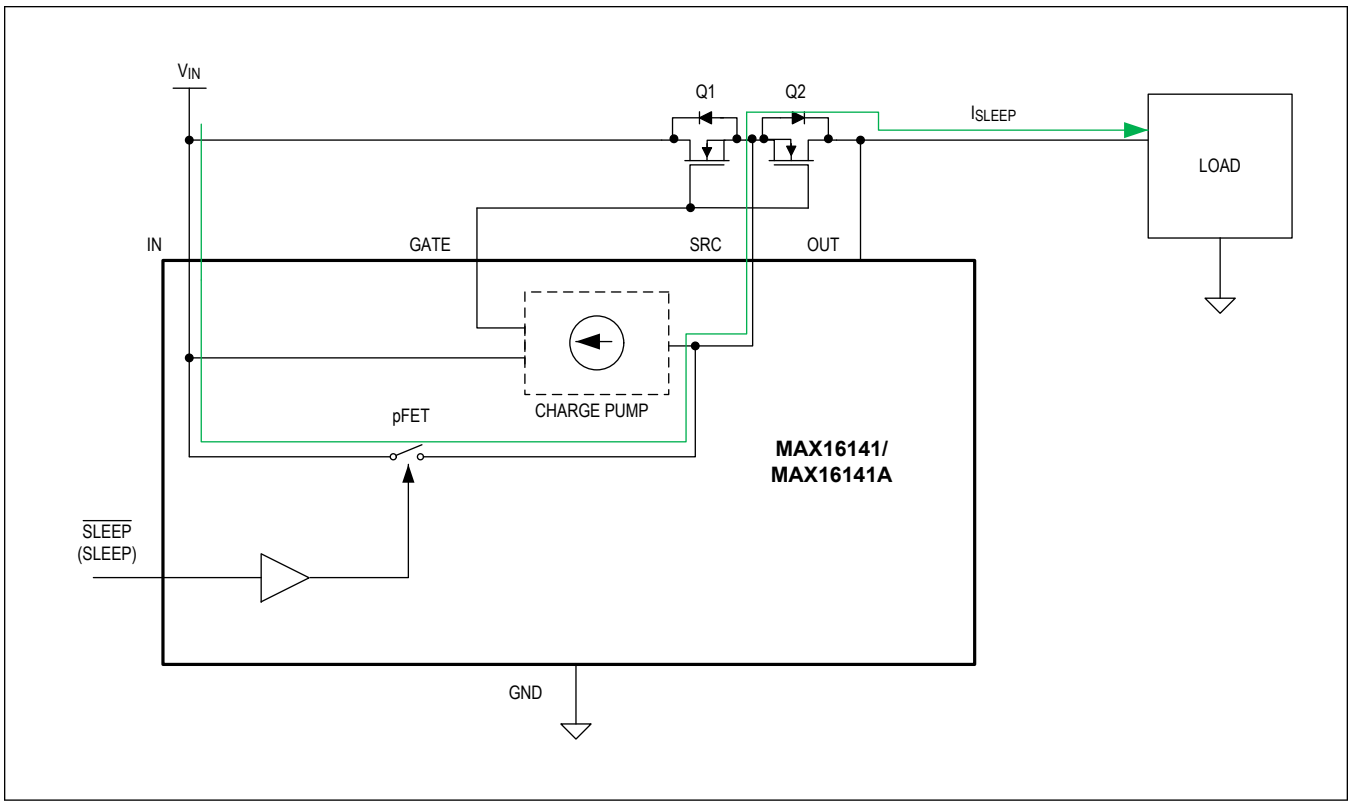


Figure 1. Sleep Mode Operation

Note: *In sleep mode, the drain of the pFET is internally clamped to 18V. Increasing the input voltage above 18V increases the sleep mode current of the device. See the Typical Operating Characteristics section for more detail.*

Gate Charge Pump

An internal charge pump generates the GATE-to-SRC voltage to enhance the external MOSFETs. After the input voltage exceeds the input undervoltage threshold, the charge pump turns on after a 450µs startup (t_{SU}) delay.

During the reverse-voltage fault condition, GATE is disabled with a 280mA (typ) pulldown current. Upon recovery from reverse voltage, if the V_{CC} voltage is below the undervoltage threshold, the gate drive is enabled and its ramp rate is determined by the resistor value between GRC and ground. If upon reverse-voltage recovery the V_{CC} voltage is above the undervoltage threshold, the charge pump sources 1200µA (typ) to enable the gate drive in fast mode. Allowing the gate voltage to ramp up in fast mode helps minimize output voltage droop after reverse-voltage or short battery voltage interruptions.

TERM Connection

The TERM connection has an internal switch to V_{CC}. In shutdown ($\overline{SHDN}$ = low), this switch is open. By connecting the voltage threshold resistive divider to TERM instead of directly to V_{CC}, power dissipation in the resistive divider can be eliminated and the supply current in shutdown mode reduced.

During shutdown mode, the (V_{CC} - V_{TERM}) can be as high as 60V, but (V_{TERM} - V_{CC}) must be limited to < 1V due to a parasitic diode.

$\overline{FAULT}$ Output

$\overline{FAULT}$ is an open-drain output that indicates fault conditions. During startup, $\overline{FAULT}$ is initially low and goes high-impedance when V_{OUT} is greater than 90% of V_{IN} if no fault conditions are present. $\overline{FAULT}$ asserts low during shutdown

mode, reverse-current, overcurrent, overvoltage, thermal shutdown, or undervoltage faults, or when V_{OUT} falls below 90% of V_{IN}.

Auto-Retry

The MAX16141/MAX16141A enter auto-retry mode of 300ms (typ) during overcurrent, output short-circuit, and thermal shutdown faults. In auto-retry mode, the gate drive is enabled every 300ms (typ) to check if the fault condition is removed. If the fault is present, the gate pulls low after a short duration of 20ms (typ). If the fault condition is removed, the gate pulls high and the MAX16141/MAX16141A resume normal operation. During fault conditions, $\overline{FAULT}$ asserts low and deasserts once the fault conditions are removed.

Applications Information

Setting Overvoltage/Undervoltage Threshold

The MAX16141/MAX16141A feature window-detection threshold comparators. The noninverting input of the undervoltage comparator shares the same reference voltage connected to the inverting input of the overvoltage comparator. This configuration allows using three-resistor network to set both undervoltage and overvoltage thresholds. The top of the resistive divider network connects to TERM. See Figure 2. When the input voltage falls outside the set window threshold, the gate voltage is disabled and the n-channel MOSFETs are turned off. Use the following equations to set the thresholds:

$$V_{UVTH} = \left(V_{TH} - V_{TH_HYS}\right)\left[\frac{R_{TOTAL}}{R2 + R3}\right]$$

$$V_{OVTH} = \left(V_{TH}\right)\left[\frac{R_{TOTAL}}{R3}\right]$$

where V_{UVTH} and V_{OVTH} are the undervoltage and overvoltage thresholds respectively, R_{TOTAL} = R1 + R2 + R3 + R_{TERM}, V_{TH} is the 0.5V OVSET and UVSET threshold, and the V_{TH_HYS} is the hysteresis, R_{TERM} is the TERM on-resistance whose typical value is 0.7kΩ.

Use the following steps to determine values for R1, R2, and R3:

1. Choose a value for R_{TOTAL}: the sum of R1, R2, R3, and R_{TERM}.
2. Calculate R3 based on R_{TOTAL} and the desired overvoltage threshold point, V_{OVTH}:

$$R3 = \left(\frac{V_{TH} \times R_{TOTAL}}{V_{OVTH}}\right)$$

3. Calculate R2 based on R_{TOTAL}, R3, and the desired undervoltage threshold point, V_{UVTH}:

$$R2 = \left(\frac{\left(V_{TH} - V_{TH_HYS}\right) \times R_{TOTAL}}{V_{UVTH}}\right) - R3$$

4. Calculate R1 based on R_{TOTAL}, R2, R3, and R_{TERM}:

$$R1 = R_{TOTAL} - R2 - R3 - R_{TERM}$$

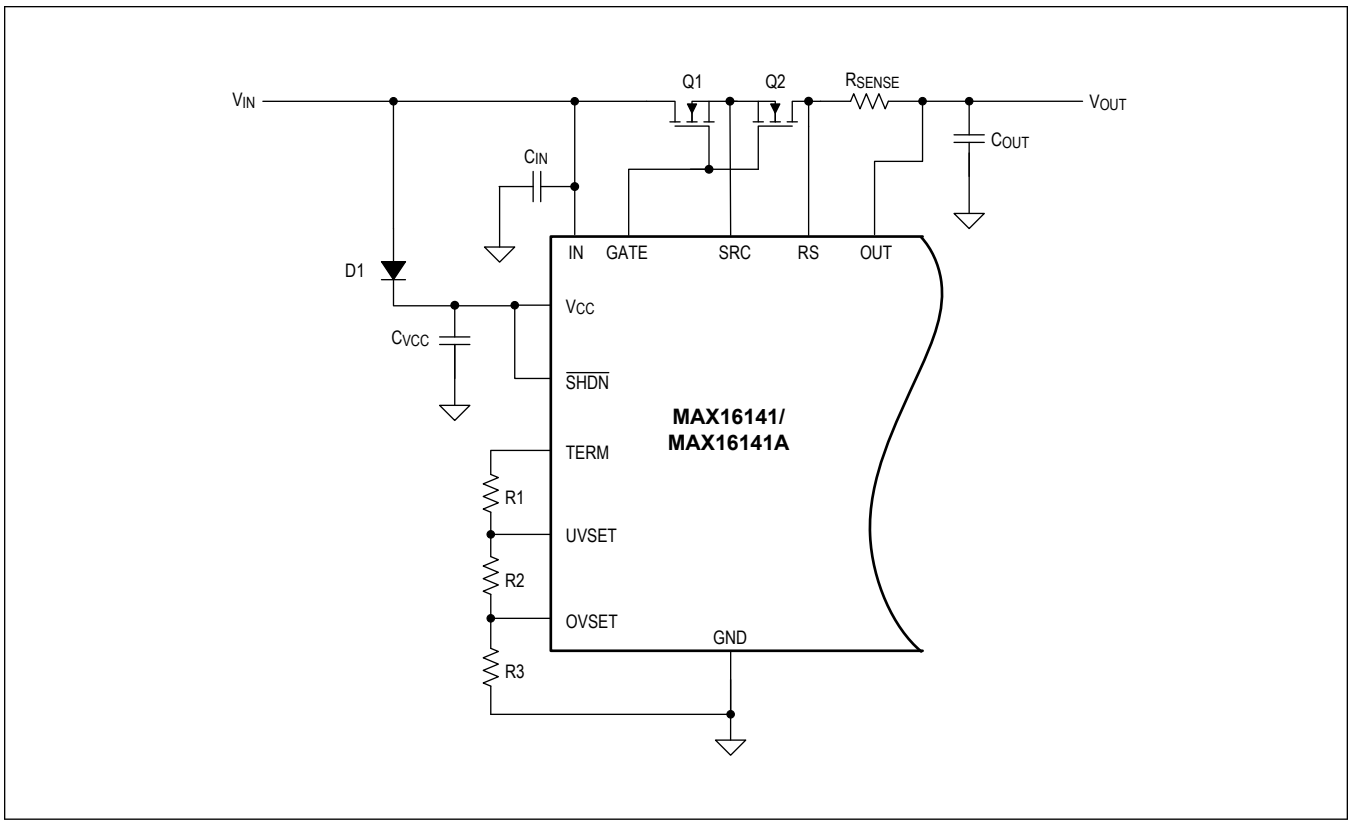


Figure 2. UVSET and OVSET Threshold Setting

The MAX16141/MAX16141A offer factory-set threshold hysteresis for undervoltage and overvoltage threshold settings. See Figure 7 for available options.

Reverse-Voltage Protection

Traditionally, discrete diodes have been used to block reverse current flow and prevent output capacitor discharge. However, for high-current applications, ideal diode controllers (FET-based solutions) are more appealing due to their low power dissipation. But, unlike a discrete diode that blocks reverse current instantaneously, a typical ideal diode controller reacts much more slowly. To prevent heavy discharge of the load-side capacitor in the case of a fault that shorts the input to ground, the MAX16141/MAX16141A disable the gate drive within 1µs (max) of detection of the reverse-voltage condition. See Figure 3.

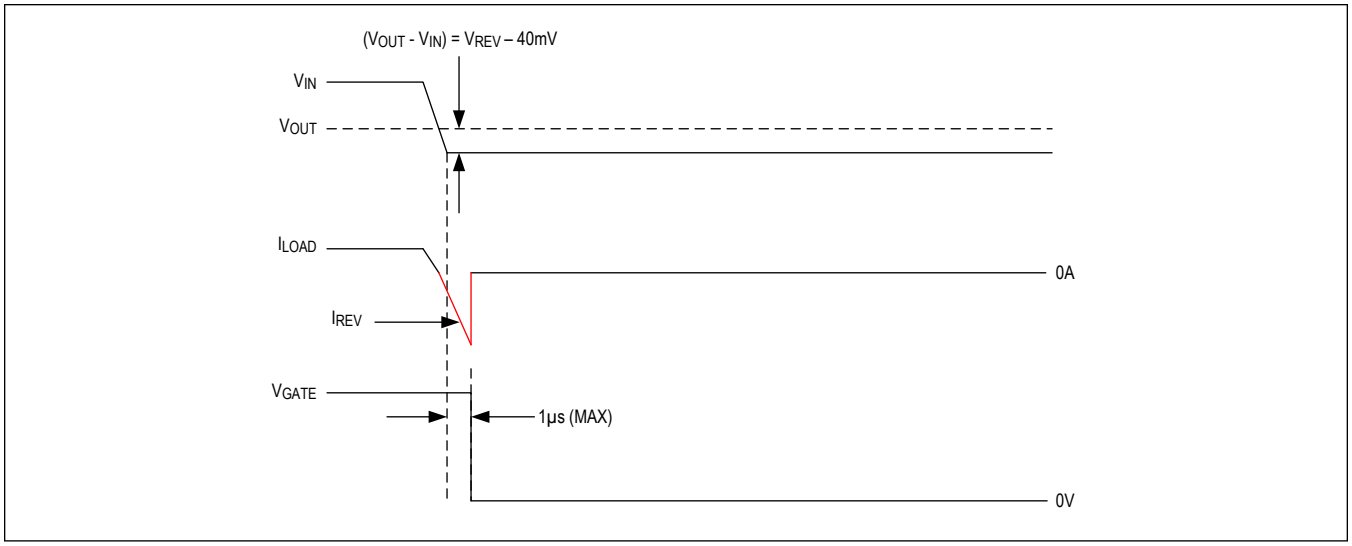


Figure 3. Reverse-Voltage Fault

Automotive circuits generally require supply voltage protection from various transients that occur in automotive systems. Some of these transients extend beyond the MAX16141/MAX16141A protection range. To protect against these transients, automotive systems generally use external TVSs. Figure 4 shows the recommended circuit for the MAX16141/MAX16141A.

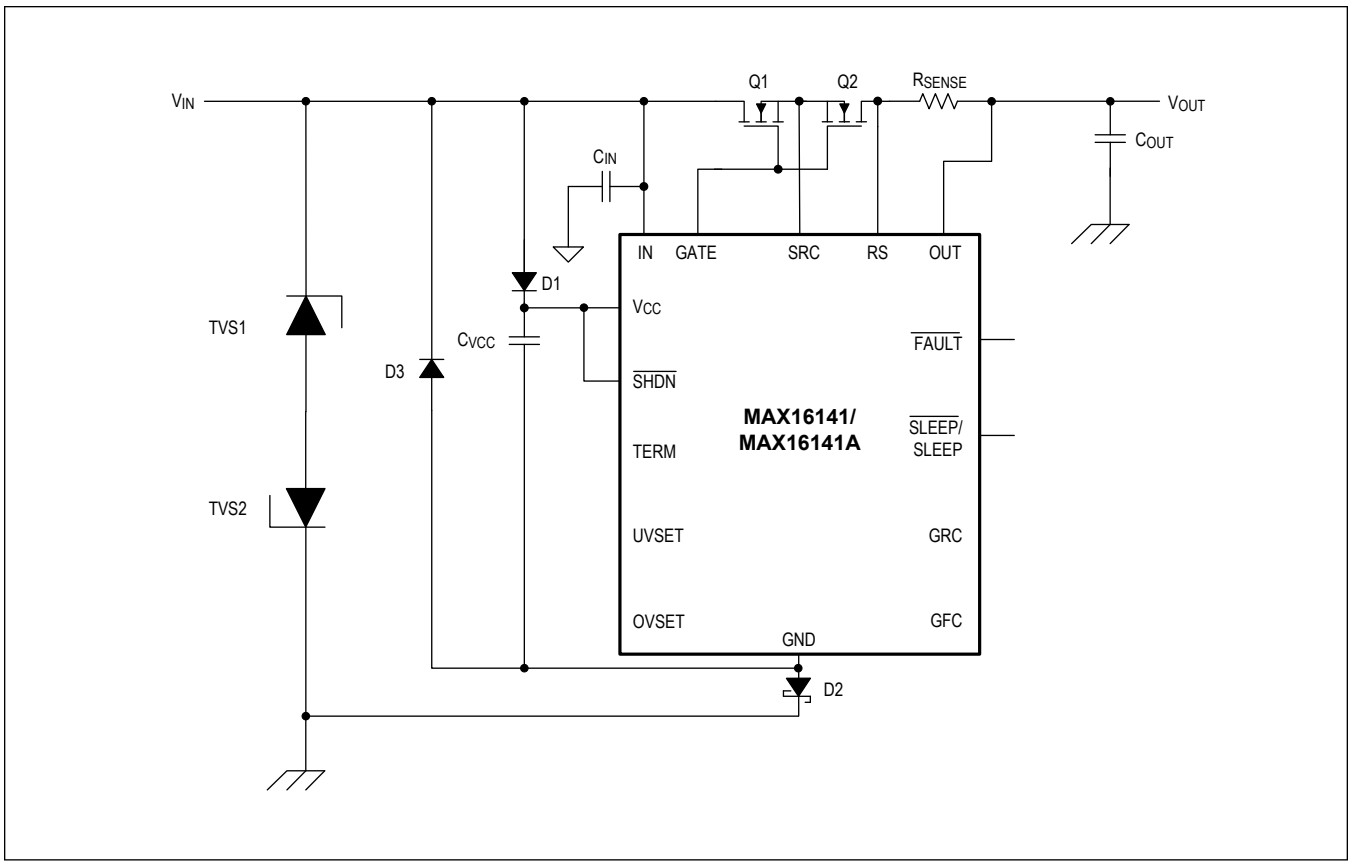


Figure 4. Recommended Reverse-Voltage Protection Circuit

Overcurrent Threshold Setting

Use the following formula to set the overcurrent threshold:

$$I_{OC} = V_{(RS\text{-}OUT)}/R_{SENSE}$$

where $V_{(RS\text{-}OUT)}$ is the overcurrent threshold voltage in volts, and R_{SENSE} is the resistor in ohms connected between RS and OUT.

Short Power Interruptions

In an automotive environment, systems usually experience brief power interruptions where the main supply is shorted to ground. The power interruption may last for several seconds and the only source of power to system load is the output capacitance. To ensure fast recovery, an auxiliary input (V_{CC}) helps keep the MAX16141/MAX16141A in standby mode for 100µs (typ). When the main supply input (IN) recovers, the MAX16141/MAX16141A initiate a fast recovery mode that allows the gate to reach its peak voltage within 70µs (max). See Figure 5 for more detail. Therefore, brief power supply interruptions will not affect operation of the load, as long as the load-side capacitance is sufficiently large to power the load during the interruption.

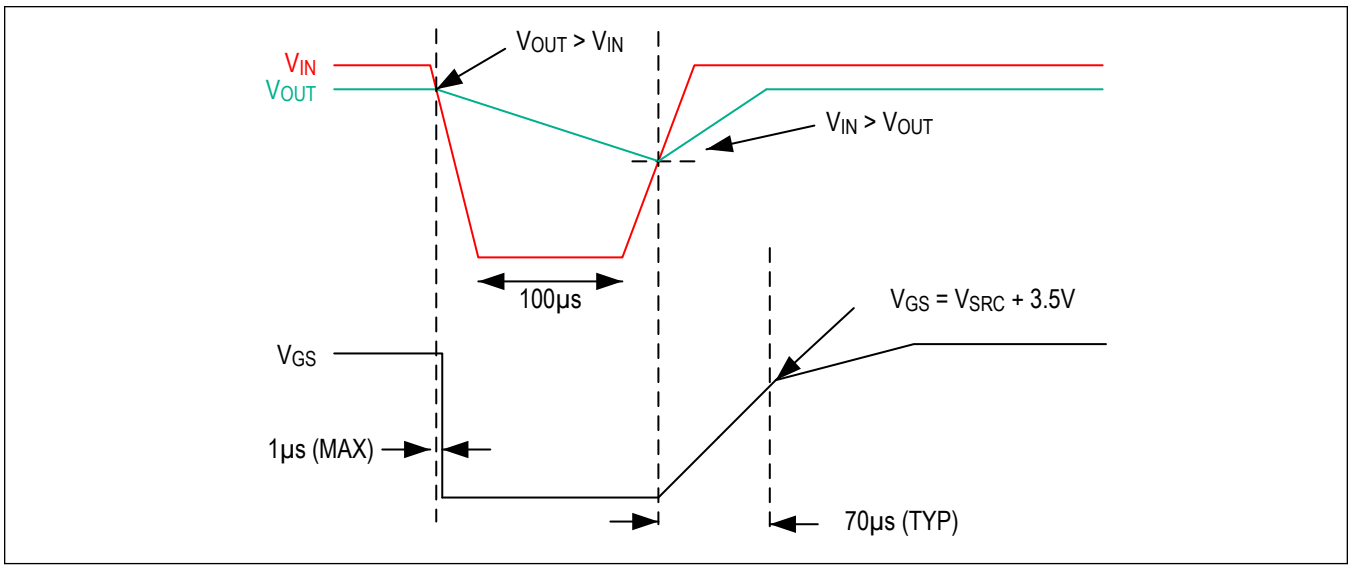


Figure 5. Short Power Interruption and Recover

Since V_{CC} provides power to the MAX16141 when the main supply is shorted to ground, a low-leakage diode such as CMPD4150 from V_{IN} to V_{CC} and a bulk capacitance is required to keep the MAX16141/MAX16141A in standby mode. See the *Typical Application Circuit* for proper connection. The size of the bulk capacitance is dictated by the expected duration of the power interruption and supply current of the MAX16141/MAX16141A. Below is a simple bulk capacitance calculation for 100µs power interruption and 1V drop in V_{CC} voltage.

$$C_{VCC} = \frac{\left(I_{CC} \times 100 \times 10^{-6}\right)}{\Delta V_{CC}}$$

where C_{VCC} is the bulk capacitance at V_{CC}, I_{CC} is the supply current in amperes, and ΔV_{CC} is the desired droop in V_{CC} in volts.

$$\frac{\left(3 \times 10^{-3}(A) \times 100 \times 10^{-6}(s)\right)}{1V} \simeq 0.33\mu F$$

Note: *If the input voltage sags slowly and the output follows, the differential voltage between the input and output may always be less than factory-set threshold. In this case, the reverse-current fault may not occur. Instead, an undervoltage fault may eventually be detected; causing the gate drive to be disabled.*

Gate Rise Time Control

The gate rise time control connection, GRC, allows the MAX16141/MAX16141A to control the gate ramp-up rate with respect SRC. The gate rise time specifications in the *Electrical Characteristics* table are based on a 7nF gate-to-source capacitance. If the combined gate-to-source capacitance of the MOSFETs is higher than 7nF, the gate voltage might not reach its final nominal voltage within the internal timer selected by R_{GRC}. As a result, upon the expiration of the internal timer, the internal charge pump increases its drive current (fast mode) to force the gate voltage to its final nominal voltage. See Figure 6 for more detail. This sudden jump in the gate voltage could cause a high dV/dt across the output capacitor and result in huge inrush current. To avoid this scenario, increase the gate rise time using a different R_{GRC}, as specified in the *Electrical Characteristics* table.

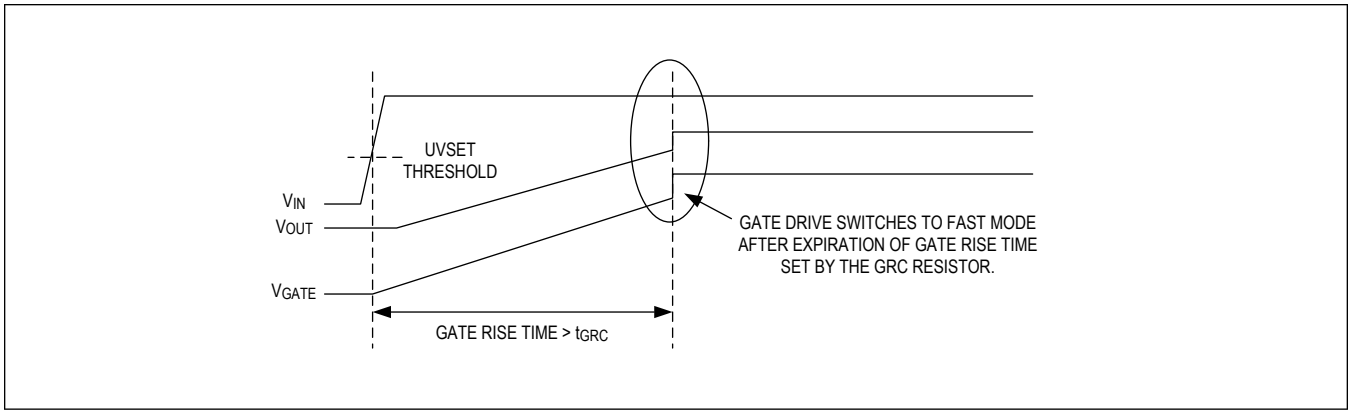


Figure 6. Gate Voltage Slow to Fast-Mode Transition

MOSFET Selection

MOSFET selection is critical to design a proper protection circuit. Several factors must be considered: the gate capacitance, the drain-to-source voltage rating, the on-resistance ($R_{DS(ON)}$), the peak power dissipation capability, and the average power dissipation limit. In general, both MOSFETs should have the same part number. For size-constrained applications, a dual MOSFET can conserve board area. Select the drain-to-source voltage so that the MOSFETs can handle the highest voltage that might be applied to the circuit. Gate capacitance is not as critical, but it does determine the maximum turn-on and turn-off time. MOSFETs with more gate capacitance tend to respond more slowly.

MOSFET Power Dissipation

The $R_{DS(ON)}$ must be low enough to limit the MOSFET power dissipation during normal operation. Power dissipation (per MOSFET) during normal operation can be calculated using this formula:

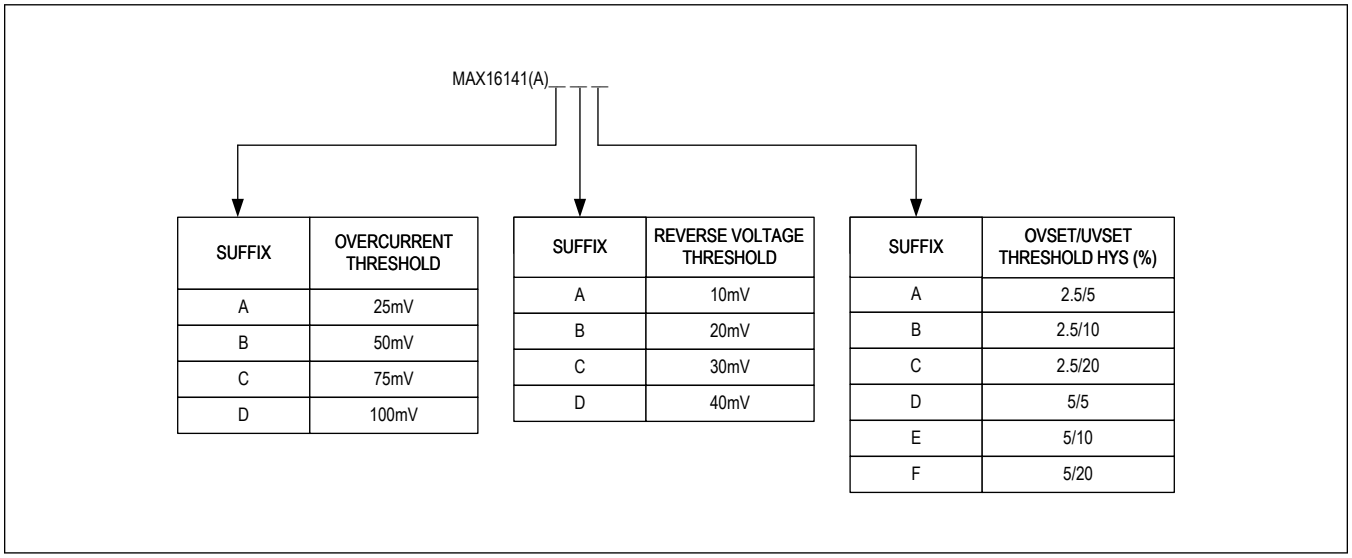
$$P = I^2_{LOAD} \times R_{DS(ON)}$$

where P is the power dissipated in each MOSFET, and I_{LOAD} is the average load current.

During a fault condition in switch mode, the MOSFETs turn off and do not dissipate power.

Since limiter mode can involve high switching currents when the GATE is turning on at the start of a limiting cycle (especially when the output capacitance is high), it is important to ensure the circuit does not violate the peak power rating of the MOSFETs. Check the pulse power ratings in the MOSFET data sheet.

Selector Guide



SUFFIX	OVERCURRENT THRESHOLD
A	25mV
B	50mV
C	75mV
D	100mV

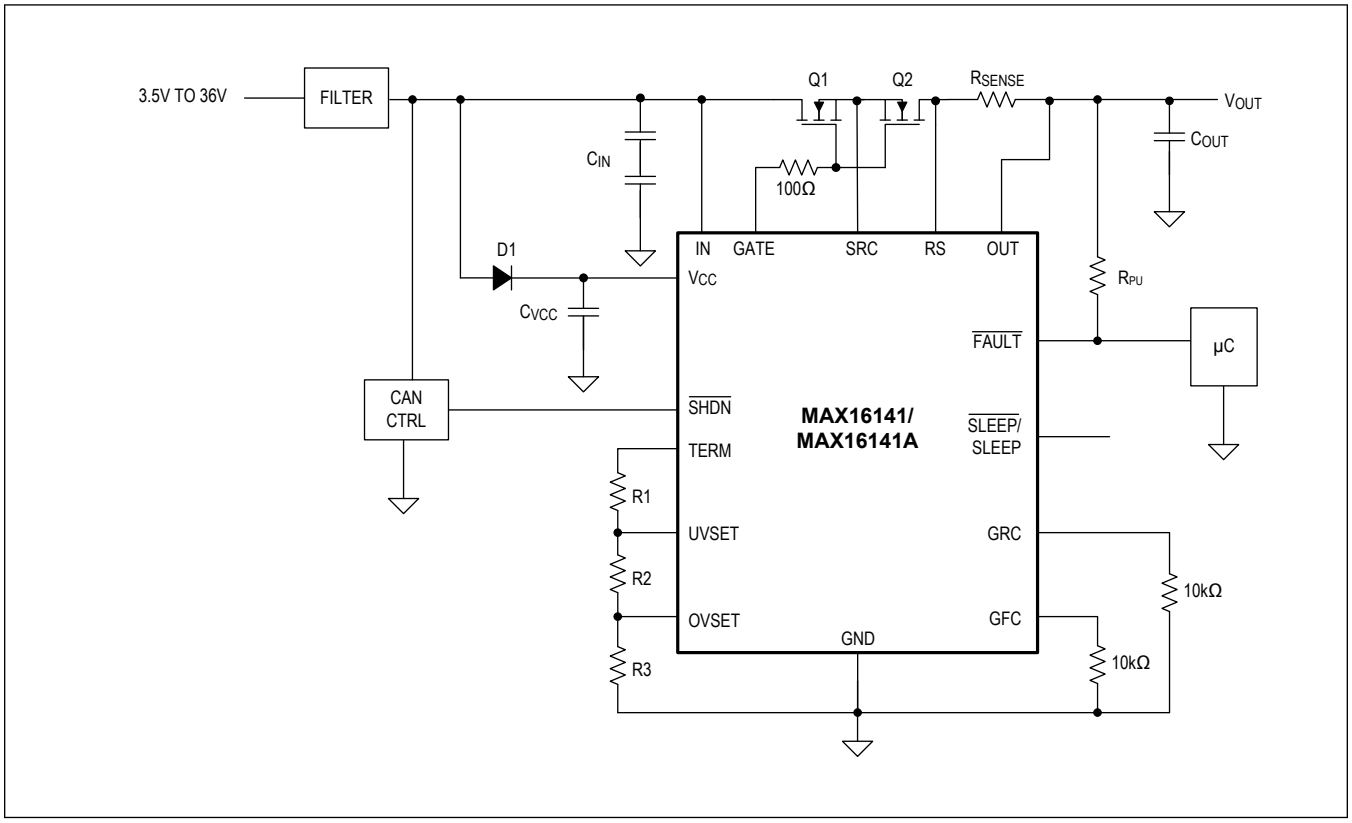
SUFFIX	REVERSE VOLTAGE THRESHOLD
A	10mV
B	20mV
C	30mV
D	40mV

SUFFIX	OVSET/UVSET THRESHOLD HYS (%)
A	2.5/5
B	2.5/10
C	2.5/20
D	5/5
E	5/10
F	5/20

Figure 7. Selector Guide

Typical Application Circuit

Typical Automotive Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX16141AAF+T	-40°C to +125°C	16 TQFN	T1644+4A
MAX16141AAF/V+T	-40°C to +125°C	16 TQFN	T1644+4A
MAX16141AAAA/VY+T	-40°C to +125°C	16 TQFN	T1644Y+4
MAX16141AAAF/VY+T	-40°C to +125°C	16 TQFN	T1644Y+4
MAX16141ADF/V+T	-40°C to +125°C	16 TQFN	T1644+4A
MAX16141BAF/V+T	-40°C to +125°C	16 TQFN	T1644+4A
MAX16141AADA/VY+T*	-40°C to +125°C	16 TQFN	T1644Y+4

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

/V denotes automotive qualified parts.

** Future product—contact factory for availability.*

Note: *See Figure 7 for overcurrent, reverse-current, overvoltage, and undervoltage hysteresis options. Contact factory for availability of variants not listed in the Ordering Information table (10k units minimum order quantity).*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	7/18	Updated *Electrical Characteristics* table, *Detailed Description* section, *Ordering Information* table, and *Applications Information* section	6, 12, 14, 16, 19
2	12/18	Updated *Benefits and Features*, *Simplified Block Diagram*, *Package Information*, *Functional Diagram*, and *Reverse-Voltage Protection*	1–3, 11, 13
3	2/19	Added MAX16141A to data sheet	1–19
4	6/19	Updated *Benefits and Features*, *Typical Operating Characteristics*, *Pin Configuration*, *Functional Diagram*, *Detailed Description*, and *Ordering Information*	1, 9, 11, 13–15, 19
5	11/19	Updated *Electrical Characteristics* table and *Ordering Information*	4, 19
6	4/21	Updated *General Description*, *Benefits and Features*, *Typical Application Circuit*, *Electrical Characteristics* table, *Pin Descriptions*, *Detailed Description*, *Applications Information*, *Selector Guide*, and *Ordering Information*	1, 2, 4, 5, 9–23
7	8/21	Updated *Applications Information*	16
8	1/22	Updated *Absolute Maximum Ratings, Electrical Characteristics* table, and *Ordering Information* table	3–5, 23
9	4/22	Removed *MOSFET Gate Protection* section	21