MP6531A

5V - 60V, Three-Phase, Brushless, DC Motor Pre-Driver

The Future of Analog IC Technology®

DESCRIPTION

The MP6531A is a gate driver IC designed for three-phase, brushless, DC motor driver applications. The MP6531A is capable of driving three half-bridges consisting of six N-channel power MOSFETs up to 60V.

The MP6531A uses a bootstrap capacitor to generate a supply voltage for the high-side MOSFET driver. An internal trickle-charge circuit maintains a sufficient gate driver voltage at 100% duty cycle.

Internal safety features include programmable over-current protection (OCP), adjustable dead-time control, under-voltage lockout (UVLO), and thermal shutdown.

The MP6531A is available in 28-pin TSSOP-EP (9.7mmx6.4mm) and QFN-28 (4mmx4mm) packages with exposed thermal pads on the back.

FEATURES

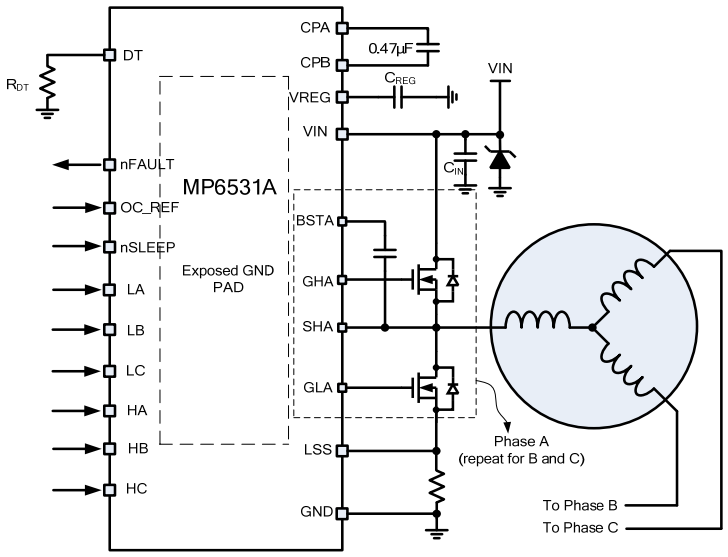
- Wide 5V to 60V Input Voltage Range
- Bootstrap Gate Driver with Trickle-Charge Circuit Supports 100% Duty Cycle Operation
- Low-Power Sleep Mode for Battery-Powered Applications
- Programmable Over-Current Protection of the External MOSFETs
- Adjustable Dead-Time Control to Prevent Shoot-Through
- Thermal Shutdown and UVLO Protection
- Fault Indication Output
- Thermally Enhanced Surface-Mounted Packages

APPLICATIONS

- Three-Phase, Brushless, DC Motors
- Permanent Magnet Synchronous Motors
- Power Drills
- Impact Drivers
- E-Bikes

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6531AGF*	TSSOP-28 EP	*See Below*
MP6531AGR**	QFN-28 (4mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6531AGF–Z)
** For Tape & Reel, add suffix –Z (e.g. MP6531AGR–Z)

TOP MARKING (MP6531AGF)

MPSYYWW
MP6531A
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6531A: Part number
LLLLLLLLL: Lot number

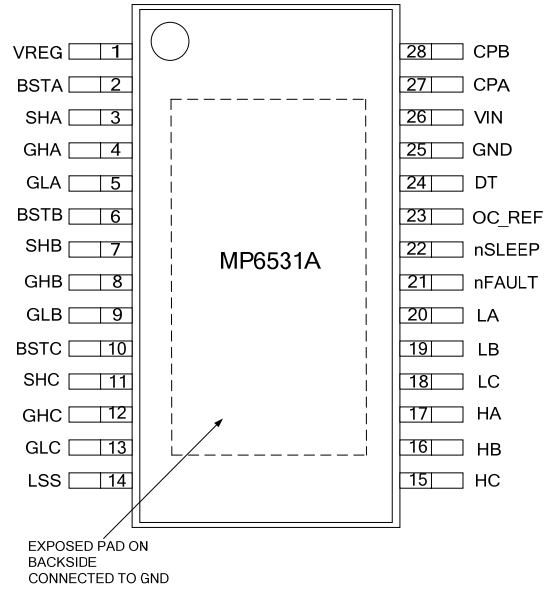
TOP MARKING (MP6531AGR)

MPSYWW
M6531A
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M6531A: Part number
LLLLLL: Lot number

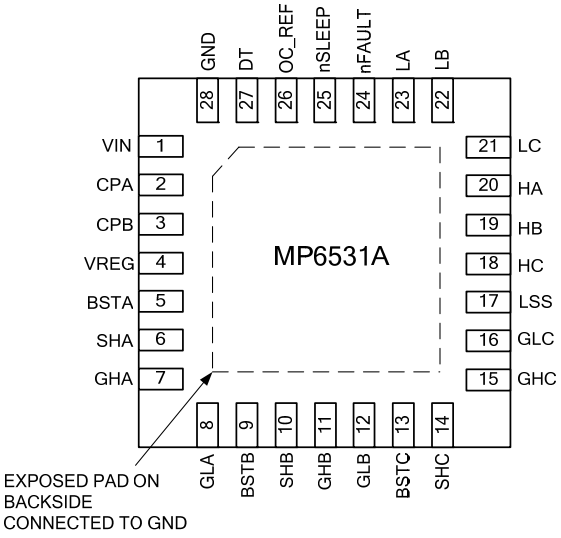
PACKAGE REFERENCE

TOP VIEW



TSSOP-28 EP

TOP VIEW



QFN-28 (4mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (VIN) ..... -0.3V to 65V
CPA ..... -0.3V to 60V
CPB ..... -0.3V to 12.5V
VREG ..... -0.3V to 13V
BSTA/B/C ..... -0.3V to 70V
GHA/B/C ..... -0.3V to 70V
GHA/B/C (Transient, 2μS) ..... -8V to 70V
SHA/B/C ..... -0.3V to 65V
SHA/B/C (Transient, 2μS) ..... -8V to 65V
GLA/B/C ..... -0.3V to 13V
LSS ..... -0.3V to 1V
All other pins to AGND ..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
TSSOP-28 EP 3.9W
QFN-28 (4mmx4mm) 2.9W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... +150°C
Lead temperature (solder) ..... +260°C

Recommended Operating Conditions (3)

Input voltage (VIN) ..... +5V to 60V
OC_REF voltage (V_{OC}) ..... 0.125V to 2.4V
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
TSOP28-EP	32	6	°C/W
QFN-28 (4mmx4mm)	42	9	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN = 24V, T_A = 25°C, unless otherwise noted.

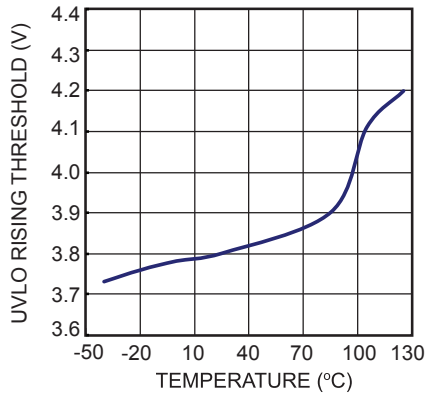
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		5		60	V
Quiescent current	I_Q	nSLEEP = 1, gate not switching		1.8	2.3	mA
	I_{SLEEP}	nSLEEP = 0			1	µA
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		20	µA
nSLEEP pull-down current	$I_{SLEEP-PD}$			1		µA
Internal pull-down resistance	R_{PD}			800		kΩ
Fault Outputs (Open-Drain Outputs)						
Output low voltage	V_{OL}	I_O = 5mA			0.5	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	µA
Protection Circuit						
UVLO rising threshold	V_{IN_RISE}		3.3	3.9	4.5	V
UVLO hysteresis	V_{IN_HYS}			250		mV
VREG rising threshold	V_{REG_RISE}		6.8	7.8	8.5	V
VREG hysteresis	V_{REG_HYS}			0.6	1	V
VREG start-up delay	t_{REG}			850		µs
OC_REF threshold	V_{OC}	V_{OC} = 1V	0.8	1	1.2	V
		V_{OC} = 2.4V	2.18	2.4	2.62	V
OCP deglitch time	t_{OC}			3		µs
nSLEEP wake-up time	t_{SLEEP}			1		ms
LSS OCP threshold	$V_{LSS-OCP}$		0.4	0.5	0.6	V
Thermal shutdown	T_{TSD}			190		°C
Gate Drive						
Bootstrap diode forward voltage	V_{FBOOT}	I_D = 10mA			0.9	V
		I_D = 100mA			1.4	V
VREG output voltage	V_{REG}	VIN = 5.5V - 60V	10	11.5	13	
		VIN = 5V	$2xV_{IN}$-1			V
Maximum source current	I_{OSO} (5)			0.8		A
Maximum sink current	I_{OSI} (5)	HS gate drive		1		A
		LS gate drive		2		A
Gate drive pull-up resistance	R_{UP}	V_{DS} = 1V		8		Ω
HS gate drive pull-down resistance	R_{HS-DN}	V_{DS} = 1V	1		5.5	Ω
LS gate drive pull-down resistance	R_{LS-DN}	V_{DS} = 1V	1		5.8	Ω
LS passive pull-down resistance	R_{LS-PDN}			590		kΩ
LS automatic turn-on time	t_{LS}	At power-up		0.5		µs
Charge pump frequency	f_{CP}			110		kHz
Dead time	t_{DEAD}	R_{DT} = 100kΩ		5.7		µs
		R_{DT} = 10kΩ		0.7		µs
		DT tied to GND		130		ns

NOTE:

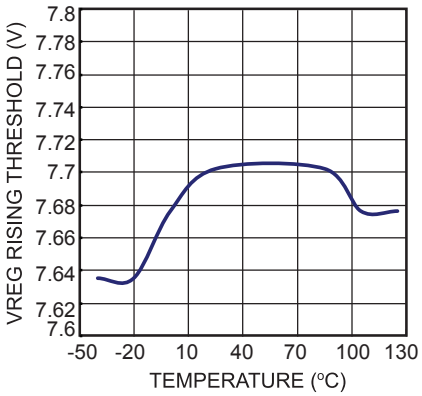
5) Guarantee by design.

TYPICAL CHARACTERISTICS

UVLO Rising Threshold vs. Temperature

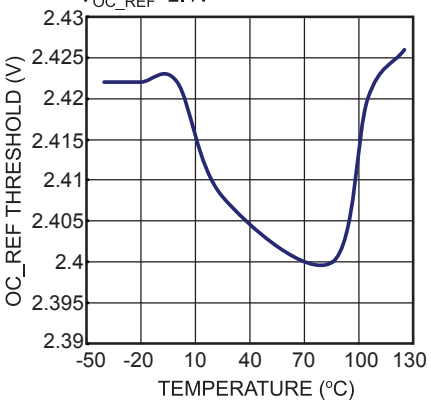


VREG Rising Threshold vs. Temperature

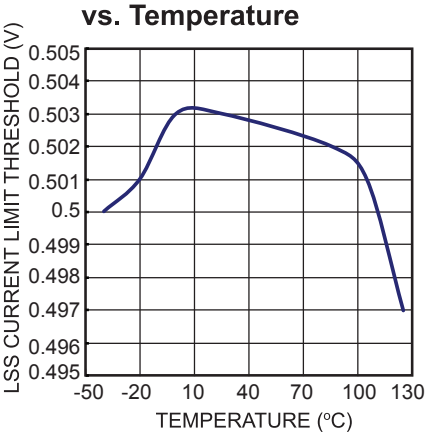


OC_REF Threshold vs. Temperature

V_{OC_REF}=2.4V



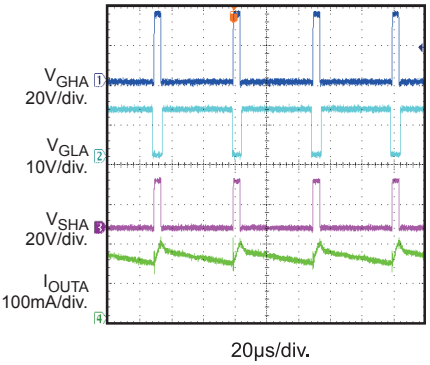
LSS Current Limit Threshold vs. Temperature



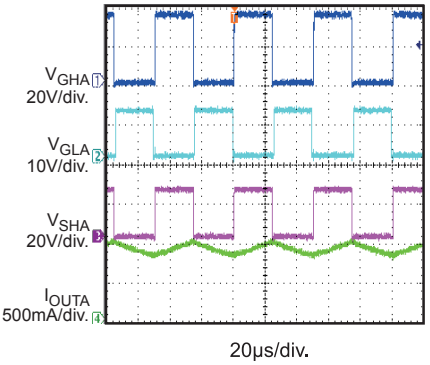
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 24V, OC_REF = 0.5V, R_{DT} = 20kΩ, F_{PWMA} = 20kHz, LB = 5V, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

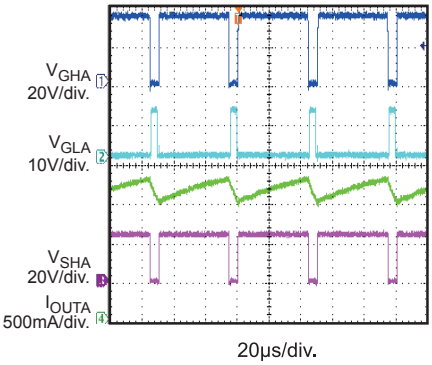
Steady State
Duty=10%



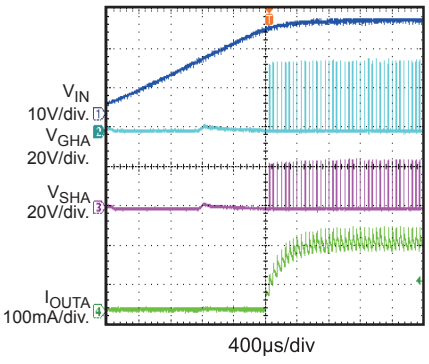
Steady State
Duty=50%



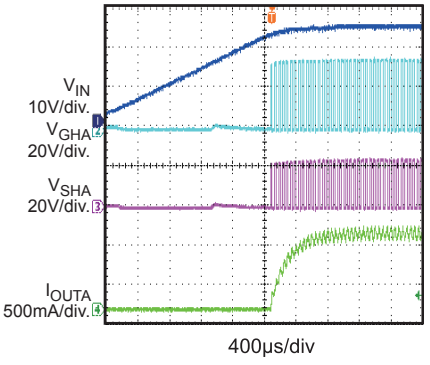
Steady State
Duty=90%



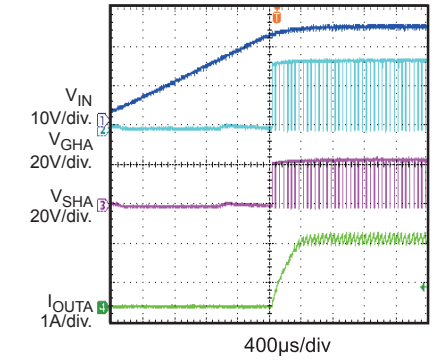
Power Ramp Up
Duty=10%



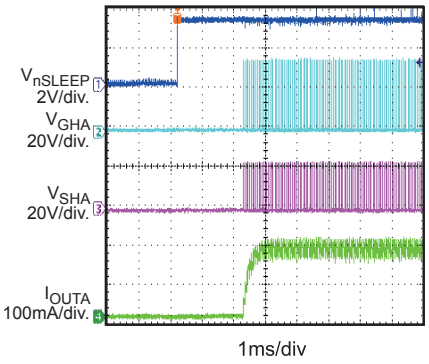
Power Ramp Up
Duty=50%



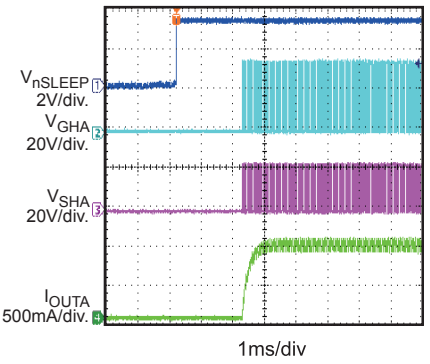
Power Ramp Up
Duty=90%



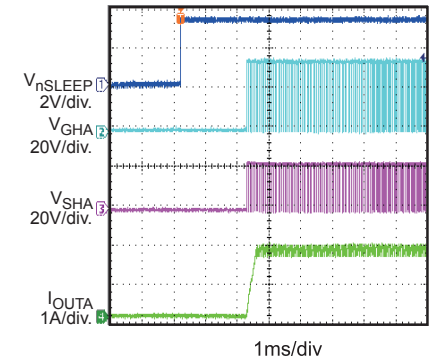
Sleep Recovery
Duty=10%



Sleep Recovery
Duty=50%



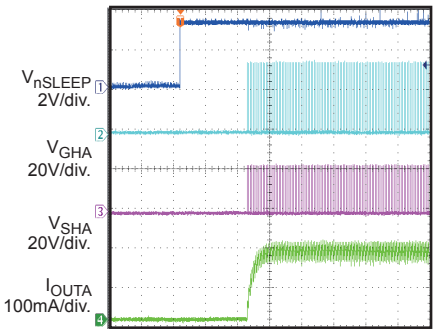
Sleep Recovery
Duty=90%



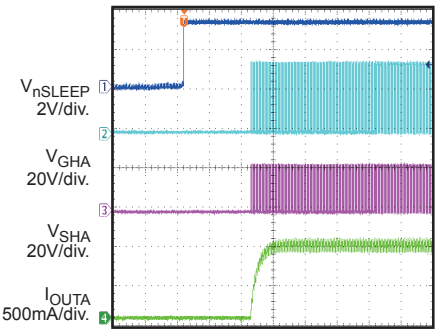
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 24V, OC_REF = 0.5V, R_{DT} = 20kΩ, F_{PWMA} = 20kHz, LB = 5V, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

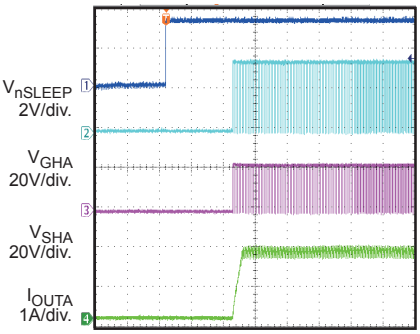
Sleep Recovery
Duty=10%



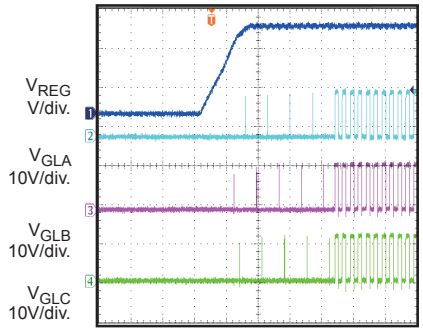
Sleep Recovery
Duty=50%



Sleep Recovery
Duty=50%



VREG Startup
F_{PWMX}=20kHz with duty=50%, No load



PIN FUNCTIONS

QFN Pin #	TSSOP Pin #	Name	Description
1	26	VIN	**Input supply voltage.** Bypass VIN to ground with a ceramic capacitor. Additional bulk capacitance may be required. See the Applications Information section for more detail.
2	27	CPA	**Charge pump capacitor.** Connect a ceramic capacitor between CPA and CPB. See the Applications Information section for more detail.
3	28	CPB	
4	1	VREG	**Gate drive supply output.** Connect a ceramic capacitor between VREG and ground. See the Applications Information section for more detail.
5	2	BSTA	**Bootstrap phase A.** Connect a ceramic capacitor to SHA. See the Applications Information section for more detail.
6	3	SHA	**High-side source connection phase A.**
7	4	GHA	**High-side gate drive phase A.**
8	5	GLA	**Low-side gate drive phase A.**
9	6	BSTB	**Bootstrap phase B.** Connect a ceramic capacitor to SHB. See the Applications Information section for more detail.
10	7	SHB	**High-side source connection phase B.**
11	8	GHB	**High-side gate drive phase B.**
12	9	GLB	**Low-side gate drive phase B.**
13	10	BSTC	**Bootstrap phase C.** Connect a ceramic capacitor to SHC. See the Applications Information section for more detail.
14	11	SHC	**High-side source connection phase C.**
15	12	GHC	**High-side gate drive phase C.**
16	13	GLC	**Low-side gate drive phase C.**
17	14	LSS	**Low-side source connection.**
18	15	HC	**Phase C high-side input.**
19	16	HB	**Phase B high-side input.**
20	17	HA	**Phase A high-side input.**
21	18	LC	**Phase C low-side input.**
22	19	LB	**Phase B low-side input.**
23	20	LA	**Phase A low-side input.**
24	21	nFAULT	**Fault indication.** nFAULT is an open-drain output. nFAULT is logic low when in a fault condition.
25	22	nSLEEP	**Sleep mode input.** Drive nSLEEP logic low to enter low-power sleep mode; drive nSLEEP logic high to enable the device. nSLEEP has an internal pull-down resistor.
26	23	OCREF	**Over-current protection reference voltage input.**
27	24	DT	**Dead time setting.** Connect a resistor between DT and ground to set the dead time. See the Applications Information section for more detail.
28	25	GND	**Ground.**

BLOCK DIAGRAM

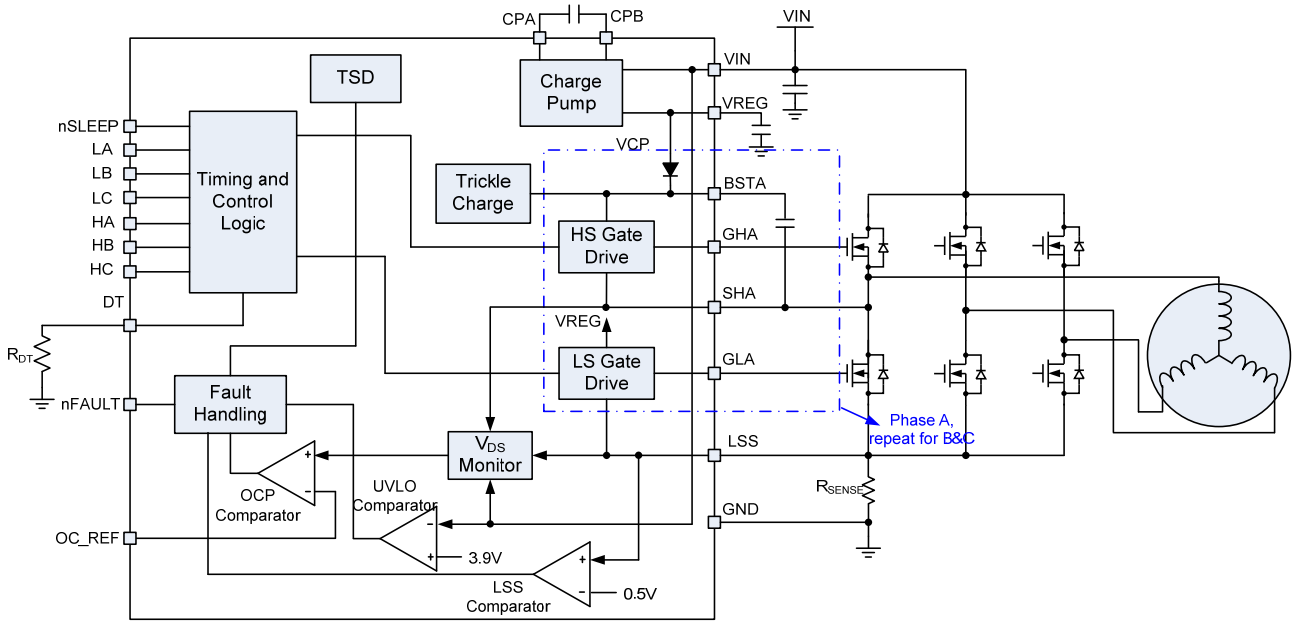


Figure 1: Functional Block Diagram

OPERATION

The MP6531A is a three-phase BLDC motor pre-driver that drives three external N-channel MOSFET half-bridges with an 0.8A source and 1A of sink current capability. The MP6531A operates over a wide input voltage range of 5V to 60V, generating a boosted gate drive voltage when the input supply is below 12V. The MP6531A features low-power sleep mode, which disables the device and draws a very low supply current. The MP6531A provides several flexible functions, such as adjustable dead-time control and over-current protection, which allow the device to cover a wide range of applications.

Power-Up Sequence

The power-up sequence is initiated by the application of voltage to VIN. To initiate power-up, VIN must be above the under-voltage lockout threshold (V_{IN_RISE}).

After power-up begins, the VREG supply begins operating. VREG must rise above VREG rising threshold (V_{REG_RISE}) before the device becomes functional.

After VREG exceeds V_{REG_RISE}, the MP6531A sequentially turns on each low-side MOSFET (LS-FET) in succession to charge the bootstrap capacitors for a short period of time (t_{LS}).

The power-up process takes between 1ms and 2ms, after which the MP6531A responds to the logic inputs and drives the outputs.

Gate Drive Power Supplies

Gate drive voltages are generated from the input power (VIN). A regulated charge pump voltage doubler circuit supplies a voltage of approximately 11.5V to VREG. This voltage is used for the low-side gate drive supply. The charge pump requires external capacitors between CPA and CPB and from VREG to ground.

The high-side gate drive is generated by a combination of a bootstrap capacitor and an internal trickle charge pump. Bootstrap capacitors are charged to VREG when the low-side MOSFET (LS-FET) is turned on. This charge is then used to drive the high-side MOSFET (HS-FET) gate when it is turned on.

To keep the bootstrap capacitors charged and allow for operation at 100% duty cycle, an internal trickle charge pump supplies a small current (about 5µA) to overcome leakages that would discharge the bootstrap capacitors.

Sleep Mode (nSLEEP Input)

Driving nSLEEP low puts the device into a low-power sleep state. In this state, all internal circuits are disabled, and all inputs are ignored. nSLEEP has an internal pull-down resistor, so the pin must be driven high for the MP6531A to operate. When exiting sleep mode, the MP6531A initiates the power-up sequence.

Input Logic

HC, HB, or HA are used to control the gate drive for the HS-FET of each phase. LC, LB, or LA are used to control the gate drive for the low-side FET. Positive dead time is enforced by the device, and if both HX and LX are driven high, neither FET is driven (see Table 1).

Table 1: Input Logic Truth Table

LX	HX	SHX
H	H	High impedance
H	L	GND
L	H	VIN
L	L	High impedance

nFAULT

The nFAULT output reports to the system when a fault condition (such as output short-circuit, over-current, or over-temperature) is detected. nFAULT is an open-drain output and is driven low when a fault condition occurs. If the fault condition is released, nFAULT is pulled high by an external pull-up resistor.

Short-Circuit Protection (SCP) (V_{DS} Sensing)

To protect the power stage from damage caused by high currents, V_{DS} sensing circuitry is implemented in the MP6531A. The voltage drop across each MOSFET is sensed. This voltage is proportional to the $R_{DS(ON)}$ of the MOSFET and the I_{DS} current passing through it. If this voltage exceeds the voltage supplied to the OC_REF terminal, a short circuit is recognized. In the event of a short circuit, the MP6531A disables all of the gate drive outputs. nFAULT is driven active low. The device remains latched off until it is reset by nSLEEP or VIN UVLO.

Short circuit protection can be disabled by connection a 100kΩ resistor from VREG to the OCREF pin.

Over-Current Protection (OCP)

The MP6531A can implement output over-current protection (OCP) by monitoring the current through a low-side shunt resistor connected to the LS-FETs. This resistor is connected to the LSS input pin and the LS-FET source terminals. If the OCP function is not desired, LSS and the MOSFET source terminals should all be connected to ground directly.

If the LSS voltage (the voltage across the shunt resistor) exceeds the LSS OCP threshold voltage ($V_{LSS-OCP}$), an OCP event is recognized. Once an OCP event is detected, the MP6531A enters a latched fault state and disables all functions. The device remains latched off until it is reset by nSLEEP or VIN UVLO. The OCP current limit level is selected by the value of the current sense resistor at LSS.

OCP protection can be disabled by connection a 100kΩ resistor from VREG to the OCREF pin.

Short-Circuit and OCP Deglitch Time

There is often a current spike during switching transitions caused by the body diode reverse-recovery current or the distributed capacitance of the load. This current spike requires filtering to prevent it from erroneously triggering OCP. An internal fixed deglitch time (t_{OC}) blanks the output of the VDS monitor when the outputs are switched.

Dead-Time Adjustment

To prevent shoot-through in any phase of the bridge, it is necessary to have a dead time (t_{DEAD}) between a high- or low-side turn-off and the next complementary turn-on event. The dead time for all three phases is set by a single dead-time resistor (R_{DT}) between DT and ground with Equation (1):

$$t_{DEAD}(nS) = 70*R(k\Omega) \quad (1)$$

If DT is tied to ground directly, an internal minimum dead time (130ns) is applied.

Under-Voltage Lockout (UVLO) Protection

If at any time the voltage on VIN falls below the under-voltage lockout threshold (V_{IN_RISE}), all circuitry in the device is disabled, and the internal logic is reset. Operation resumes with the power-up sequence when VIN rises above the UVLO thresholds.

After power-up, if the voltage on VREG drops below the V_{REG_RISE} threshold, the MP6531A enters a latched fault state and disables all functions. nFAULT is driven active low. The device remains latched off until it is reset by nSLEEP or VIN UVLO.

Thermal Shutdown

If the die temperature exceeds safe limits, the MP6531A enters a latched fault state and disables all functions. The device remains latched off until it is reset by nSLEEP or VIN UVLO.

APPLICATION INFORMATION

Input Voltage (VIN)

VIN supplies all power to the device. VIN must be properly bypassed with a capacitor to ground. The normal operating range of VIN is between 5V and 60V.

VIN should never be allowed to exceed the absolute maximum ratings, even in a short-term transient condition, or damage to the device may result. In some cases, especially where mechanical energy can turn a motor into a generator, it may be necessary to use some form of over-voltage protection, such as a TVS diode, between VIN and ground.

Component Selection

MOSFET Selection

Correctly selecting the power MOSFETs used to drive a motor is crucial to designing a successful motor drive. The MOSFET must have a VDS breakdown voltage higher than the supply voltage. A considerable margin (10-15V) should be added to prevent MOSFET damage from transient voltages caused by parasitic inductances in the PCB layout and wiring. For example, for 24V power supply applications, MOSFETs with a breakdown voltage of 40-60V minimum are recommended. More margin is desirable in high-current applications, since the transients caused by parasitic inductances may be larger. There are also conditions such as regenerative braking that can inject current back into the power supply. Care must be taken so that this does not increase the power supply voltage enough to damage components.

The MOSFETs must be able to safely pass the current needed to run the motor. The highest current condition (which is normally when the motor is first started or stalled) must be supported. This is called the stall current of the motor.

Similar to the current capability of the MOSFET is the $R_{DS(ON)}$, which is the resistance of the MOSFET when it is fully turned on. The MOSFET dissipates power proportional to the $R_{DS(ON)}$ and the motor current, shown in Equation (1):

$$P = I^2R \quad (1)$$

$R_{DS(ON)}$ must be selected so that for the desired motor current, the heat generated in this power can be dissipated safely. In some cases, this may require special PCB design considerations and/or external heatsinks to be used for the MOSFETs.

Consideration should be made for the safe operating area (SOA) of the MOSFETs during fault conditions such as a short circuit. The IC acts quickly in the event of a short, but there is still a very short amount of time (about 3µs) where large currents can flow in the MOSFETs while the protection circuits recognize the fault and disable the outputs.

External Capacitor Selection

The MP6531A can provide a gate drive voltage (VREG) of 10-12V, even if the input supply voltage drops as low as 5V. This gate drive voltage is generated by a charge pump inside the part, which uses external capacitors.

The charge pump flying capacitor (C_{CP}) should have a capacitance of 470nF. The capacitor must be rated to withstand the maximum VIN power supply voltage. An X7R or X5R ceramic capacitor is recommended. With a 470nF capacitor, VREG can output approximately 10mA when VIN is 5V. If operation below 10V is not needed, a 220nF capacitor can be used. To provide the large peak currents needed to turn on the HS-FET, use bootstrap capacitors. These capacitors are charged when the output is driven low, and then the charge in the bootstrap capacitor is used to turn on the HS-FET when the output is driven high. Note that an internal charge pump keeps the bootstrap capacitor charged when the output is held high for an extended period.

Bootstrap capacitors are selected depending on the MOSFET total gate charge. When the HS-FET is turned on, the charge stored in the bootstrap capacitor is transferred to the HS-FET gate. As a simplified approximation, the minimum bootstrap capacitance can be estimated with Equation (2):

$$C_{BOOT} > 8*Q_G \quad (2)$$

Where Q_G is the total gate charge of the MOSFET in nC, and C_{BOOT} is in nF.

The bootstrap capacitors should not exceed 1µF or they may cause improper operation at start-up. For most applications, the recommended bootstrap capacitors are between 0.1µF and 1µF, X5R or X7R ceramic, and rated for 25V minimum.

VREG requires a 10µF bypass capacitor to ground. This should be an X7R or X5R ceramic capacitor rated for 16V minimum.

VIN requires a bypass capacitor to ground placed as close to the device as possible. At a minimum, this capacitor should be a 0.1µF, X5R or X7R ceramic capacitor rated for the VIN voltage.

Depending on the power supply impedance and the distance between the MOSFETs and the power supply, additional bulk capacitance is usually needed. Low ESR electrolytic capacitors between 47µF and 470µF are used, typically.

Dead Time Resistor Selection

During the transition between driving an output low and high, there is a short period when neither the HS-FET or LS-FET are turned on. This period is called dead time and is needed to prevent any overlap in conduction between the HS-FET and LS-FET, which effectively provides a short circuit directly between the power supply and ground. This condition, referred to as shoot-through, causes large transient currents and can destroy the MOSFETs.

Since motors are naturally inductive, once current is flowing in the motor, it cannot stop immediately, even if the MOSFETs are turned off. This recirculation current continues to flow in the original direction until the magnetic field has decayed. When the MOSFETs are turned off, this current flows through the body diode, which is inherent in the MOSFET device. MOSFET body diodes have a much higher voltage drop than the MOSFET has during conduction, so more power is dissipated during body diode conduction than during the on time. Because of this, it is desirable to minimize the dead time. However, the dead time must be large enough to guarantee under all conditions that the HS-FET and LS-FET are never turned on at the same time.

Dead time can be set over a large range by selecting the value of the external resistor connected to DT. Usually, a good dead time is about 1µs, which requires a 14kΩ resistor on DT. If faster switching and/or a high PWM frequency (over ~30kHz) is used, a shorter dead time may be desirable. If the switching is slowed by using external gate resistors, a longer dead time may be needed.

The waveform in Figure 2 shows a ~300ns dead time between the LS gate turn-off and the HS gate turn-on.

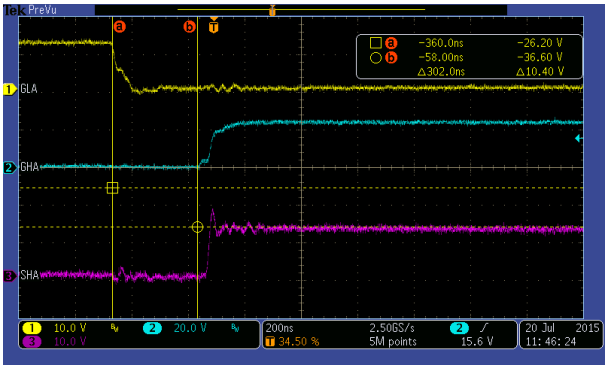


Figure 2: Dead Time

LSS Resistor Selection

If the LSS voltage exceeds 500mV, an over-current event is recognized. The external sense resistor is sized to provide a drop less than 500mV at the maximum expected motor current. For example, if a 50mΩ resistor is used, a current of 10A would cause a 500mV drop and activate over-current protection. If this function is not needed, connect LSS to ground directly.

OC_REF Voltage Selection

An internal comparator compares the voltage drop across each MOSFET with a voltage externally provided on the OC_REF input. This voltage is provided normally by an external resistor divider from a convenient power supply. If the drop across any MOSFET exceeds the voltage on OC_REF, a short-circuit event is recognized. If this function is not needed, connect OC_REF to VREG through a 100kΩ resistor.

Gate Drive Considerations

The gate characteristics of the selected MOSFETs affect how fast they are switched on and off. The gate drive outputs of the device can be connected to the gates of the power MOSFETs directly, which results in the fastest possible turn-on and turn-off times. However, it may be advantageous to add external components (resistors and/or diodes) to modify the MOSFET turn-on and turn-off characteristics.

Adding an external series resistance (typically between 10-100Ω) limits the current that charges and discharges the gate of the MOSFET, which slows down the turn-on and turn-off times. This is sometimes desirable for controlling EMI and noise. However, slowing the transition down too much results in a large power dissipation in the MOSFET during switching.

In some cases, it is desirable to have a slow turn-on but a fast turn-off. This can be implemented by using a series resistor in parallel with a diode (see Figure 3). During turn-on, the resistor limits the current flow into the gate. During turn-off, the gate is discharged quickly through the diode.

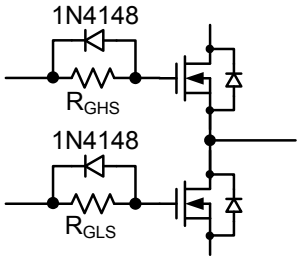


Figure 3: Gate Circuit for Fast Turn-Off

This waveform in Figure 4 shows the gates of the LS-FET and HS-FET and the phase node (output) with no series resistance. The gates transition quickly, and the resulting rise time on the phase node is quite fast (note the scale of 100ns/div).

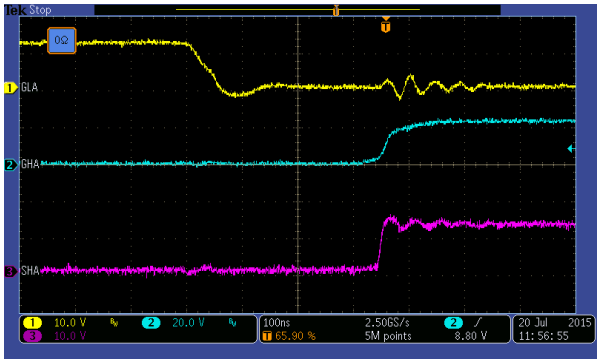


Figure 4: Switching with No Series Resistance

The waveform in Figure 5 shows the effect of adding a 100Ω series resistor between GLA and GHA and the MOSFET gates. The rise time on the phase node has been slowed significantly (note the scale here is 200ns/div).

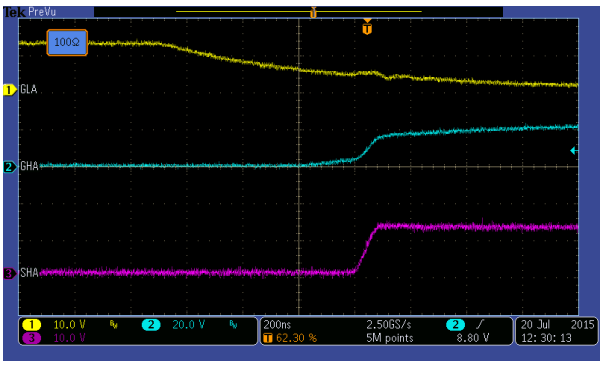


Figure 5: Switching with 100Ω Series Resistance

The waveform in Figure 6 shows the effect of adding a 1N4148 diode in parallel with the 100Ω resistors with the cathode connected to the IC. The fall time of the LS gate is quite fast compared to the HS gate rise time. The phase node moves even slower because of a longer period of time between when the LS-FET is turned off and the HS-FET is turned on.

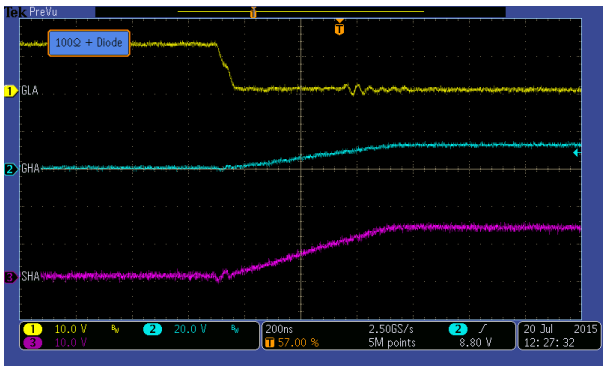


Figure 6: Switching with Resistance and Diode

PCB Layout Guidelines

Efficient PCB layout is critical for the performance of the MOSFET gate drivers. In particular, the connection between the HS source and LS drain must be as direct as possible to avoid a negative undershoot on the phase node due to parasitic inductances. The pre-driver is designed to accommodate a negative undershoot, but if it is excessive, unpredictable operation or damage to the IC can result. For best results, refer to Figure 7 (which shows the similar MP6532 IC) and follow the guidelines below.

1. Use surface-mounted N-channel MOSFETs, which allow for a very short connection between the HS-FET and LS-FET.
2. Use wide copper areas for all of the high-current paths.
3. Connect the low-side sense resistor (composed of three resistors in parallel (R25, R26, and R27)) to the input supply ground and LS-FET source terminals with wide copper areas.
4. Place the charge pump and supply bypass capacitors very close to the IC.
5. Connect the grounded side of these capacitors to a ground plane connected to the device ground pin and exposed pad.
6. Keep the high-current ground path between the input supply, input bulk capacitor (C19), and MOSFETs away from this area.

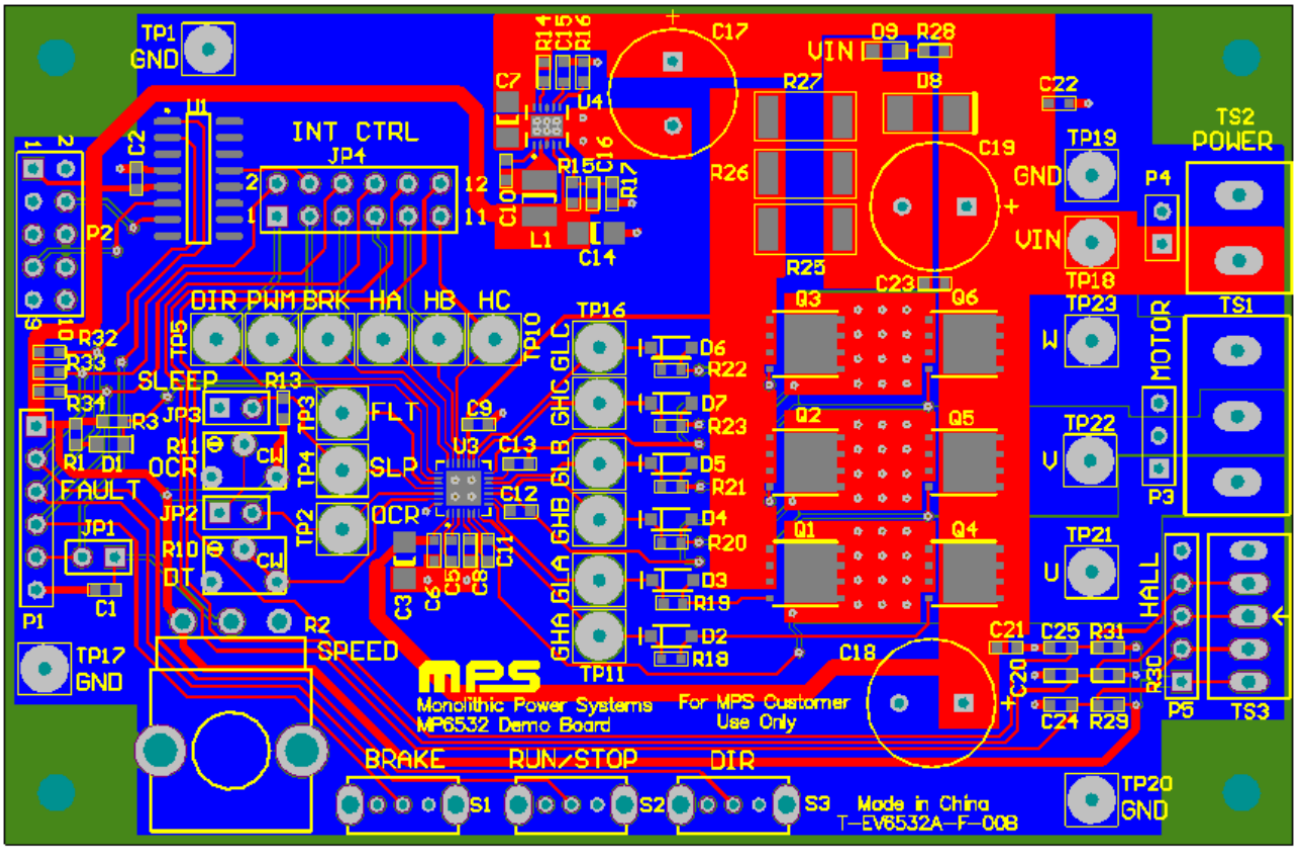
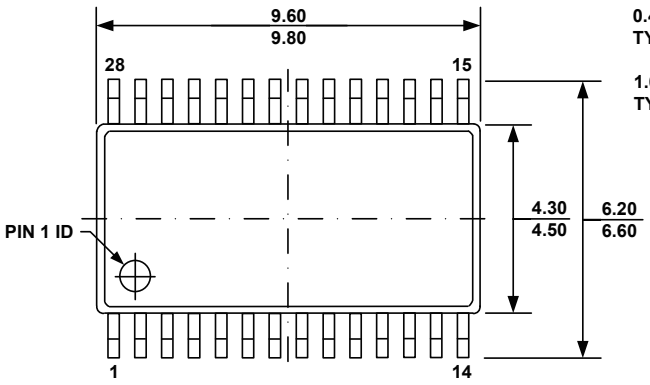


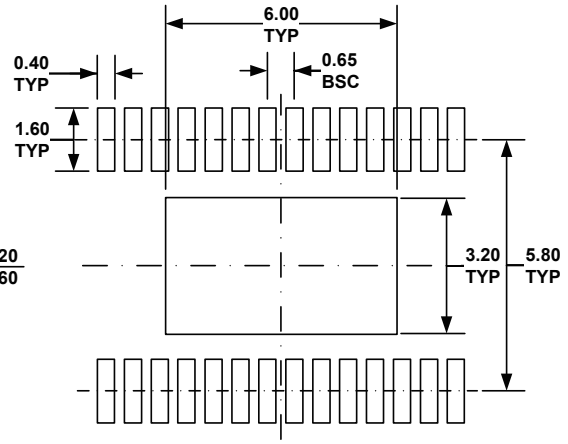
Figure 7: Recommended Layout

PACKAGE INFORMATION

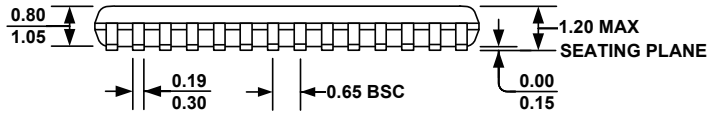
TSSOP-28 EP



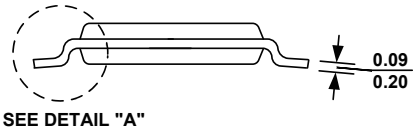
TOP VIEW



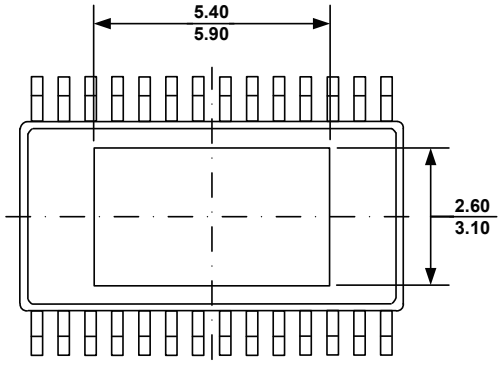
RECOMMENDED LAND PATTERN



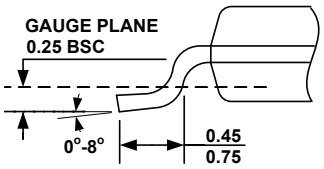
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



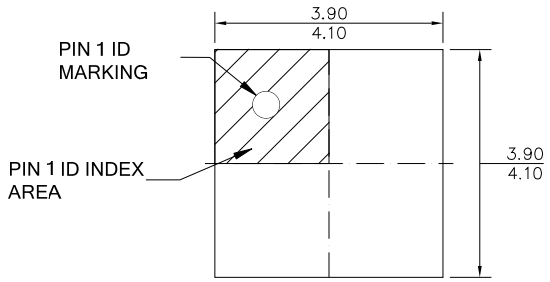
DETAIL "A"

NOTE:

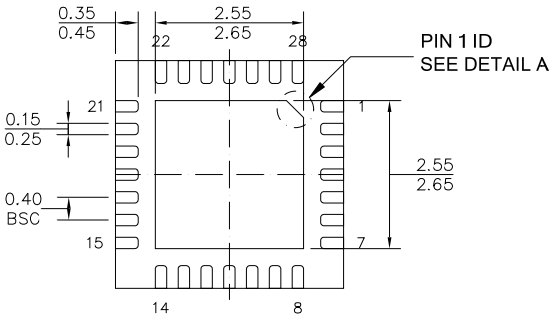
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

QFN-28 (4mmx4mm)



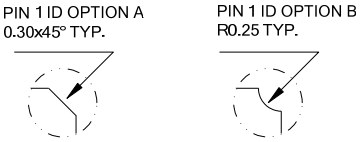
TOP VIEW



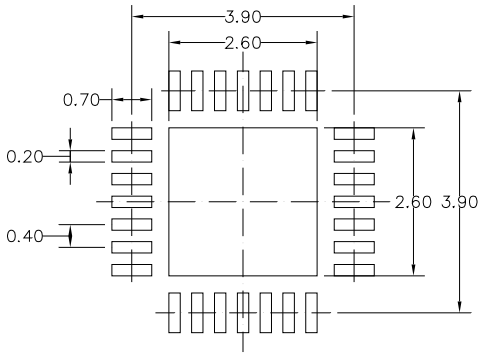
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING CONFORMS TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.