SGM814/SGM815/SGM816
Ultra-Low Power Voltage Detectors with Optional Watchdog

GENERAL DESCRIPTION

The SGM814, SGM815 and SGM816 are a family of complete microprocessor supervisory devices which combine ultra-low power, supervisory circuits and timer circuits. System reliability is significantly improved by such integration compared to the designs using individual ICs or discrete components. These devices feature a wide supply voltage from 1V to 5V. Regardless of whether the detection voltage is high or low, the output can be forced low through the manual reset pin (nMR).

If the supply voltage (V_{DD}) exceeds 0.5V during the power-on period, nRESET will assert low. And when V_{DD} is under the default voltage threshold, the nRESET output keeps low. The V_{HYS} design on V_{DD} can avoid nRESET triggering by mistake.

The SGM814 and SGM815 both have an active-low open-drain reset output, and can monitor two different voltages, either PFI or SENSE trigger the threshold, the nRESET will assert. The SGM816 has an active-low push-pull reset output and a watchdog timer to monitor the process.

The devices are available in a Green SOT-23-6 package. They operate over a junction temperature range of -40℃ to +125℃.

FEATURES

- **High Accuracy Fixed Detection Options: 1.2V, 1.5V, 1.6V, 2V and 3.3V**
- **High Trigger Accuracy: 1% (TYP)**
- **Low Quiescent Current: 1.6μA (TYP)**
- **Low nRESET Defined Input Voltage: 0.5V**
- **Delay Time for the Power-on Reset Generator: 140ms**
- **Reset Output Options:**
  - **Open-Drain: SGM814 and SGM815**
  - **Push-Pull: SGM816**
- **Available in a Green SOT-23-6 Package**

APPLICATIONS

Microprocessor Systems
Controllers
Battery-Powered Systems
Portable Equipment
Instruments and Apparatus
Communications-Equipment

TYPICAL APPLICATION

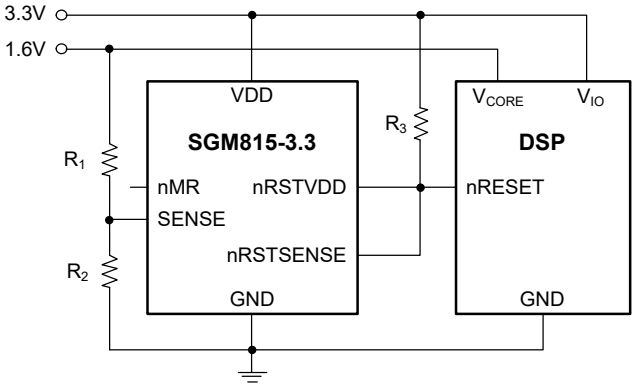


Figure 1. Typical Application Circuit Example

AVAILABLE OPTIONS

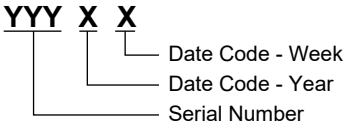
Device	nRESET Output	nRSTSENSE, nRSTVDD Output	nPFO Output	WDI Input	PFI Input	nMR Input	SENSE Input
SGM814	√ (Open-Drain)		√ (Open-Drain)		√	√	
SGM815		√ (Open-Drain)				√	√
SGM816	√ (Push-Pull)			√		√	√

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM814-1.2	SOT-23-6	-40℃ to +125℃	SGM814-1.2XN6G/TR	G6DXX	Tape and Reel, 3000
SGM814-1.5	SOT-23-6	-40℃ to +125℃	SGM814-1.5XN6G/TR	G6GXX	Tape and Reel, 3000
SGM814-2.0	SOT-23-6	-40℃ to +125℃	SGM814-2.0XN6G/TR	OU9XX	Tape and Reel, 3000
SGM814-3.3	SOT-23-6	-40℃ to +125℃	SGM814-3.3XN6G/TR	G6HXX	Tape and Reel, 3000
SGM815-1.6	SOT-23-6	-40℃ to +125℃	SGM815-1.6XN6G/TR	G6IXX	Tape and Reel, 3000
SGM815-3.3	SOT-23-6	-40℃ to +125℃	SGM815-3.3XN6G/TR	G5LXX	Tape and Reel, 3000
SGM816-1.2	SOT-23-6	-40℃ to +125℃	SGM816-1.2XN6G/TR	SWXXX	Tape and Reel, 3000
SGM816-1.5	SOT-23-6	-40℃ to +125℃	SGM816-1.5XN6G/TR	G6LXX	Tape and Reel, 3000
SGM816-3.3	SOT-23-6	-40℃ to +125℃	SGM816-3.3XN6G/TR	G6MXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... -0.3V to 6V
nMR, nRESET (Push-Pull), V_{nMR}, V_{nRESET} (Push-Pull)
.....-0.3V to V_{DD} + 0.3V
All Other Pins..... -0.3V to 6V
Maximum Low Output Current, I_{OL}.....±5mA
Maximum High Output Current, I_{OH}.....±5mA
Input Current, I_{IK} (V_{SENSE} < 0V or V_{SENSE} > V_{DD}).....±10mA
Output Current, I_{OK} (V_{OUT} < 0V or V_{OUT} > V_{DD}) (2) .....±10mA
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 230℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM (SGM814, SGM815).....1500V
HBM (SGM816) 3000V
CDM 1000V

NOTES:
1. To ensure the reliable running of the device, the continuous running time of the device at 5V cannot exceed t = 1000h.
2. For push-pull outputs, the output is clamped by the back gate diodes inside to the IC, and there is no clamp in the open-drain outputs.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD}.....1V to 5V
SENSE Voltage, V_{SENSE} ..... 0V to V_{DD}
WDI
High-level Input Voltage (V_{IH}) at nMR .....0.8 × V_{DD} (MIN)
Low-level Input Voltage (V_{IL}) at nMR ..... 0.3 × V_{DD} (MAX)
Input Transition Rise and Fall Rates at Δt/ΔV at nMR
..... 100ns/V (MAX)
nMR, PFI Voltage ..... 0V to V_{DD}
Operating Junction Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION AND DESCRIPTION

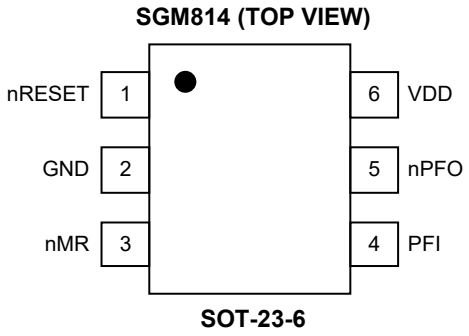


Table 1. SGM814 Pin Description

PIN	NAME	I/O	FUNCTION
1	nRESET	O	Active-Low Open-Drain Reset Output Pin.
2	GND	G	Ground.
3	nMR	I	Manual Reset Input Pin. nRESET keeps low when nMR is low. When nMR is high, nRESET becomes high after a timeout period. Leave it floating or connect it to V_{DD} if not used.
4	PFI	I	Power-Fail Voltage Monitor Input Pin. When PFI is less than 0.551V, nPFO goes low. Connect it to VDD if not used.
5	nPFO	O	Power-Fail Output Pin. Power-fail output goes low and sinks current when PFI is less than 0.551V; otherwise nPFO stays high.
6	VDD	I	Power Supply Voltage Pin. Monitor the voltage on VDD.

NOTE: I: input, O: output, G: ground.

Table 2. SGM814 Function Table

nMR	V_{PFI} > 0.551V	V_{DD} > V_{IT-}	nRESET	nPFO
L	0	X (1)	L	L
L	1	X	L	H
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

NOTE:
1. X = Don’t care.

PIN CONFIGURATION AND DESCRIPTION (continued)

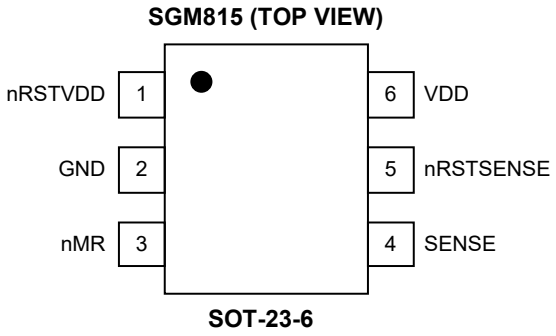


Table 3. SGM815 Pin Description

PIN	NAME	I/O	FUNCTION
1	nRSTVDD	O	Active-Low Open-Drain Reset Output Pin. The logic level is related to V_{DD} and nMR state.
2	GND	G	Ground.
3	nMR	I	Manual Reset Input Pin. Pull it low to force a reset. nRSTVDD and nRSTSENSE keeps low when nMR is low. When nMR is high, nRESET becomes high after a timeout period. Leave it floating or connect it to VDD if not used.
4	SENSE	I	Sense Voltage Pin. If the voltage is below 0.551V, the reset asserts. Connect it to VDD if not used.
5	nRSTSENSE	O	Active-Low Open-Drain Reset Output Pin. The logic level is related to SENSE voltage and nMR state.
6	VDD	I	Power Supply Voltage Pin. Monitor the voltage on VDD.

NOTE: I: input, O: output, G: ground.

Table 4. SGM815 Function Table

nMR	V_{SENSE} > 0.551V	V_{DD} > V_{IT-}	nRSTVDD	nRSTSENSE
L	X (1)	X	L	L
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

NOTE:
1. X = Don’t care.

PIN CONFIGURATION AND DESCRIPTION (continued)

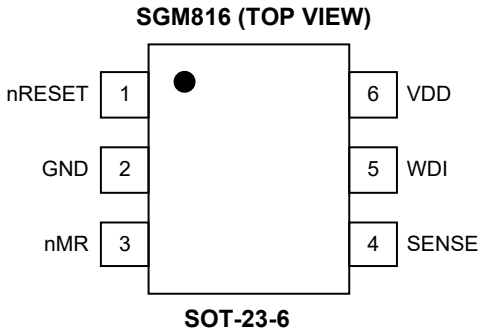


Table 5. SGM816 Pin Description

PIN	NAME	I/O	FUNCTION
1	nRESET	O	Active-Low Push-Pull Reset Output Pin.
2	GND	G	Ground.
3	nMR	I	Manual Reset Input Pin. Pull it low to force a reset. nRESET keeps low when nMR is low. When nMR is high, nRESET becomes high after a timeout period. Leave it floating or connect it to V_{DD} if not used.
4	SENSE	I	Sense Voltage Pin. If the voltage is below 0.551V, the reset asserts. Connect it to VDD if not used.
5	WDI	I	Watchdog Timer Input Pin. If the WDI remains high or low for more than the watchdog timeout period, the watchdog timer expires. The internal watchdog timer is kept clear while a reset is asserted. The timer is also cleared if the WDI input is changed (on rising or falling edges).
6	VDD	I	Power Supply Voltage Pin. Monitor the voltage on VDD.

NOTE: I: input, O: output, G: ground.

Table 6. SGM816 Function Table (1)

nMR	V_{SENSE} > 0.551V	V_{DD} > V_{IT-}	nRESET
L	X (2)	X	L
H	0	0	L
H	0	1	L
H	1	0	L
H	1	1	H

NOTES:
1. The watchdog timer function is not included.
2. X = Don't care.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
High-Level Output Voltage	V_{OH}	V_{DD} = 3.3V, I_{OH} = -3mA		0.8 × V_{DD}			V
		V_{DD} = 1.8V, I_{OH} = -2mA		0.8 × V_{DD}			
		V_{DD} = 1.5V, I_{OH} = -1mA		0.8 × V_{DD}			
		V_{DD} = 1.2V, I_{OH} = -0.4mA		0.8 × V_{DD}			
Low-Level Output Voltage	V_{OL}	V_{DD} = 3.3V, I_{OL} = 3mA				0.3	V
		V_{DD} = 1.5V, I_{OL} = 2mA				0.3	
		V_{DD} = 1.2V, I_{OL} = 1mA				0.3	
		V_{DD} = 1V, I_{OL} = 500μA				0.3	
Low-Level Output Voltage (nRESET Only)	V_{OL}	V_{DD} = 0.5V, I_{OL} = 5μA				0.1	V
Negative-Going Input Threshold Voltage (1)	V_{IT-}	SGM81x-1.2	T_J = +25℃	1.131	1.142	1.154	V
		SGM81x-1.5		1.420	1.434	1.449	
		SGM81x-1.6		1.506	1.521	1.537	
		SGM81x-2.0		1.825	1.843	1.861	
		SGM81x-3.3		2.911	2.941	2.971	
		SGM81x-1.2	T_J = -40℃ to +125℃	1.108		1.176	
		SGM81x-1.5		1.391		1.477	
		SGM81x-1.6		1.476		1.566	
		SGM81x-2.0		1.788		1.898	
		SGM81x-3.3		2.852		3.030	
Negative-Going Input Threshold Voltage (1) (SENSE, PFI)	$V_{IT-(S)}$	T_J = +25℃		0.534	0.551	0.568	V
		T_J = -40℃ to +125℃		0.523		0.579	
Temperature Coefficient of V_{IT-}, PFI, SENSE	T_K	T_J = -40℃ to +125℃			-0.003	-0.019	%/K
Hysteresis Accuracy at VDD Input	V_{HYS}/V_{IT-}				1.5		%
Hysteresis at SENSE, PFI Input	$V_{HYS(S)}$	V_{DD} ≥ 1V			15		mV
High-Level Input Current (nMR)	I_{IH}	nMR = V_{DD}, V_{DD} = 3.3V		-50		50	nA
High-Level Input Current (SENSE, PFI)		SENSE, PFI = V_{DD}, V_{DD} = 3.3V		-40		40	
High-Level Input Current (WDI)		WDI = V_{DD}, V_{DD} = 3.3V		-60		60	
Low-Level Input Current (nMR)	I_{IL}	nMR = 0V, V_{DD} = 3.3V		-39	-32	-25	μA
Low-Level Input Current (SENSE, PFI)		SENSE, PFI, WDI = 0V, V_{DD} = 3.3V		-30		30	nA
Low-Level Input Current (WDI)		WDI = 0V, V_{DD} = 3.3V		-75		75	
High-Level Output Current at nRESET (2) (Open-Drain)	I_{OH}	V_{DD} = V_{IT-} + 0.2V, V_{OH} = 3.3V				200	nA
Supply Current	I_{DD}	V_{DD} = 1V (average current)	T_J = -40℃ to +125℃		1.6	4.5	μA
		V_{DD} = 2V (average current)			1.7	5	
		V_{DD} = 3.6V (average current)			1.8	5	
		V_{DD} = 5.0V (average current)			2	5	
Internal Pull-Up Resistor at nMR	R_{nMR}			70	100	130	kΩ
Input Capacitance at nMR, SENSE, PFI, WDI	C_{IN}	V_{IN} = 0V to V_{DD}			4		pF

NOTES:

1. Place a 0.1μF bypass capacitor near VDD to ensure the stability of the threshold voltage.
2. Also refers to nRSTVDD and nRSTSENSE.

TIMING REQUIREMENTS

(At R_L = 1MΩ, C_L = 50pF and T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timeout Period at WDI	t_{T_OUT}		0.5	1.2	1.9	s
Pulse Duration at VDD	t_W	V_{IH} = 1.1 × V_{IT-}, V_{IL} = 0.9 × V_{IT-}, V_{IT-} = 1.142V	40			μs
Pulse Duration at nMR		V_{DD} ≥ V_{IT-} + 0.2V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.8 × V_{DD}	2			
Pulse Duration at SENSE		V_{DD} ≥ V_{IT-}, V_{IH} = 1.1 × $V_{IT-(S)}$, V_{IL} = 0.9 × $V_{IT-(S)}$	25			
Pulse Duration at PFI		V_{IH} = 1.1 × $V_{IT-(S)}$, V_{IL} = 0.9 × $V_{IT-(S)}$	25			
Pulse Duration at WDI		V_{DD} ≥ V_{IT-}, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	0.2			

SWITCHING CHARACTERISTICS

(At R_L = 1MΩ, C_L = 50pF and T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delay Time	t_D	V_{DD} ≥ 1.1 × V_{IT-}, nMR = 0.8 × V_{DD}, see Timing Requirements	40	140	250	ms
VDD to nRESET or nRSTVDD Propagation Delay Time, High-to-Low Level Output	t_{PHL_VDD}	V_{IH} = 1.1 × V_{IT-}, V_{IL} = 0.9 × V_{IT-}			50	μs
SENSE to nRESET or nRSTSENSE Propagation Delay Time, High-to-Low Level Output	t_{PHL_SENSE}	V_{IH} = 1.1 × V_{IT-}, V_{IL} = 0.9 × V_{IT-}			20	μs
PFI to nPFO Propagation Delay Time, High-to-Low Level Output	t_{PHL_nPFO}	V_{IH} = 1.1 × V_{IT-}, V_{IL} = 0.9 × V_{IT-}			20	μs
PFI to nPFO Propagation Delay Time, Low-to-High Level Output	t_{PLH_nPFO}	V_{IH} = 1.1 × V_{IT-}, V_{IL} = 0.9 × V_{IT-}			550	μs
nMR to nRESET, nRSTVDD, nRSTSENSE Propagation Delay Time, High-to-Low Level Output	t_{PHL_MR}	V_{DD} ≥ V_{IT-}, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.8 × V_{DD}		1	1.5	μs

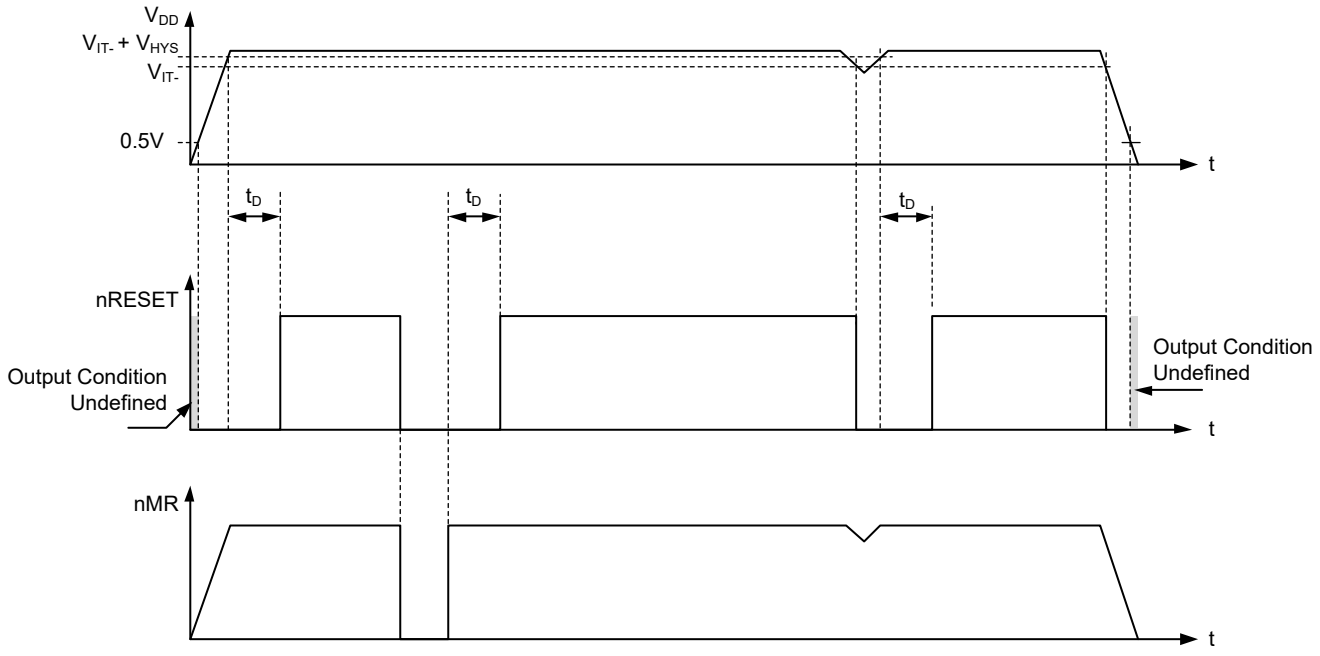


Figure 2. nRESET Timing Diagram for SGM814

SWITCHING CHARACTERISTICS (continued)

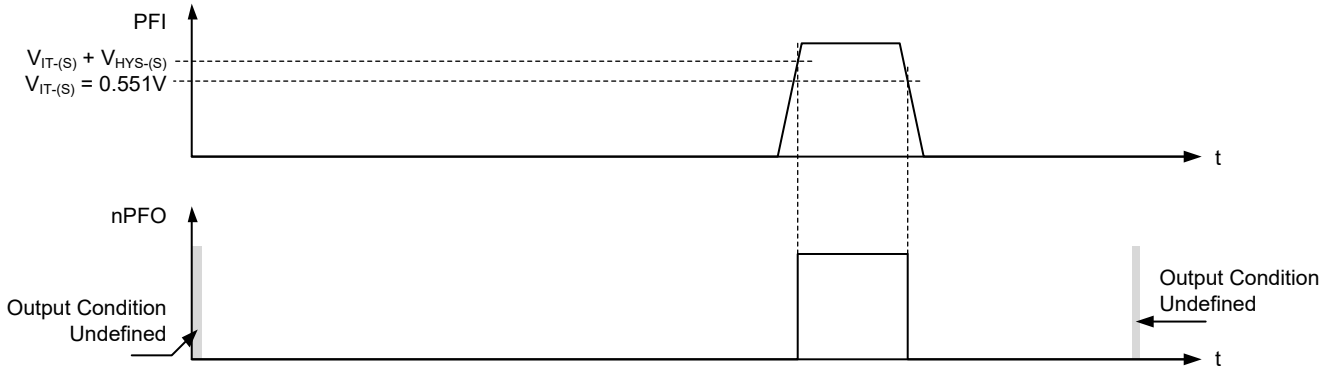


Figure 3. nPFO Timing Diagram for SGM814

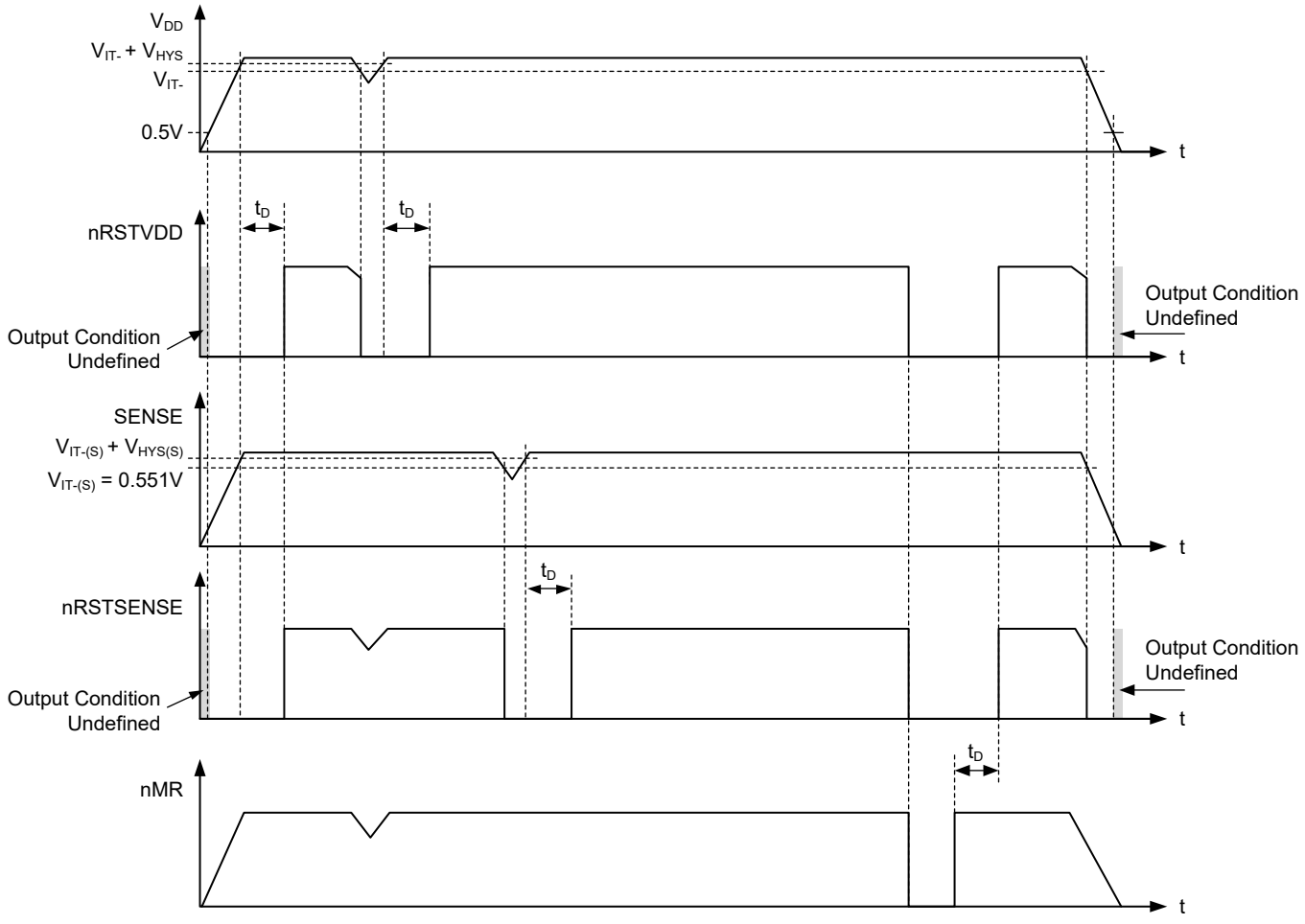


Figure 4. Timing Diagram for SGM815

SWITCHING CHARACTERISTICS (continued)

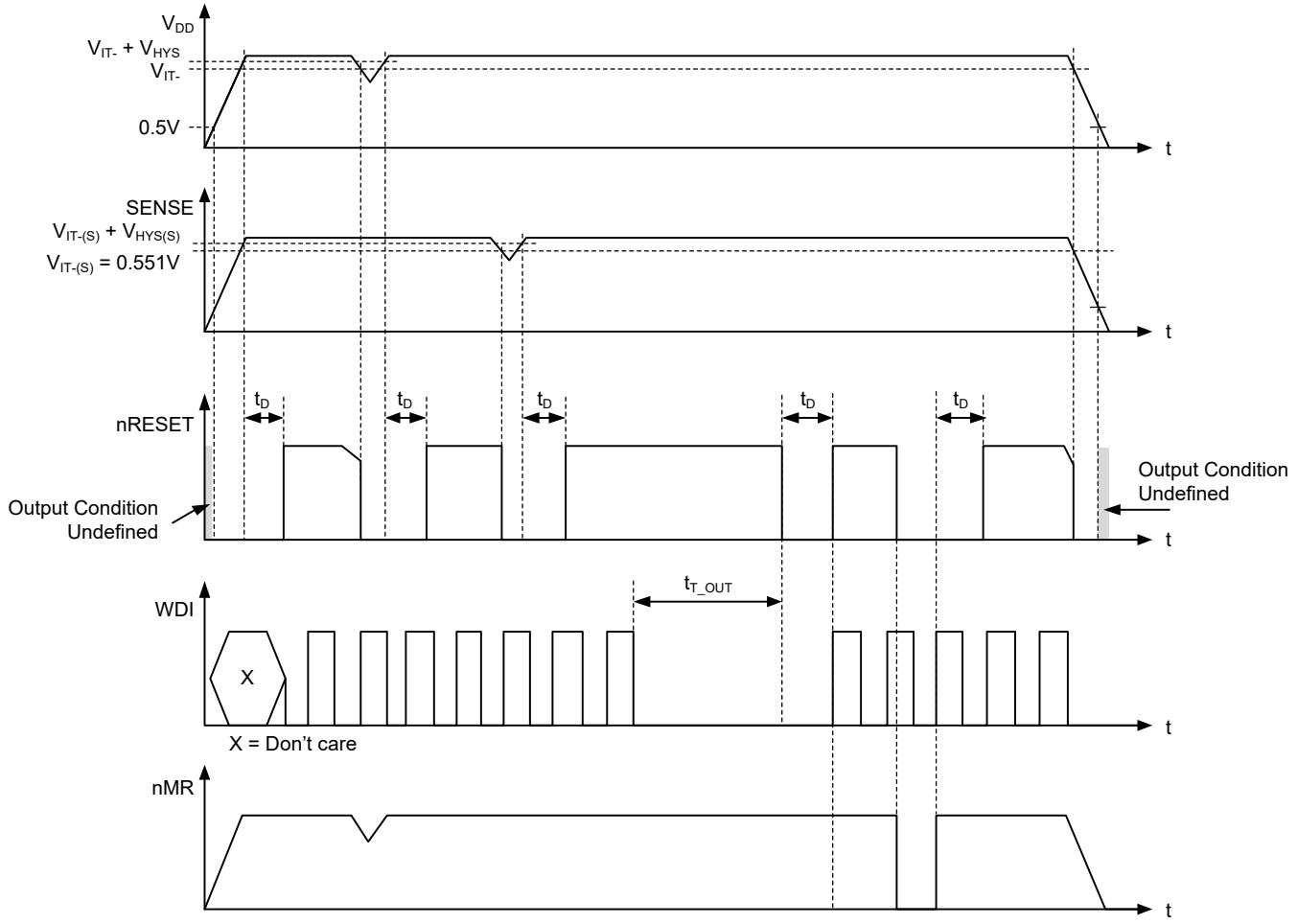
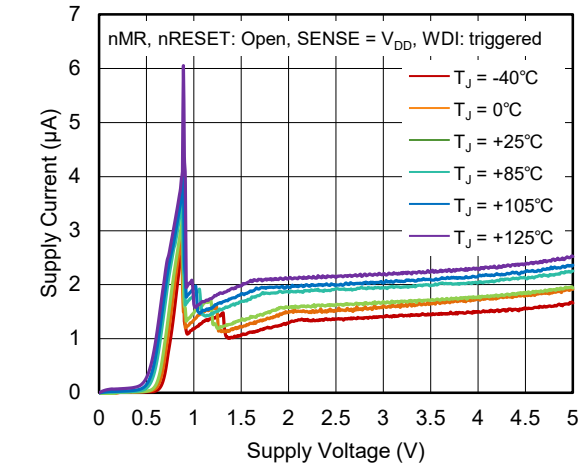


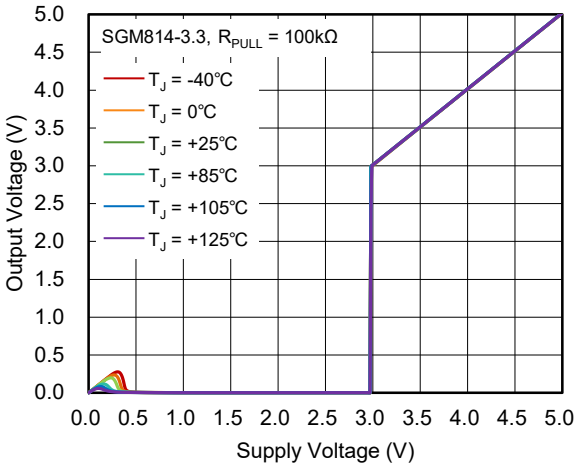
Figure 5. Timing Diagram for SGM816

TYPICAL PERFORMANCE CHARACTERISTICS

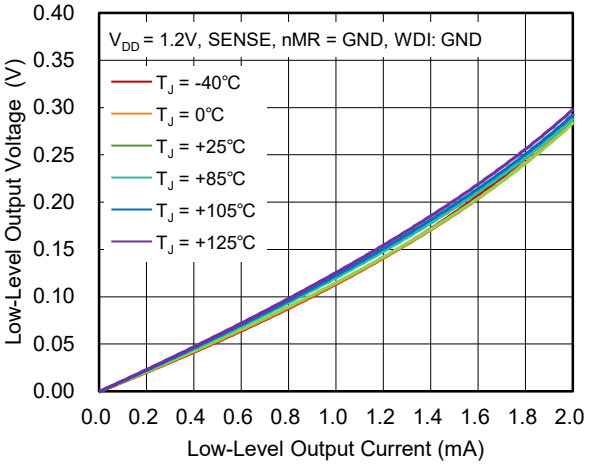
Supply Current vs. Supply Voltage



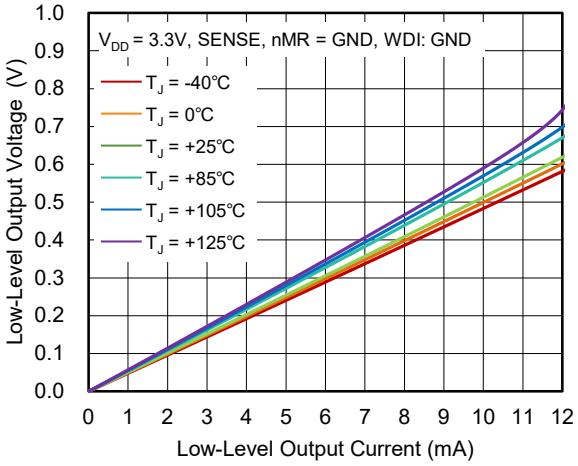
Output Voltage vs. Supply Voltage



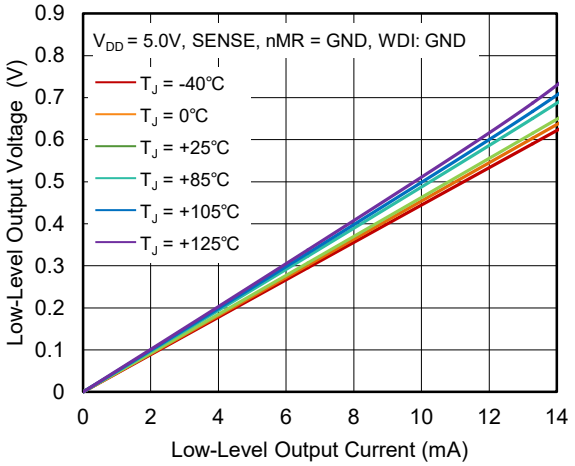
Low-Level Output Voltage vs. Low-Level Output Current



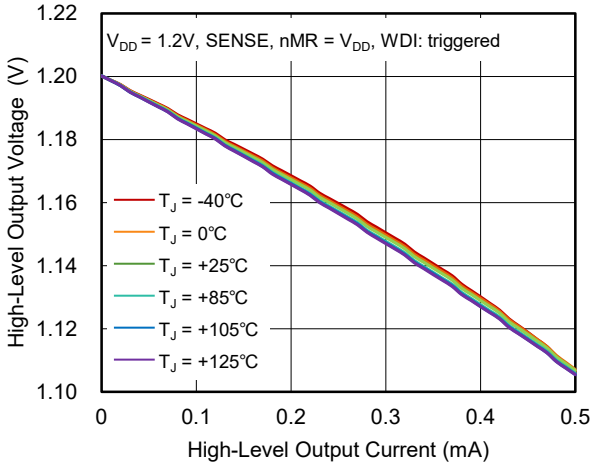
Low-Level Output Voltage vs. Low-Level Output Current



Low-Level Output Voltage vs. Low-Level Output Current

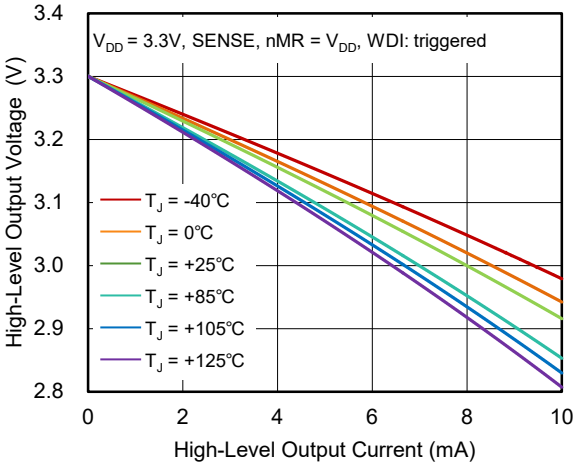


High-Level Output Voltage vs. High-Level Output Current

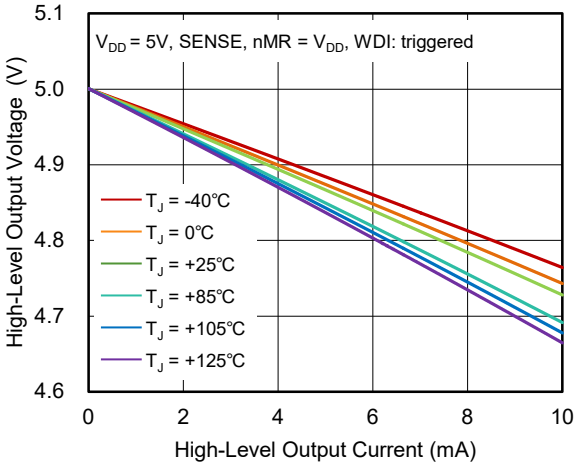


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

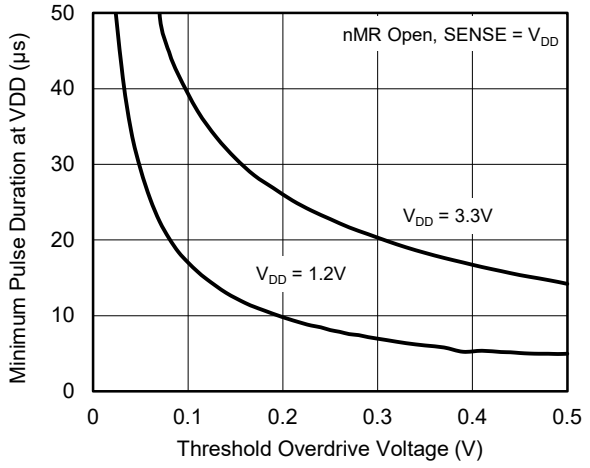
High-Level Output Voltage vs. High-Level Output Current



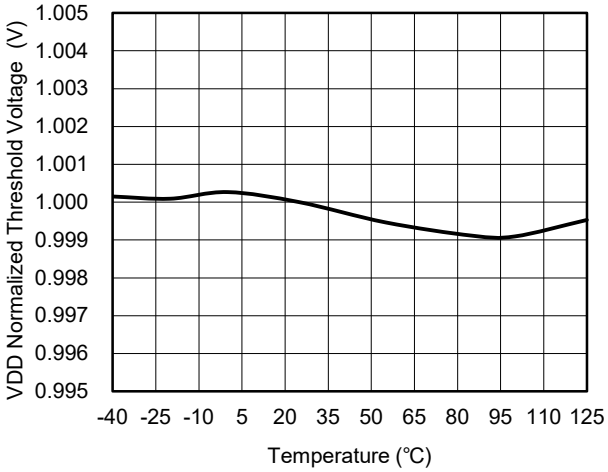
High-Level Output Voltage vs. High-Level Output Current



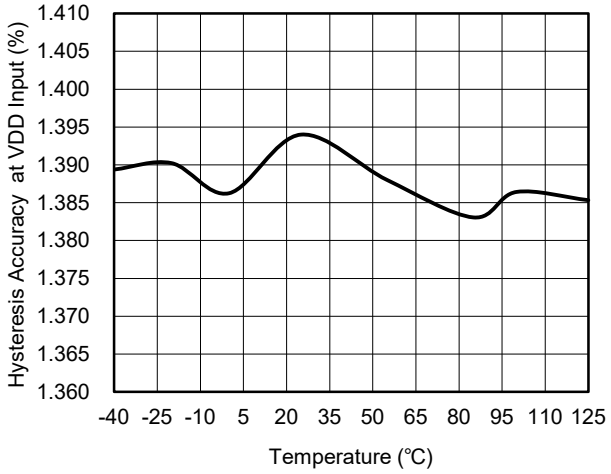
Minimum Pulse Duration at VDD vs. Threshold Overdrive Voltage



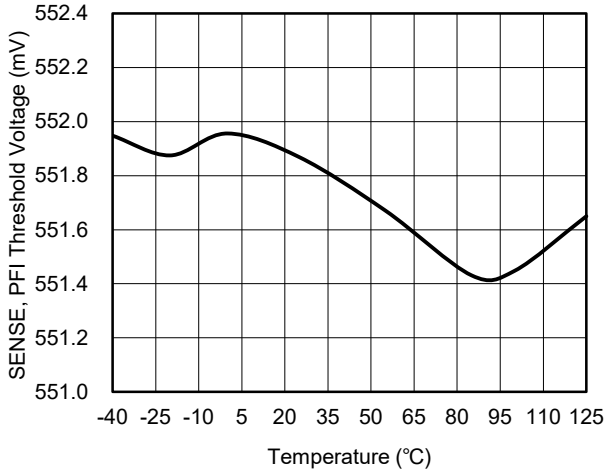
VDD Normalized Threshold Voltage vs. Temperature



Hysteresis Accuracy at VDD Input vs. Temperature

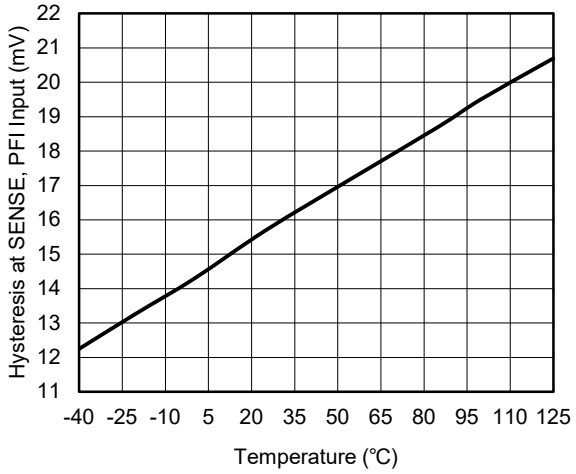


SENSE, FPI Threshold Voltage vs. Temperature

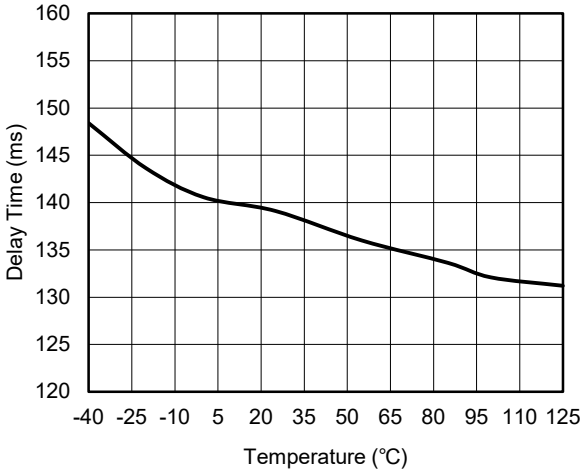


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Hysteresis at SENSE, FPI Input vs. Temperature



Delay Time vs. Temperature



FUNCTIONAL BLOCK DIAGRAMS

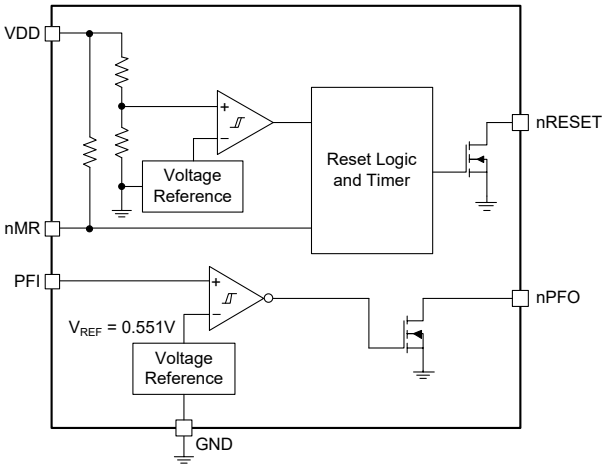


Figure 6. SGM814 Block Diagram

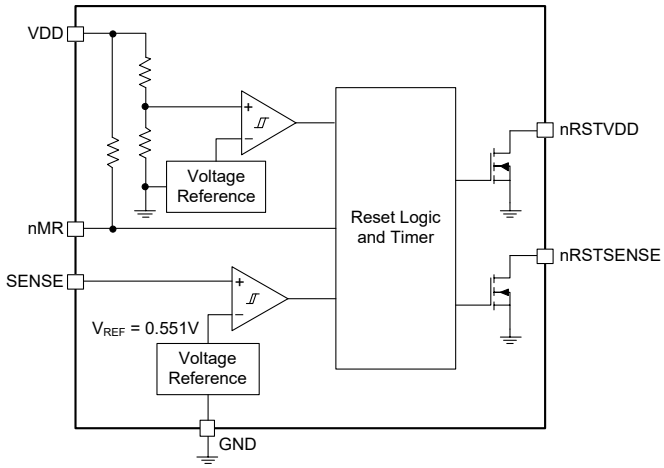


Figure 7. SGM815 Block Diagram

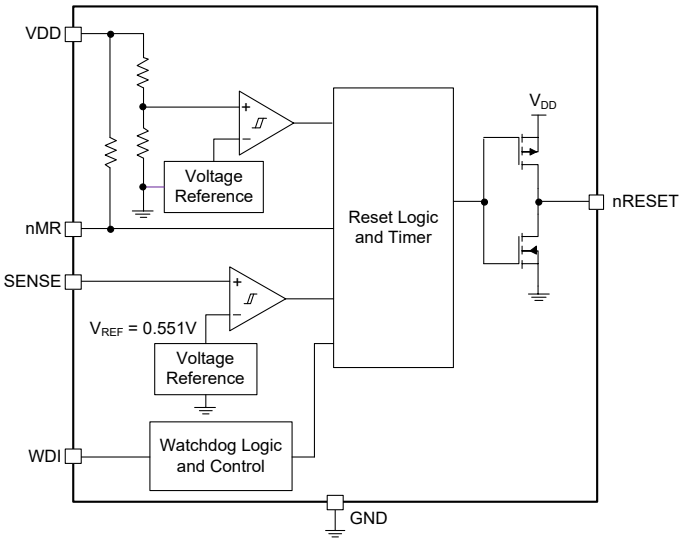


Figure 8. SGM816 Block Diagram

DETAILED DESCRIPTION

Manual Reset (nMR)

The manual reset (nMR) input allows the operator, test technician, or external logic circuit to initiate a reset. A logic low on nMR forces the nRESET low. After nMR returns to a logic high, nRESET is deasserted after a reset delay time period (t_D). nMR is pulled up to V_{DD} with an internal 100kΩ resistor. This pin can be floating if nMR is not used. It is recommended to connect a 0.1μF capacitor between nMR pin and GND to reduce ambient noise interference.

PFI, nPFO (SGM814 Only)

For SGM814, PFI (Power-Fail Input) and nPFO (Power-Fail Open-Drain Output) pins can be used for power-fail warning or monitoring a power supply other than the device power supply, and doesn't affect nRESET pin.

The internal voltage reference (0.551V) is used for compare with PFI pin, once the PFI voltage is lower than the negative-going input threshold voltage ($V_{IT-(S)}$), the nPFO goes low. Once PFI voltage exceeds 0.551V plus a hysteresis of about 15mV, the output goes high. Connecting a resistor divider externally can monitor any voltage above 0.551V.

To assure the PFI pin leakage current compared with the current through the resistor divider can be neglected and minimize the resistor power consumption, the sum of two resistors should be about 1MΩ. To ensure the accuracy of the detection voltage, the tolerance of the external resistor should be less than 1%. It is recommended to leave nPFO floating and connect PFI to VDD if the PFI comparator is not used.

SENSE (SGM815 and SGM816 Only)

A 0.551V reference voltage is intergraded in sense block, then the voltage at SENSE input will compare with it. If the SENSE voltage falls below $V_{IT-(S)}$, the nRESET goes low. For the SGM815, there is a dedicated nRSTSENSE output. For the SGM816, the logic signal of SENSE is OR-wired with the signal of VDD or nMR. Once the sensed voltage exceeds 0.551V plus a hysteresis of about 15mV, the output returns to the inactive state after a fixed delay by the internal timer.

Watchdog (SGM816 Only)

A watchdog timer is integrated in SGM816 only. It must be periodically triggered by a rising edge or a falling edge of WDI. If the monitoring system cannot retrigger the watchdog circuit during the timeout period, the nRESET becomes active within the t_D period, which will also clear the watchdog timer.

APPLICATION INFORMATION

The SGM814, SGM815 and SGM816 are excellent voltage detectors that integrate a manual reset pin. The SGM814 and SGM815 have an active-low open-drain reset output, and the SGM816 has an active-low push-pull reset output. For the SGM814, the PFI and its corresponding nPFO can be used to monitor power supplies other than the input power supply. It also has a short delay time that can realize more direct trigger output. While the SGM815 has a SENSE input and corresponding output (nRSTSENSE) to monitor two different voltages, and its delay time is longer than the SGM814 which can reduce accidental triggering of the output. The SGM816 features a watchdog timer to monitor the running of the microprocessor.

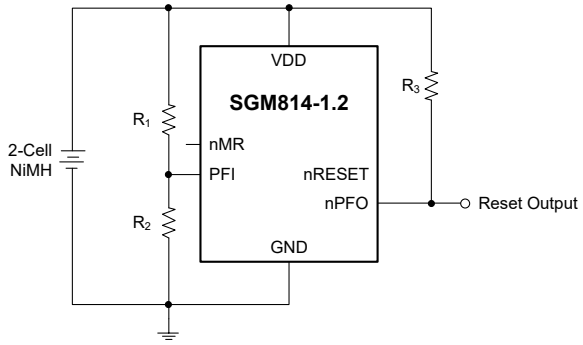


Figure 9. Battery Monitoring with Low Supply Current

Design Requirements

Both the SGM814 and SGM815 are suitable for some applications that need low quiescent current during the reset period. The SGM815 has two reset outputs, nRSTVDD and nRSTSENSE, which are triggered by the monitoring result of VDD voltage and the monitoring result of SENSE voltage respectively. The SGM814-1.2 used to monitor the input voltage of battery is shown in Figure 9. The threshold voltage V_{IT-} is 1.142V. Select low V_{IT-} to ensure the supply voltage higher than the VDD threshold voltage. And the battery voltage can be monitored by the SENSE pin.

Detailed Design Process

The voltage divider can be calculated by Equation 1, asserting a reset using the nRSTSENSE output at 2 × 0.8V = 1.6V.

$$R_1 = R_2 \times \left(\frac{V_{TRIP}}{V_{IT-(S)}} - 1 \right) \quad (1)$$

where:

V_{TRIP} is the battery voltage when a reset is asserted.

$V_{IT-(S)}$ is the SENSE threshold voltage (0.551V).

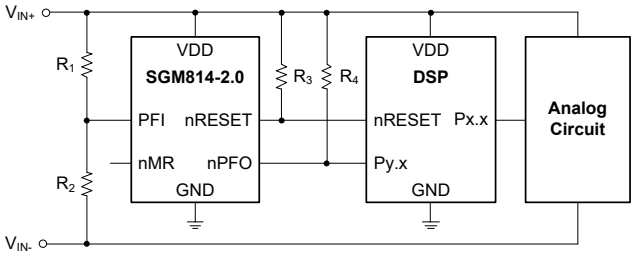
R_1 is selected for a resistor current within 1μA.

When V_{TRIP} is 1.6V, R_1 is 1.9 × R_2. Therefore, R_1 is 820kΩ and R_2 is 430kΩ.

Power Supply Recommendations

The devices operate with a wide input range from 1V to 5V. A 0.1μF ceramic capacitor is recommended between the VDD and GND pin to reduce the input supply noise.

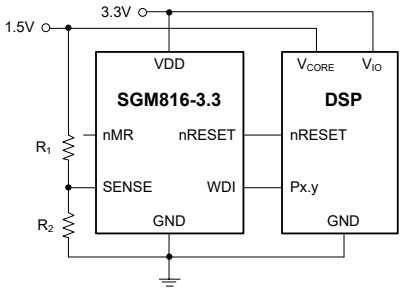
Typical Application Example



$$V_{TH\_VIN-} = 0.551V - \frac{R_2}{R_1}(V_{DD} - 0.551V) \quad (2)$$

NOTE: 1. R_3 and R_4 can be integrated in a microcontroller.

Figure 10. SGM814 Monitoring a Negative Voltage



$$V_{TH\_CORE} = 0.551V \times \frac{R_1 + R_2}{R_2} \quad (3)$$

Figure 11. SGM816 in a DSP-System Monitoring Both Supply Voltages

APPLICATION INFORMATION (continued)

Layout

It is recommended to connect the VDD decoupling capacitor to the device as close as possible. Use short and wide PCB traces for the VDD supply node. Because the trace between VDD and the capacitor will form parasitic inductance, then the parasitic inductance and the VDD capacitor will form an LC resonant circuit which will cause a ringing with peak voltages higher than the maximum V_{DD} value.

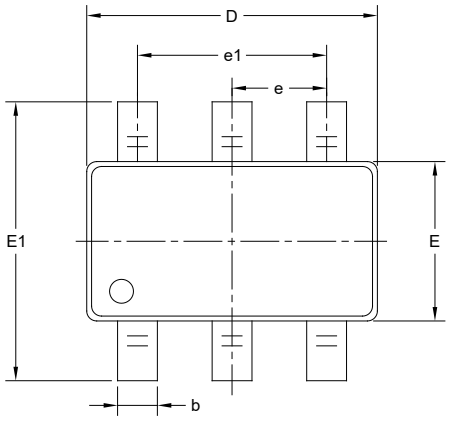
REVISION HISTORY

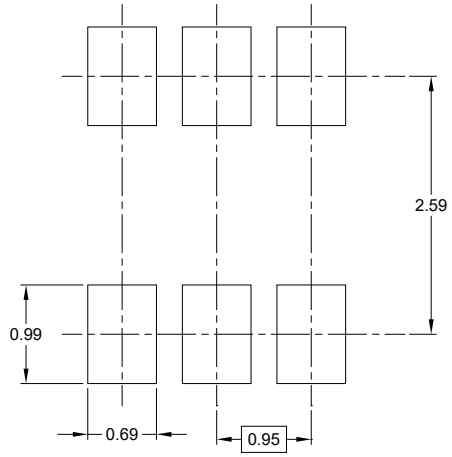
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (MAY 2022) to REV.A	Page
Changed from product preview to production data	All

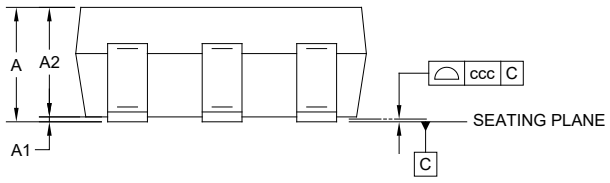
PACKAGE OUTLINE DIMENSIONS

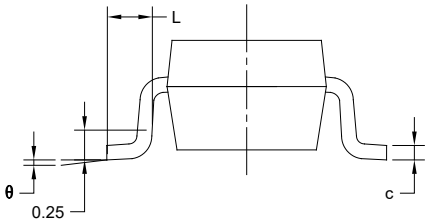
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



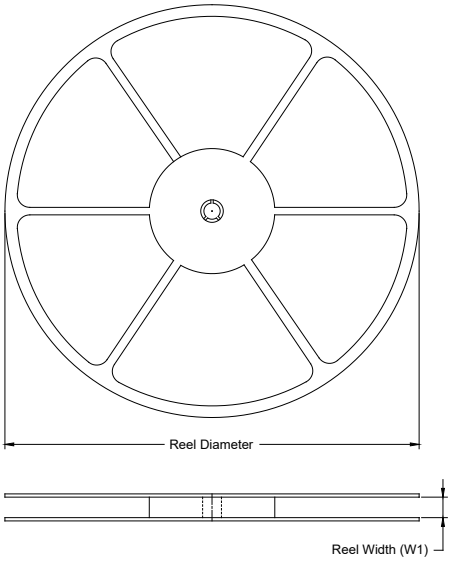


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

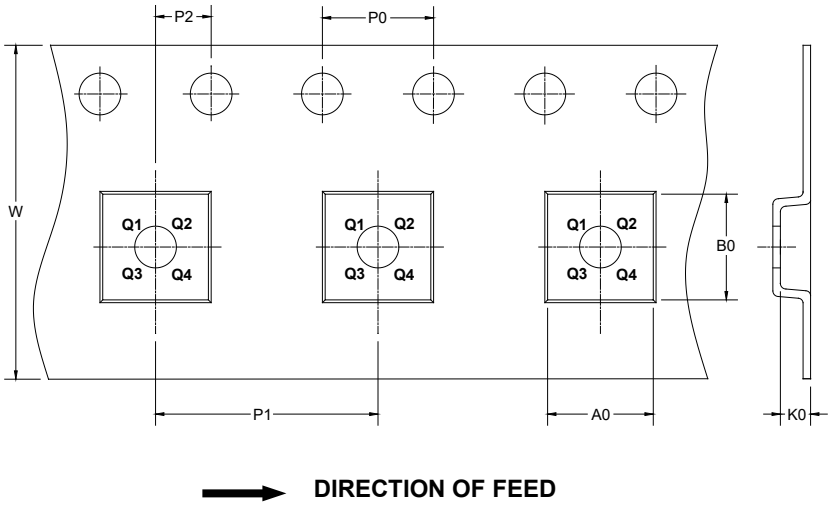
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



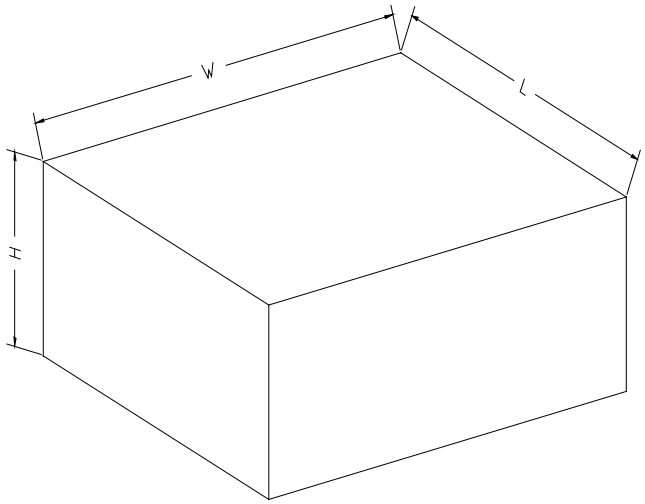
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002