SGM7300A/SGM7300B
3.3V, Differential 2-Channel, 2:1 Multiplexer/Demultiplexer Switches

GENERAL DESCRIPTION

The SGM7300A/SGM7300B are differential 2-channel switches which can be used for both multiplexer (MUX) and demultiplexer (DEMUX) configurations. The devices can be used for PCI Express Generation 3, USB 3.1 and other high-speed serial interface applications.

The products can switch dual differential signals to 1-of-2 locations. Using these design techniques, we minimizes the impedance of the switch so that the attenuation observed through the switch can be ignored and minimizes the inter-channel skew and inter-channel crosstalk required for high-speed serial interfaces. The SGM7300A and SGM7300B can achieve extremely low power consumption by extending existing high-speed ports. In order to achieve high ESD tolerance, The ESD protection circuits are integrated into integrated circuits.

We optimize the pins to match the product to different application layouts. The SGM7300A is suitable for edge connectors with different signal sources on the motherboard, with input and output pins on opposite sides of the package. The SGM7300B can be placed between two connectors to multi-channel differential signals from the controller, with output pins on both sides of the package.

The SGM7300A and SGM7300B both are available in a Green TLGA-2.5×4.5-20L package, RoHS compliant and halogen free. When no external DC is applied, there is no need for external DC blocking capacitors, thus saving PCB area and cost.

FEATURES

- **2 Bidirectional Differential Channel, 2:1 Multiplexer/Demultiplexer**
- **High-Speed Signal Switching for 10Gbps Applications**
- **High Bandwidth: 10GHz at -3dB**
- **Low Insertion Loss:**
  - **-0.4dB at 100MHz**
  - **-0.9dB at 4.0GHz**
- **Low Return Loss: -15dB at 4GHz**
- **Low Crosstalk: -35dB at 4GHz**
- **Low Off-State Isolation: -15dB at 4GHz**
- **Low Intra-Pair Skew: 10ps (TYP)**
- **Low Intra-Pair Skew: 50ps (MAX)**
- **V_{DD} Operating Range: 3.3V ± 10%**
- **Available in a Green TLGA-2.5×4.5-20L Package**

APPLICATIONS

Routing of High-Speed Differential Signals with Low Signal Attenuation

PCIe Gen3

DisplayPort 1.2

USB 3.1

SATA 6Gbit/s

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM7300A	TLGA-2.5×4.5-20L	-40℃ to +85℃			
SGM7300B	TLGA-2.5×4.5-20L	-40℃ to +85℃			

Green (RoHS & HSF): We define "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} .... -0.3V to 3.6V
Junction Temperature ....+150℃
Storage Temperature Range .... -55℃ to +150℃
Lead Temperature (Soldering, 10s) ....+260℃
ESD Susceptibility
HBM 1000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range .... -40℃ to +85℃
Supply Voltage, V_{DD} ....3.0V to 3.6V
Input Voltage, V_{IN} .... V_{DD}

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

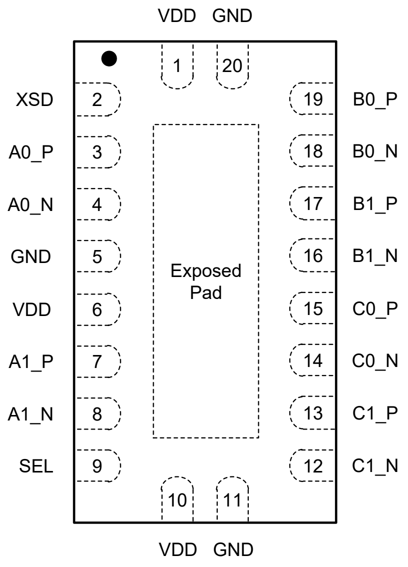
This integrated circuit can be damaged if ESD protections are not considered carefully. It recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

We reserve the right to make any change in circuit design, or specifications without prior notice.

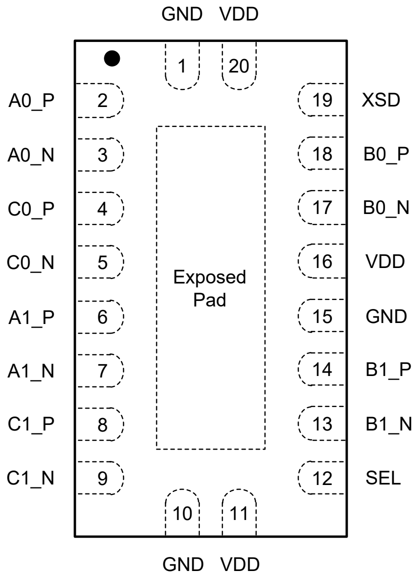
PIN CONFIGURATIONS

SGM7300A (TOP VIEW)



TLGA-2.5×4.5-20L

SGM7300B (TOP VIEW)



TLGA-2.5×4.5-20L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
SGM7300A	SGM7300B			
3	2	A0_P	I/O	Channel 0, Port A, Positive/Negative Signal.
4	3	A0_N	I/O	
7	6	A1_P	I/O	Channel 1, Port A, Positive/Negative Signal.
8	7	A1_N	I/O	
19	18	B0_P	I/O	Channel 0, Port B, Positive/Negative Signal.
18	17	B0_N	I/O	
17	14	B1_P	I/O	Channel 1, Port B, Positive/Negative Signal.
16	13	B1_N	I/O	
15	4	C0_P	I/O	Channel 0, Port C, Positive/Negative Signal.
14	5	C0_N	I/O	
13	8	C1_P	I/O	Channel 1, Port C, Positive/Negative Signal.
12	9	C1_N	I/O	
9	12	SEL	CMOS Single-ended Input	Operation Mode Select Pin. SEL = low: A ↔ B SEL = high: A ↔ C
2	19	XSD	CMOS Single-ended Input	Shutdown Pin should be Driven low or Connected to V_{SS} for Normal Operation. When high, all paths are switched off (non-conducting high-impedance state), and supply current consumption is minimized.
1, 6, 10	11, 16, 20	VDD	Power	Positive Supply Voltage.
5, 11, 20	1, 10, 15	GND	Power	Ground.
Exposed Pad		GND	Power	Ground. Exposed pad must be connected to ground.

BLOCK DIAGRAM

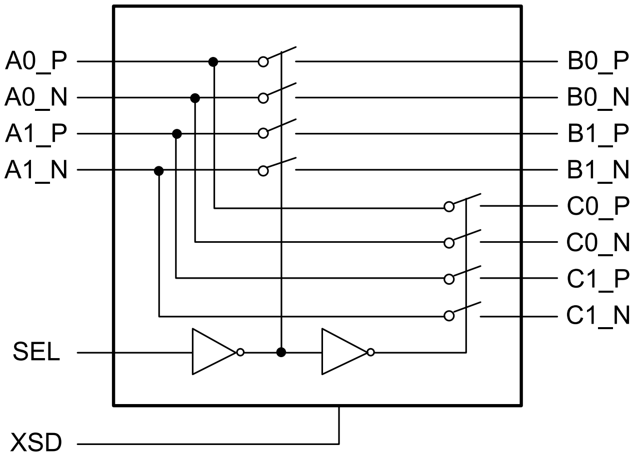


Figure 1. SGM7300A/SGM7300B Block Diagram

FUNCTIONAL DESCRIPTION

To minimize power consumption for inactive applications, the SGM7300A and SGM7300B provide shutdown functionality while still providing power. The XSD pin (active high) reduces current consumption to near zero and places all channels in a high impedance state (non-conductive). When XSD pin is low, the device operates normally. Refer to Figure 1.

Table 1. Function Selection

XSD	SEL	FUNCTION
HIGH	*X*	An, Bn and Cn Pins are High-Z
HIGH	LOW	An to Bn and Vice Versa
LOW	HIGH	An to Cn and Vice Versa

X = Don't care

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ± 10%, T_A = -40℃ to +85℃, typical values are at V_{DD} = 3.3V, T_A = +25°C, and maximum loading, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (1)	MAX	UNITS
Static Characteristics						
Supply Current	I_{DD}	Operating mode, V_{DD} = max, XSD = low		150	200	μA
		Shutdown mode, V_{DD} = max, XSD = high		150	200	
High-Level Input Current	I_{IH}	V_{DD} = max, V_I = V_{DD}			±5 (1)	μA
Low-Level Input Current	I_{IL}	V_{DD} = max, V_I = GND			±5 (1)	μA
High-Level Input Voltage	V_{IH}	SEL, XSD pins	$0.65V_{DD}$			V
Low-Level Input Voltage	V_{IL}	SEL, XSD pins			$0.35V_{DD}$	V
Input Voltage	V_{IN}	Differential pins			2.4	V
		SEL, XSD pins			V_{DD}	
Common-Mode Input Voltage	V_{IC}		0		2	V
Differential Input Voltage	V_{ID}	Peak to peak			1.6	V

NOTES:

1. Input leakage current is ±50μA if differential pairs are pulled to High and Low.

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = 3.3V ± 10%, T_{OP} = -25℃ to +85℃, typical values are at V_{DD} = 3.3V, T_{OP} = +25°C, and maximum loading, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (1)	MAX	UNITS
Dynamic Characteristics							
Differential Insertion Loss	DDIL	Channel is off	f_0 = 4GHz		-15		dB
			f_0 = 100MHz		-40		
		Channel is on	f_0 = 4GHz		-0.9		
			f_0 = 100MHz		-0.4		
Differential Near-End Crosstalk	DDNEXT	Adjacent channels are on	f_0 = 4GHz		-35		dB
			f_0 = 100MHz		-65		
-3dB Bandwidth	B_{-3dB}				10		GHz
Differential Return Loss	DDRL	f_0 = 4GHz			-15		dB
		f_0 = 100MHz			-25		
On-State Resistance	R_{ON}	V_{DD} = 3.3V, V_{IN} = 2V, I_{IN} = 19mA			5		Ω
On-State Input/Output Capacitance	C_{IO_ON}				1.5		pF
Propagation Delay	t_{PD}	From port A to port B, or port A to port C, or vice versa			100		ps
Switching Characteristics							
Start-Up Time	$t_{startup}$	Supply voltage valid or XSD going low to channel specified operating conditions				20	μs
Off-State to High Propagation Delay	t_{PZH}					500	ns
Off-State to Low Propagation Delay	t_{PZL}					100	ns
High to Off-State Propagation Delay	t_{PHZ}					100	ns
Low to Off-State Propagation Delay	t_{PLZ}					100	ns
Differential Skew Time	$t_{SK(DIF)}$	Intra-pair			10		ps
Skew Time	t_{SK}	Inter-pair				50	ps

TYPICAL APPLICATION CIRCUITS

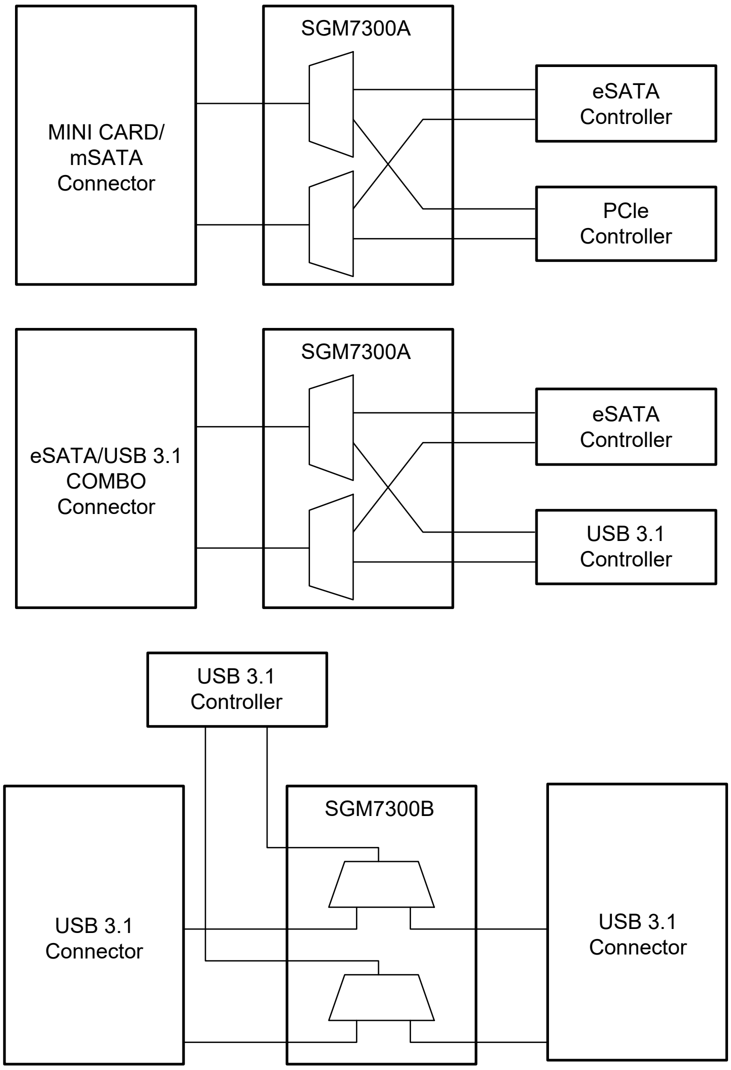
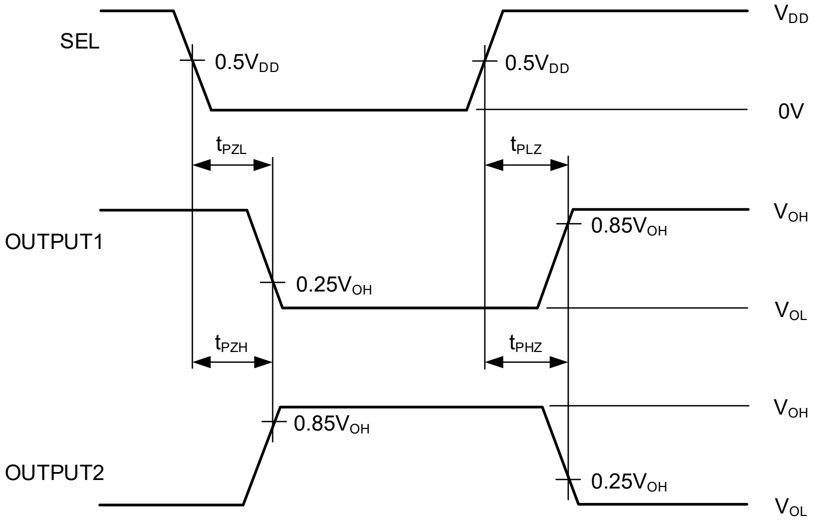


Figure 2. SGM7300A/SGM7300B Typical Application Circuits

VOLTAGE WAVEFORMS



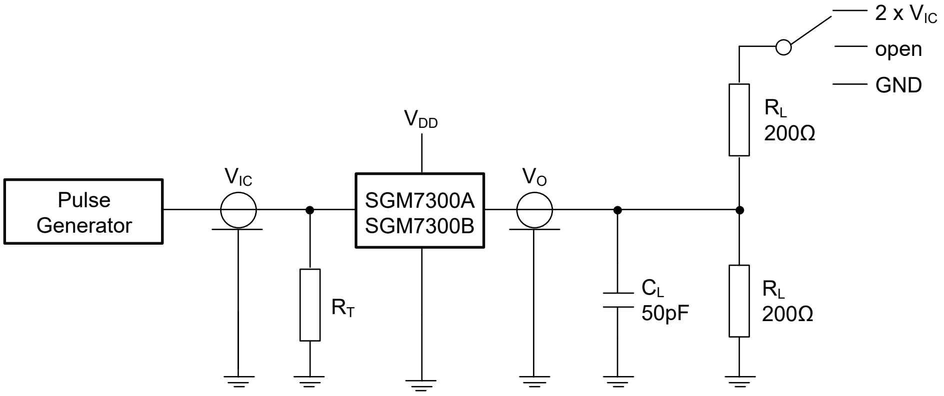
Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

The outputs are measured one at a time with one transition per measurement.

Figure 3. SGM7300A/SGM7300B Voltage Waveforms for Enable and Disable Times

TEST INFORMATION



C_L = load capacitance; includes jig and probe capacitance.
R_T = termination resistance; should be equal to Z_O of the pulse generator.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 5MHz; Z_O = 50Ω; t_R ≤ 2.5ns; t_F ≤ 2.5ns.

Figure 4. SGM7300A/SGM7300B Test Circuitry for Switching Times

1. For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.

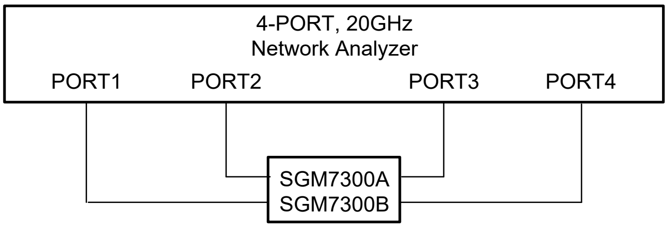


Figure 5. SGM7300A/SGM7300B Test Circuit

Table 2. Test Data

TEST	LOAD		SWITCH
	C_L	R_L	
t_{PLZ}, t_{PZL} (output on B side)	50pF	200Ω	2 × V_{IC}
t_{PHZ}, t_{PZH} (output on B side)	50pF	200Ω	GND
t_{PD}		200Ω	Open

PACKAGE OUTLINE DIMENSIONS

TLGA-2.5×4.5-20L