2.5W/CH Stereo Filterless Class-D Audio Amplifier with 64-Step DC Volume Control

DESCRIPTION

The EUA2073 is a high efficiency, 2 channel bridged-tied load (BTL), class-D audio power amplifier. Operating from a 5V power supply, EUA2073 is capable of delivering 2.5W/channel of continuous output power to a 4Ω load with 10% THD+N. The EUA2073 features an advanced 64-step DC volume control which offers a range of speaker gain from -70dB to 24dB. The new filter-less architecture allows the device to drive the speaker directly, without low-pass output filters, which will save system cost and PCB area.

The EUA2073 also features short-circuit and thermal protection preventing the device from being damaged during a fault condition. The EUA2073 is available in 16-pin SOP packages.

FEATURES

- Wide Supply Voltage: 2.7V to 5.5V
- Unique Modulation Scheme Reduces EMI Emission
- 2.5W/ch into an 4Ω Load From 5V Supply
- 64-Step DC Volume Control
- Thermal and Short-Circuit Protection
- Integrated Click and Pop Suppression
- Available in SOP-16 Packages
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- LCD Monitors/TVs
- All-in-One PCs
- Portable Audio
- Notebook PC

Typical Application Circuit

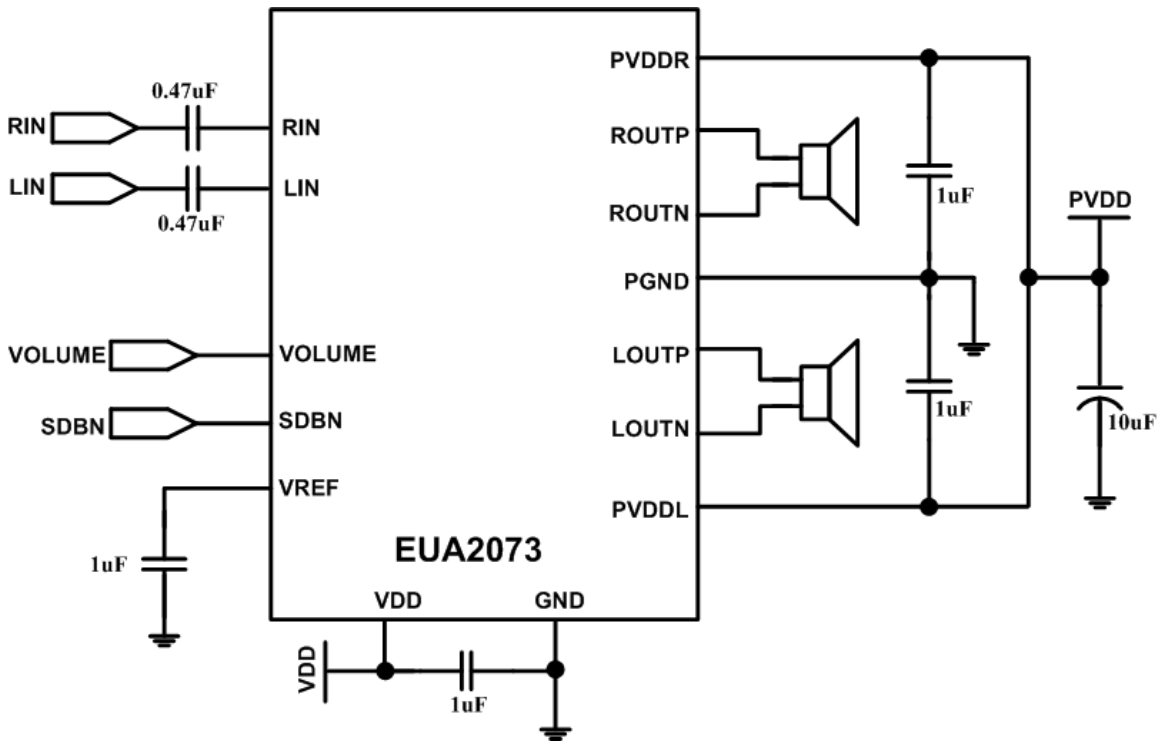
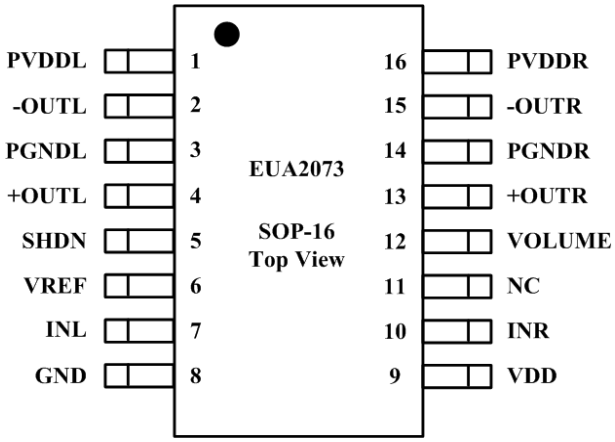


Figure1.

Pin Configurations

Package Type	Pin Configurations
SOP-16	

Pin Description

PIN	SOP-16	DESCRIPTION
PVDDL	1	Left Channel Power Supply
-OUTL	2	Left Channel Negative Output
PGNDL	3	Left Channel Power GND
+OUTL	4	Left Channel Positive Output
SHDN	5	Shutdown mode control input. Pulling low the voltage on this pin shuts off the IC.
VREF	6	Bias voltage for power amplifier.
INL	7	Input of left channel power amplifier.
GND	8	Ground.
VDD	9	Power.
INR	10	Input of right channel power amplifier.
NC	11	No connection.
VOLUME	12	Gain setting input. Connect to VDD to set max gain=24dB.
+OUTR	13	Right Channel Positive Output
PGNDR	14	Right Channel Power GND
-OUTR	15	Right Channel Negative Output
PVDDR	16	Right Channel Power Supply

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUA2073DIR1	SOP-16	xxxxx A2073	2500	-40 °C to +85°C

EUA2073 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen-Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  D: SOP

Block Diagram

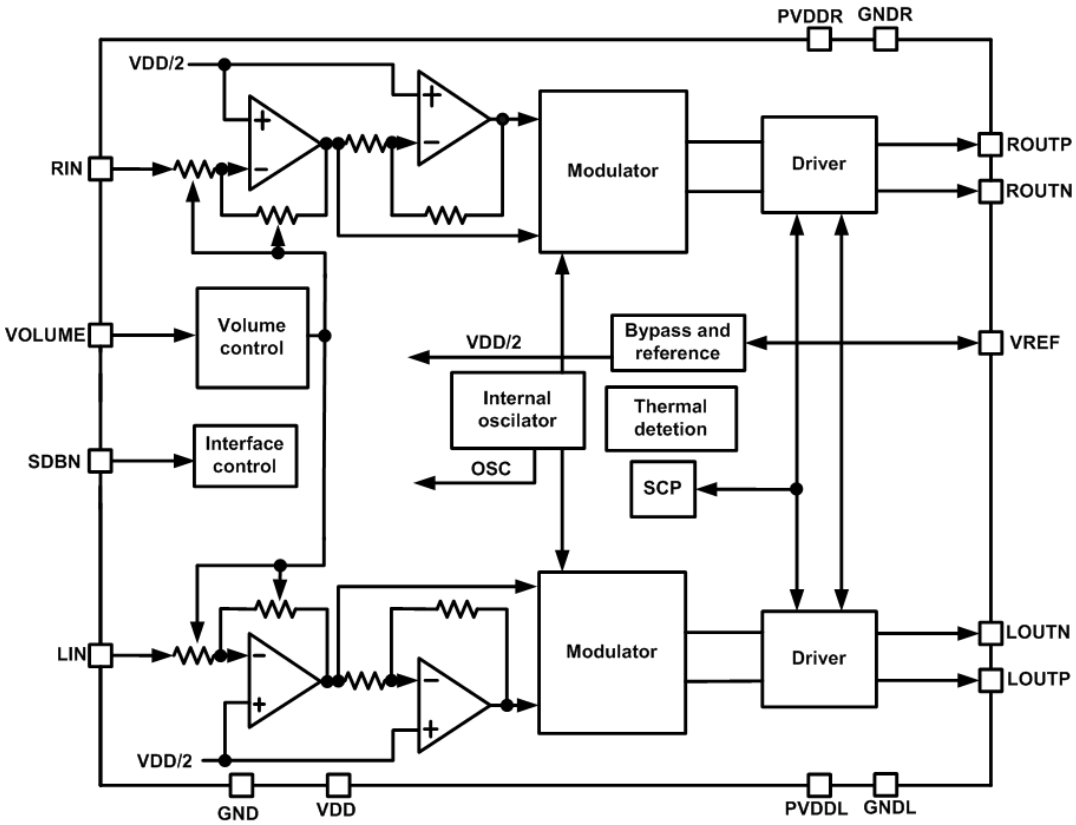


Figure2.

Absolute Maximum Ratings (1)

- Supply Voltage ---------- 0.3 V to 6V
- Input Voltage ---------- -0.3 V to V_{DD} +0.3V
- Junction Temperature, T_J ---------- -40°C to 125°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to 150°C
- ESD Susceptibility ---------- 2kV
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- Thermal Resistance

  θ_{JA} (SOP-16) ---------- 80°C/W

Recommended Operating Conditions (2)

	Min.	Max.	Unit
Supply voltage	2.7	5.5	V
Operating free-air temperature, T_A	-40	85	°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

V_{DD}=5V, Gain=Maximum, R_L=4Ω, T_A = +25°C (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2073			Unit
				Min.	Typ.	Max.	
BTL Mode							
V_{DD}	Supply Voltage Range			2.7		5.5	V
I_Q	Quiescent Current	V_{MUTE}=0V, V_{SHDN}=5V, No Load			6.5	15	mA
I_{SD}	Shutdown Current	V_{MUTE}=0V, V_{SHDN}=0V, No Load				1	μA
$\|V_{OS}\|$	Output Offset Voltage	No Load			10	50	mV
R_{DSON}	Drain-Source On-State Resistance	I_{DS}=0.1A	P MOSFET		350		mΩ
			N MOSFET		250		
P_O	Output Power	f=1kHz	R_L=4Ω		2.5		W
			R_L=8Ω		1.23		
THD+N	Total Harmonic Distortion Plus Noise	f=1kHz	R_L=4Ω,P_O=1.6W		0.2		%
			R_L=8Ω,P_O=0.8W		0.2		
PSRR	Power Supply Ripple Rejection	Input AC-GND, f=1kHz, Vpp=200mV			-60		dB
C_S	Channel Separation	P_O=1W, f=1kHz			-80		dB
f_{OSC}	Oscillator Frequency				500		kHz
V_n	Noise	A-weighting			70	110	μVrms
SNR	Signal Noise Ratio	F=20-20kHz, THD=1%			-88		dB

Electrical Characteristics (continued)

V_{DD}=5V, Gain=Maximum, R_L=4Ω, T_A = +25°C (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2073			Unit
			Min.	Typ.	Max.	
Control Section						
VIH	High Level Threshold Voltage	SHDN	2			V
VIL	Low Level Threshold Voltage	SHDN			0.8	V
OTP	Over Temperature Protection			165		℃
OTH	Over Temperature Hysteresis			30		℃

Table 1. DC Volume Control

Step	Decreasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Increasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Gain (dB)
1	100.0 - 89.2	90.2 - 100.0	24.0
2	89.2 - 87.8	88.8 - 90.2	23.6
3	87.8 - 86.4	87.4 - 88.8	23.2
4	86.4 - 85.0	86.0 - 87.4	22.8
5	85.0 - 83.6	84.6 - 86.0	22.4
6	83.6 - 82.2	83.2 - 84.6	22.0
7	82.2 - 80.8	81.8 - 83.2	21.6
8	80.8 - 79.4	80.4 - 81.8	21.2
9	79.4 - 78.0	79.0 - 80.4	20.8
10	78.0 - 76.6	77.6 - 79.0	20.4
11	76.6 - 75.2	76.2 - 77.6	20.0
12	75.2 - 73.8	74.8 - 76.2	19.6
13	73.8 - 72.4	73.4 - 74.8	19.2
14	72.4 - 71.0	72.0 - 73.4	18.8
15	71.0 - 69.6	70.6 - 72.0	18.4
16	69.6 - 68.2	69.2 - 70.6	18.0
17	68.2 - 66.8	67.8 - 69.2	17.6
18	66.8 - 65.4	66.4 - 67.8	17.2
19	65.4 - 64.0	65.0 - 66.4	16.8
20	64.0 - 62.6	63.6 - 65.0	16.4
21	62.6 - 61.2	62.2 - 63.6	16.0
22	61.2 - 59.8	60.8 - 62.2	15.6
23	59.8 - 58.4	59.4 - 60.8	15.2
24	58.4 - 57.0	58.0 - 59.4	14.8
25	57.0 - 55.6	56.6 - 58.0	14.4
26	55.6 - 54.2	55.2 - 56.6	14.0
27	54.2 - 52.8	53.8 - 55.2	13.6
28	52.8 - 51.4	52.4 - 53.8	13.2
29	51.4 - 50.0	51.0 - 52.4	12.8
30	50.0 - 48.6	49.6 - 51.0	12.4
31	48.6 - 47.2	48.2 - 49.6	12.0
32	47.2 - 45.8	46.8 - 48.2	11.6
33	45.8 - 44.4	45.4 - 46.8	11.2
34	44.4 - 43.0	44.0 - 45.4	10.8
35	43.0 - 41.6	42.6 - 44.0	10.4
36	41.6 - 40.2	41.2 - 42.6	10.0
37	40.2 - 38.8	39.8 - 41.2	9.6
38	38.8 - 37.4	38.4 - 39.8	9.2
39	37.4 - 36.0	37.0 - 38.4	8.8
40	36.0 - 34.6	35.6 - 37.0	8.4
41	34.6 - 33.2	34.2 - 35.6	8.0
42	33.2 - 31.8	32.8 - 34.2	7.6
43	31.8 - 30.4	31.4 - 32.8	7.2
44	30.4 - 29.0	30.0 - 31.4	6.8
45	29.0 - 27.6	28.6 - 30.0	6.4
46	27.6 - 26.2	27.2 - 28.6	6.0
47	26.2 - 24.8	25.8 - 27.2	5.6
48	24.8 - 23.4	24.4 - 25.8	5.2
49	23.4 - 22.0	23.0 - 24.4	4.8
50	22.0 - 20.6	21.6 - 23.0	4.4
51	20.6 - 19.2	20.2 - 21.6	4.0
52	19.2 - 17.8	18.8 - 20.2	3.0
53	17.8 - 16.4	17.4 - 18.8	2.0
54	16.4 - 15.0	16.0 - 17.4	1.0
55	15.0 - 13.6	14.6 - 16.0	-1.0
56	13.6 - 12.2	13.2 - 14.6	-3.0
57	12.2 - 10.8	11.8 - 13.2	-5.0
58	10.8 - 9.4	10.4 - 11.8	-7.0
59	9.4 - 8.0	9.0 - 10.4	-13.0
60	8.0 - 6.6	7.6 - 9.0	-19.0
61	6.6 - 5.2	6.2 - 7.6	-25.0
62	5.2 - 3.8	4.8 - 6.2	-31.0
63	3.8 - 2.4	3.4 - 4.8	-37.0
64	2.4 - 0.0	0.0 - 3.4	-70.0

Typical Characteristics

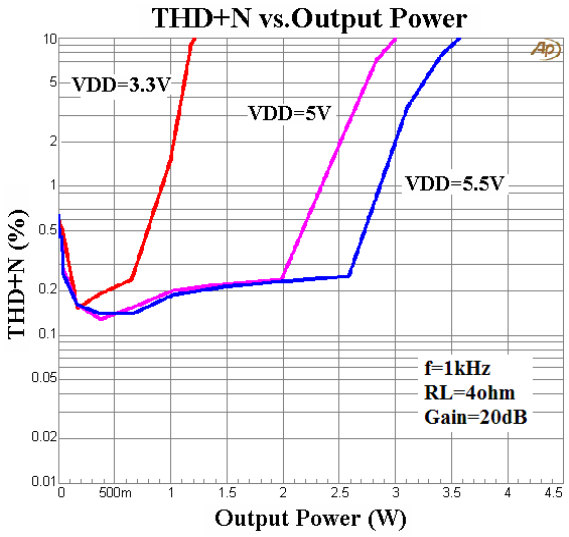
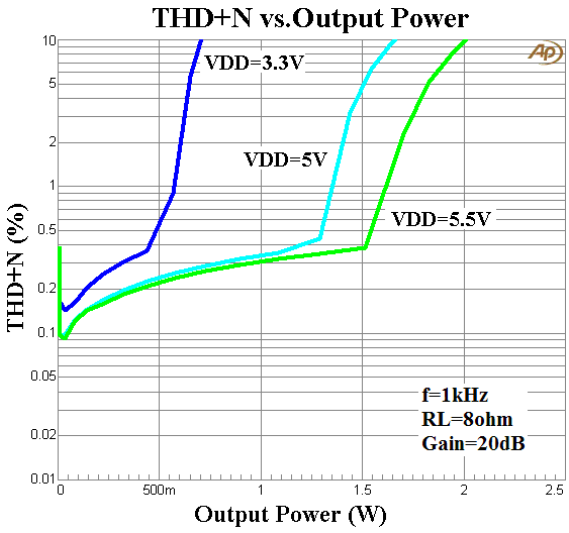


Figure3.



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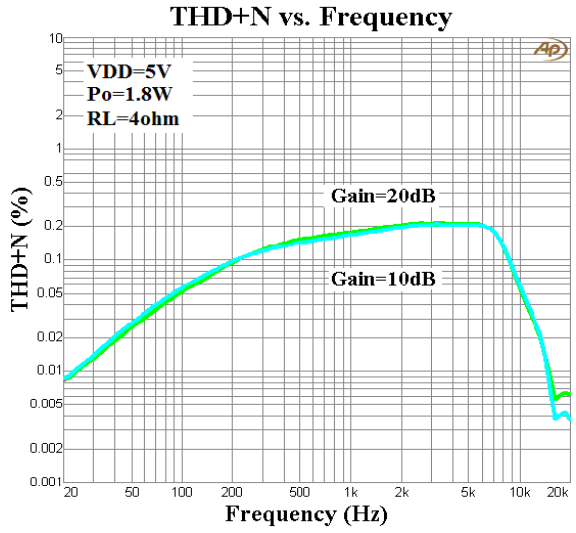

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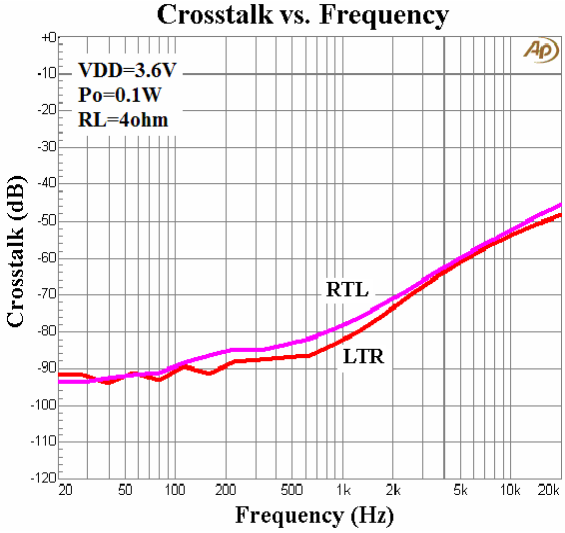

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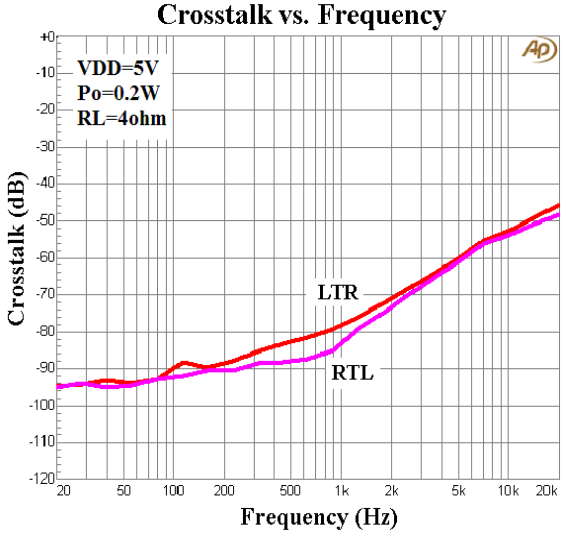

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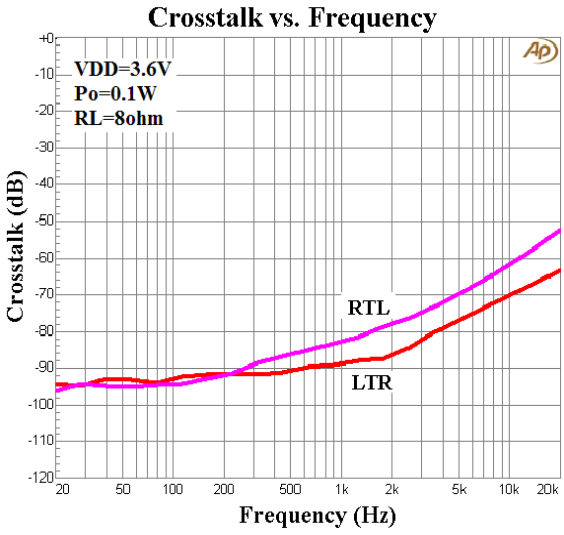
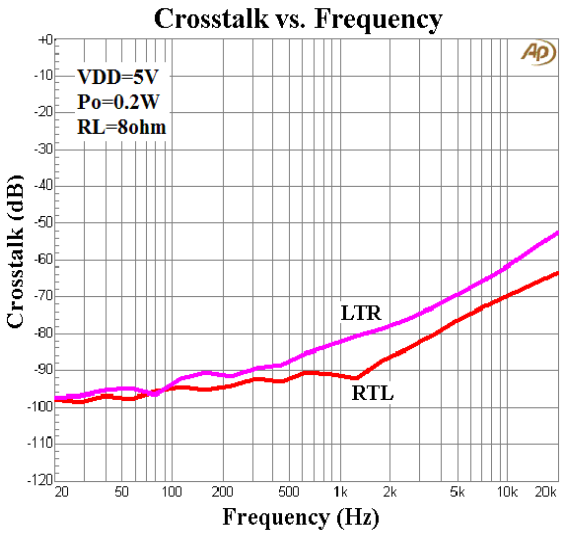


Figure8.

Typical Characteristics (continued)



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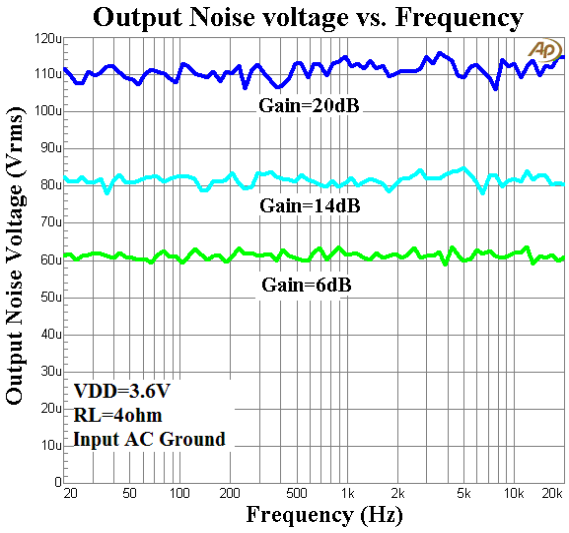

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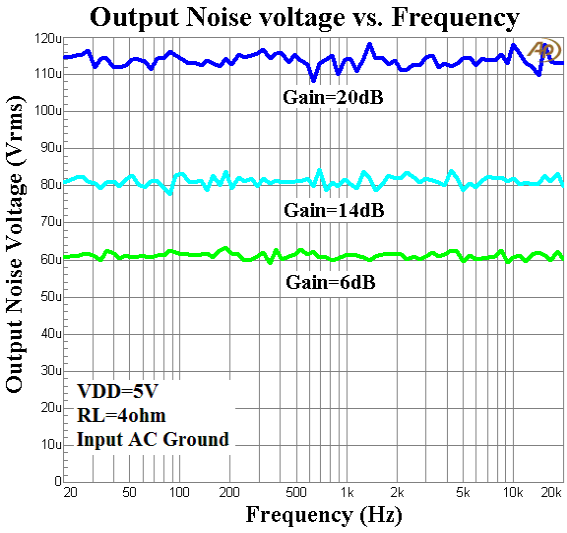

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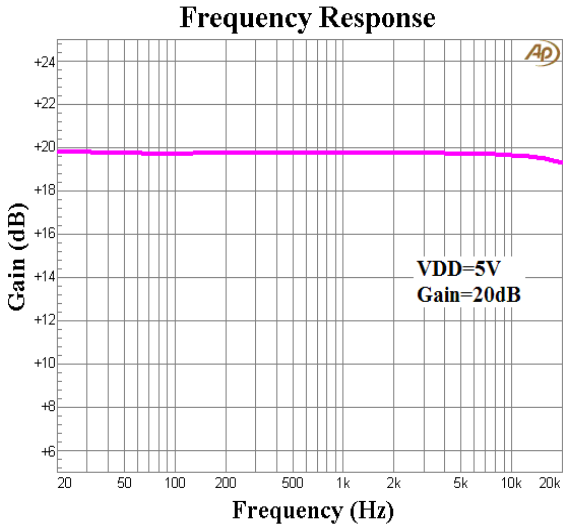

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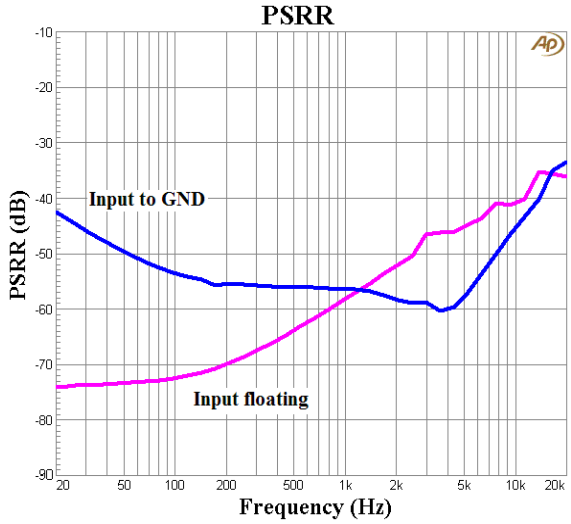


Figure13.

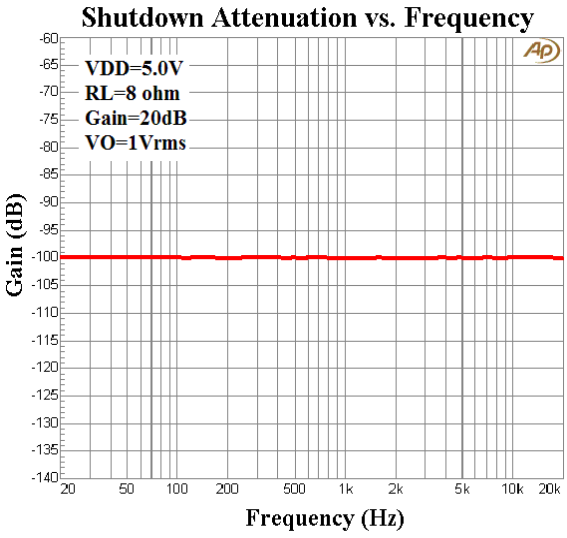
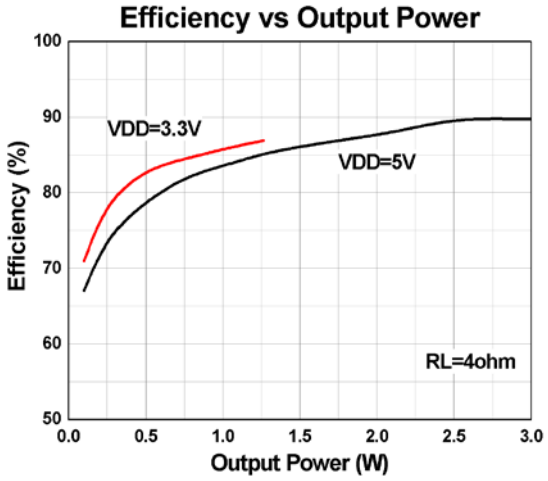


Figure14.

Typical Characteristics (continued)



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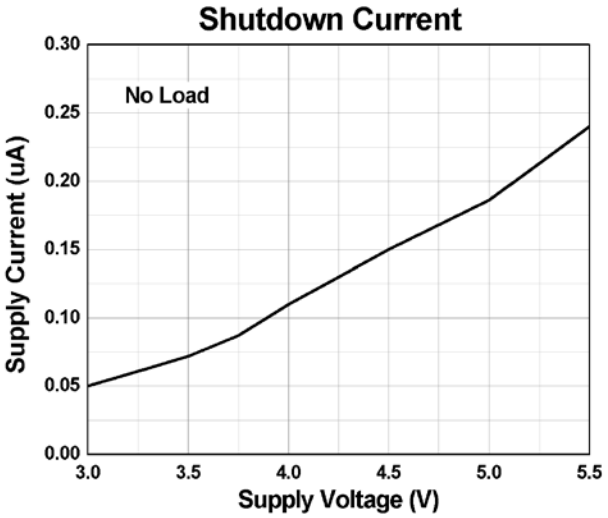

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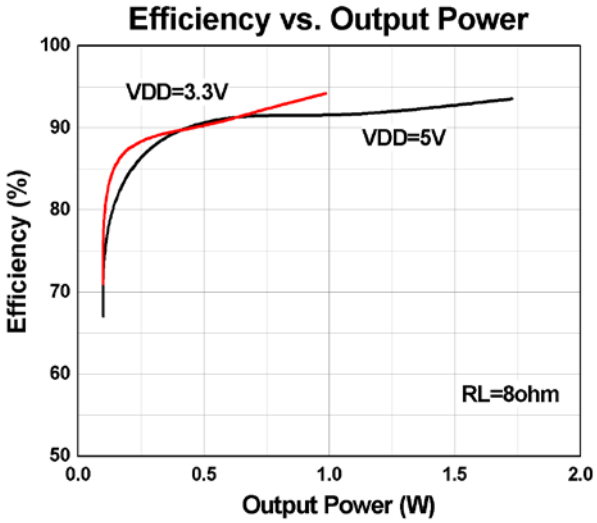


Figure17.

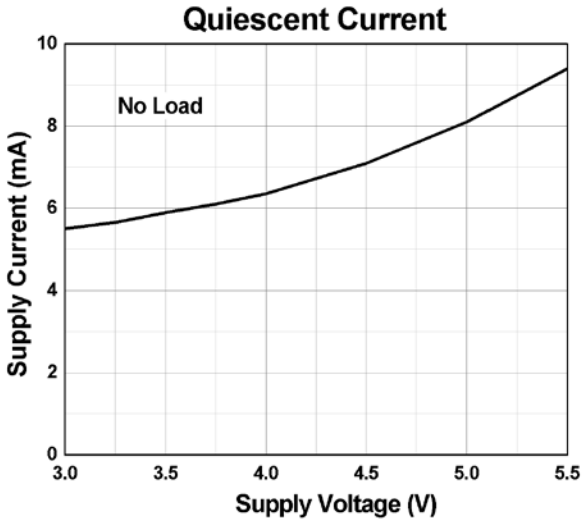


Figure18.

Application Information

Volume Control Operation

The VOLUME terminal controls the internal amplifier gain. This pin is controlled with a dc voltage, which should not exceed VDD. Table 1 lists the gain as determined by the voltage on the VOLUME pin in reference to the voltage on VDD.

A resistor divider can be connected across VDD and GND. For fixed gain, calculate the resistor divider values necessary to center the voltage between the two percentage points given in the first column of Table 1.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another.

The timing of the volume control circuitry is controlled by an internal 30-Hz clock. This clock determines the rate at which the gain changes when adjusting the voltage on the external volume control pins. The gain updates every clock cycle (nominally 32 ms) to the next step until the final desired gain is reached.

FADE Operation

During power-up or recovery from the shutdown state (a logic high is applied to the SHDN terminal), the volume is smoothly ramped up from the mute state, -70dB, to the desired volume setting determined by the voltage on the volume control terminal. Conversely, the volume is smoothly ramped down from the current state to the mute state when a logic low is applied to the SHDN terminal.

Shutdown Operation

In order to reduce power consumption while not in use, the EUA2073 contains shutdown circuitry to turn off the amplifier's bias circuitry. The amplifier is turned off when logic low is placed on the SHDN pin. By switching the SHDN pin connected to GND, the EUA2073 supply current draw will be minimized in idle mode. The SHDN pin can't be left floating.

For the best power on/off pop performance, the amplifier should be placed in the Mute mode prior to turning on/off the power supply.

Power Supply Decoupling

The EUA2073 is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR are as low as possible. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF, placed as close as possible to the device VDD terminal works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Input Capacitor (Ci)

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance. In this case, input capacitor (Ci) and input resistance (Ri) of the amplifier form a high-pass filter with the corner frequency determined equation below:

$$f_c = \frac{1}{2\pi RiCi}$$

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, Ci. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Analog Reference Vref Capacitor (C_{vref})

The Analog Reference Vref Capacitor (C_{vref}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{vref} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N. A ceramic bypass capacitor (C_{vref}) of 1μF to 2.2μF is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

Short Circuit Protection (SCP)

The EUA2073 has short circuit protection circuitry on the outputs that prevents the device from damage when output-to-output and output-to-GND short. When a short circuit is detected on the outputs, the outputs are disabled immediately. The IC will turn on the output after about 200ms. But if the short circuit condition is still remain, the output will be disabled again. The situation will circulate until the short circuit condition is removed.

Over Temperature Protection

Thermal protection on the EUA2073 prevents the device from damage when the internal die temperature exceeds 165°C. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. This large hysteresis will prevent motor boating sound well. The device begins normal operation at this point without external system interaction.

How to Reduce EMI (Electro Magnetic Interference)

A simple solution is to put an additional capacitor 1000μF at power supply terminal for power line coupling if the traces from amplifier to speakers are short (<20CM). Most applications require a ferrite bead filter as shown at Figure 19. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at low frequency.

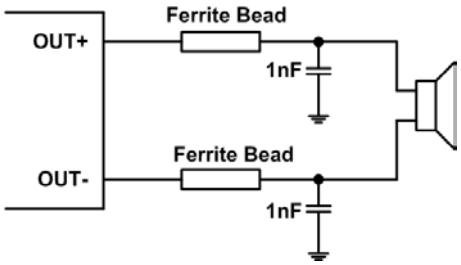
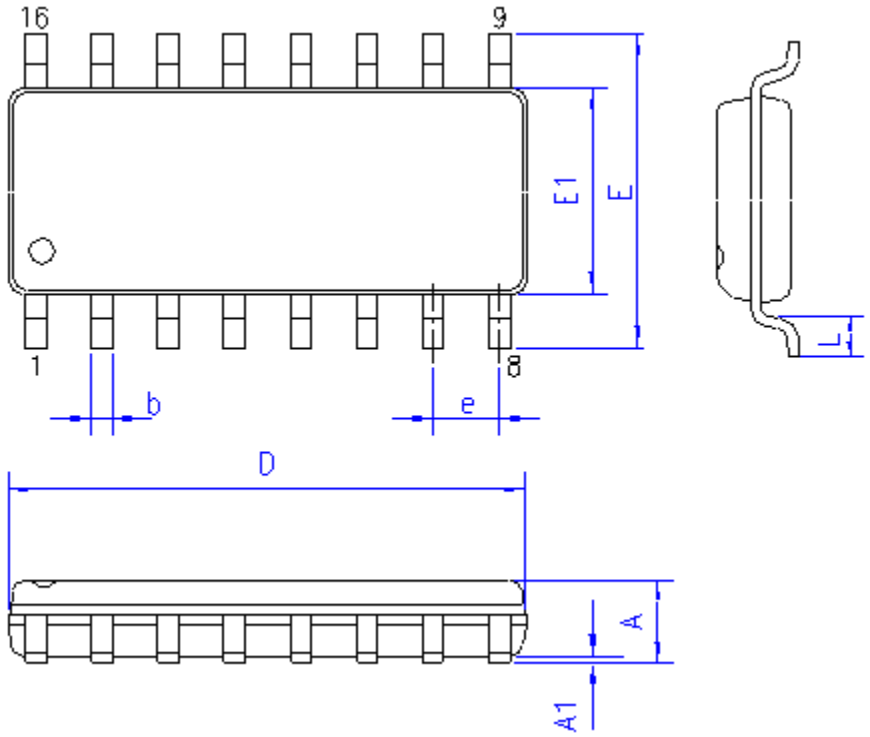


Figure 19. Ferrite Bead output filter

Packaging Information

SOP-16



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.31	0.51	0.012	0.020
D	9.90		0.389	
E1	3.90		0.153	
E	5.79	6.20	0.228	0.244
e	1.27		0.050	
L	0.38	1.27	0.015	0.050