10-W Inductor Free Stereo Audio Amplifier with Low EMI

DESCRIPTION

The EUA2380 is a high efficiency 2 channel bridged-tied load (BTL) Class-D audio power amplifier, driving stereo speakers at up to 10W/CH with 6Ω or 8Ω Load. The EUA2380 features a differential input architecture offering improved noise immunity over a single-ended (SE) input amplifier.

Advanced EMI Suppression Technology with Spread Spectrum Control enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements for system cost reduction.

EUA2380 is not only fully protected against shorts and overload, an adjustable power limiter and a DC detection circuit for protection of the connected speakers. The DC detect and Pin-to-Pin, Pin-to-Ground and Pin-to-Power Short Circuit protection circuit protect the speakers from output DC and pin shorts caused in production. The short circuit protection and thermal protection includes an auto recovery feature.

EUA2380 is available in thermally efficient 28-pin TSSOP package and will be able to output full power on a 2-layer PCB.

FEATURES

- Wide Supply Voltage: 4.5V to 14.5V
- Enhanced Modulation Scheme Reduces EMI Emission
- 10-W/ch into an 6-Ω Load From a 12-V Supply
- 10-W/ch into an 8-Ω Load From a 13-V Supply
- Differential Inputs or Single-Ended input
- Speaker Protection Circuitry
- 26-dB Fixed Gain
- Power Limit Function
- Thermal and Short-Circuit Protection
- 28-pin TSSOP Package with Thermal Pad
- RoHS compliant and 100% lead(Pb)-free Halogen-Free

APPLICATIONS

- Televisions
- USB Speaker
- Mini Speaker
- Consumer Audio Equipment

Typical Application Circuit

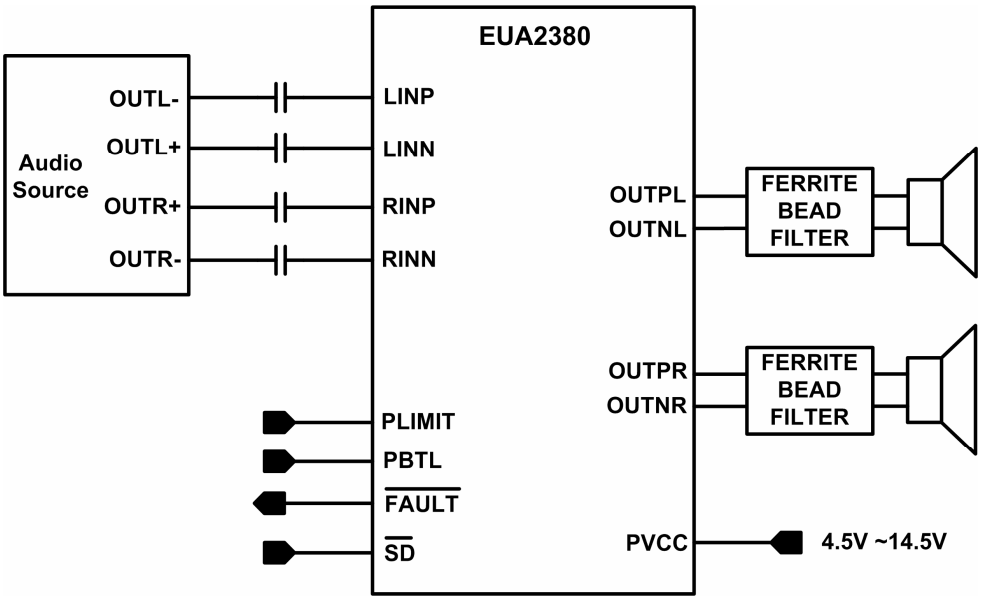
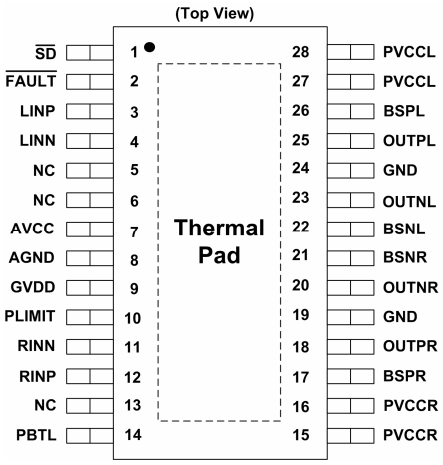


Figure1. Simplified Application Schematic

Pin Configurations

Package Type	Pin Configurations
TSSOP-28 (EP)	

Pin Description

PIN	TSSOP-28(EP)	I/O/P	DESCRIPTION
$\overline{SD}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z，HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
LINP	3	I	Positive audio input for left channel. Biased at 2V.
LINN	4	I	Negative audio input for left channel. Biased at 2V.
NC	5,6,13	I	No connect pin. Can be shorted to PVCC or shorted to GND or left open.
AVCC	7	P	Analog supply
GND	8	P	Analog signal ground. Connect to the thermal pad.
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 4.5V. Also should be used as supply for PLIMIT function.
PLIMIT	10	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
RINN	11	I	Negative audio input for right channel. Biased at 2V.
RINP	12	I	Positive audio input for right channel. Biased at 2V.
PBTL	14	I	Parallel BTL mode select pin.
PVCCR	15,16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
GND	19,24	P	Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.

Pin Description (Continued)

PIN	TSSOP-28(EP)	I/O	DESCRIPTION
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	O	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	27,28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUA2380XIR1	TSSOP-28 (EP)	xxxxx EUA2380	2500	-40 °C to +85°C

EUA2380 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  X:TSSOP (EP)

Absolute Maximum Ratings

- Supply Voltage, AVCC to GND, PVCC to GND ---------- -0.3 V to 16V
- Input Voltage, $\overline{SD}$, $\overline{FAULT}$,PBTL ---------- -0.3 V to AVCC +0.3V
- Input Voltage, PLIMIT ---------- -0.3 V to GVDD +0.3V
- Input Voltage, RINN,RINP,LINN,LINP ---------- -0.3 V to 6.3V
- Thermal Resistance θ_{JA} (TSSOP-28) ---------- 34°C /W
- Free-air Temperature Range, T_A ---------- -40°C to +85°C
- Junction Temperature Range, T_J ---------- -40°C to +150°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to +150°C
- Lead Temperature ---------- 260°C
- Load Resistance, R_{LOAD} (BTL, PVCC>12V)---------- 4.8Ω
- Load Resistance, R_{LOAD} (BTL, PVCC≤12V)---------- 3.2Ω
- Load Resistance, R_{LOAD} (PBTL, PVCC>12V) ---------- 2.5Ω
- Load Resistance, R_{LOAD} (PBTL, PVCC≤12V)---------- 2Ω
- ESD Susceptibility (HBM) ---------- 2kV

Recommended Operating Conditions

		Min.	Max.	Unit
Supply voltage, V_{CC}	PVCC,AVCC	4.5	14.5	V
High-level input voltage, V_{IH}	$\overline{SD}$,PBTL	2		V
Low-level input voltage, V_{IL}	$\overline{SD}$,PBTL		0.8	V
High-level input current, I_{IH}	$\overline{SD}$,PBTL,V_I=2V,V_{CC}=12V		50	μA
Low-level input current, I_{IL}	$\overline{SD}$,PBTL,V_I=0.8V,V_{CC}=12V		5	μA
Low-level output voltage, V_{OL}	$\overline{FAULT}$, $R_{PULL-UP}$=100k, V_{CC}=12V		0.8	V
Oscillator frequency, f_{OSC}		280	360	kHz
Operating free-air temperature, T_A		-40	85	°C

DC Characteristics T_A = +25°C ,V_{CC}=12V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2380			Unit
				Min.	Typ.	Max.	
$\lvert V_{OS}\rvert$	Class-D output offset voltage (measured differentially)	V_I= 0V			5	50	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ =2V, no load, PV_{CC}=12V			22	40	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ =0.8V, no load, PV_{CC}=12V			110	500	μA
r_{DS}(on)	Drain-source on-state resistance	V_{CC}=12V, I_O=100mA, T_J=25°C	High side		240		mΩ
			Low side		240		
G	Gain			25	26	27	dB
t_{ON}	Turn-on time	$\overline{SD}$ =2V			112		ms
t_{OFF}	Turn-off time	$\overline{SD}$ =0.8V			28		ms
GVDD	Gate Drive Supply	I_{GVDD}=100μA		4.2	4.5	4.8	V
t_{DCDET}	DC Detect time	$V_{(INN)}$=5V, $V_{(INP)}$=0V			420		ms

DC Characteristics T_A = +25°C ,V_{CC}=14.5V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2380			Unit
				Min.	Typ.	Max.	
$\|V_{OS}\|$	Class-D output offset voltage (measured differentially)	V_I= 0V			5	50	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ =2V, no load, PV_{CC}=14.5V			23	40	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ =0.8V, no load, PV_{CC}=14.5V			120	500	μA
r_{DS}(on)	Drain-source on-state resistance	V_{CC}=12V, I_O=100mA, T_J=25°C	High side		240		mΩ
			Low side		240		
G	Gain			25	26	27	dB
t_{ON}	Turn-on time	$\overline{SD}$ =2V			112		ms
t_{OFF}	Turn-off time	$\overline{SD}$ =0.8V			28		ms
GVDD	Gate Drive Supply	I_{GVDD}=100μA		4.2	4.5	4.8	V
t_{DCDET}	DC Detect time	$V_{(INN)}$=5V, $V_{(INP)}$=0V			420		ms

AC Characteristics T_A = +25°C ,V_{CC}=12V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2380			Unit
			Min.	Typ.	Max.	
K_{SVR}	Power supply ripple rejection	200mV_{PP} ripple at 1kHz, Inputs ac-coupled to AGND		-60		dB
P_O	Continuous output power	THD+N=10%, f=1kHz, V_{CC}=12V		8.5		W
THD+N	Total harmonic distortion +noise	V_{CC}=12V,f=1kHz, Po=4W(half-power)		0.07		%
Vn	Output integrated noise	20Hz to 22kHz, A-weighted filter		200		μV
				-74		dBV
	Crosstalk	V_I=1Vrms, f=1kHz		-84		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N< 1%, f=1kHz,A-weighted		94		dB
f_{OSC}	Oscillator frequency		280	320	360	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			30		°C

AC Characteristics T_A = +25°C ,V_{CC}=14.5V, R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2380			Unit
			Min.	Typ.	Max.	
K_{SVR}	Power supply ripple rejection	200mV_{PP} ripple at 1kHz, Inputs ac-coupled to AGND		-60		dB
P_O	Continuous output power	THD+N=10%, f=1kHz, V_{CC}=14.5V		12		W
THD+N	Total harmonic distortion +noise	V_{CC}=14.5V,f=1kHz,Po=6W(half-power)		0.07		%
Vn	Output integrated noise	20Hz to 22kHz, A-weighted filter		200		μV
				-74		dBV
	Crosstalk	V_I=1Vrms, f=1kHz		-84		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N< 1%, f=1kHz, A-weighted		94		dB
f_{OSC}	Oscillator frequency		280	320	360	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			30		°C

Block Diagram

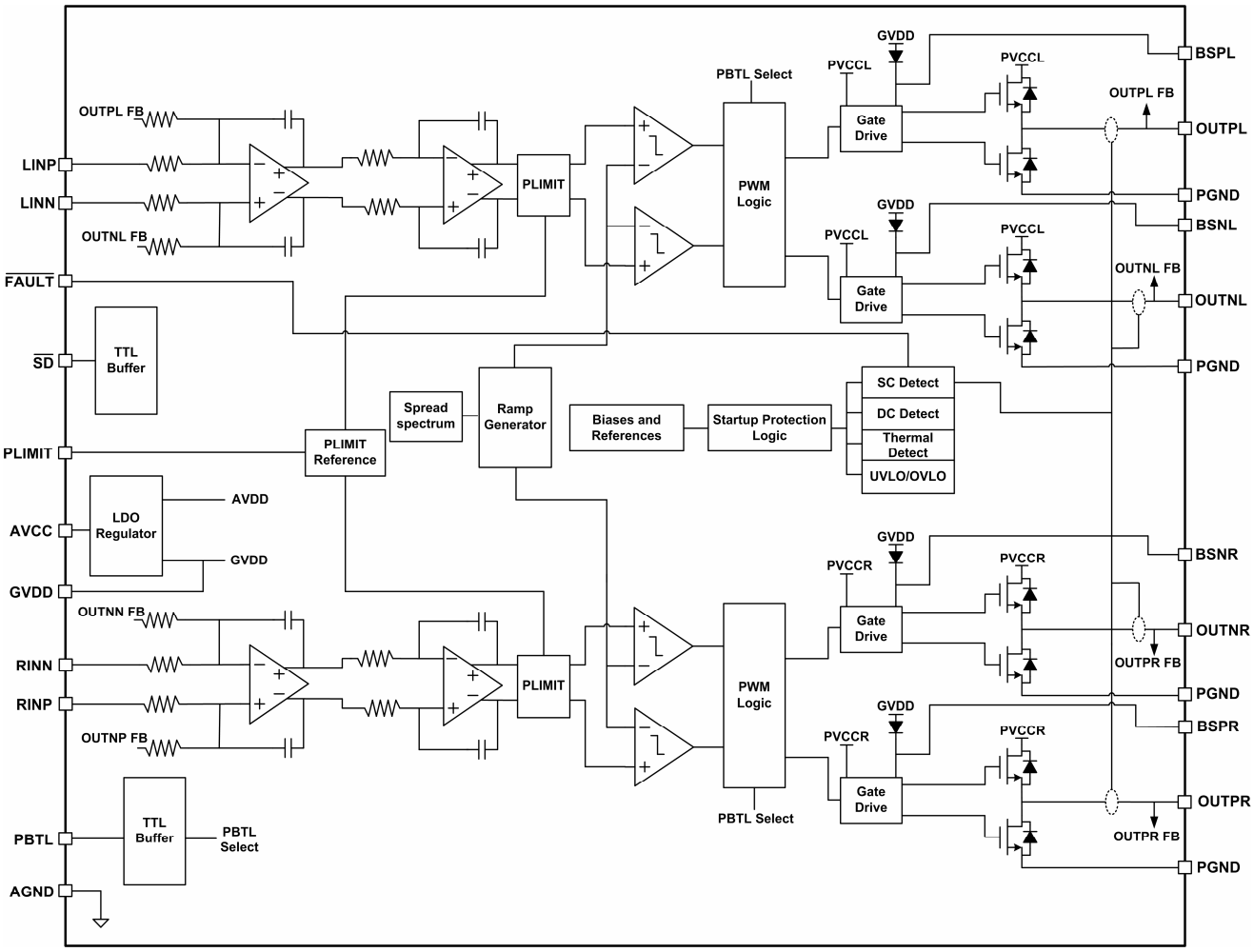


Figure2.

Typical Characteristics

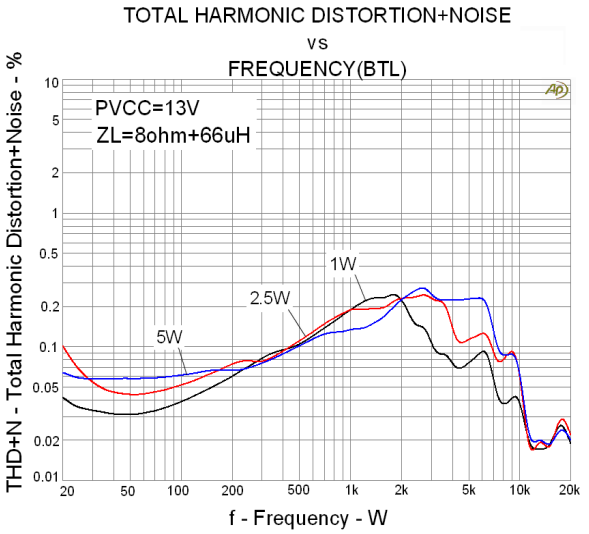


Figure3.

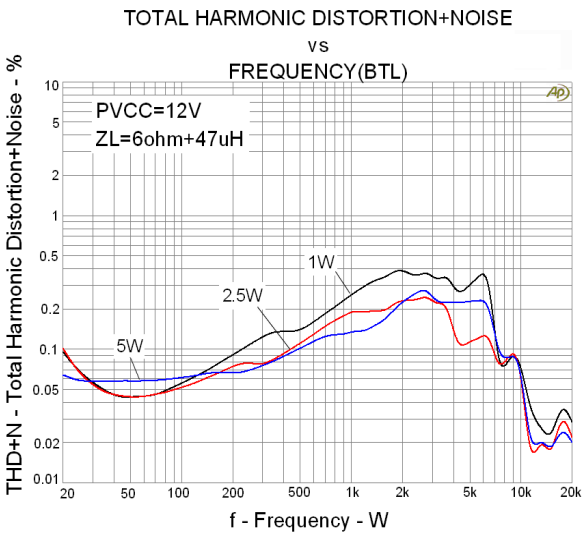


Figure4.

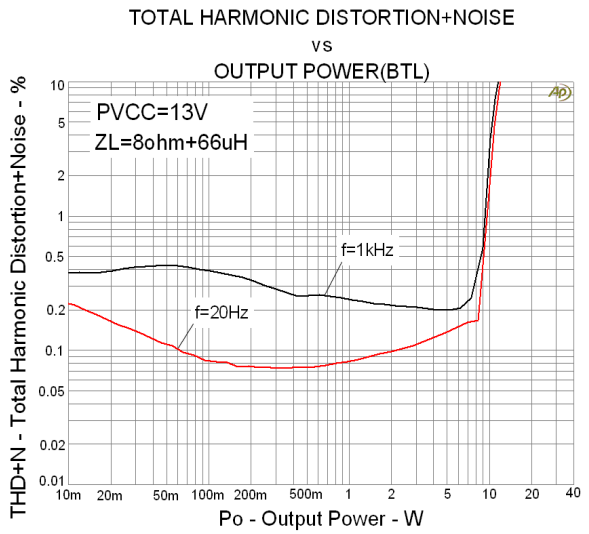


Figure5.

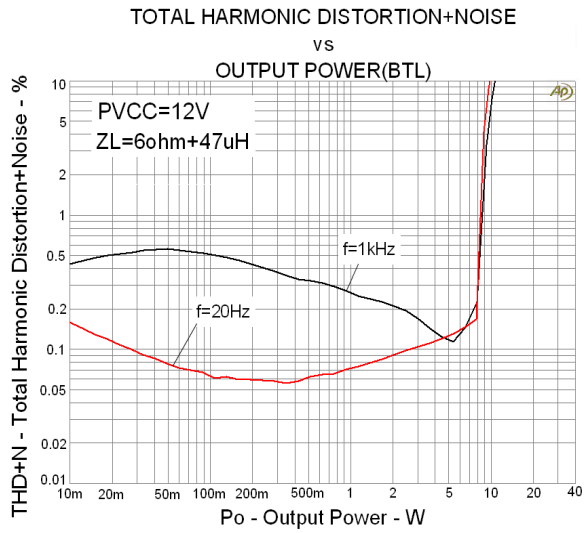


Figure6.

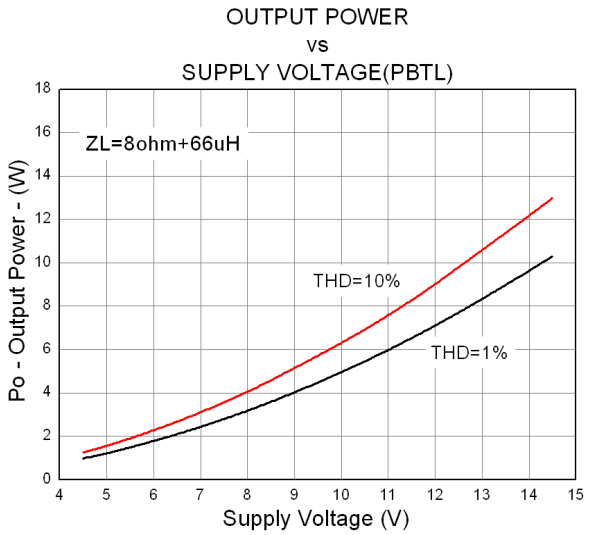


Figure7.

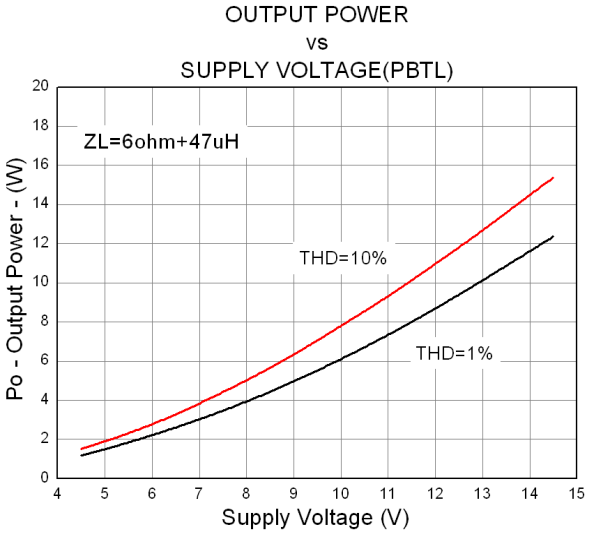


Figure8.

Typical Characteristics (continued)

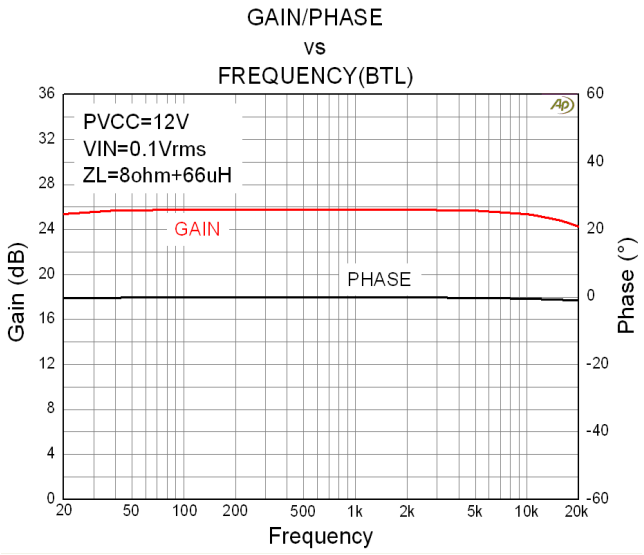


Figure9.

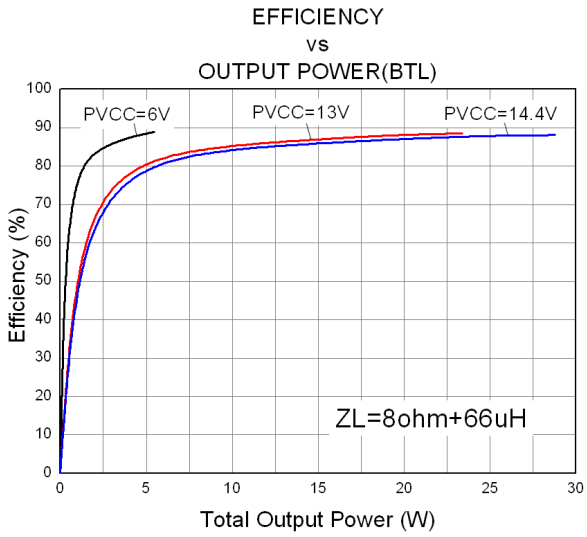


Figure10.

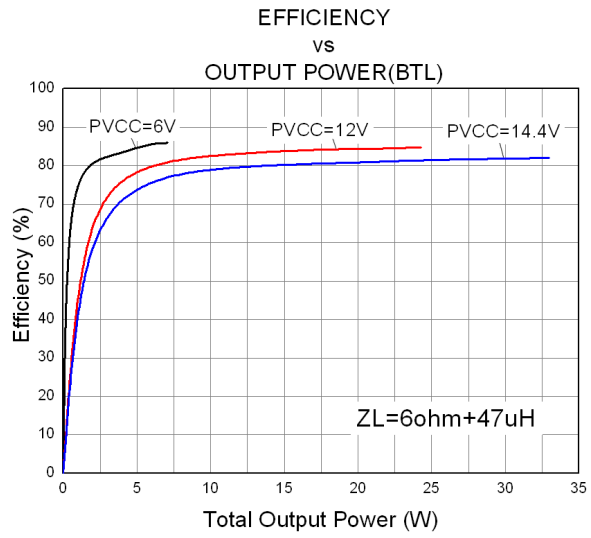


Figure11.

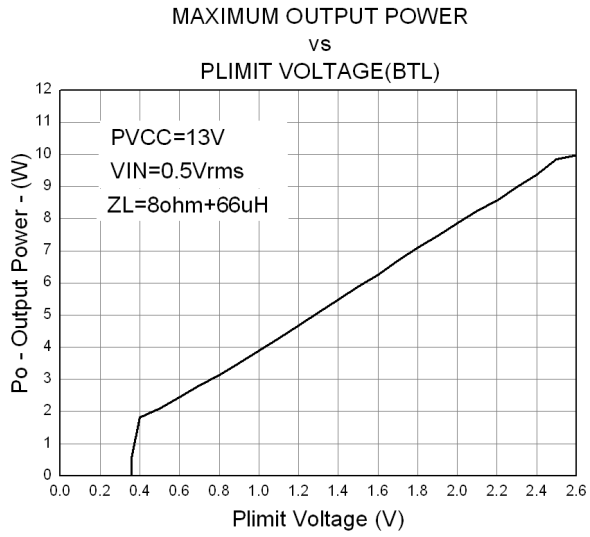


Figure12.

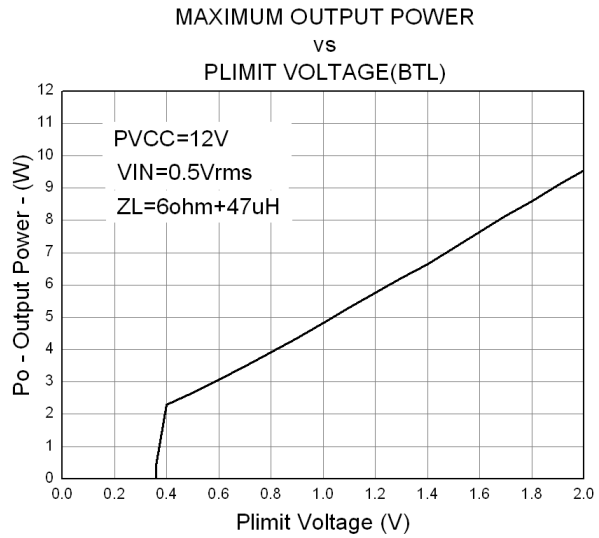


Figure13.

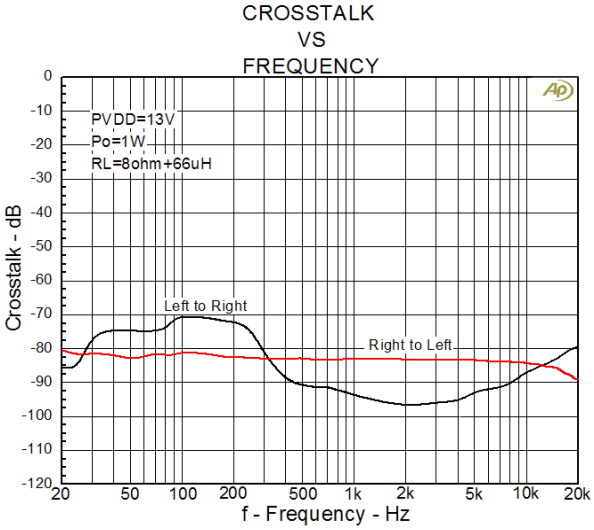
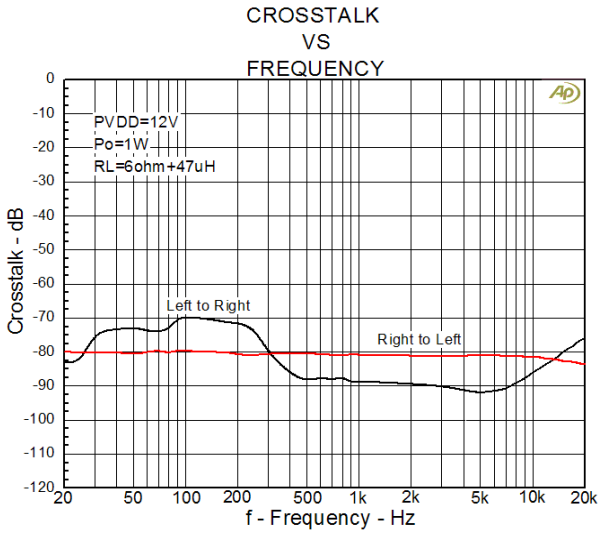


Figure14.

Typical Characteristics (continued)



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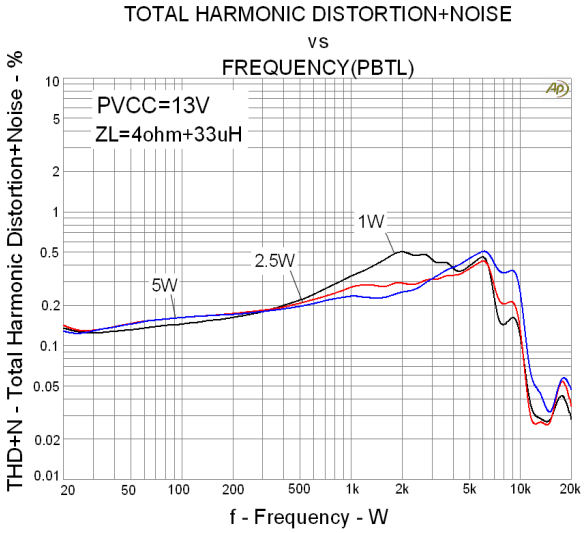

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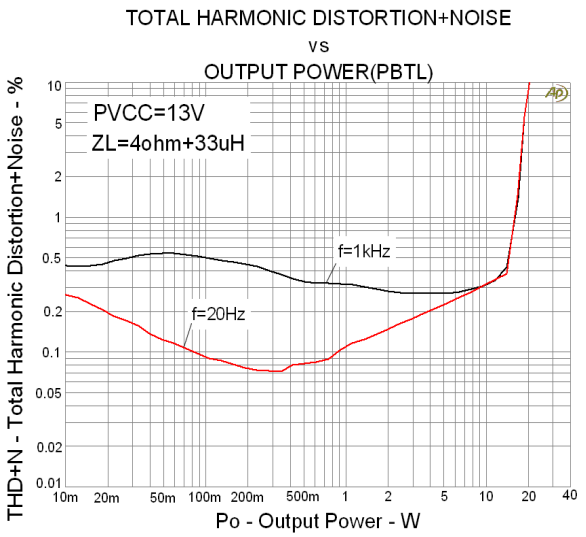


Figure17.

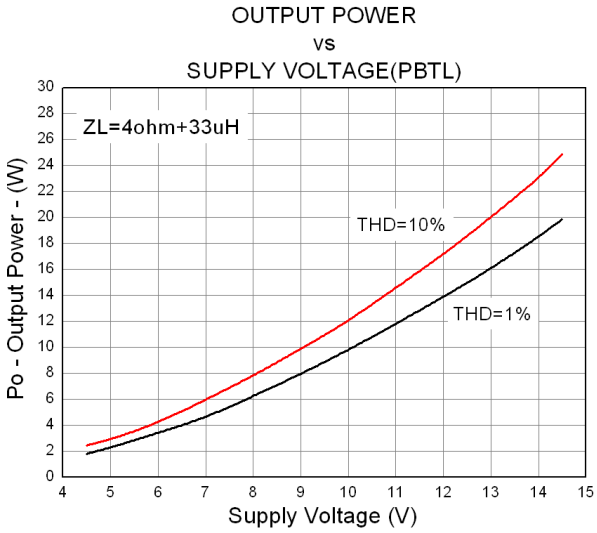


Figure18.

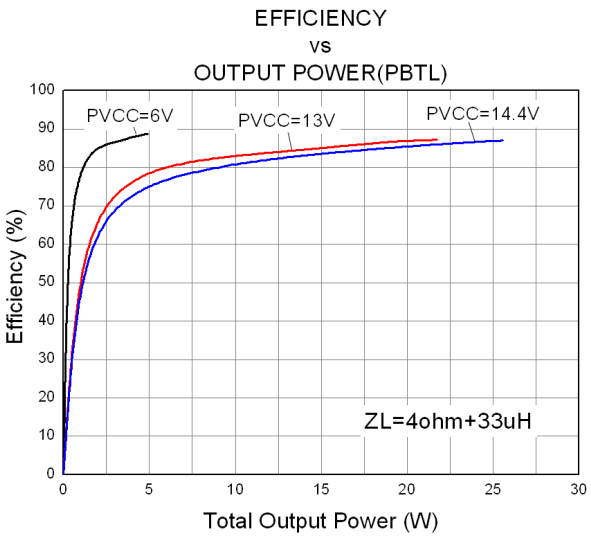


Figure19.

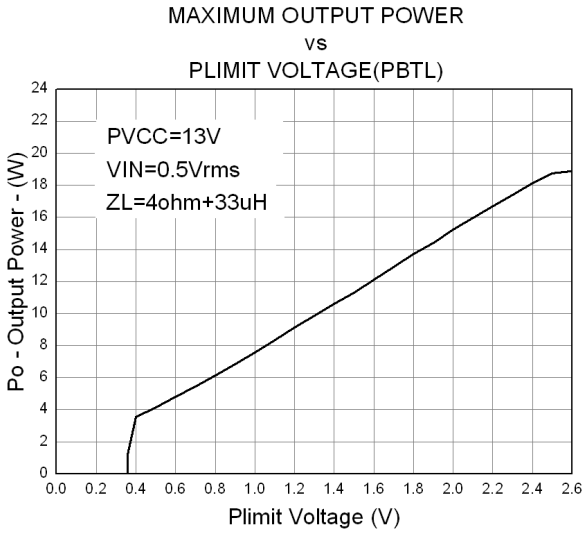


Figure20.

Detailed Description

Overview

To facilitate system design, the EUA2380 needs only a single power supply between 4.5V and 14.5V for operation. An internal voltage regulator provides suitable voltage levels for the gate driver, digital and low-voltage analog circuitry. Additionally, the built-in bootstrap circuitry with a few external bootstrap capacitors provides the floating voltage required by the high-side gate driver.

In order to provide high performance, the PWM signal path for the output stage is designed as independent half bridges. Accordingly, each half bridge has separated bootstrap pins (BSXX). Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. Inductance between the power-supply pins and decoupling capacitors must be avoided.

The Four half bridge output stages use only NMOS transistors, the properly functioning bootstrap circuit is required. For the high side NMOS of each half bridge operation correctly, a bootstrap capacitor must be connected from each bootstrap pin (BSXX) to the corresponding output pin(OUTXX) function as a floating power supply for the high side NMOS gate drive circuitry. When the power stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate drive regulator output pin and the bootstrap pin. During each high side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high side MOSFETS turned on.

Special attention should be paid to the power-stage power supply: this includes component selection, PCB placement, and routing. For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVCC pin is decoupled with ceramic capacitors placed as close as possible to each supply pin. The PVCC power supply should have low output impedance and low noise. The power-supply ramp and SD release sequence is not critical for device reliability as facilitated by the internal power-on-reset circuit, but it is recommended to release SD after the power supply is settled for minimum turn on audible artifacts.

Feature Description

Gain

The EUA2380 has a fixed gain 26dB.

$\overline{SD}$ Operation

Connect $\overline{SD}$ to a logic high for normal operation. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier enter a low current state. Never leave $\overline{SD}$ unconnected because amplifier operation would be unpredictable. For the best power off pop performance, place the amplifier in the shutdown prior to removing the power supply voltage. The $\overline{SD}$ input pin should be held high (see specification table for trip point) during normal operation when the amplifier is in use.

PLIMIT

The voltage at pin 10 can be used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to Ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1uF capacitor from pin 10 to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a " virtual " rail is 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2R_S}\right) \times 2V_P\right)^2}{2 \times R_L} \quad \text{----------} \ (1)$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output, V_{INP} is the input peak amplitude.

$V_P = 4 \times V_{PLIMIT}$ voltage if $V_{PLIMIT} < 4 \times V_P$

Table.1 PLIMIT Typical Operation

Test Conditions	Plimit Voltage	Output Power (W)	Output Voltage Amplitude(V_{P-P})
PVCC=13V, Vin=0.6Vrms, R_L=8	0.7	3	13.9
PVCC=13V, Vin=0.6Vrms, R_L=8	1.2	5	17.9
PVCC=13V, Vin=0.6Vrms, R_L=8	1.43	6	19.7
PVCC=13V, Vin=0.6Vrms, R_L=8	1.87	8	22.6
PVCC=12V, Vin=0.6Vrms, R_L=8	0.7	3	13.9
PVCC=12V, Vin=0.6Vrms, R_L=8	1.2	5	17.9
PVCC=12V, Vin=0.6Vrms, R_L=8	1.42	6	19.6

Spread Spectrum and De-Phase Control

The EUA2380 has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM outputs to improve EMI performance. De-phase inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity.

GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1-μF capacitor to ground at this pin.

DC Detect

The EUA2380 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVCC supply. Cycling SD will NOT clear a DC detect fault.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 20% (for example (+60%,-40%) for more than 420 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2Hz.To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signal at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

PBTL Select

The EUA2380 offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin (pin 14) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs with OUTPL connected to OUTNL and OUTPR connected to OUTNR. Connect the positive and negative output together for best efficiency. For an example of the PBTL connection, see the schematic in the APPLICATION INFORMATION section.

For normal BTL operation, connect the PBTL pin to local ground.

Short-Circuit Protection and Automatic Recovery Feature

The EUA2380 has protection from over current conditions caused by a short circuit on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-VCC shorts. The short circuit protection fault is reported on the FAULT pin as a low state. The amplifier outputs are disabled when the short circuit is detected on the outputs. A latched fault flag is resulted and can be cleared by cycling the SD pin through the low state.

The EUA2380 can automatic recover for normal operation if short was removed. If the short was not removed, the protection circuitry again activates.

Thermal Protection

Thermal protection on the EUA2380 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±10°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. The thermal fault is cleared once the temperature of the die is reduced by 30 °C. The device begins normal operation at this point with no external system interaction.

Application Information

Differential Input

The differential input stage of the amplifier cancels any common-mode noise that appears on both input lines of the audio channel. To use the EUA2380 with a differential source, connect the positive signal of the audio source to the INP pin and negative signal from the audio source to the INN pin (Figure 21).

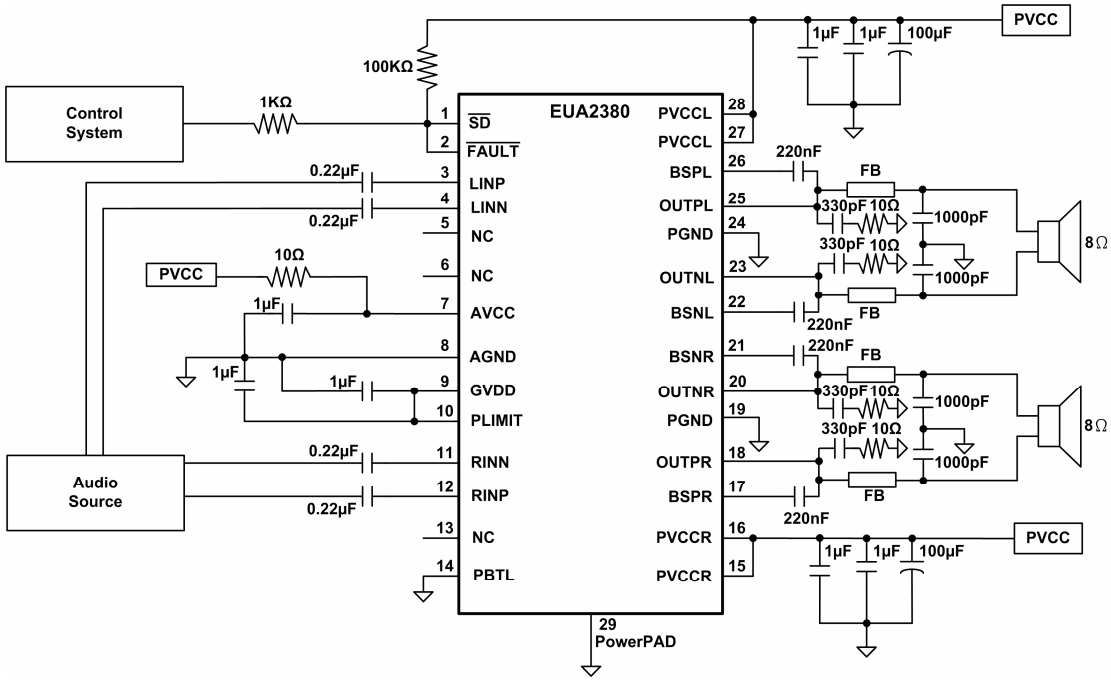


Figure21. Different input

Single-Ended Input

When using an audio source with a single-ended “out”, it is important to connect the RINN and LINN pins to the GND of the audio source with coupling capacitors (Figure22).

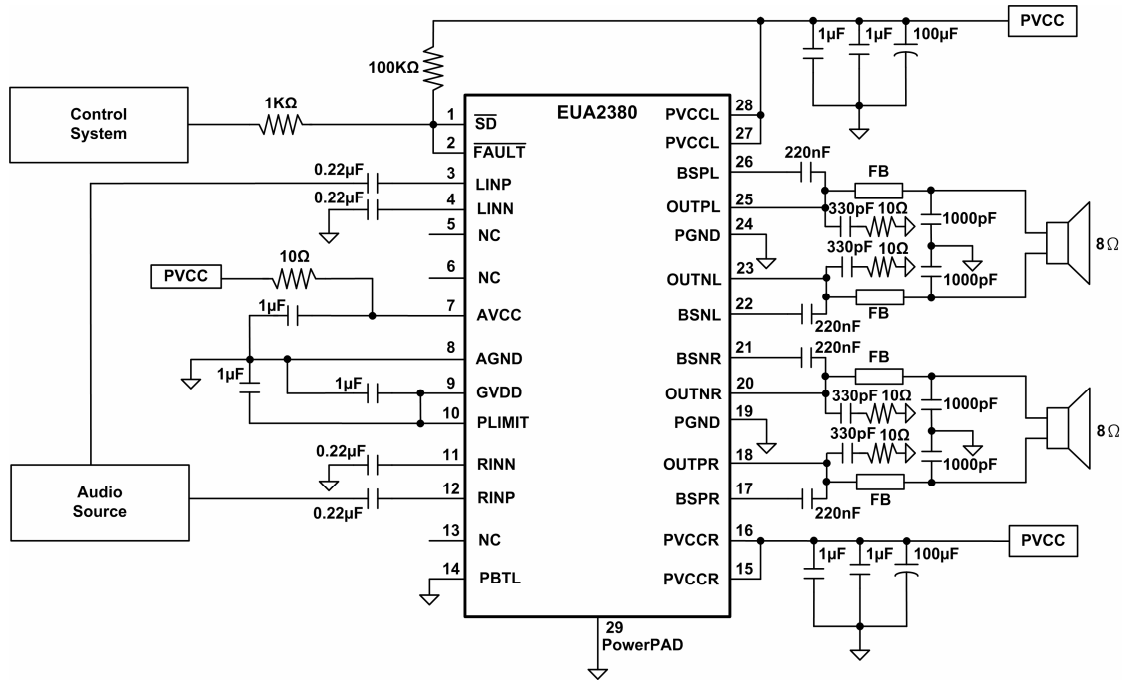


Figure22. Single-Ended Input Different input

Application Information (continued)

PBTL Mode

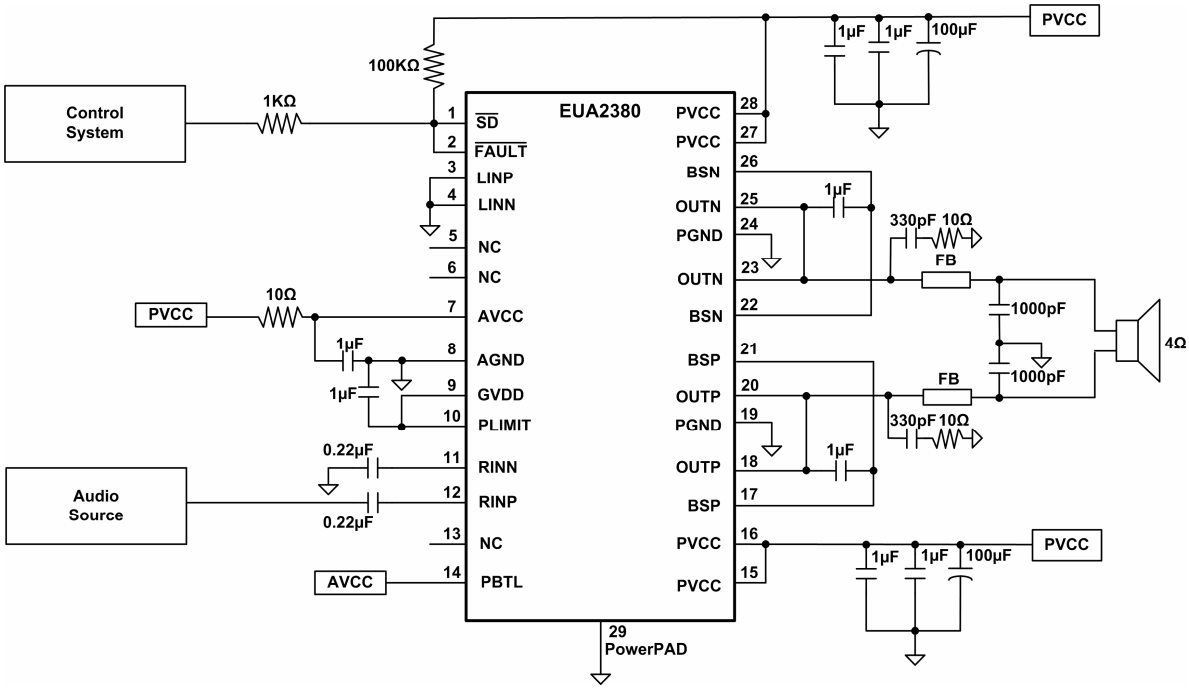
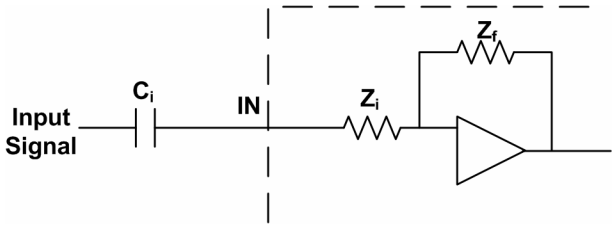


Figure23. PBTL Output

Design Requirements

Input Resistance

The input resistance of amplifier is fixed to 30KΩ ± 20%. If a single capacitor is used in the input high-pass filter, the -3dB or cutoff frequency may change when changing gain steps.

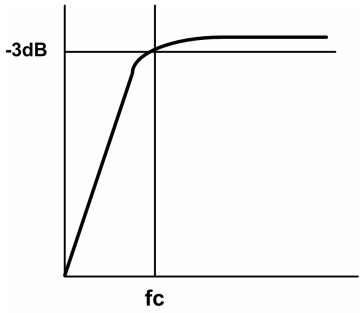


The -3dB frequency can be calculated using Equation 2.

$$f_c = \frac{1}{2\pi Z_I C_I} \quad \text{----------(2)}$$

Input Capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.



$$f_c = \frac{1}{2\pi Z_I C_I} \quad \text{----------(3)}$$

The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 50 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_I = \frac{1}{2\pi Z_I f_I} \quad \text{---------- (4)}$$

In this example, C_I is 0.16μF; so, one would likely choose a value of 0.22μF as this value is commonly used. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I). This leakage current creates a dc offset voltage at the input to the amplifier. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF~1μF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. The bootstrap capacitors connected between the BSXX pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on. Specifically, one capacitor must be connected from OUTPx to BSPx, and one capacitor must be connected from OUTNx to BSNx.

Differential Inputs

When use differential input signal, any noise that appears on both input lines of the channel can be cancelled. To use the EUA2380 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the EUA2380 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

In order to allow the input dc blocking capacitors to become completely charged during power-up time, the impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. If the input capacitors cannot be charged completely, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

Using Low-ESR Capacitors

Use capacitors with an ESR less than 100mΩ for optimum performance. Low ESR ceramic capacitors minimize the output resistance. For best performance over the extended temperature range, select X7R capacitors.

Power Supply Decoupling, CS

The EUA2380 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the

amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF to 1µF placed as close as possible to the device VCC lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 100µF or greater placed near the audio power amplifier is recommended. The 100µF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 100µF or larger capacitor should be placed on each PVCC terminal. A 10µF capacitor on the AVCC terminal is adequate. In practice, with a well designed system power, 100µF, 16V will most applications with 12V power supply, and 25V capacitor rating is recommended for power supply voltage higher than 12V.

Output Filter

With enhanced modulation scheme, EUA2380 make it possible to design using a low-cost ferrite bead filter. Ferrite bead are different effective range due to their material. The ferrite bead used in the filter should be selected carefully. Many specifications limit emissions of the consumer electronic greater than 30MHz, a ferrite bead with good performance in the 10 to 100MHz range is important to block radiation in the 30MHz and above range. For EUA2380 is high power amplifier, it is important that the ferrite bead is large enough to maintain impedance at the peak currents expected. A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Use an LC output filter allowing the switching current to flow through the filter instead of the load will increasing efficiency.

When both an LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.

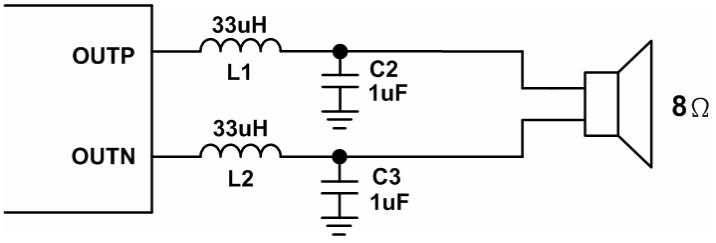


Figure24.

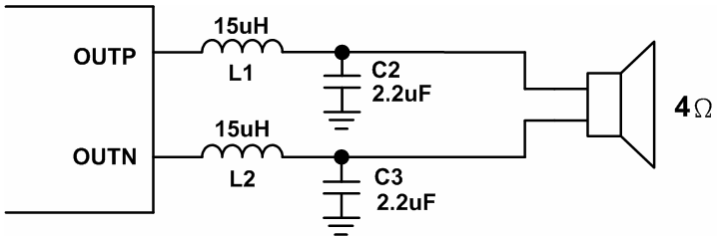


Figure25.

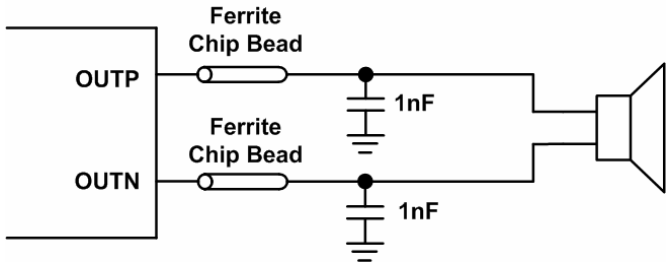
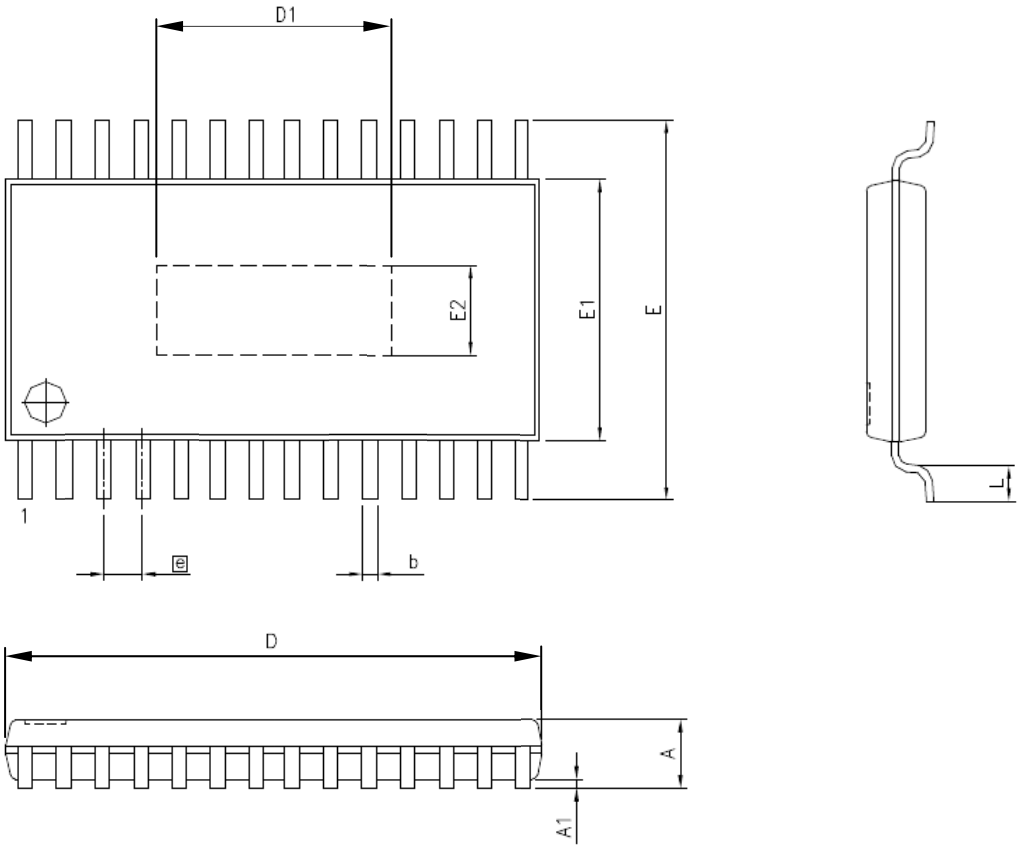


Figure26.

Package Information

TSSOP-28 (EP)



Note: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40 REF		0.173 REF	
D	9.60	9.80	0.378	0.386
D1	2.80	6.30	0.110	0.248
E	6.20	6.60	0.244	0.260
E2	2.10	3.30	0.083	0.130
e	0.65 REF		0.026 REF	
L	0.45	0.75	0.018	0.030