5A, 3MHz Synchronous Step-Down DC-DC with I²C Compatible Interface

DESCRIPTION

The EUP3265 is a high-frequency, high-current synchronous step-down dc-dc converter optimized to supply the different sub systems of smart-phones, Tablets, and portable applications powered by one cell Li−Ion or three cell Alkaline/NiCd/NiMH batteries. The device is able to deliver up to 5A, with programmable output voltage from 0.6 V to 1.4V.

The EUP3265 operates at 3-MHz fixed switching frequency which allows the use of small low cost inductors and capacitors. During light load conditions, the regulator includes a PFM mode to enhance light-load efficiency. The regulator transitions smoothly between PWM and PFM modes. Synchronous rectification and automatic PWM/PFM transitions improve overall efficiency.

The serial interface is compatible with Fast/Standard and High-Speed mode I²C specification allowing transfers at up to 3.4 Mbps. This communication interface is used for dynamic voltage scaling with voltage steps down to 6.25 mV, for reprogramming the mode of operation (PFM or Forced PWM) or disable/enabling the output voltage.

FEATURES

- 2.7V to 5.5V Input Voltage Range
- 3MHz Constant Switching Frequency
- 5A Available Load Current
- I²C Control Interface with Dynamic Voltage Scaling Support
- Programmable Output Voltage: 0.6V to 1.4V in 6.25mV Steps
- Small size, 0.33µH or 0.47µH Inductor Solution
- 52µA Typical Quiescent Current
- PFM/PWM Operation for Optimum Increased Efficiency
- Excellent Load and Line Transient Response
- Short Circuit and Thermal Protection
- Available in 2.0mm×1.6mm WCSP-20 Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- Smart Phones
- Tablets
- Low-Voltage DSPs and Processors Core Power Supplies

Typical Application Circuit

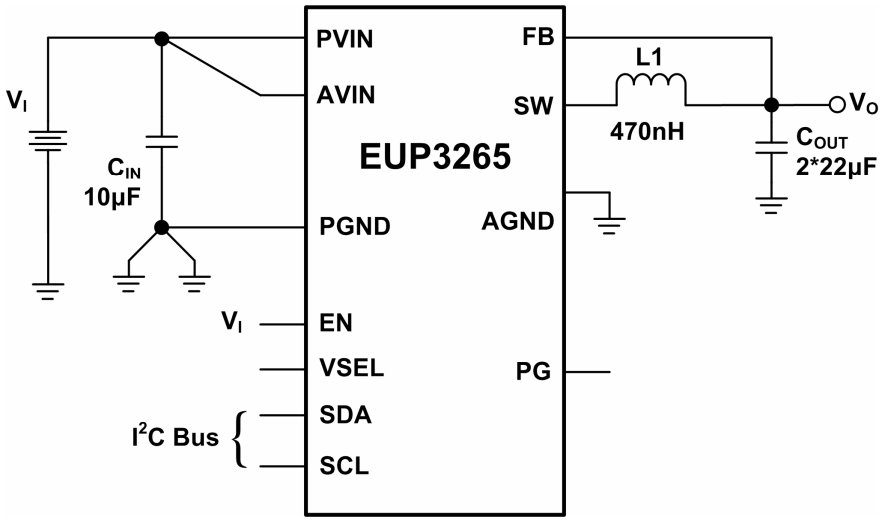


Figure 1.

Typical Application Circuit (Continued)

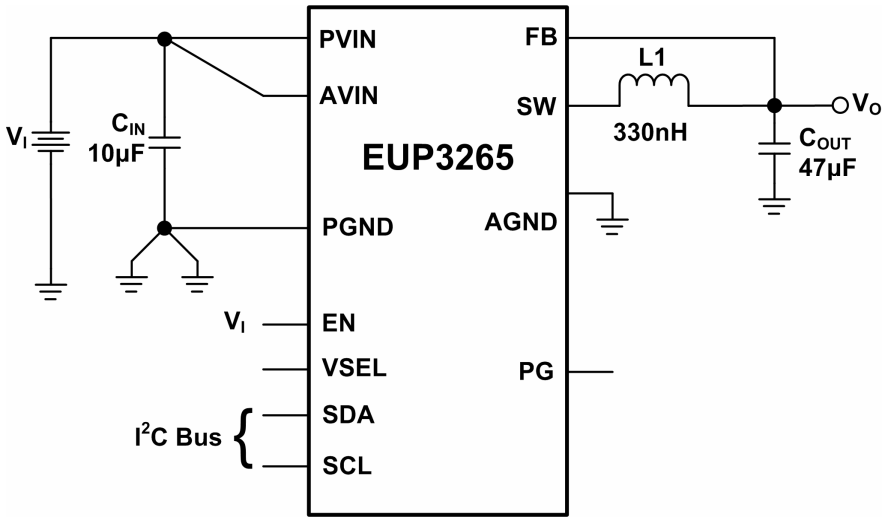


Figure 2.

Block Diagram

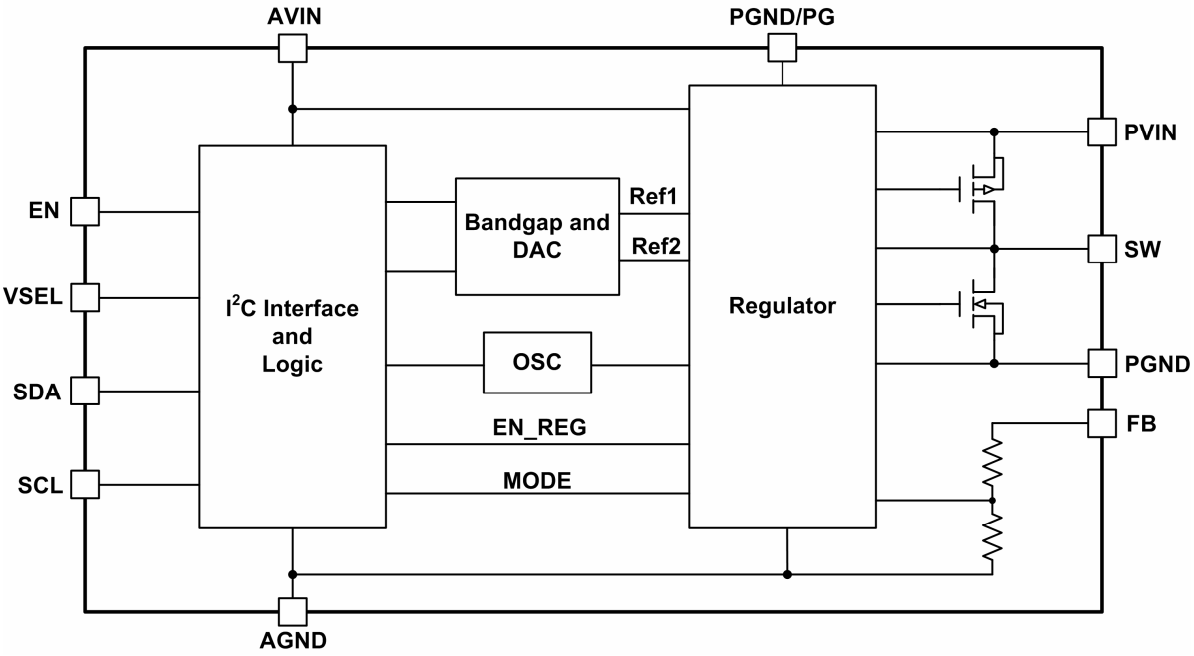
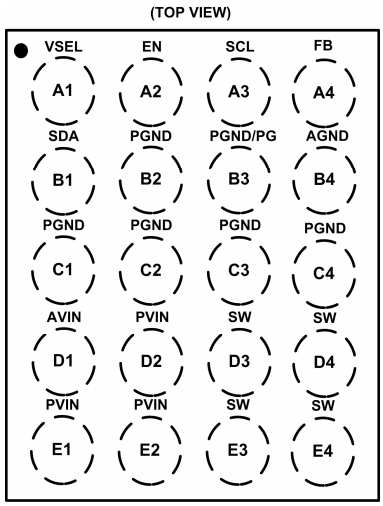


Figure 3.

Pin Configurations

Package Type	Pin Configurations
WCSP-20	

Pin Description

Name	WCSP-20	DESCRIPTION
PVIN	D2,E1,E2	Power Input Voltage. Connect to input power source. The connection from this pin to C_{IN} should be as short as possible.
AVIN	D1	Analog Input Voltage. Connect to input power source as close as possible to the input bypass capacitor.
SW	D3,D4,E3,E4	Switching Node. Connect to the inductor.
PGND	B2,C1,C2, C3,C4	Power GND. Connect to the (-) terminal of output capacitor and (-) terminal of input capacitor.
AGND	B4	Analog GND. This is the signal ground reference for the IC.
SDA	B1	SDA. I^2C interface serial data. There is an internal pull down resistor on this pin; could be left open if not used.
SCL	A3	SCL. I^2C interface serial clock. There is an internal pull down resistor on this pin; could be left open if not used.
VSEL	A1	Output voltage and mode selection. This pin determines which of the two programmable configurations to utilize. This behavior can be overridden through I^2C register settings. There is an internal pull down resistor on this pin; could be left open if not used.
EN	A2	Enable. When HIGH, the circuit is enabled. There is an internal pull down resistor on this pin.
FB	A4	Feedback Voltage Input. Tie this pin to the output voltage.
PGND/PG	B3	Power Good open drain output. If not used has to be connected to ground.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP3265HIR1	WCSP-20	xxx Y00	-40°C to +85°C

EUP3265 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  H: WCSP

Absolute Maximum Ratings (1)

- Input Supply Voltage(AVIN,PVIN) ---------- -0.3V to 6V
- SW Voltage ---------- -0.3V to VIN+0.3V
- SDA, SCL, VSEL, EN, FB Voltages ---------- -0.3V to 6V
- Package Thermal Resistance
  WCSP-20,θ_{JA} ---------- 65°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- -65°C to 150°C
- ESD Susceptibility (HBM) ---------- 2kV

Recommended Operating Conditions (2)

- Supply Voltage ---------- 2.7V to 5.5V
- Operating Temperature ---------- -40°C to +85°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

(The ● denote the Spec. apply over the full operating temperature range, otherwise Spec. are T_A =+25°C. V_{IN} =3.6V unless otherwise specified.)

Symbol	Parameter	Conditions		EUP3265			Unit
				Min.	Typ.	Max.	
V_{IN}	Input Voltage Range	-40°C≤T_A≤+85°C	●	2.7		5.5	V
UVLO	Input Undervoltage Lockout	Rising			2.2		V
ΔV_{OUT}	Output Voltage Load Regulation	I_O= 0 to 5A, V_{OUT}=1.15V, PWM Mode			0.1		%/A
	Output Voltage Line Regulation	I_O= 0A, V_{IN}=2.7V to 5.5V, V_{OUT}=1.15V, PWM Mode			0.1		%/V
V_{IH}	High-Level Input Voltage	EN,VSEL,SCL,SDA		1.2			V
V_{IL}	Low-Level Input Voltage					0.4	V
I_Q	Quiescent Current	I_O=0mA, PFM mode, no switching			52		µA
		I_O=0mA, PWM mode, switching			14		mA
I_{SHDN}	OFF Mode Current	EN,VSEL,SLEEP_mode bit low	●		0.3	5	µA
I_{SLEEP}	SLEEP Mode Current	EN high, DC-DC off (or EN low, VSEL low, SLEEP_mode bit high)			17		µA
I_{PEAK}	Peak Inductor Current				8		A
f_{OSC}	Oscillator Frequency			2.65	3	3.35	MHz
I_{LSW}	SW Leakage Current	EN=0V, SW=0V				5	µA
		EN=0V, SW=3.6V				5	µA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW}=500mA, VIN=5V			31		mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW}=500mA, VIN=5V			17		mΩ
T_{SD}	Thermal Shutdown				150		°C
T_{SD}-Hys	Thermal Shutdown Hysteresis				20		°C

I²C Timing Specifications

Symbol	Parameter	Conditions	EUP3265			Unit
			Min.	Typ.	Max.	
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
		High-Speed Mode, $C_B \leqq 100pF$			3.4	MHz
		High-Speed Mode, $C_B \leqq 400pF$			1.7	MHz
t_{BUF}	Bus-Free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
$t_{HD;STA}$	START or Repeated-START Hold Time	Standard Mode		4		µs
		Fast Mode		100		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		ns
		High-Speed Mode, $C_B \leqq 100pF$		160		ns
		High-Speed Mode, $C_B \leqq 400pF$		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \leqq 100pF$		60		ns
		High-Speed Mode, $C_B \leqq 400pF$		120		ns
$t_{SU;STA}$	Repeat-START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		ns
		High-Speed Mode		10		ns
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \leqq 100pF$	0		70	ns
		High-Speed Mode, $C_B \leqq 400pF$	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \leqq 100pF$		10	80	ns
		High-Speed Mode, $C_B \leqq 400pF$		20	160	ns
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \leqq 100pF$		10	40	ns
		High-Speed Mode, $C_B \leqq 400pF$		20	80	ns
t_{RCL1}	Rise Time of SCL After a Repeated START Condition and After ACK Bit	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \leqq 100pF$		10	80	ns
		High-Speed Mode, $C_B \leqq 400pF$		20	160	ns
t_{RDA}	SDA Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \leqq 100pF$		10	80	ns
		High-Speed Mode, $C_B \leqq 400pF$		20	160	ns

I²C Timing Specifications (continued)

Symbol	Parameter	Conditions	EUP3265			Unit
			Min.	Typ.	Max.	
t_{FDA}	SDA Fall Time	Standard Mode		20+0.1C_B	300	ns
		Fast Mode		20+0.1C_B	300	ns
		High-Speed Mode, C_B≦100pF		10	80	ns
		High-Speed Mode, C_B≦400pF		20	160	ns
$t_{SU;STO}$	STOP Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

I²C Timing Diagrams

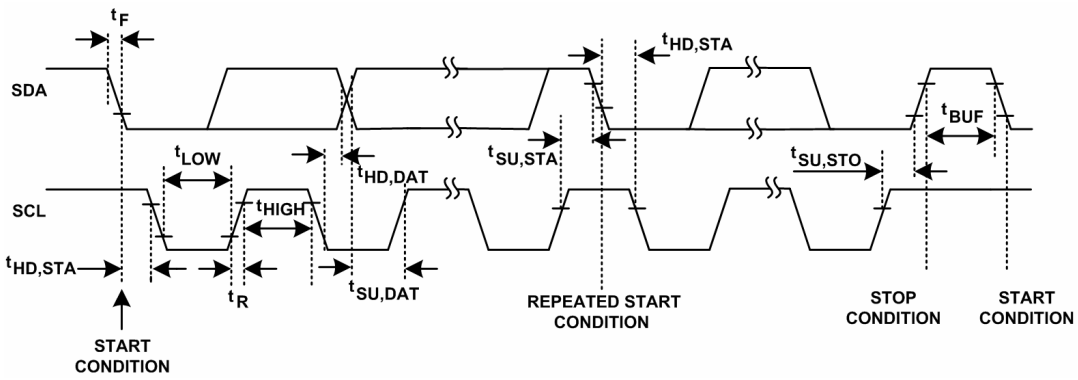
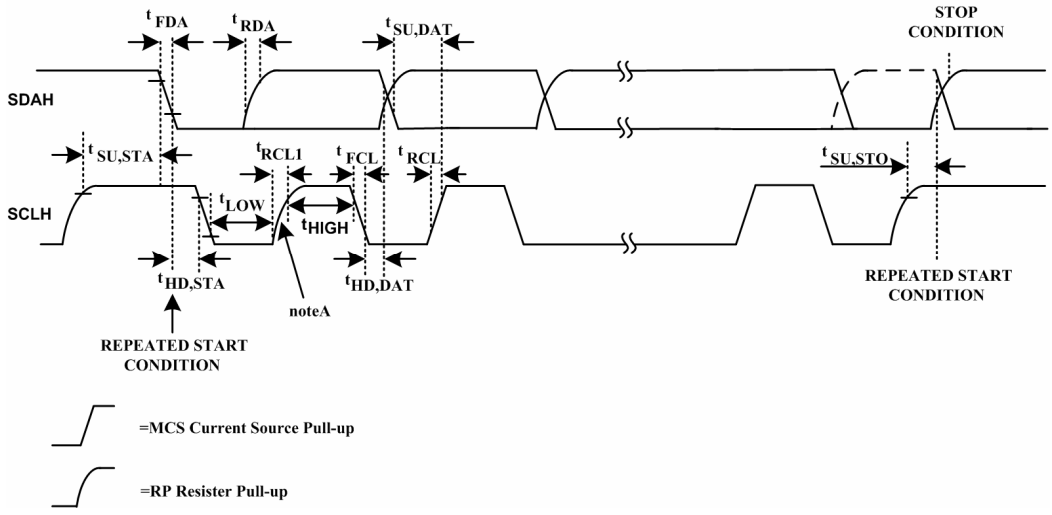


Figure 4. I²C Interface Timing for Fast and Standard (F/S) Modes

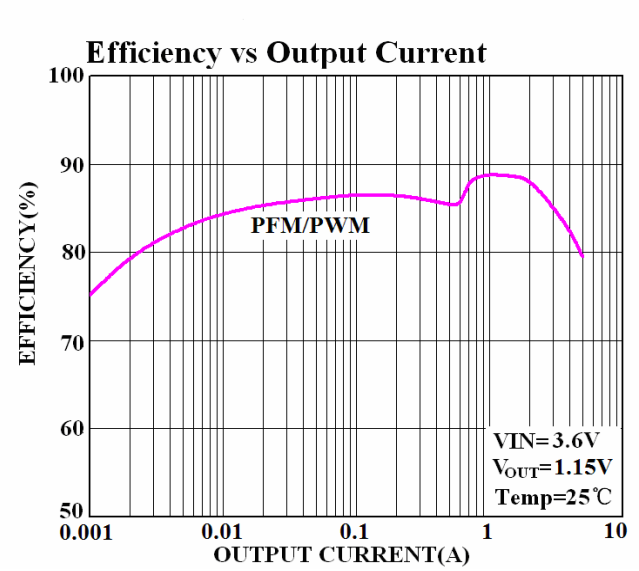


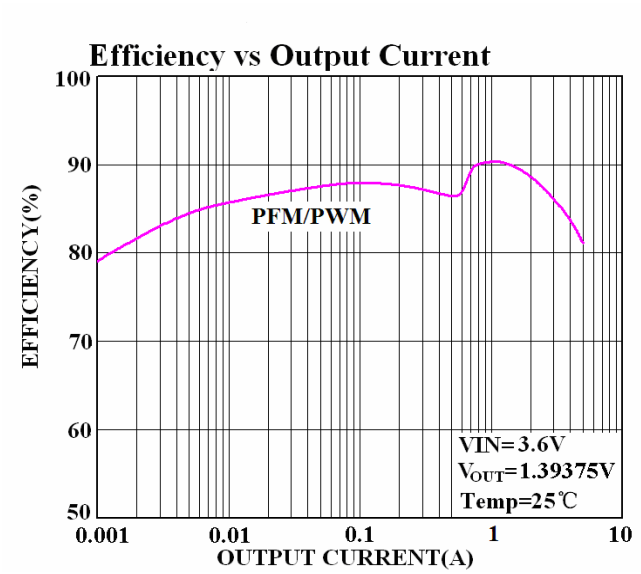
Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

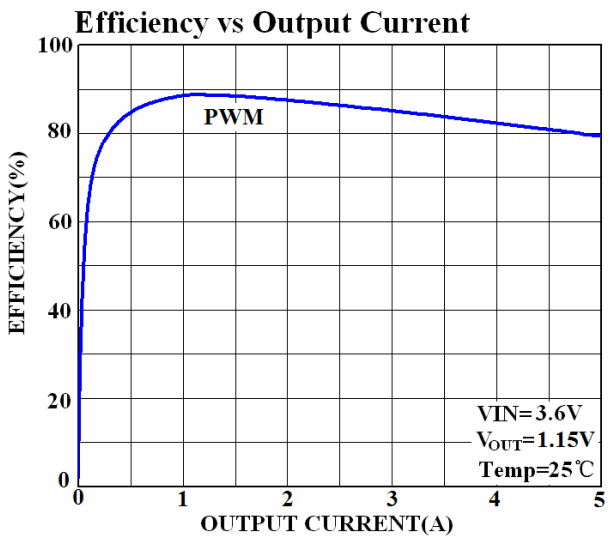
Figure 5. I²C Interface Timing for High Speed (HS) Mode

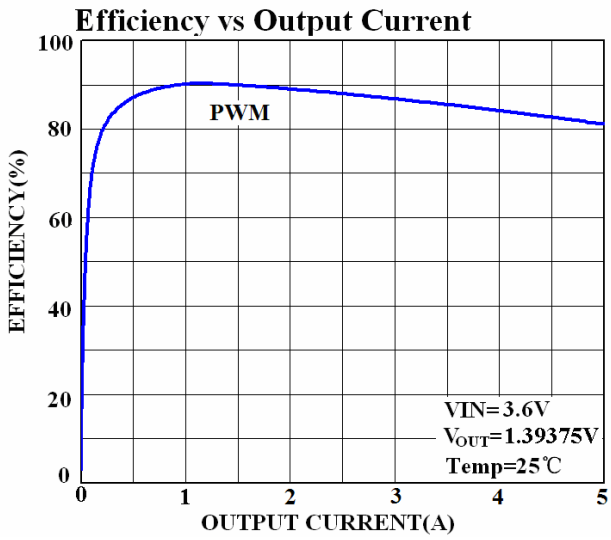
Typical Operating Characteristics

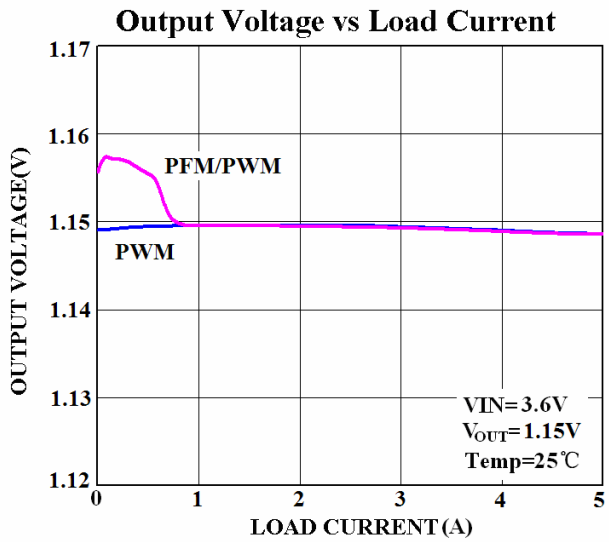
(AVIN=PVIN=3.6V, L=0.47µH, C_{OUT}=2×22µF)

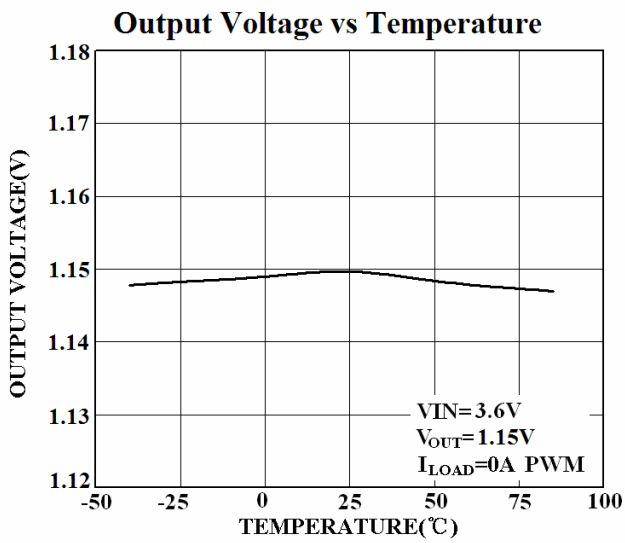






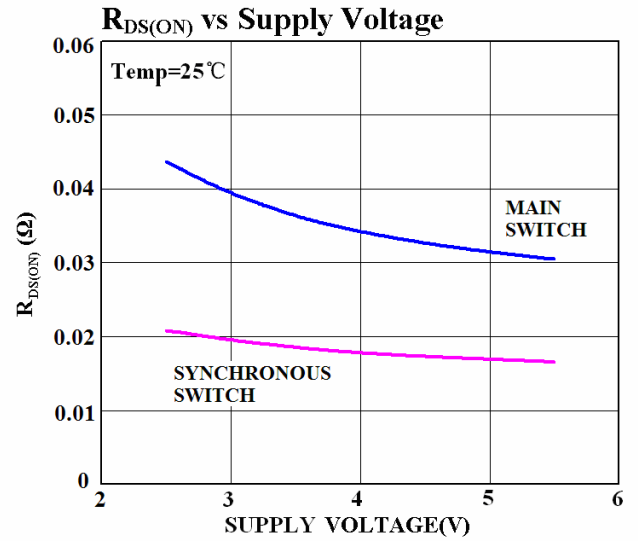


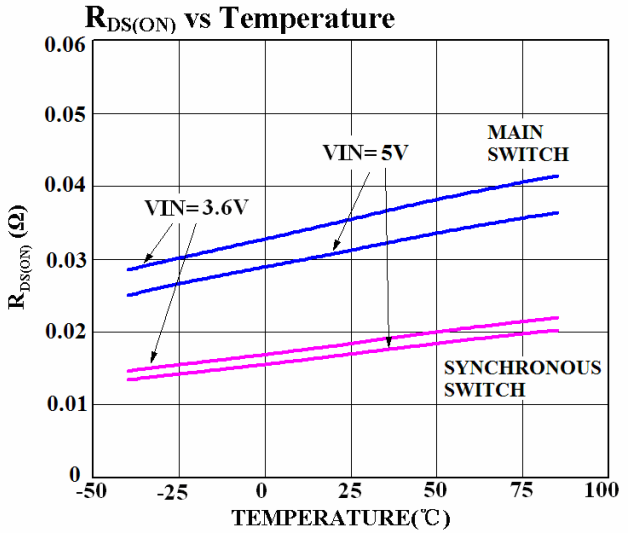


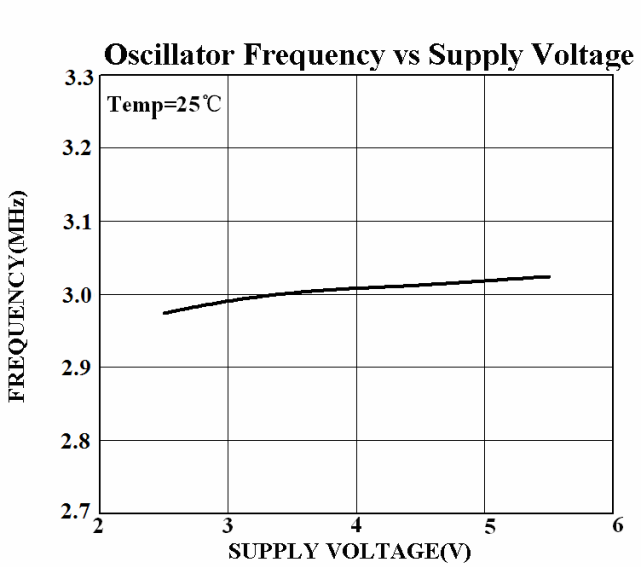


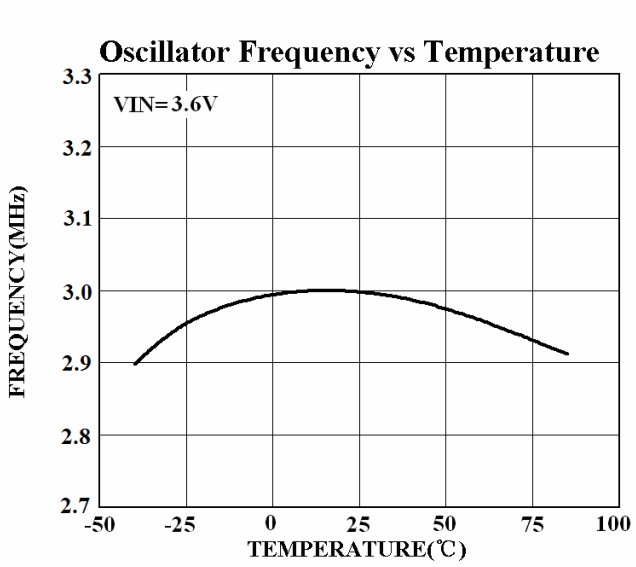
Typical Operating Characteristics (continued)

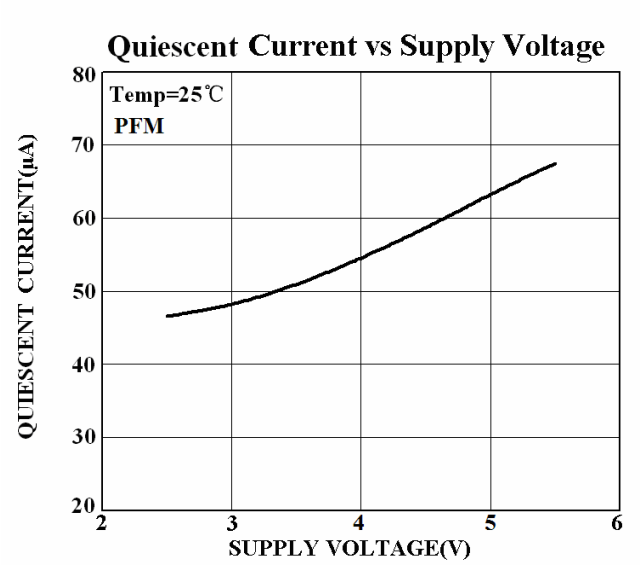
(AVIN=PVIN=3.6V, L=0.47µH, C_{OUT}=2×22µF)

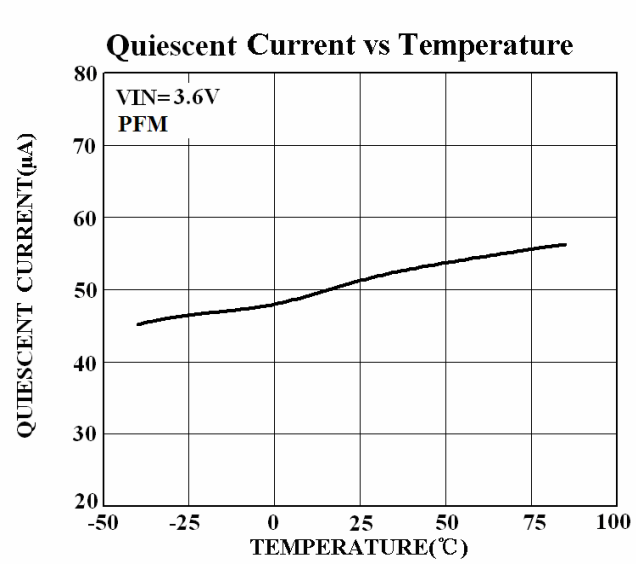








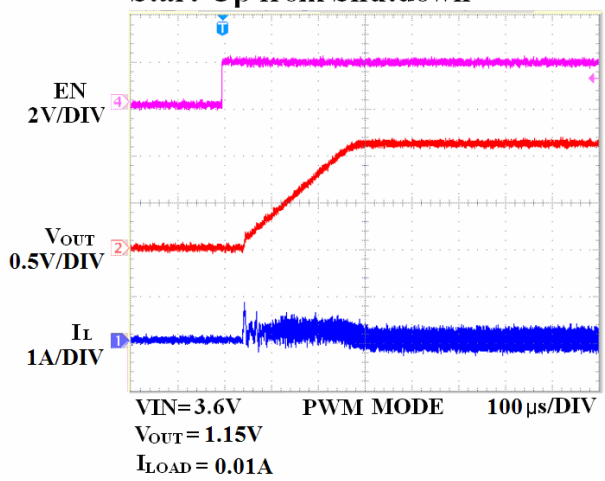




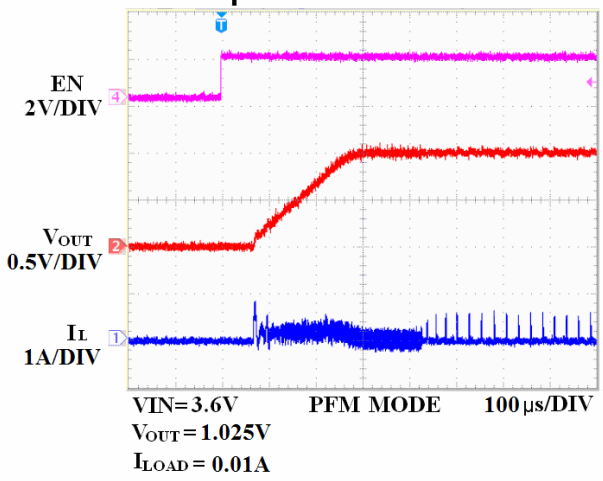
Typical Operating Characteristics (continued)

(AVIN=PVIN=3.6V, L=0.47µH, C_{OUT}=2×22µF)

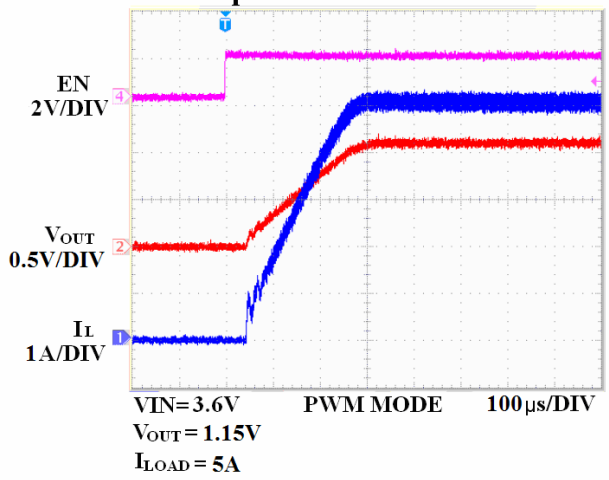
Start-Up from Shutdown



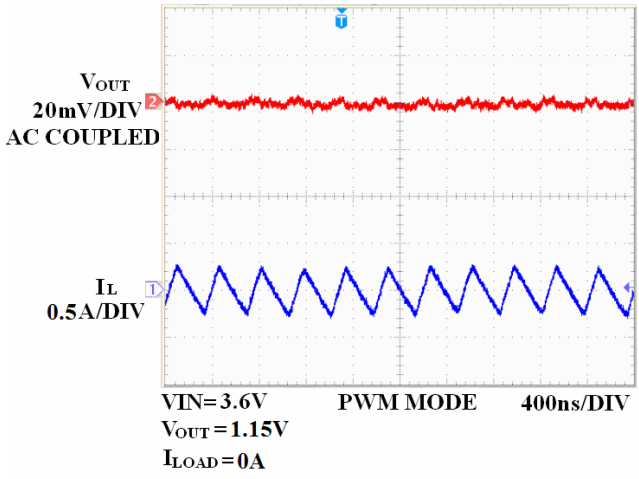
Start-Up from Shutdown



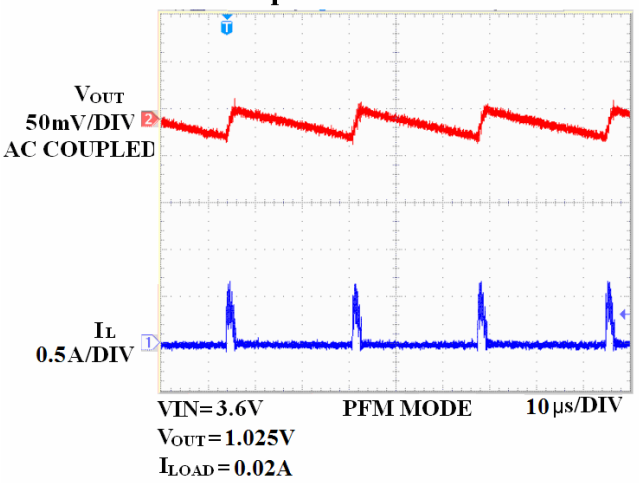
Start-Up from Shutdown



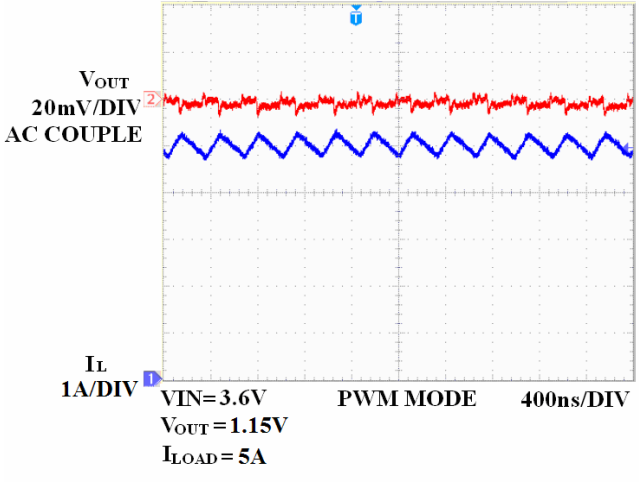
PWM Operation



PFM Operation



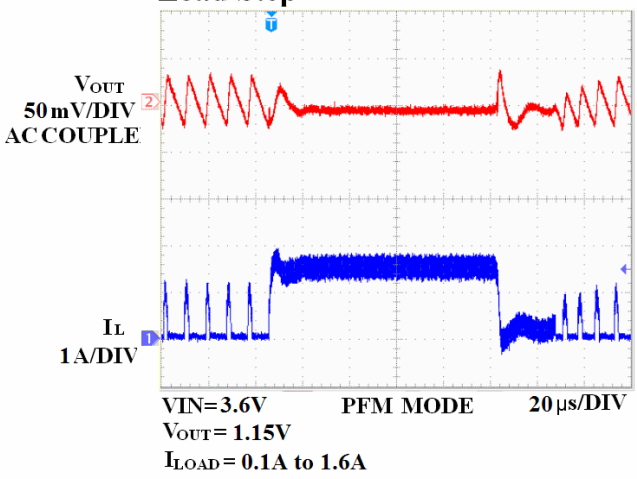
PWM Operation



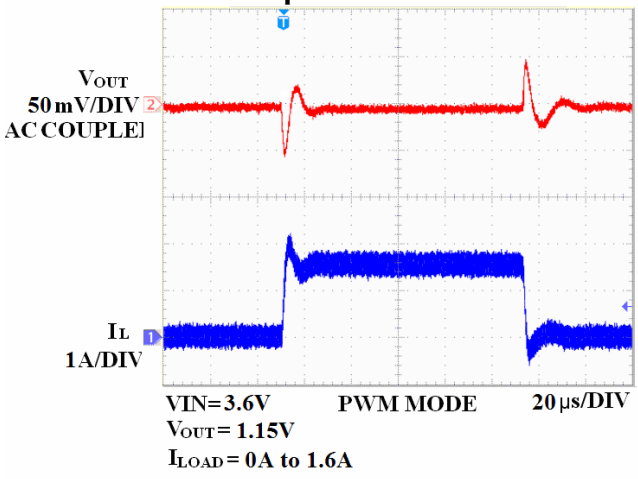
Typical Operating Characteristics (continued)

(AVIN=PVIN=3.6V, L=0.47µH, C_{OUT}=2×22µF)

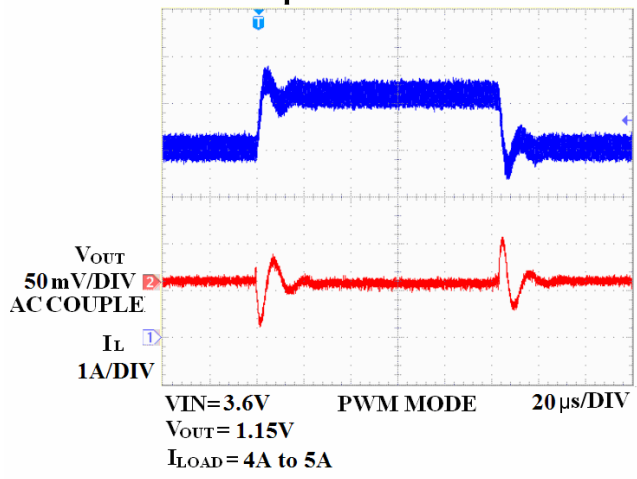
Load Step



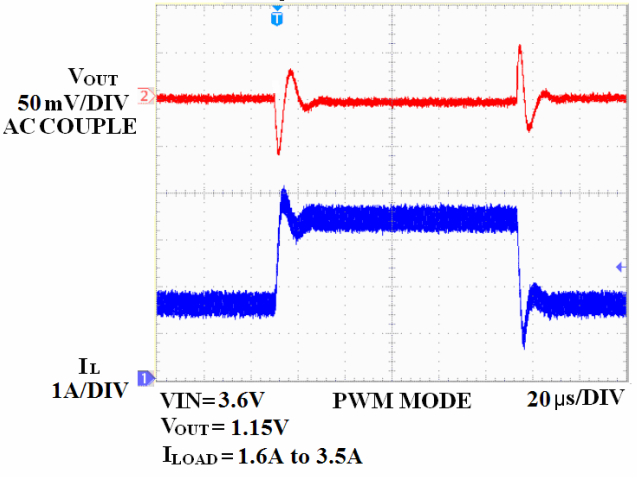
Load Step



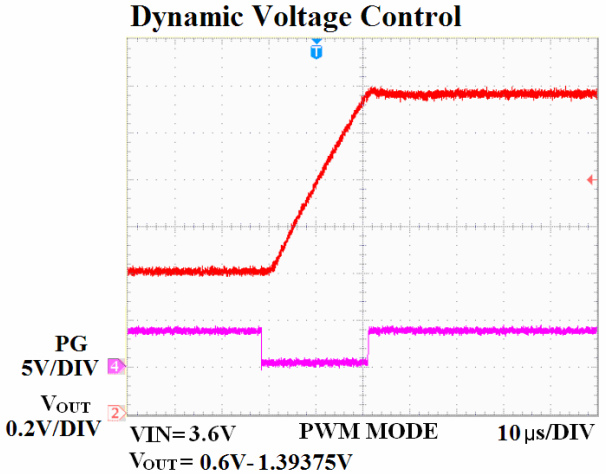
Load Step



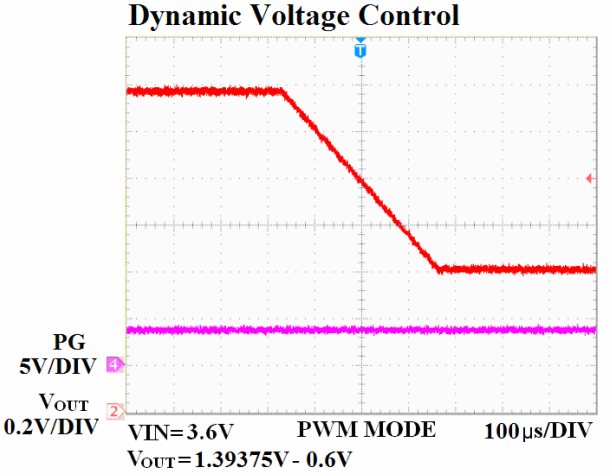
Load Step



Dynamic Voltage Control

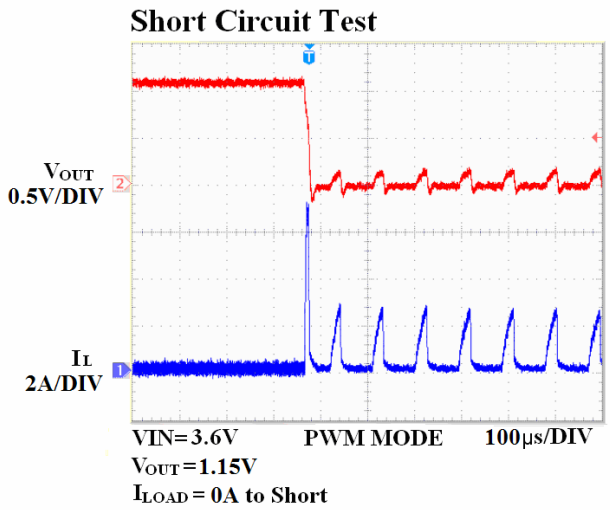


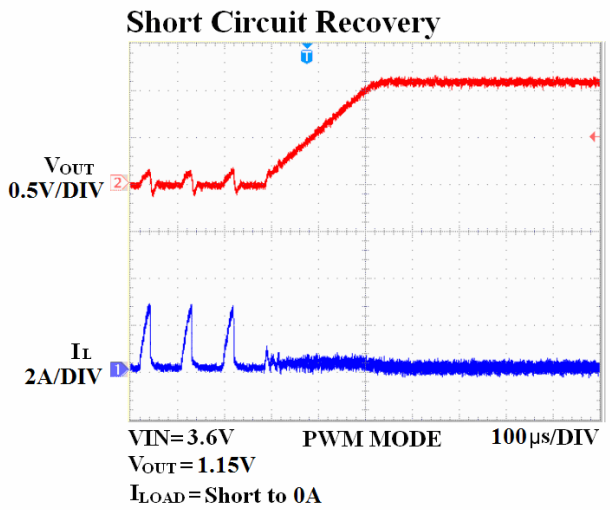
Dynamic Voltage Control



Typical Operating Characteristics (continued)

(AVIN=PVIN=3.6V, L=0.47µH, C_{OUT}=2×22µF)





OPERATION

Functional Description

The EUP3265 is a synchronous step-down converter typically operating with a 3-MHz fixed frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter could be programmed to operate with pulse frequency modulation (PFM) to improve efficiency. Both the main (P-Channel MOSFET) and the synchronous (N-Channel MOSFET) switches are internal. The EUP3265 uses voltage mode architecture with input voltage feed-forward. This achieves good load and line response and allows the use of tiny inductors and small ceramic input and output capacitors.

The EUP3265 integrates an I^2C compatible interface allowing transfers up to 3.4 Mbps. This communication interface can be used for dynamic voltage scaling with voltage steps down to 6.25 mV, for reprogramming the mode of operation (PFM or forced PWM) or disable/enabling the output voltage for instance. For more details, see the I^2C interface and register description section.

Forced PWM Operation

Selecting forced PWM mode operation, the EUP3265 regulates output voltage by switching at a constant frequency and then modulating the power transferred to the load each cycle using PWM comparator. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up until the PWM comparator trips and the control logic turns off the switch. The duty cycle is controlled by two weighed differential signals: the output of error amplifier and the sawtooth ramp. Forced PWM operation provides low ripple noise. The EUP3265 can be programmed to only use PWM and disable the transition to PFM if desired (PWMVSEL0/ PWMVSEL1 bits of COMMAND register).

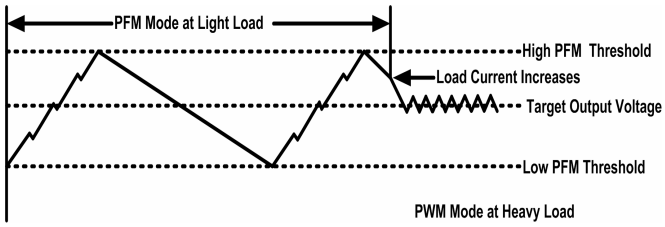


Figure 6. Operation in PFM mode and transfer to PWM mode

PFM/PWM Operation

The EUP3265 could operate at PFM mode to save power and improve efficiency when the load current is very low. In this case, the converter will automatically switch between PFM state and PWM state based on load demand. At light loads, the device enters PFM mode and operates with reduced switching frequency and quiescent current to maintain high efficiency. During PFM operation, there are two thresholds to control the loop and limit the output ripple as shown in Figure 6. With the increase of load current, the converter changes from PFM to PWM mode with smooth transition.

Output Voltage

Output voltage level of the EUP3265 can be programmed in the 0.6 V to 1.4 V range by 6.25 mV steps. Writing in the VoutVSEL0[6..0] bits of the PROGVSEL0 register or VoutVSEL1[6..0] bits of the PROGVSEL1 register will change settings. The VSEL pin and VSELGT bit will determine which register between PROGVSEL0 and PROGVSEL1 will set the output voltage.

- If VSELGT=1 AND VSEL=0, Output voltage is set by VoutVSEL0[6..0] bits (PROGVSEL0 register)
- Else, Output voltage is set by VoutVSEL1[6..0] bits (PROGVSEL1 register)

When the VSEL pin is set high, the EUP3265 has a default output voltage of 1.15V. When the VSEL pin is set low, the default output voltage changes to 1.025V.

Undervoltage Lockout

The undervoltage lockout circuit prevents device from misoperation at low input voltages. It prevents the converter from turning on the main and synchronous switches under undervoltage state.

Thermal Shutdown

As soon as the junction temperature of the IC exceeds 150°C typical, the device goes into thermal shutdown. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are turned off.

When EUP3265 returns from thermal shutdown, it can restart in two different configurations depending on REARM bit in the LIMCONF register (see register description section):

- If REARM = 0, EUP3265 does not restart after TSD. To restart, an EN pin toggle is required.
- If REARM = 1, EUP3265 restarts with register values set prior to thermal shutdown. The device recovers its operation when the junction temperature falls below 130°C typical again.

Active Output Discharge

To make sure that no residual voltage remains in the power supply rail, an active discharge path can ground the EUP3265 output voltage. For maximum flexibility, this feature can be easily disabled or enabled with DISCHG bit in PGOOD register. By default the discharge path is disabled.

Enabling

The EN pin controls EUP3265 start up. EN pin Low to High transition starts the power up sequencer. If EN is made low, the DC-DC converter is turned off and device enters:

- In Sleep Mode if Sleep_Mode I^2C bit is high or VSEL is high.
- In Off Mode if Sleep_Mode I^2C bit and VSEL are low.

When EN pin is set to high level, the DC-DC converter can be enabled/disabled by writing the ENVSEL0 or ENVSEL1 bit of the PROGVSEL0 and PROGVSEL1 registers: If ENVSELx bit is high, DC-DC is activated. If ENVSELx bit is low, DC-DC converter is turned off and device enters in Sleep Mode.

A built in pull down resistor disables the device when this pin is left unconnected or not driven.

Dynamic Voltage Scaling (DVS)

This converter supports dynamic voltage scaling (DVS) allowing the output voltage to be reprogrammed via I^2C commands and provides the different voltages required by the processor. The change between set points is managed in a smooth fashion without disturbing the operation of the processor. When programming a higher voltage, output raises in equidistant steps, which are 6.25mV/0.166us, such that the dV/dt is controlled. When programming a lower voltage, output will decrease in equidistant steps per defined time period such that the dV/dt is controlled (default 6.25mV/2.666us) by writing DVS[1..0] bits in TIME register. DVS sequence is automatically initiated by changing output voltage settings. There are two ways to change these settings:

- Directly change the active setting register value (VoutVSEL0[6..0] of PROGVSEL0 register or VoutVSEL1[6..0] of the PROGVSEL1 register) via I^2C command.
- Change the VSEL internal signal level by toggling VSEL pin.

The second method eliminates the I^2C latency and therefore faster.

VSEL Pin

By changing VSEL pin levels, the user has a latency free way to change EUP3265 configuration: operating mode (Auto or PWM forced), the output voltage as well as enable. VSEL pin action can be masked by writing 0 to the VSELGT bit in the COMMAND register. In that case I^2C bit corresponding to VSEL high will be taken into account.

Power Good Pin (Optional)

To indicate the output voltage level is established, a power good signal is available. The power good pin is pulled down when the DC-DC converter is off. Once the output voltage reaches 93% of the expected output level, the power good logic signal becomes high and the open drain output becomes high impedance. During operation when the output drops below 90% of the programmed level, the power good logic signal goes low and the open drain signal transitions to a low impedance state, which indicates a power failure. When the voltage rises again to above 93% the power good signal goes high again.

During a positive DVS sequence, when target voltage is higher than initial voltage, the Power Good logic signal will be set low during output voltage ramping and transition to high once the output voltage reaches 93% of the target voltage. When the target voltage is lower than the initial voltage, Power Good pin will remain at high level during transition.

Power Good signal during normal operation can be disabled by clearing the PGDCDC bit in PGOOD register.

Power Good operation during DVS can be controlled by setting / clearing the bit PGDVS in PGOOD register.

In order to generate a Reset signal, a delay can be programmed between the output voltage gets 93% of its final value and Power Good pin is released to high level. The delay is set through the TOR[1..0] bits in the TIME register. The default delay is 0 ms.

I^2C interface

Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The EUP3265 device works as a slave and supports the following data transfer modes, as defined in the I^2C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The data transfer protocol for standard and fast modes is exactly the same. Therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is identical with the F/S-mode except the bus speed, and it is referred to as HS-mode.

The EUP3265 device supports 7-bit addressing. The 7 MSBs are 0011100.

Fast/Standard (F/S) Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 7. All I^2C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 8. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge bit, see Figure 9, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 7. This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

High Speed (HS) Mode

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode.

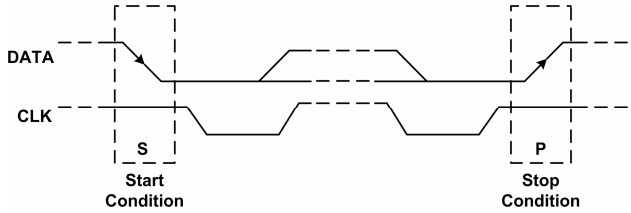


Figure7.Start and Stop conditions

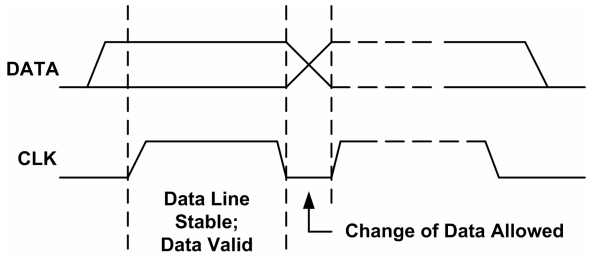


Figure8.Bit Transfer on the Serial Interface

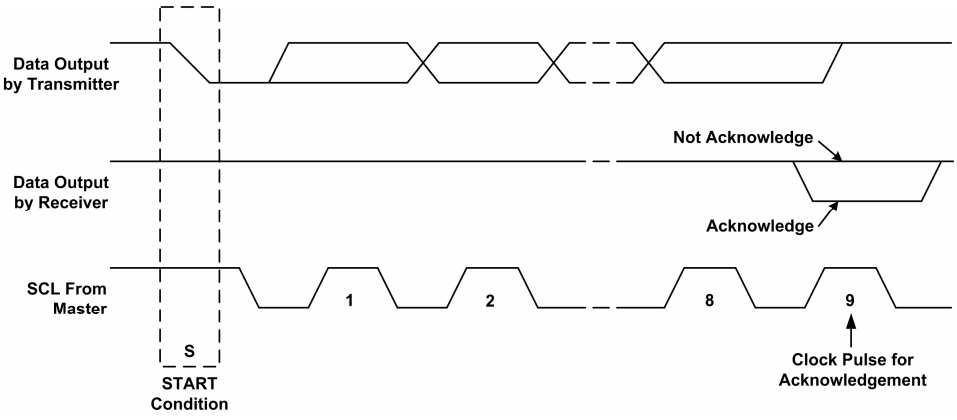


Figure9.Acknowledge on the I^2C Bus

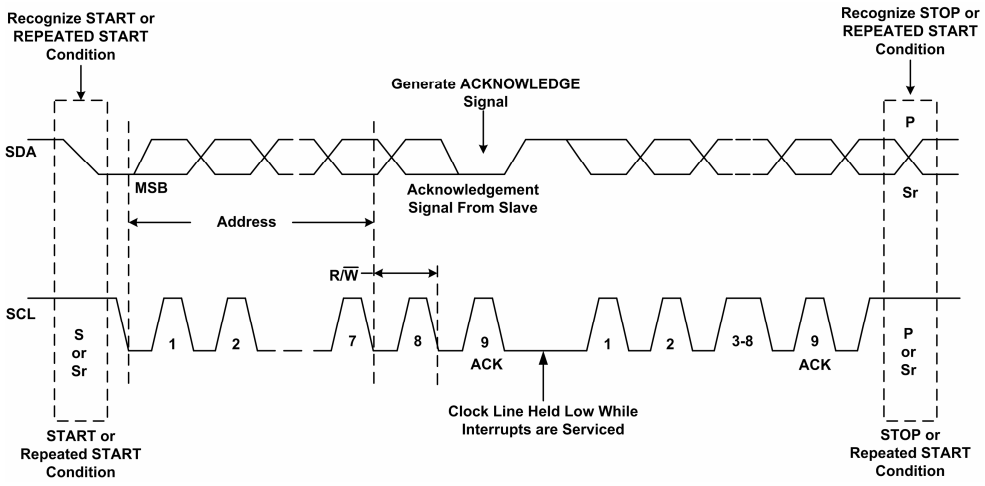


Figure10.Bus Protocol

Read and Write transactions

The EUP3265 requires a start condition, a valid I^{2}C address, a register address byte, and a data byte for a single update. After the receipt of each byte, the EUP3265 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^{2}C address selects the EUP3265. EUP3265 performs an update on the falling edge of the LSB byte.

When EN pin is tied to ground, the registers can be updated via the I^{2}C interface.

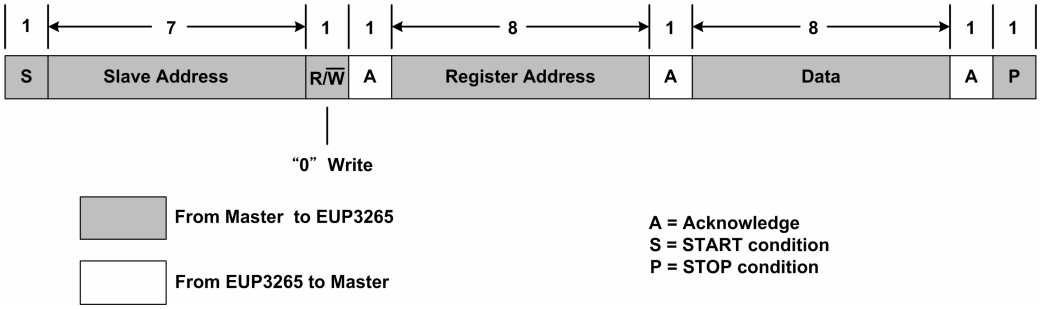


Figure11. "Write" Data Transfer Format in F/S-Mode

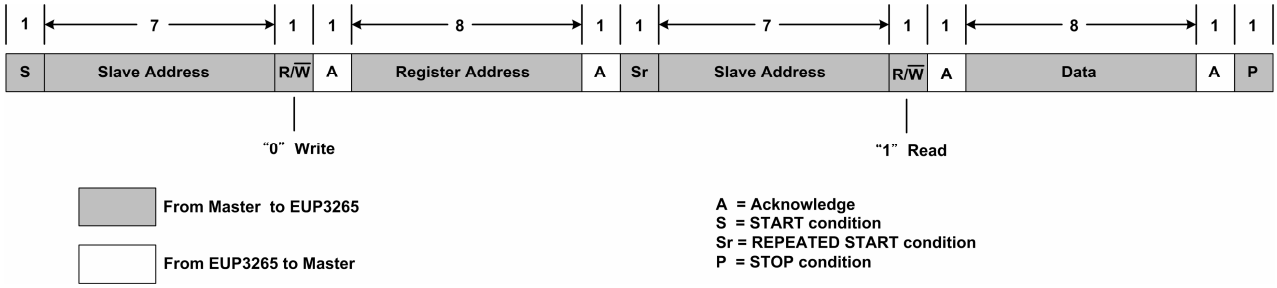


Figure12. "Read" Data Transfer Format in F/S-Mode

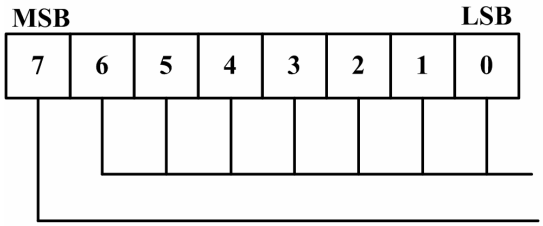
Configurations

Default values of EUP3265 are shown below:

- I^{2}C Address: 0011100
- VOUT_VSEL1: 1.15V
- VOUT_VSEL0: 1.025V
- MODE_VSEL1: Forced PWM
- MODE_VSEL0: PWM/PFM Auto Mode
- IPEAK: 8A

Register Description

POWERNMOS REGISTER (READ/WRITE)

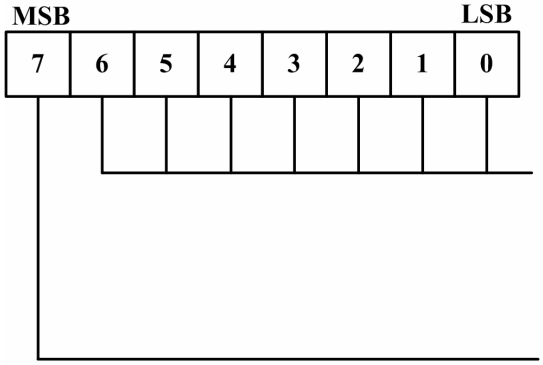


Address: 03h
Default state: 00h

SPARE=0

NMOS_CTL
Power NMOS gate control for sharing output rail
0 : Disabled
1 : Enabled

PROGVSEL1 REGISTER (READ/WRITE)

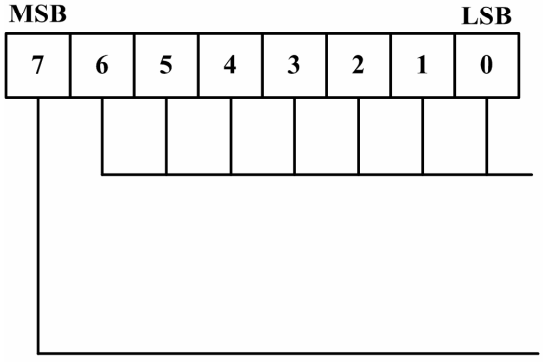


Address: 10h
Default state: D8h

VoutVSEL1[6..0]
Sets the DC-DC converter output voltage when VSEL pin=1 or when VSEL pin function is disabled in register COMMAND.D0
0000000b=600mV, 1111111b=1393.75mV (step of 6.25mV)

ENVSEL1
EN pin gating for VSEL internal signal = High
0 : Disabled
1 : Enabled

PROGVSEL0 REGISTER (READ/WRITE)

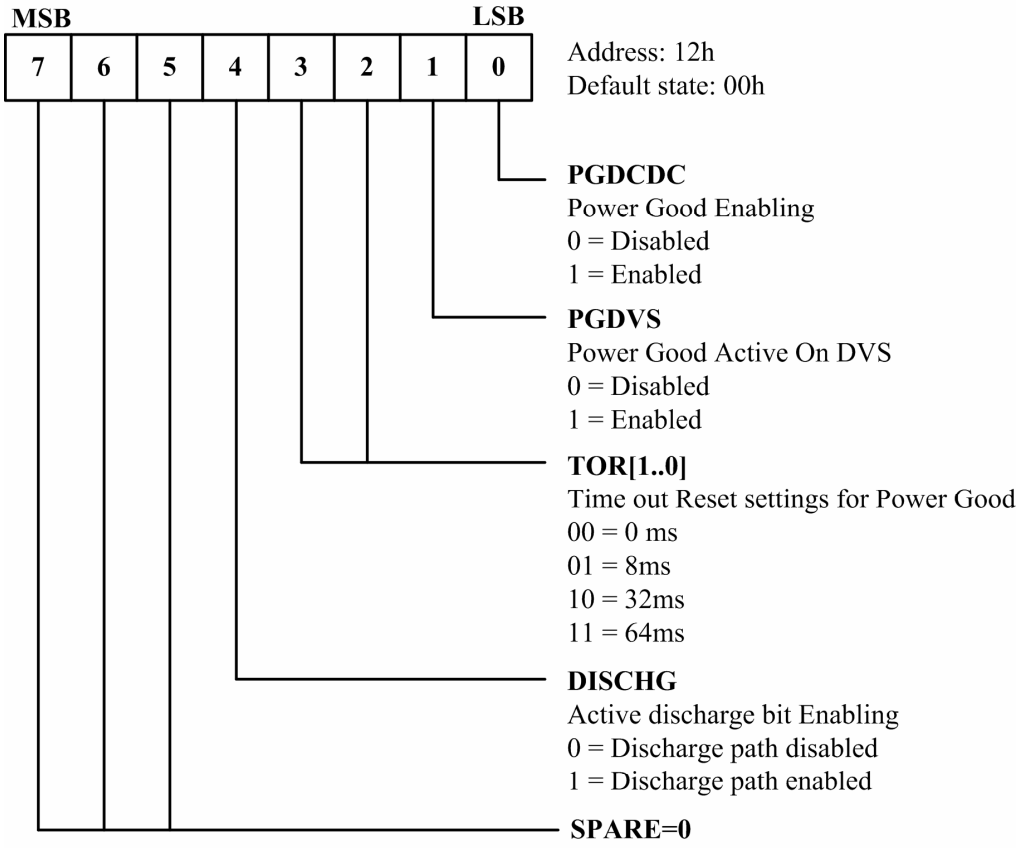


Address: 11h
Default state: C4h

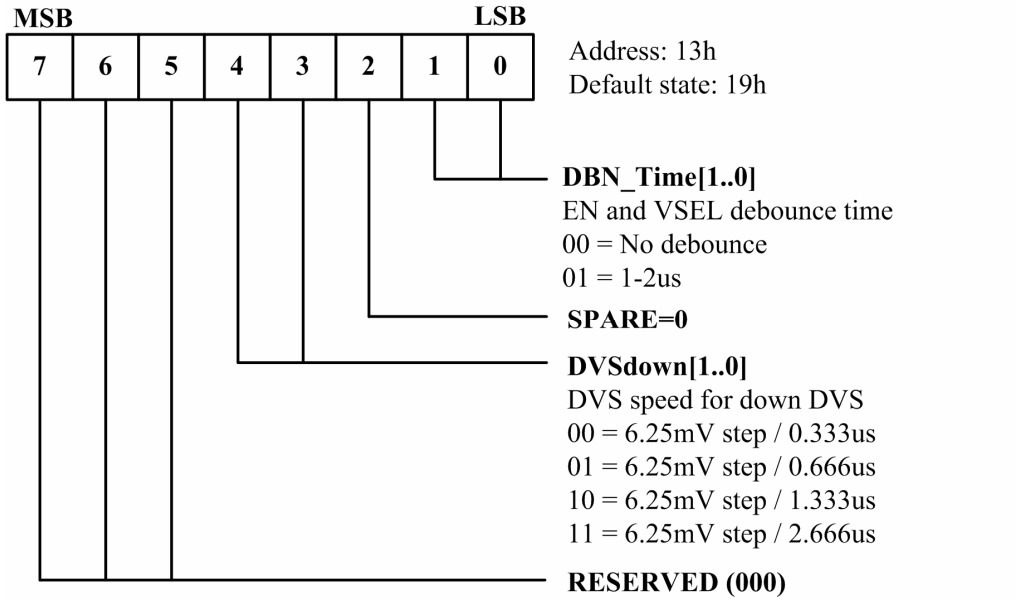
VoutVSEL[6..0]
Sets the DC-DC converter output voltage when VSEL pin=0 (and VSEL pin function is enabled in register COMMAND.D0)
0000000b=600mV, 1111111b=1393.75mV (step of 6.25mV)

ENVSEL0
EN pin gating for VSEL internal signal = Low
0 : Disabled
1 : Enabled

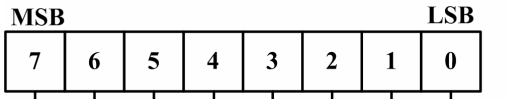
PGOOD REGISTER (READ/WRITE)



TIME REGISTER (READ/WRITE)



COMMAND REGISTER (READ/WRITE)



Address: 14h
Default state: 41h

VSELGT
VSEL Pin Gating
0 = Disabled
1 = Enabled

SPARE=0

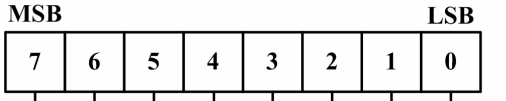
SLEEP_MODE
0 = Low Iq mode when EN and VSEL low
1 = Force product in sleep mode (when EN and VSEL are low)

SPARE=0

PWMVSEL1
Operating mode for VSEL internal signal = High
0 = Auto
1 = Forced PWM

PWMVSEL0
Operating mode for VSEL internal signal = Low
0 = Auto
1 = Forced PWM

LIMCONF REGISTER (READ/WRITE)



Address: 16h
Default state: E3h

REARM
Rearming of device after TSD
0 = No re-arming after TSD
1 = Rearming after TSD with no reset of I2C registers

RSTSTATUS
Reset Indicator Bit
0 = Must be written to 0 after register reset
1 = Default (loaded after Registers reset)

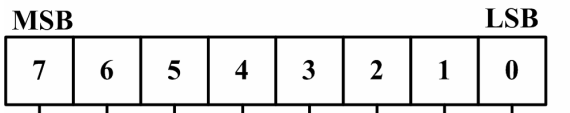
FORCERST
Force Reset Bit
0 = Default value. Self cleared to 0
1 = Force reset of internal registers to default

SPARE=0

RESERVED (10)

IPEAK
Inductor peak current settings
00 = 5A
01 = 5.5A
10 = 6A
11 = 8A

MODULE REGISTER (READ/WRITE)



Address: 15h
Default state: C0h

SPARE=0

SWITCHSIZE
0 = Full switch size
1 = Selects 1/3 of full switch size in PFM (increase light load efficiency)

Cannot write
This bit is the reverse signal of SWITCHSIZE

PFMTRAN
PFM/PWM mode transition point
0 = Determined by the current of synchronous switch (In low duty cycle, please select 0)
1 = Determined by the currents of main switch and synchronous switch

Applications Information

Inductor Selection

The EUP3265 typically uses a 0.33µH or 0.47µH inductor. The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. The DC resistance of the inductor directly influences the efficiency of the converter. Therefore for better efficiency, choose a low DC-resistance inductor.

CIN and COUT Selection

In continuous mode, the source current of the P-Channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the EUP3265. A low ESR input capacitor sized for the maximum RMS current must be used. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A typically C_{IN} value is around 10µF. If the wire of supply is too long, larger input capacitor should be used, 22µF is preferred.

The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The output capacitor C_{OUT} has a strong effect on loop stability. The selection of C_{OUT} is driven by the required effective series resistance (ESR). ESR is a direct function of the volume of the capacitor; that is, physically larger capacitors have lower ESR. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the IRIPPLE(P-P) requirement. The output ripple ΔV_{OUT} in PWM mode is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Thermal Considerations

To avoid the EUP3265 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R=(P_D)(\theta_{JA})$$

Where $P_D=I_{LOAD}^2\times R_{DS(ON)}$ is the power dissipated by the regulator ; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J=T_A+T_R$$

Where T_A is the ambient temperature.

TJ should be below the maximum junction temperature of 150°C.

PC Board Layout Checklist

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems.

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3265.

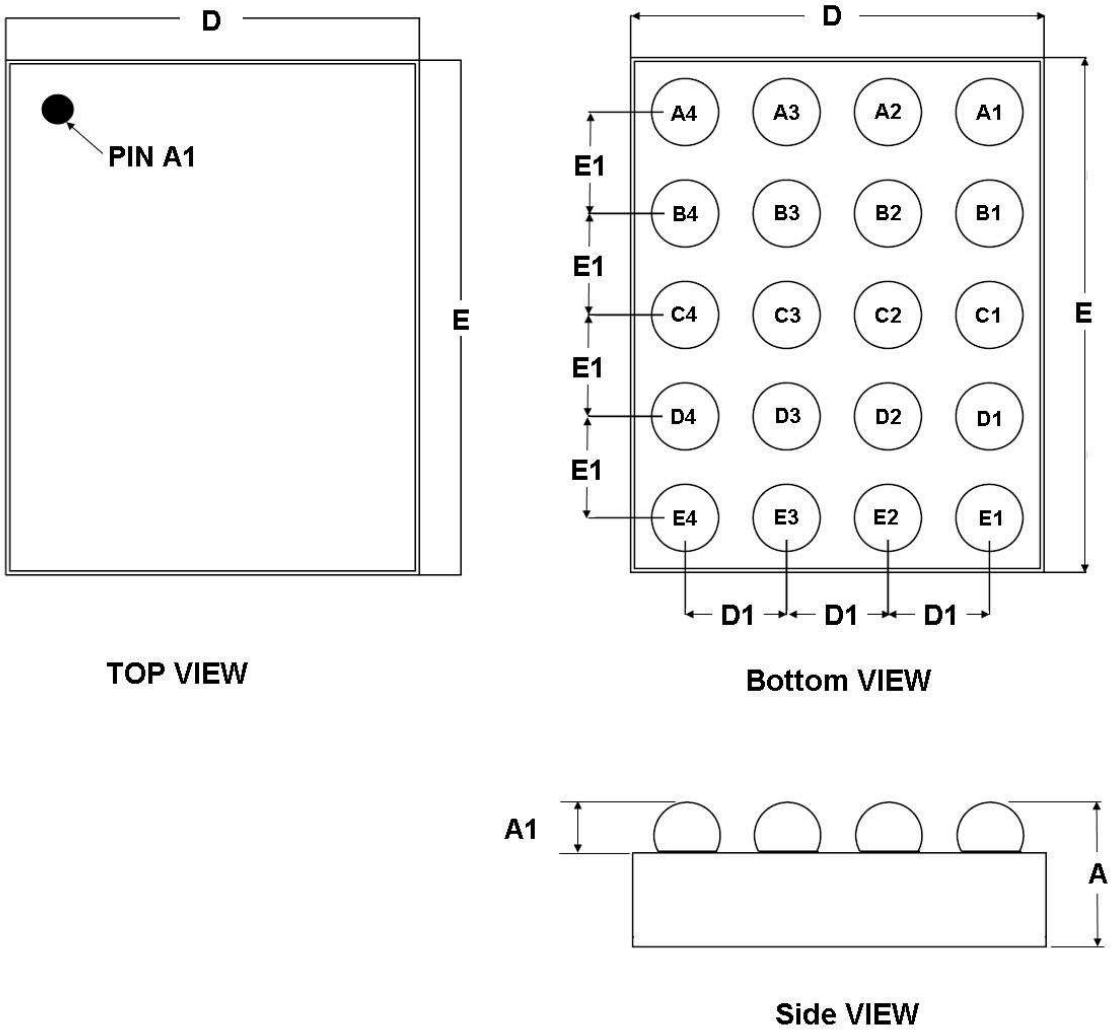
The input capacitor C_{IN} should connect to V_{IN} as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.

The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.

For good thermal coupling, PCB vias are required from the Pad for the thermal paddle to the ground plane.

Packaging Information

WCSP-20



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	0.60	-	0.024
A1	0.15	0.23	0.006	0.009
D	1.60	1.66	0.063	0.065
D1	0.40 REF		0.016 REF	
E	2.00	2.06	0.079	0.081
E1	0.40 REF		0.016 REF	