74LVTH125
3.3V, Quad Buffer/Line Driver with 3-State Outputs

GENERAL DESCRIPTION

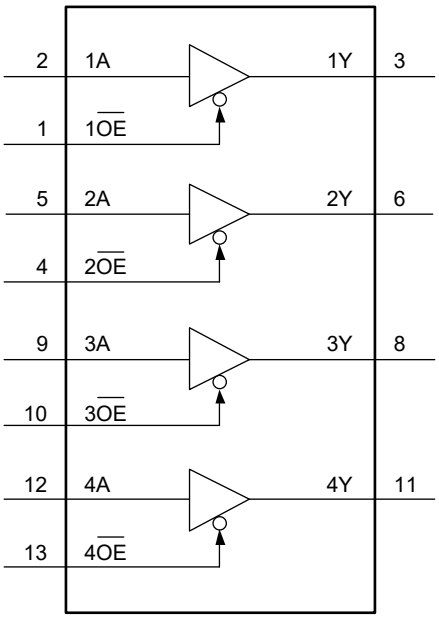
The 74LVTH125 is a high-performance product with 3-state bus outputs and it is designed for 3.3V V_{CC} operation. The device is organized as a quad buffer with separate output enable ($n\overline{OE}$) inputs, each controlling one of the 3-state outputs. When $n\overline{OE}$ is low, the device passes data from the nA inputs to the nY outputs. When $n\overline{OE}$ is high, the outputs are in the high-impedance state.

The device combines low static and dynamic power dissipation with high speed and high output drive. The 74LVTH125 bus hold on data inputs eliminates the need for external pull-up/pull-down resistors to hold unused inputs.

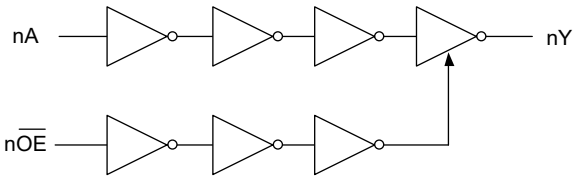
FEATURES

- **Quad Bus Interface**
- **3-State Buffers**
- **Output Capability: +64mA/-32mA**
- **TTL Input and Output Switching Levels**
- **Input and Output Interface Capability to Systems at 5V Supply**
- **Bus Hold on Data Inputs Eliminates the Need for External Pull-Up/Pull-Down Resistors**
- **Live Insertion and Extraction Permitted**
- **Power-Up 3-State**
- **No Bus Current Loading When Output is Tied to 5V Bus**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOIC-14 Package**

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

CONTROL INPUT	INPUT	OUTPUT
$n\overline{OE}$	**nA**	**nY**
L	L	L
L	H	H
H	*X*	Z

H = High Voltage Level

L = Low Voltage Level

Z = High-Impedance State

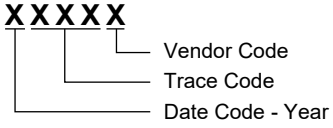
X = Don't Care

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVTH125	SOIC-14	-40℃ to +125℃	74LVTH125XS14G/TR	74LVTH125XS14 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 4.6V
Input Voltage, V_I (2) ..... -0.5V to 7V
Output Voltage, V_O (2)
Output in 3-State or High-State ..... -0.5V to 7V
Input Clamping Current, I_{IK} (V_I < 0V) ..... -50mA
Output Clamping Current, I_{OK} (V_O < 0V) ..... -50mA
Output Current, I_O
Output in High-State ..... -64mA
Output in Low-State 128mA
Supply Current, I_{CC} 128mA
Ground Current, I_{GND} ..... -256mA
Junction Temperature (3) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 8000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 2.7V to 3.6V
Input Voltage, V_I ..... 0V to 5.5V
High-Level Output Current, I_{OH} ..... -32mA
Low-Level Output Current, I_{OL} 64mA
Input Transition Rise and Fall Rate, Δt/ΔV
..... 10ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

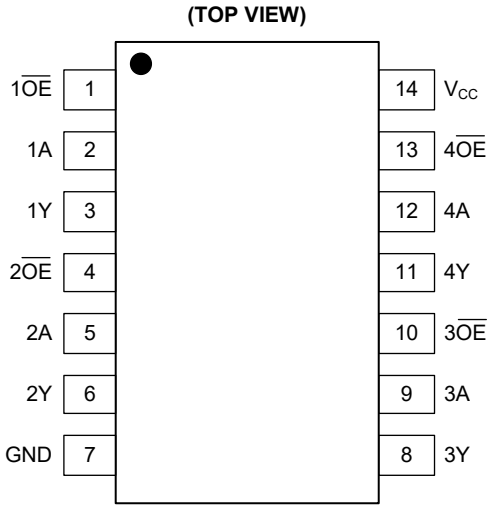
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 4, 10, 13	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output Enable Inputs (Active Low).
2, 5, 9, 12	1A, 2A, 3A, 4A	Data Inputs.
3, 6, 8, 11	1Y, 2Y, 3Y, 4Y	Data Outputs.
7	GND	Ground.
14	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Input Clamping Voltage	V_{IK}	V_{CC} = 2.7V, I_{IK} = -18mA		Full	-1.2	-0.78		V
High-Level Input Voltage	V_{IH}	V_{CC} = 2.7V to 3.6V		Full	2.0			V
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.7V to 3.6V		Full			0.8	V
High-Level Output Voltage	V_{OH}	V_{CC} = 2.7V to 3.6V, I_{OH} = -100µA		Full	V_{CC} - 0.05	V_{CC} - 0.001		V
		V_{CC} = 2.7V, I_{OH} = -8mA		Full	2.45	2.60		
		V_{CC} = 3.0V, I_{OH} = -32mA		Full	2.10	2.65		
Low-Level Output Voltage	V_{OL}	V_{CC} = 2.7V	I_{OL} = 100µA	Full		0.001	0.05	V
			I_{OL} = 24mA	Full		0.15	0.28	
		V_{CC} = 3.0V	I_{OL} = 16mA	Full		0.1	0.18	
			I_{OL} = 32mA	Full		0.2	0.36	
			I_{OL} = 64mA	Full		0.4	0.55	
Input Leakage Current	I_I	Control pins, V_{CC} = 3.6V, V_I = V_{CC} or GND		Full		±0.01	±1	µA
		Control pins, V_{CC} = 0V or 3.6V, V_I = 5.5V		Full		0.01	5	
		Input data pins (1), V_{CC} = 0V or 3.6V, V_I = 5.5V		Full		0.4	5	
		Input data pins (1), V_{CC} = 3.6V, V_I = V_{CC}		Full		0.3	3	
		Input data pins (1), V_{CC} = 3.6V, V_I = GND		Full	-2	-0.01		
Off-State Output Current	I_{OZ}	V_{CC} = 3.6V	V_O = 3.0V	Full		0.01	2	µA
			V_O = 0.5V	Full	-2	-0.01		
Output Leakage Current	I_{LO}	Output in high-state when V_O > V_{CC}, V_O = 5.5V, V_{CC} = 3.0V		Full		1	30	µA
Power-Up/Down Output Current	$I_{O\_PU/PD}$	V_{CC} ≤ 1.2V, V_O = 0.5V to V_{CC}, V_I = GND or V_{CC}, $n\overline{OE}$ = don't care		+25℃		0.01	10	µA
Power-Off Leakage Current	I_{OFF}	V_{CC} = 0V, V_I or V_O = 0V to 5.5V		Full		0.01	10	µA
Supply Current	I_{CC}	V_{CC} = 3.6V, V_I = GND or V_{CC}, I_O = 0A	Output high	Full		13	40	µA
			Output low	Full		13	40	
			Outputs disabled (2)	Full		13	40	
Additional Supply Current (3)	ΔI_{CC}	Per input pin, V_{CC} = 3.0V to 3.6V, one input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		Full		0.2	200	µA
Input Capacitance	C_I	V_I = 0V or 3.0V		+25℃		6		pF
Output Capacitance	C_O	Outputs disabled, V_O = 0V or 3.0V		+25℃		9		pF
Bus Hold Low Current	I_{BHL}	V_{CC} = 3.0V, V_I = 0.8V		Full	50	100		µA
Bus Hold High Current	I_{BHH}	V_{CC} = 3.0V, V_I = 2.0V		Full		-130	-75	µA
Bus Hold Low Overdrive Current (4)	I_{BHLO}	Input data pins, V_{CC} = 3.6V, V_I = 0V to 3.6V		Full	500	200		µA
Bus Hold High Overdrive Current (4)	I_{BHHO}	Input data pins, V_{CC} = 3.6V, V_I = 0V to 3.6V		Full		-280	-500	µA

NOTES:

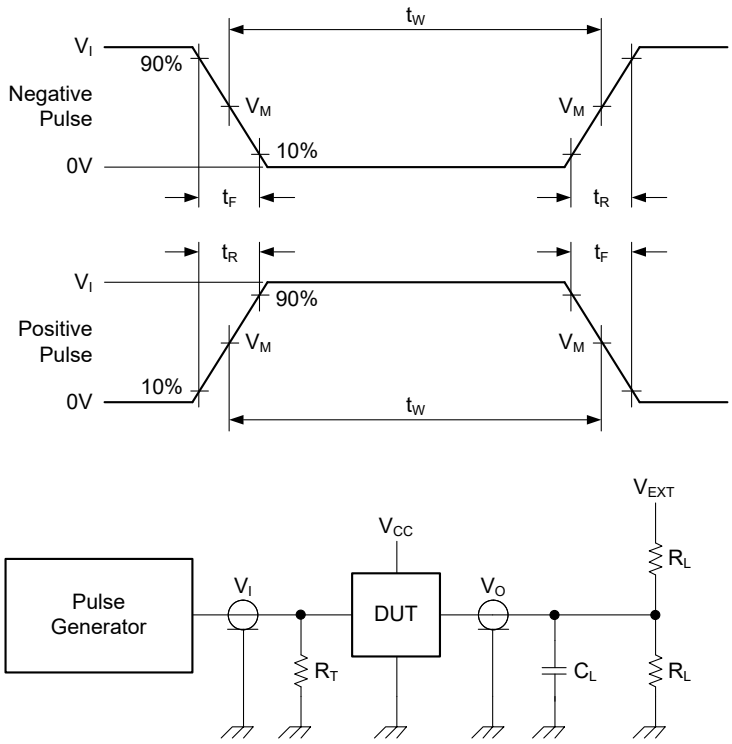
1. Unused pins at V_{CC} or GND.
2. I_{CC} is measured with outputs pulled to V_{CC} or GND.
3. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
4. This is the bus hold overdrive current required to force the input to the opposite logic state.

DYNAMIC CHARACTERISTICS

(For test circuit, see Figure 1. All typical values are measured at V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Low to High Propagation Delay	t_{PLH}	nA to nY, see Figure 2	V_{CC} = 2.7V	+25°C		4.3		ns
			V_{CC} = 3.0V to 3.6V	+25°C		4.3		
High to Low Propagation Delay	t_{PHL}	nA to nY, see Figure 2	V_{CC} = 2.7V	+25°C		3.9		ns
			V_{CC} = 3.0V to 3.6V	+25°C		3.7		
Off-State to High Propagation Delay	t_{PZH}	n$\overline{OE}$ to nY, see Figure 3	V_{CC} = 2.7V	+25°C		5.3		ns
			V_{CC} = 3.0V to 3.6V	+25°C		4.9		
Off-State to Low Propagation Delay	t_{PZL}	n$\overline{OE}$ to nY, see Figure 3	V_{CC} = 2.7V	+25°C		5.0		ns
			V_{CC} = 3.0V to 3.6V	+25°C		4.9		
High to Off-State Propagation Delay	t_{PHZ}	n$\overline{OE}$ to nY, see Figure 3	V_{CC} = 2.7V	+25°C		4.9		ns
			V_{CC} = 3.0V to 3.6V	+25°C		4.6		
Low to Off-State Propagation Delay	t_{PLZ}	n$\overline{OE}$ to nY, see Figure 3	V_{CC} = 2.7V	+25°C		5.4		ns
			V_{CC} = 3.0V to 3.6V	+25°C		5.4		

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator.

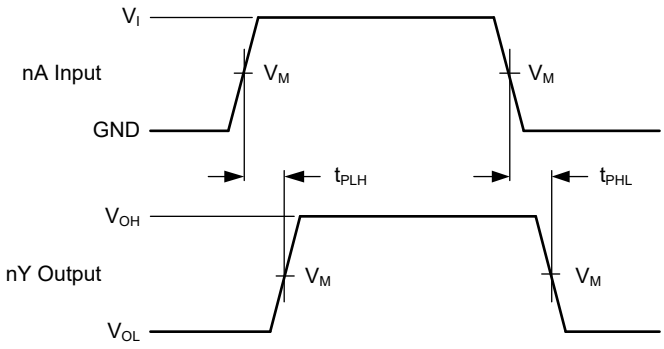
V_{EXT} = External voltage for measuring switching times.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

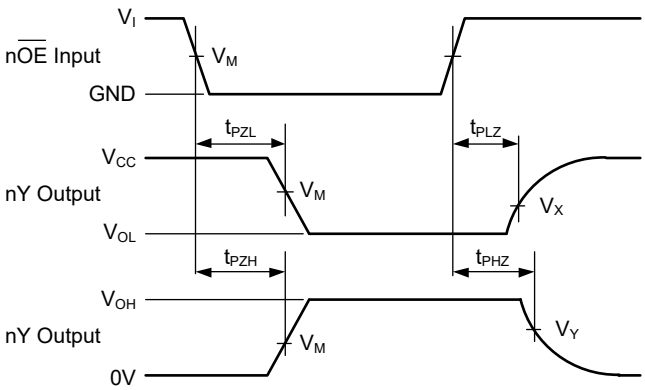
SUPPLY VOLTAGE	INPUT				LOAD		V_{EXT}		
V_{CC}	V_I	f_i	t_W	t_R, t_F	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7V to 3.6V	2.7V	≤ 10MHz	500ns	≤ 2.5ns	50pF	500Ω	GND	6V	Open

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (nA) to Output (nY) Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.7V to 3.6V	2.7V	1.5V	1.5V	V_{OL} + 0.3V	V_{OH} - 0.3V

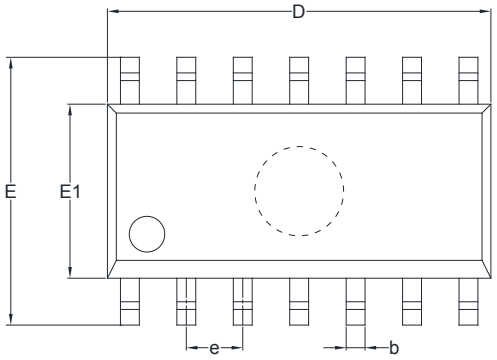
REVISION HISTORY

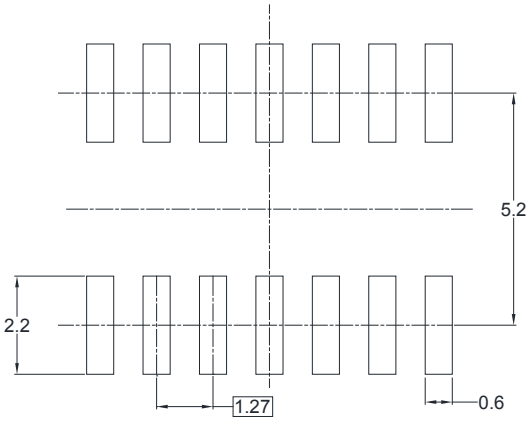
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (APRIL 2021) to REV.A	Page
Changed from product preview to production data	All

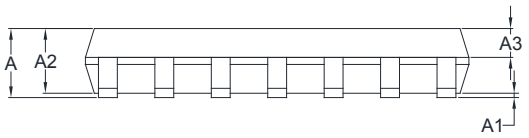
PACKAGE OUTLINE DIMENSIONS

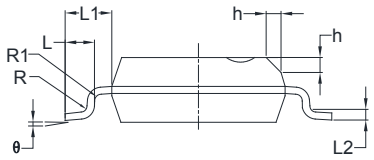
SOIC-14





RECOMMENDED LAND PATTERN (Unit: mm)

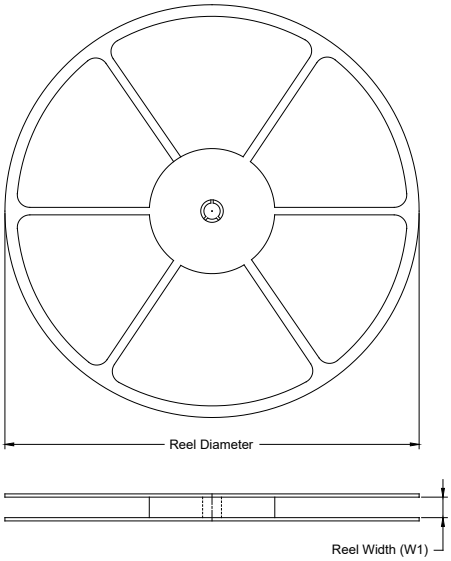




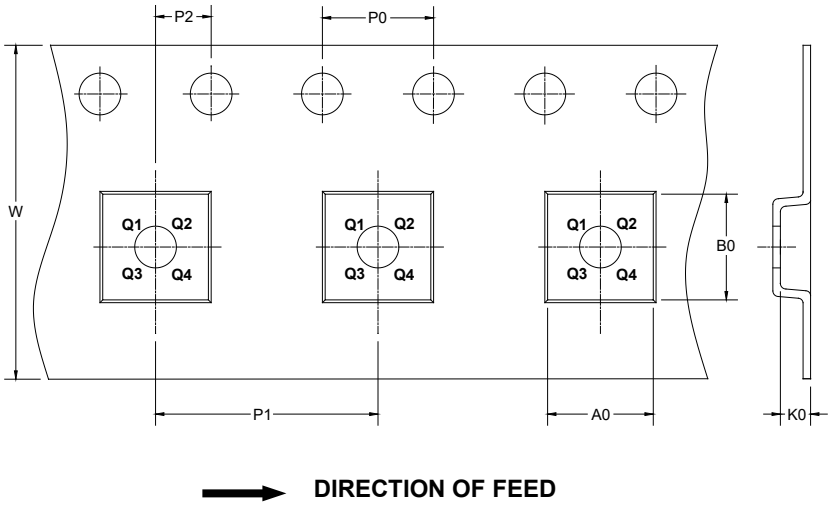
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.049	0.065
A3	0.55	0.75	0.022	0.030
b	0.36	0.49	0.014	0.019
D	8.53	8.73	0.336	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.45	0.80	0.018	0.032
L1	1.04 REF		0.040 REF	
L2	0.25 BSC		0.01 BSC	
R	0.07		0.003	
R1	0.07		0.003	
h	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



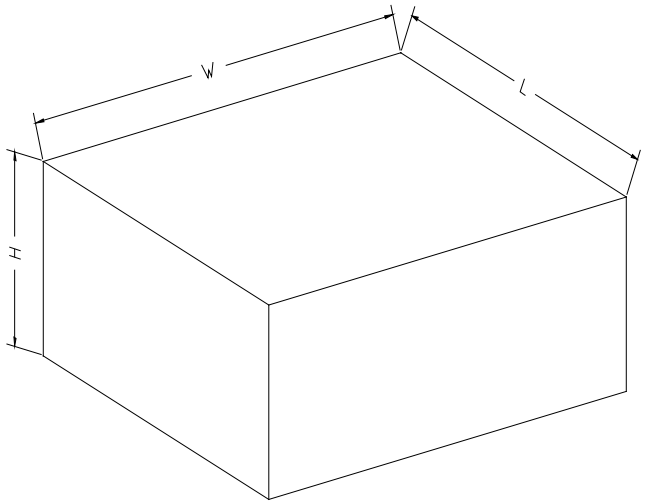
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-14	13″	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002