74LVCN16373
16-Bit D-Type Transparent Latch with 3-State Outputs

GENERAL DESCRIPTION

The 74LVCN16373 is a 16-bit transparent D-type latch which separates D-type inputs for each latch and 3-state outputs for bus-oriented applications. One latch enable (nLE) input and one output enable ($n\overline{OE}$) input are provided for each octal. Inputs can be driven from either 3.3V or 5V devices. When disabled, up to 5.5V can be applied to the outputs. These features allow the use of this device in mixed 3.3V and 5V applications.

The device can be used as two 8-bit transparent D-type latches with 3-state outputs. When nLE is high, data at the nDn inputs enter the latches. In this condition, the latches are transparent, that is, the latch-outputs change each time its corresponding D-inputs change. The latches store the information that was present at the D-inputs one set-up time (t_{SU}) preceding the high-to-low transition of nLE. When $n\overline{OE}$ is low, the contents of the 8 latches are available at the outputs. When $n\overline{OE}$ is high, the outputs go to the high-impedance state. Operation of the $n\overline{OE}$ input does not affect the state of the latches.

FEATURES

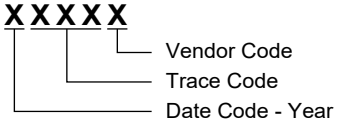
- **5V Tolerant Inputs/Outputs for Interfacing with 5V Logic**
- **Wide Supply Voltage Range: 1.2V to 3.6V**
- **CMOS Low Power Consumption**
- **Direct Interface with TTL Levels**
- **Inputs Accept Voltages up to 5.5V**
- **High-Impedance State When V_{CC} = 0V**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-48 Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVCN16373	TSSOP-48	-40℃ to +125℃	74LVCN16373XTS48G/TR	74LVCN16373 XTS48 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 6.5V
Input Voltage, V_I (2) ..... -0.5V to 6.5V
Output Voltage, V_O (2)
Output in High-State or Low-State .... -0.5V to (V_{CC} + 0.5V)
Output in 3-State ..... -0.5V to 6.5V
Input Clamping Current, I_{IK} (V_I < 0V) .....-50mA
Output Clamping Current, I_{OK} (V_O > V_{CC} or V_O < 0V)
..... ±50mA
Output Current, I_O
Output in High-State or Low-State ..... ±50mA
Supply Current, I_{CC} 100mA
Ground Current, I_{GND} .....-100mA
Junction Temperature (3) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility
HBM.....8000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Function Supply Voltage, V_{CC} .....1.2V to 3.6V
Operating Supply Voltage, V_{CC} .....1.65V to 3.6V
Input Voltage, V_I.....0V to 5.5V
High-Level Output Current, I_{OH} .....-24mA
Low-Level Output Current, I_{OL}.....24mA
Input Transition Rise and Fall Rate, Δt/ΔV
V_{CC} = 1.2V to 2.7V ..... 20ns/V (MAX)
V_{CC} = 2.7V to 3.6V ..... 10ns/V (MAX)
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

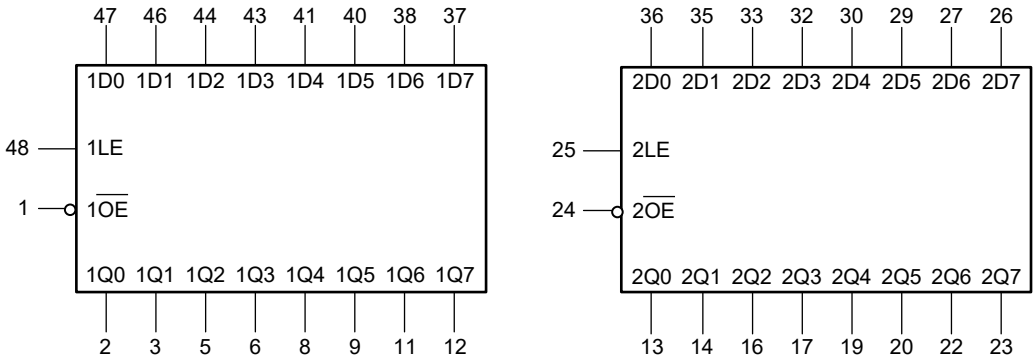
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

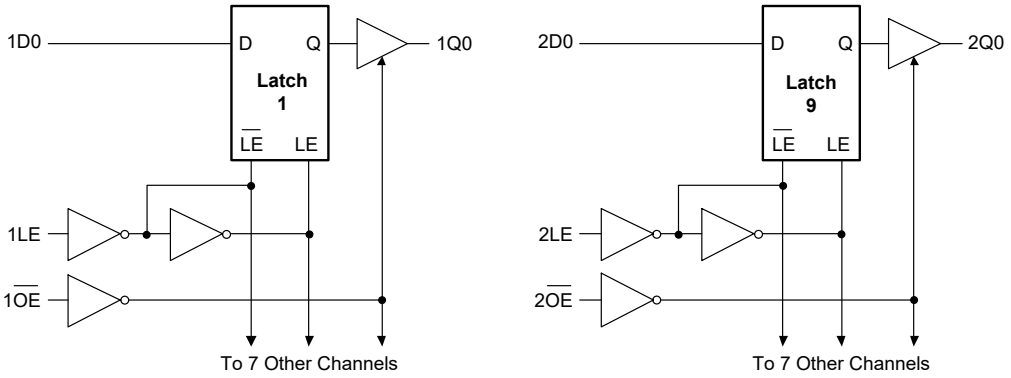
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	CONTROL INPUT			INTERNAL REGISTER	OUTPUT
	nOE	nLE	nDn		nQn
Enable and Read Register (Transparent Mode)	L	H	L	L	L
	L	H	H	H	H
Latch and Read Register	L	L	l	L	L
	L	L	h	H	H
Latch Register and Disable Outputs	H	L	l	L	Z
	H	L	h	H	Z

H = High Voltage Level

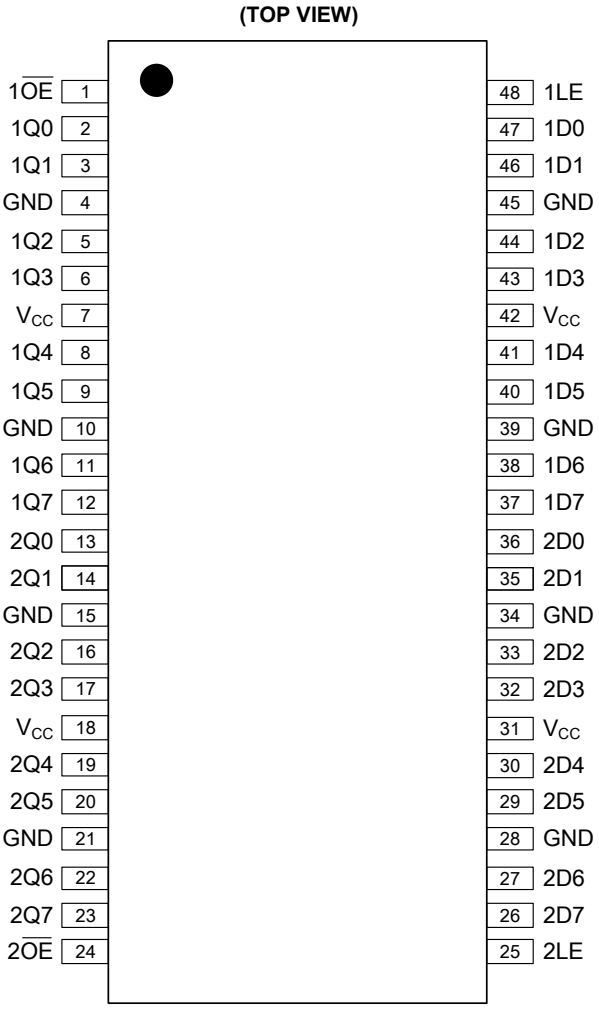
L = Low Voltage Level

h = High Voltage Level One Set-Up Time Prior to the High-to-Low LE Transition

l = Low Voltage Level One Set-Up Time Prior to the High-to-Low LE Transition

Z = High-Impedance State

PIN CONFIGURATION



TSSOP-48

PIN DESCRIPTION

PIN	NAME	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37	1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	Data Inputs.
36, 35, 33, 32, 30, 29, 27, 26	2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	Data Inputs.
1, 24	1$\overline{OE}$, 2$\overline{OE}$	Output Enable Inputs (Active Low).
48, 25	1LE, 2LE	Latch Enable Inputs (Active High).
2, 3, 5, 6, 8, 9, 11, 12	1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	Data Outputs.
13, 14, 16, 17, 19, 20, 22, 23	2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	Data Outputs.
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground.
7, 18, 31, 42	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.2V		Full	1.08			V
		V_{CC} = 1.65V to 1.95V		Full	0.65 × V_{CC}			
		V_{CC} = 2.3V to 2.7V		Full	1.7			
		V_{CC} = 2.7V to 3.6V		Full	2			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.2V		Full			0.12	V
		V_{CC} = 1.65V to 1.95V		Full			0.35 × V_{CC}	
		V_{CC} = 2.3V to 2.7V		Full			0.7	
		V_{CC} = 2.7V to 3.6V		Full			0.8	
High-Level Output Voltage	V_{OH}	V_I = V_{IH}	I_O = -100μA, V_{CC} = 1.65V to 3.6V	Full	V_{CC} - 0.05	V_{CC} - 0.003		V
			I_O = -4mA, V_{CC} = 1.65V	Full	1.43	1.54		
			I_O = -8mA, V_{CC} = 2.3V	Full	2.03	2.18		
			I_O = -12mA, V_{CC} = 2.7V	Full	2.36	2.55		
			I_O = -18mA, V_{CC} = 3.0V	Full	2.53	2.8		
			I_O = -24mA, V_{CC} = 3.0V	Full	2.35	2.73		
Low-Level Output Voltage	V_{OL}	V_I = V_{IL}	I_O = 100μA, V_{CC} = 1.65V to 3.6V	Full		0.002	0.05	V
			I_O = 4mA, V_{CC} = 1.65V	Full		0.07	0.2	
			I_O = 8mA, V_{CC} = 2.3V	Full		0.11	0.28	
			I_O = 12mA, V_{CC} = 2.7V	Full		0.16	0.35	
			I_O = 24mA, V_{CC} = 3.0V	Full		0.3	0.55	
Input Leakage Current	I_I	V_I = 5.5V or GND, V_{CC} = 3.6V		Full		±0.01	±2	μA
Off-State Output Current	I_{OZ}	V_I = V_{IH} or V_{IL}, V_O = 5.5V or GND, V_{CC} = 3.6V		Full		±0.01	±2	μA
Power-Off Leakage Current	I_{OFF}	V_I or V_O = 5.5V, V_{CC} = 0.0V		Full		0.01	5	μA
Supply Current	I_{CC}	V_I = V_{CC} or GND, I_O = 0A, V_{CC} = 3.6V		Full		1.3	20	μA
Additional Supply Current (1)	ΔI_{CC}	Per input pin, V_I = V_{CC} - 0.6V, I_O = 0A, V_{CC} = 2.7V to 3.6V		Full		0.1	80	μA
Input Capacitance	C_I			+25℃		6		pF

NOTE:

1. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

DYNAMIC CHARACTERISTICS

(For test circuit see Figure 1. All typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Propagation Delay (1)	t_{PD}	nDn to nQn, see Figure 2	V_{CC} = 1.2V	+25℃		28.4		ns
			V_{CC} = 1.65V to 1.95V	+25℃		6.8		ns
			V_{CC} = 2.3V to 2.7V	+25℃		4.7		ns
			V_{CC} = 2.7V	+25℃		4.4		ns
			V_{CC} = 3.0V to 3.6V	+25℃		4.2		ns
		nLE to nQn, see Figure 3	V_{CC} = 1.2V	+25℃		27.2		ns
			V_{CC} = 1.65V to 1.95V	+25℃		8.8		ns
			V_{CC} = 2.3V to 2.7V	+25℃		5.2		ns
			V_{CC} = 2.7V	+25℃		4.8		ns
			V_{CC} = 3.0V to 3.6V	+25℃		4.4		ns
Enable Time (1)	t_{EN}	nOE to nYn, see Figure 4	V_{CC} = 1.2V	+25℃		15.6		ns
			V_{CC} = 1.65V to 1.95V	+25℃		8		ns
			V_{CC} = 2.3V to 2.7V	+25℃		4.4		ns
			V_{CC} = 2.7V	+25℃		3.2		ns
			V_{CC} = 3.0V to 3.6V	+25℃		2.8		ns
Disable Time (1)	t_{DIS}	nOE to nYn, see Figure 4	V_{CC} = 1.2V	+25℃		12		ns
			V_{CC} = 1.65V to 1.95V	+25℃		6.8		ns
			V_{CC} = 2.3V to 2.7V	+25℃		4.4		ns
			V_{CC} = 2.7V	+25℃		4		ns
			V_{CC} = 3.0V to 3.6V	+25℃		4		ns

DYNAMIC CHARACTERISTICS (continued)

(For test circuit see Figure 1. All typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Pulse Width	t_W	nLE High, see Figure 3	V_{CC} = 1.65V to 1.95V	+25℃		2.9		ns
			V_{CC} = 2.3V to 2.7V	+25℃		2.2		ns
			V_{CC} = 2.7V	+25℃		1.5		ns
			V_{CC} = 3.0V to 3.6V	+25℃		1.5		ns
Set-Up Time	t_{SU}	nDn to nLE, see Figure 5	V_{CC} = 1.65V to 1.95V	+25℃		0.6		ns
			V_{CC} = 2.3V to 2.7V	+25℃		0.5		ns
			V_{CC} = 2.7V	+25℃		0.4		ns
			V_{CC} = 3.0V to 3.6V	+25℃		0.3		ns
Hold Time	t_H	nDn to nLE, see Figure 5	V_{CC} = 1.65V to 1.95V	+25℃		0.6		ns
			V_{CC} = 2.3V to 2.7V	+25℃		0.5		ns
			V_{CC} = 2.7V	+25℃		0.4		ns
			V_{CC} = 3.0V to 3.6V	+25℃		0.3		ns
Power Dissipation (2)	C_{PD}	Per input, V_I = GND to V_{CC}	V_{CC} = 1.65V to 1.95V	+25℃		12		pF
			V_{CC} = 2.3V to 2.7V	+25℃		13		pF
			V_{CC} = 3.0V to 3.6V	+25℃		14		pF

NOTES:

1. t_{PD} is the same as t_{PLH} and t_{PHL}. t_{EN} is the same as t_{PZL} and t_{PZH}. t_{DIS} is the same as t_{PLZ} and t_{PHZ}.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

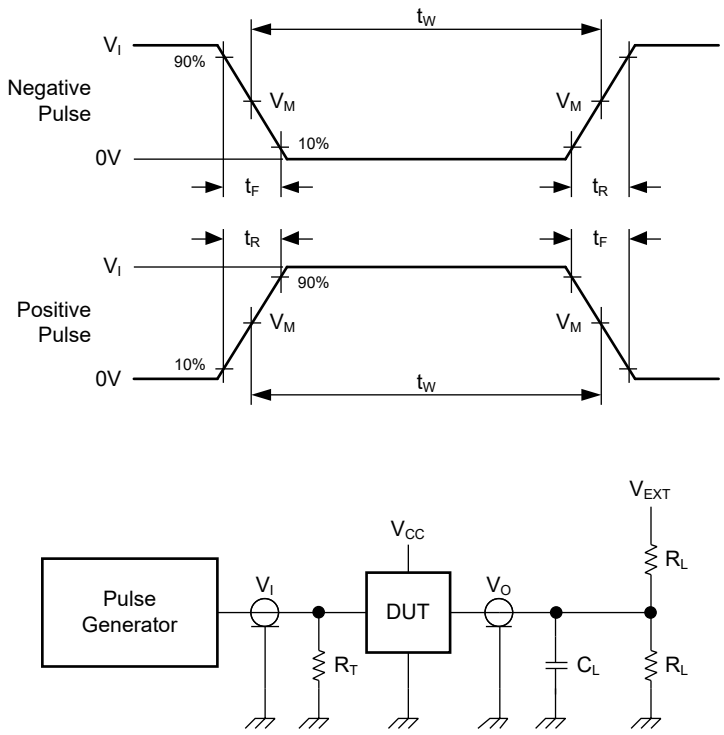
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = Sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator.

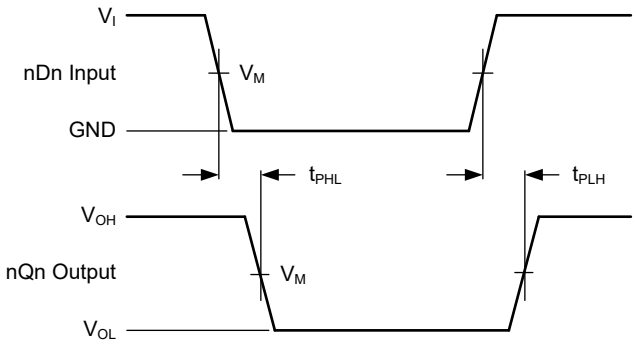
V_{EXT} = External voltage for measuring switching times.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

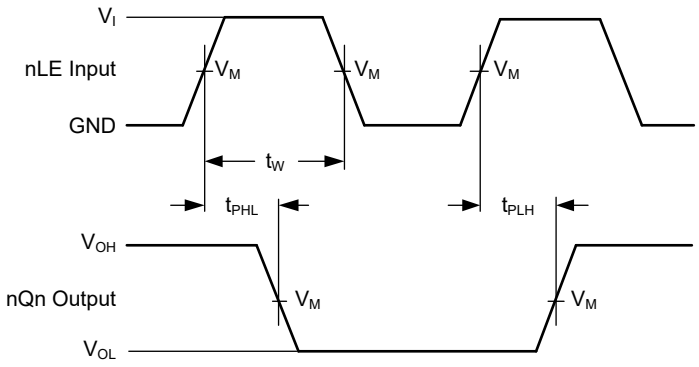
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2V	V_{CC}	≤ 2ns	30pF	1kΩ	Open	2 × V_{CC}	GND
1.65V to 1.95V	V_{CC}	≤ 2ns	30pF	1kΩ	Open	2 × V_{CC}	GND
2.3V to 2.7V	V_{CC}	≤ 2ns	30pF	500Ω	Open	2 × V_{CC}	GND
2.7V	2.7V	≤ 2.5ns	50pF	500Ω	Open	2 × V_{CC}	GND
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	Open	2 × V_{CC}	GND

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

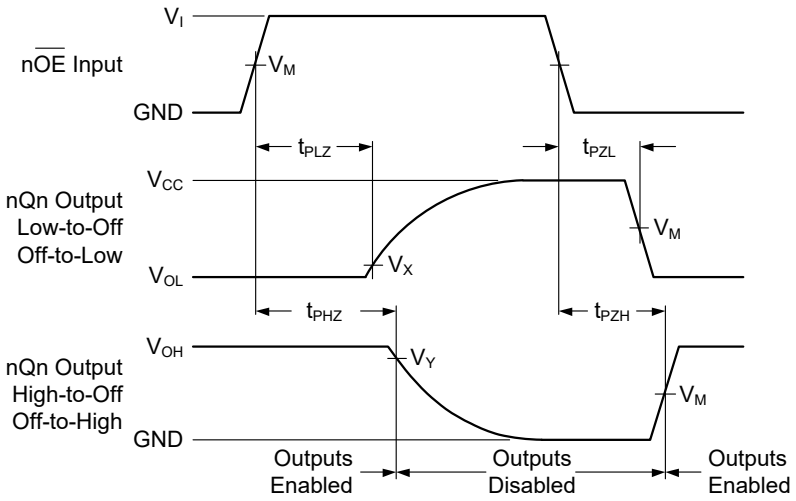
Figure 2. Input (nDn) to Output (nQn) Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Latch Enable Input Pulse Width and the Latch Enable Input to Output Propagation Delays

WAVEFORMS (continued)

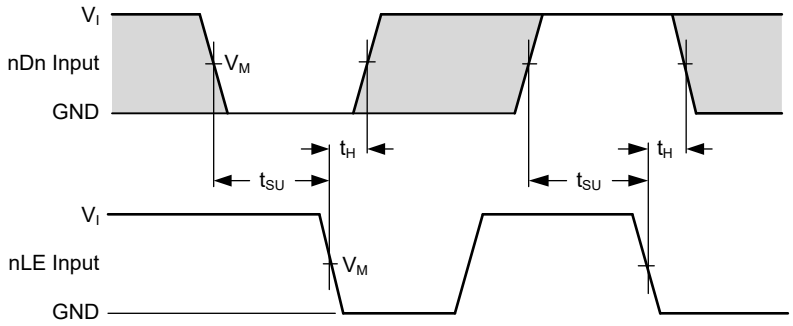


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and Disable Times



Test conditions are given in Table 1.

Measurement points are given in Table 2.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5. Data Set-Up and Hold Times for the nDn Input to the nLE Input

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15V	V_{OH} - 0.15V
1.65V to 1.95V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15V	V_{OH} - 0.15V
2.3V to 2.7V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15V	V_{OH} - 0.15V
2.7V	2.7V	1.5V	1.5V	V_{OL} + 0.3V	V_{OH} - 0.3V
3.0V to 3.6V	2.7V	1.5V	1.5V	V_{OL} + 0.3V	V_{OH} - 0.3V

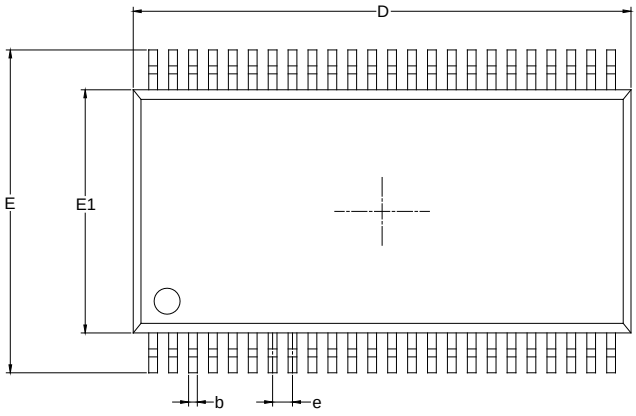
REVISION HISTORY

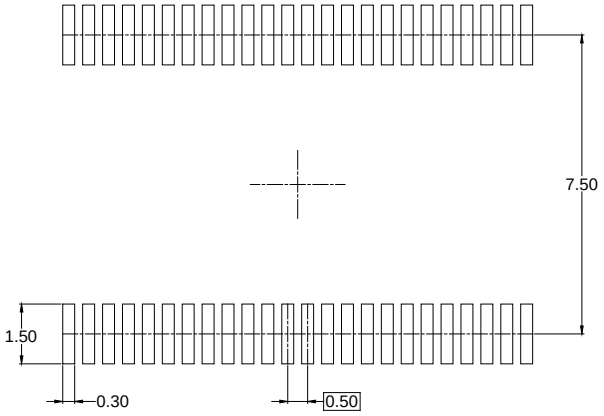
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (MARCH 2021) to REV.A	Page
Changed from product preview to production data	All

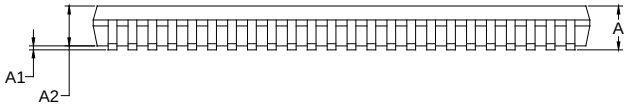
PACKAGE OUTLINE DIMENSIONS

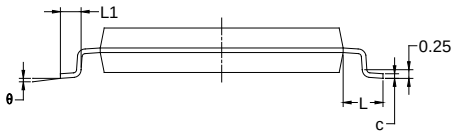
TSSOP-48





RECOMMENDED LAND PATTERN (Unit: mm)

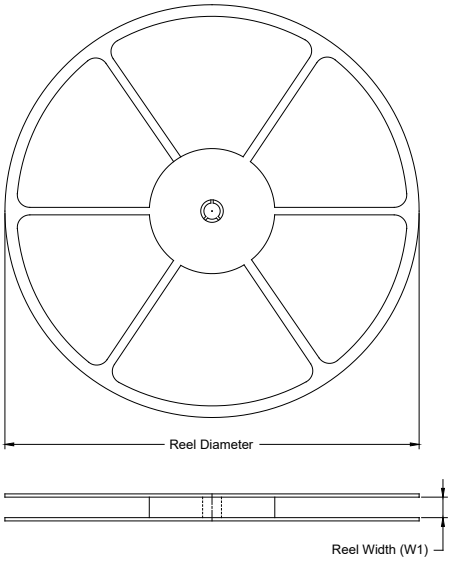




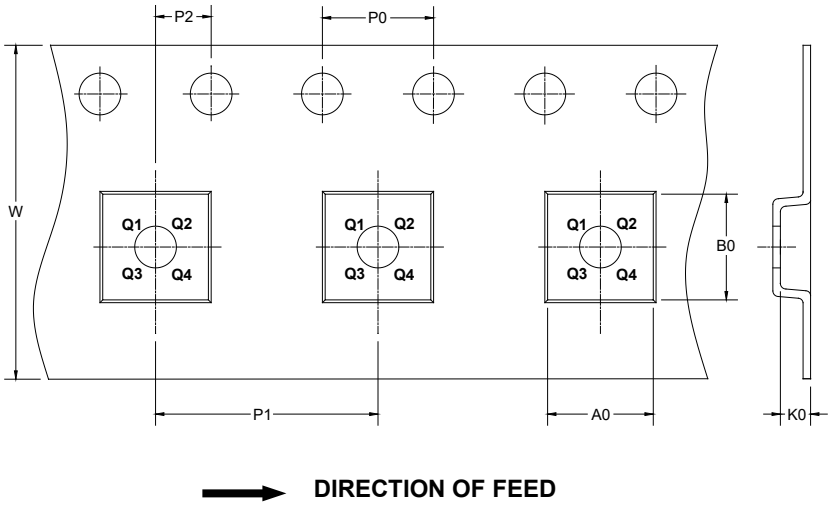
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
b	0.18		0.26
c	0.15		0.19
D	12.40	12.50	12.60
E	7.90	8.10	8.30
E1	6.00	6.10	6.20
e	0.50 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0°		8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

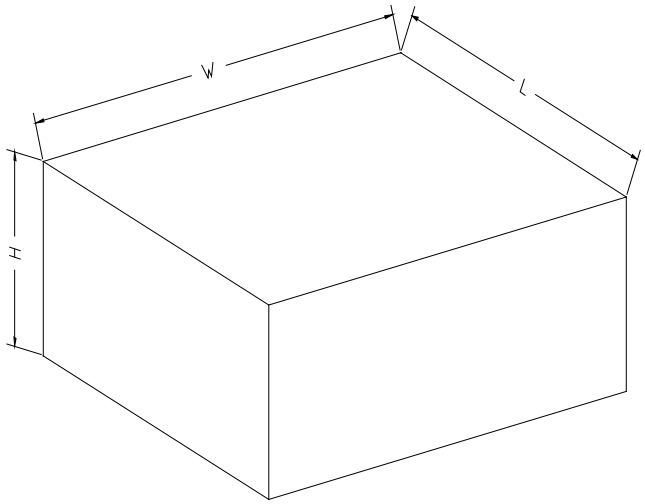
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-48	13”	24.4	8.60	13.00	1.80	4.0	12.0	2.0	24.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002