Dual 5-A High-Speed, Low-Side Gate Driver

Features

- Industry-Standard Pin-Out
- 4.5-V to 23-V Single-Supply Range
- Dual Independent Channels
- 5-A Peak Source and Sink-Drive Current
- Independent-Enable Function for Each Output
- TTL and CMOS Compatible Threshold
- Outputs Held Low During VDD-UVLO or Input Floating
- Low Propagation Delay (13-ns Typical)
- Fast Rise and Fall Times (7-ns and 6-ns Typical)
- <1-ns Typical Delay Matching Between Two Channels
- Two Outputs can be used in Parallel for Higher Drive Current
- ESD Protection Exceeds JESD 22 – 6-kV HBM, 1.5-kV CDM
- Available in SOP-8, EMSOP-8 and DFN3X3-8, DFN2X2-8 Packages

Description

The TPM2752x family is a series of dual-channel low-side gate-drivers for MOSFET, IGBT and GaN power switches.

High sourcing and sinking current capability of 5-A allows improving switching efficiencies by minimizing slew time and switching loss. The device supports maximum 25-V supply voltage and –5V improves system robustness especially in noisy industrial applications. Ultra-low propagation delay and excellent matching between two channels are designed for applications with tight timing requirements.

The TPM2752x family consists of a set of gate-drivers with different polarities, allowing customers to select based on application needs. The wide range of package support from SOP-8, EMSOP-8, DFN3X3-8 aligns with industrial standard packages. An extra ultra-small DFN2X2-8 assists design for ultra-compact synchronous rectifiers in power bricks.

Applications

- Switched-Mode Power Supplies
- DC-DC Converters
- Motor Control, Solar Inverters
- Gate & IGBT Drive

Pinout Diagram

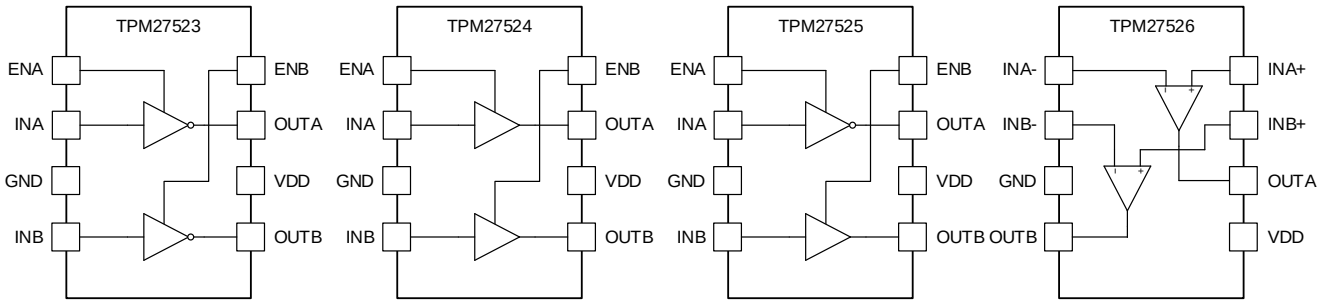


Table of Contents

Revision History

Date	Revision	Notes
2020/2/24	Rev A.0	Initial Release
2020/2/24	Rev A.1	Minor Update on Input hysteresis

Order Information

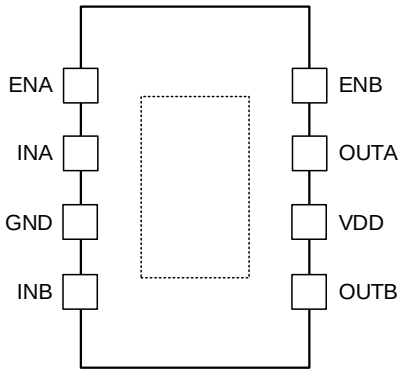
Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPM27523-SO1R	-40 °C – 125 °C (1)	SOP-8	M523	MSL3	4000
TPM27524-SO1R	-40 °C – 125 °C (1)	SOP-8	M524	MSL3	4000
TPM27525-SO1R	-40 °C – 125 °C (1)	SOP-8	M525	MSL3	4000
TPM27526-SO1R	-40 °C – 125 °C (1)	SOP-8	M526	MSL3	4000
TPM27524-DF4R	-40 °C – 125 °C (1)	DFN2X2-8	M524	MSL3	4000
TPM27524-EV1R	-40 °C – 125 °C (1)	EMSOP-8	M524	MSL3	4000
TPM27524-DF6R	-40 °C – 125 °C (1)	DFN3X3-8L	M524	MSL3	4000

(1) Ambient temperature indicates device operation condition range. Application thermal behavior needs to be taken care of when operating in high temperature scenarios.

Pin Configuration and Functions

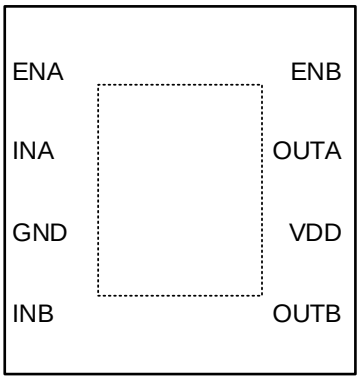
SOP-8

EMSOP-8



DFN2X2-8

DFN3X3-8



Pin Functions

Pin		I/O	Description
ENA	1	Input	Channel A Enable Input
ENB	8	Input	Channel B Enable Input
GND	3	Ground	Device Ground
INA	2	Input	Logic Input. TPM27523: Inverting Input; TPM27524: Non-inverting Input; TPM27525: Inverting Input.
INB	4	Input	Logic Input. TPM27523: Inverting Input; TPM27524: Non-inverting Input; TPM27525: Non-inverting Input.
OUTA	7	Output	Channel A Output
OUTB	5	Output	Channel B Output
VDD	6	Power	Power Supply Input

Absolute Maximum Ratings

Parameters	Rating
Power Supply Voltage, VDD	−0.3 V to 25 V
Output Voltage Range OUTA, OUTB	−0.3 V to VDD + 0.3 V –2 V to VDD + 0.3 V (200-ns pulse)
Input Voltage Range INA, INB, INA+, INA–, INB+, INB–, ENA, ENB	−5 V to 20 V
Continuous Output Channel Current OUTA, OUTB	–300 mA to 300 mA
Pulsed Output Channel Current OUTA, OUTB (500 ns)	±5 A
Operating Junction Temperature Range	–40 °C to 150 °C
Storage Temperature Range	–65 °C to 150 °C
Lead Temperature (Soldering, 10 sec)	260 °C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: Power dissipation and thermal limits must be observed.

ESD Rating

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1.5	kV

Recommended Operation Conditions

Parameters	Rating
Power Supply Voltage, VDD	4.5 V to 23 V
Input Voltage Range INA, INB, INA+, INA-, INB+, INB-, ENA, ENB	0 V to 20 V
Operating Ambient Temperature Range	–40 °C to 125 °C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP-8	122.3	60.4	°C/W
EMSOP-8	63.0	42.6	°C/W
DFN3X3-8	75	33	°C/W
DFN2X2-8	55	50	°C/W

Electrical Characteristics

All test condition is V_{DD} = 12 V, T_J = −40 °C – 150 °C, 1-µF capacitor between V_{DD} and GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(off)}$	Start-up current, based on TPM27524 circuitry	VDD = 3.4 V, INA = H, INB = H		40	100	µA
		VDD = 3.4 V, INA = L, INB = L		40	100	
V_{ON}	Supply Under Voltage Lock Out rising threshold	T_J = 25 °C	3.91	4.2	4.5	V
		T_J = −40 °C – 150 °C	3.7	4.2	4.65	
V_{OFF}	Supply Under Voltage Lock Out falling threshold	T_J = −40 °C – 150 °C	3.4	3.9	4.4	V
V_{DD_H}	Supply Under Voltage Lock Out hysteresis		0.2	0.3	0.5	V
V_{EN_H}	Enable high threshold	Enable high threshold		1.9	2.3	V
V_{EN_L}	Enable low threshold	Enable low threshold	1	1.2		V
V_{EN_HYS}	Enable hysteresis			0.7		V
V_{IN_H}	Input signal high threshold	Input high threshold		1.95	2.3	V
V_{IN_L}	Input signal low threshold	Input low threshold	1	1.25		V
V_{IN_HYS}	Input hysteresis			0.7		V
I_{OUT}	Output peak current	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±5		A
$V_{DD} - V_{OH}$	Output high voltage	I_{OUT} = −10 mA			40	mV
V_{OL}	Output low voltage	I_{OUT} = 10 mA			10	mV
R_{OH}	Output pull-up Resistance, PMOS pull-up only	I_{OUT} = −10 mA	1	1.6	3	Ω
R_{OL}	Output pull-down Resistance	I_{OUT} = 10 mA	0.15	0.5	1	Ω
t_R	Output rise-time	C_{LOAD} = 1.8 nF		7	18	ns
t_F	Output fall-time	C_{LOAD} = 1.8 nF		6	10	ns
t_M	Delay matching between OUTA and OUTB	INA = INB, OUTA and OUTB measured at 50%		1	4	ns
t_{PW}	Minimal pulse width			15	25	ns
t_{D1}	Input to output propagation delay	C_{LOAD} = 1.8 nF, 5-V INx pulse	6	13	23	ns
t_{D2}	Input to output propagation delay	C_{LOAD} = 1.8 nF, 5-V INx pulse	6	13	23	ns
t_{D3}	Enable to output propagation delay	C_{LOAD} = 1.8 nF, 5-V ENx pulse	6	13	23	ns
t_{D4}	Enable to output propagation delay	C_{LOAD} = 1.8 nF, 5-V ENx pulse	6	13	23	ns

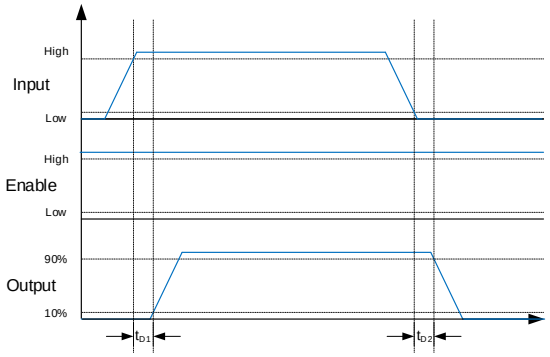


Figure 1 Input Timing Diagram

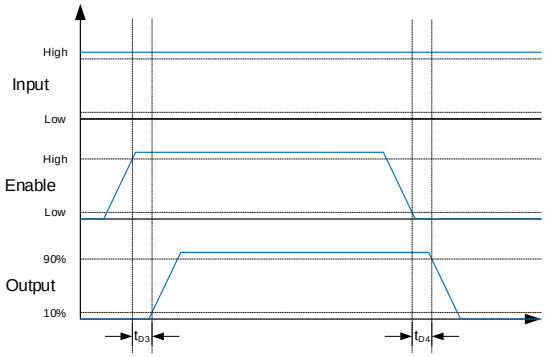


Figure 2 Enable Timing Diagram

Typical Performance Characteristics

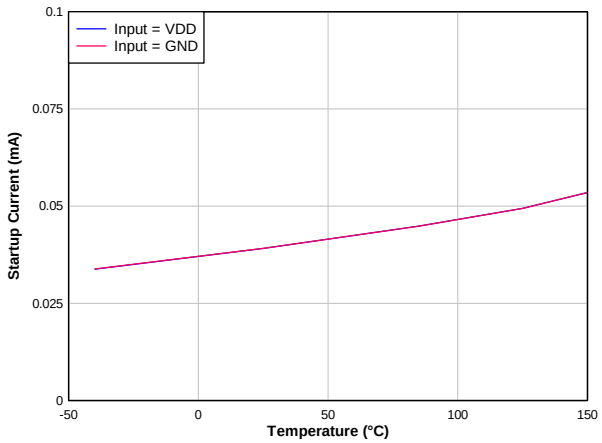


Figure 3. Start-up Current vs. Temperature

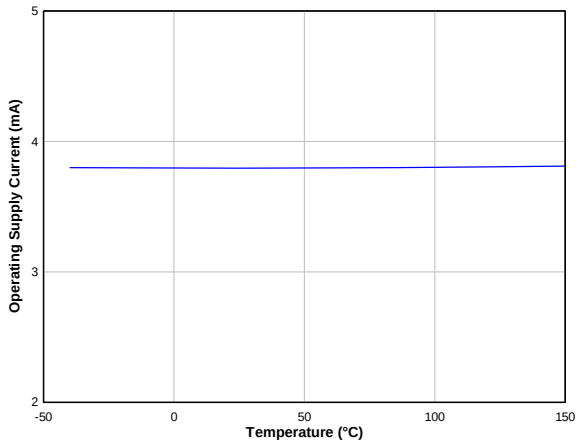


Figure 4. Operating Current vs Ambient Temperature

f = 500 kHz, C_L = 500 pF, V_{DD} = 12 V

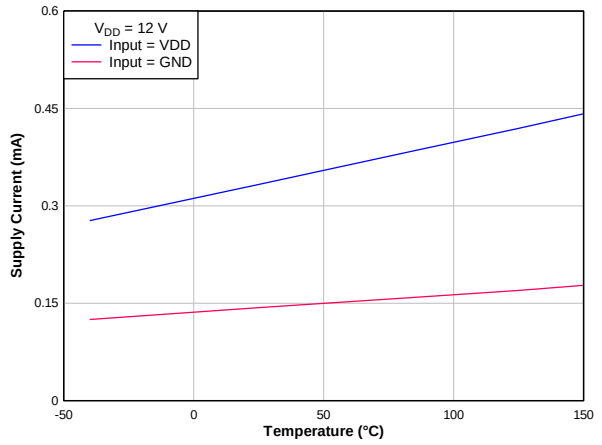


Figure 5. Supply Current vs Temperature (On/Off)

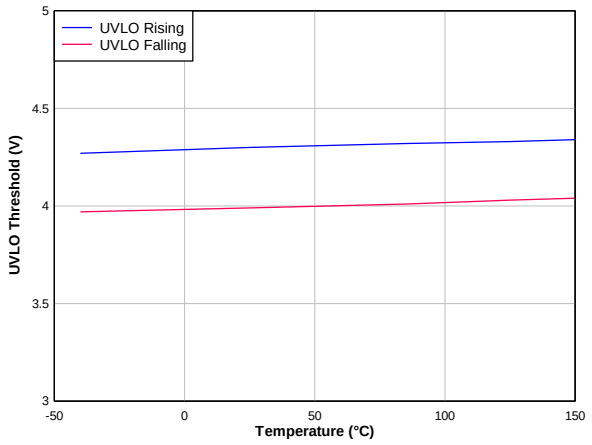


Figure 6. UVLO Threshold vs Temperature

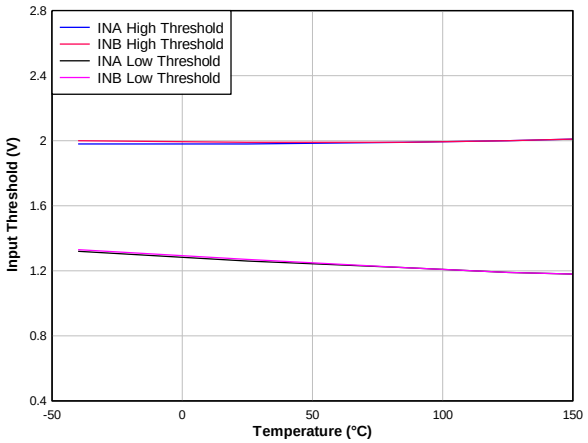


Figure 7. Input Threshold vs Temperature

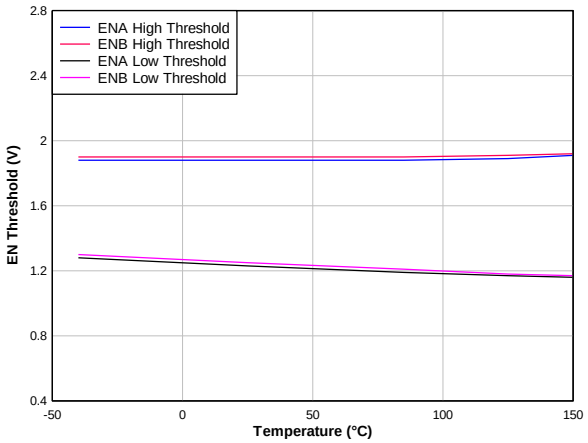


Figure 8. Enable Threshold vs Temperature

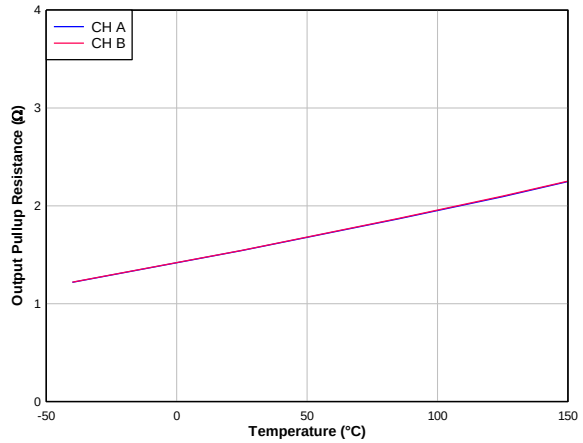


Figure 9. Output Pull-up Resistance vs Temperature

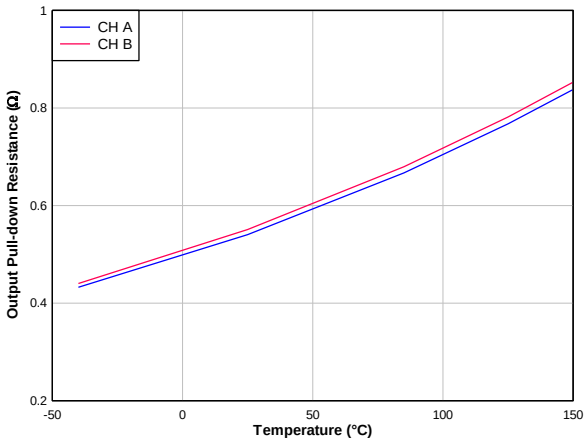


Figure 10. Output Pull-down Resistance vs Temperature

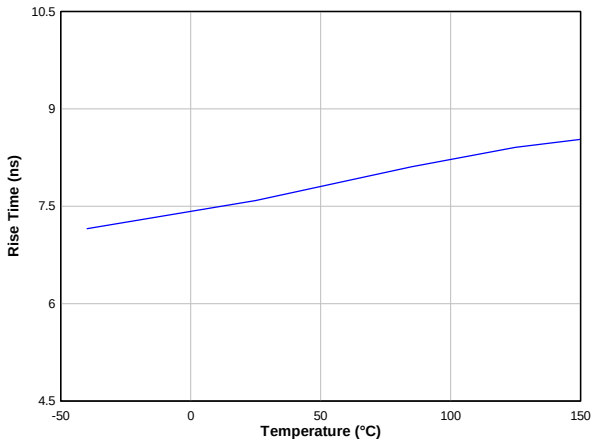


Figure 11. Rise-time vs Temperature

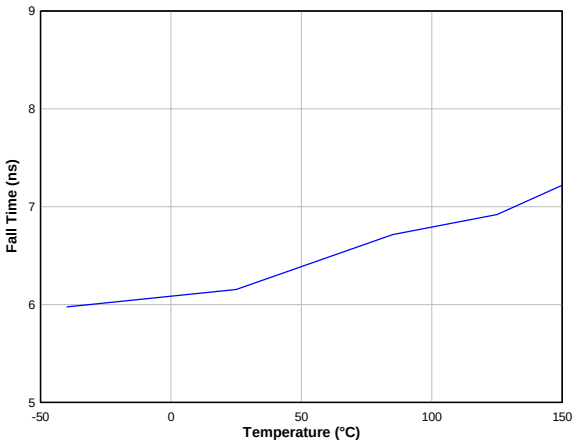


Figure 12. Fall-time vs Temperature

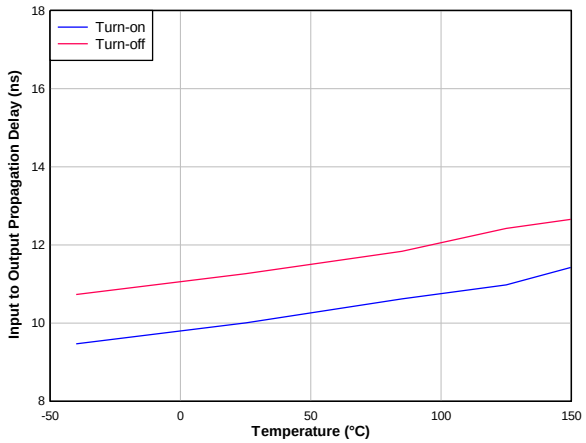


Figure 13. Input to Output Propagation Delay vs Temperature

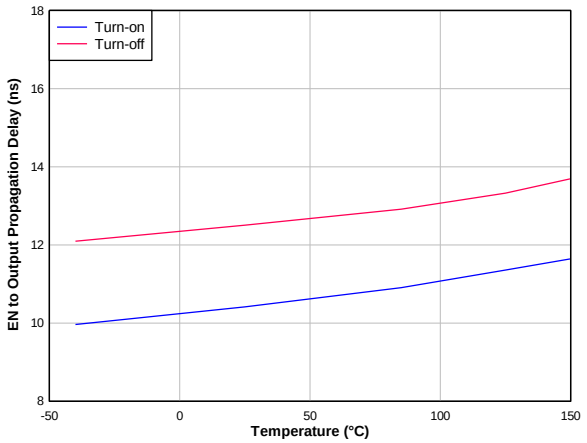


Figure 14. Enable to Output Propagation Delay vs Temperature

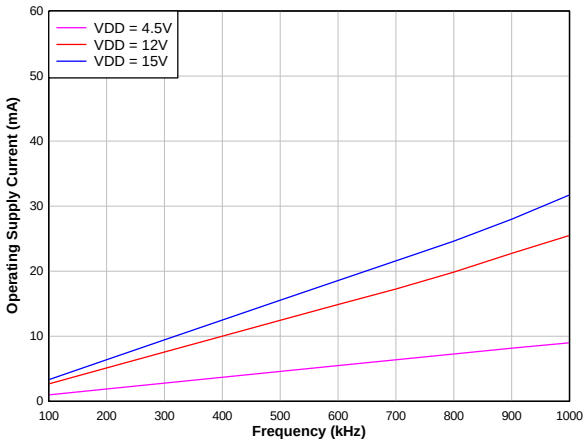


Figure 15. Operating Supply Current vs Frequency

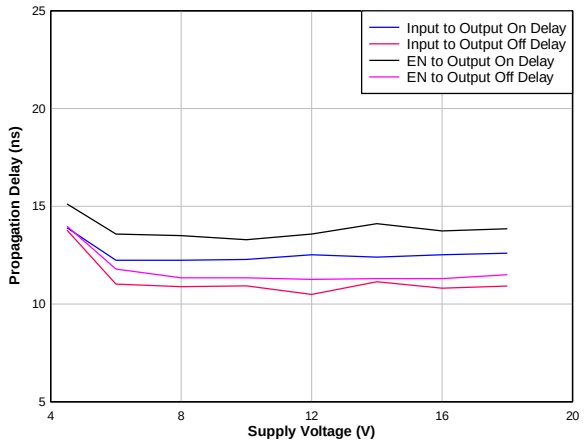


Figure 16. Propagation Delay vs Supply Voltage

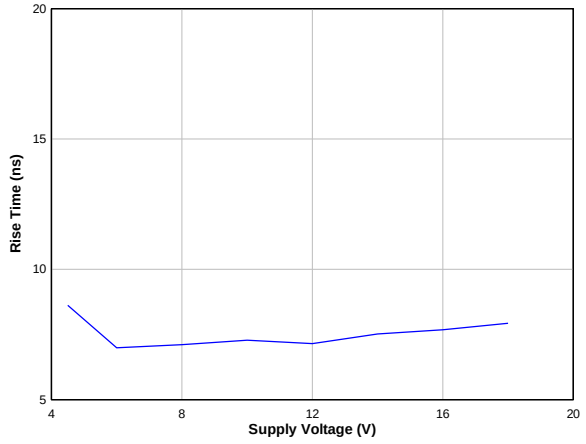


Figure 17. Rise-time vs Supply Voltage

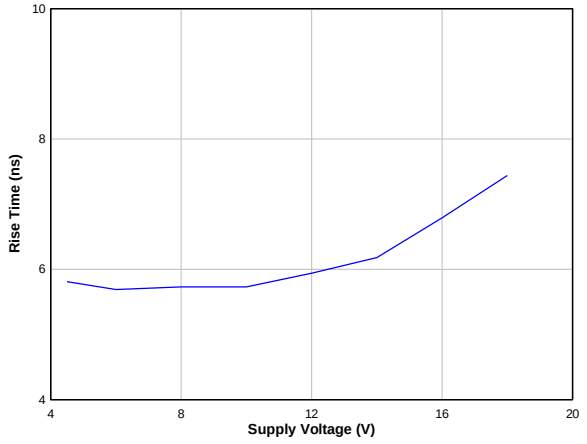


Figure 18. Fall-time vs Supply Voltage

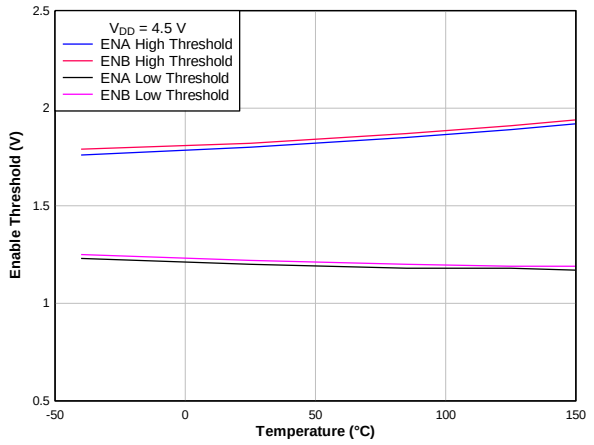


Figure 19. Enable Threshold vs Temperature

VDD = 4.5 V

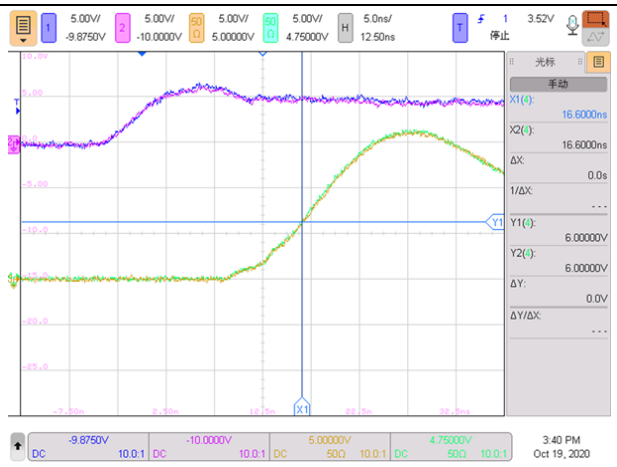


Figure 20. Rising Edge

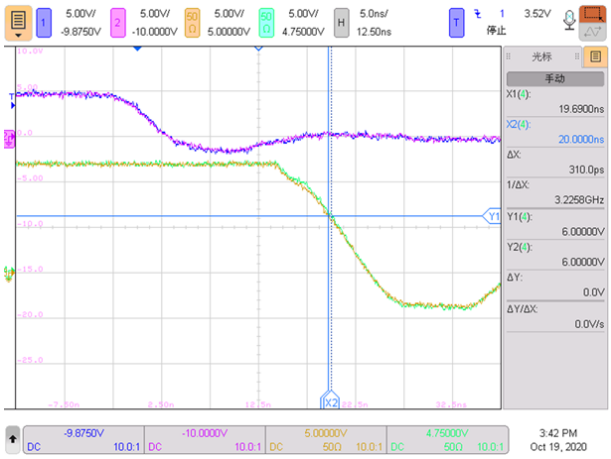


Figure 21. Falling Edge

Detailed Description

Overview

TPM2752x series of dual-channel low-side gate drivers are designed for high performance power supplies, motor controls and inverters. Designed with industrial standard pin-out and package, TPM2752x accelerates design process. With extended voltage ranges on supply voltage and negative input voltage on inputs, TPM2752x improves system level reliability. 5-A Strong driving capability improves gate driver efficiency and lowers heat generation, especially in high-frequency switching applications.

Functional Block Diagram

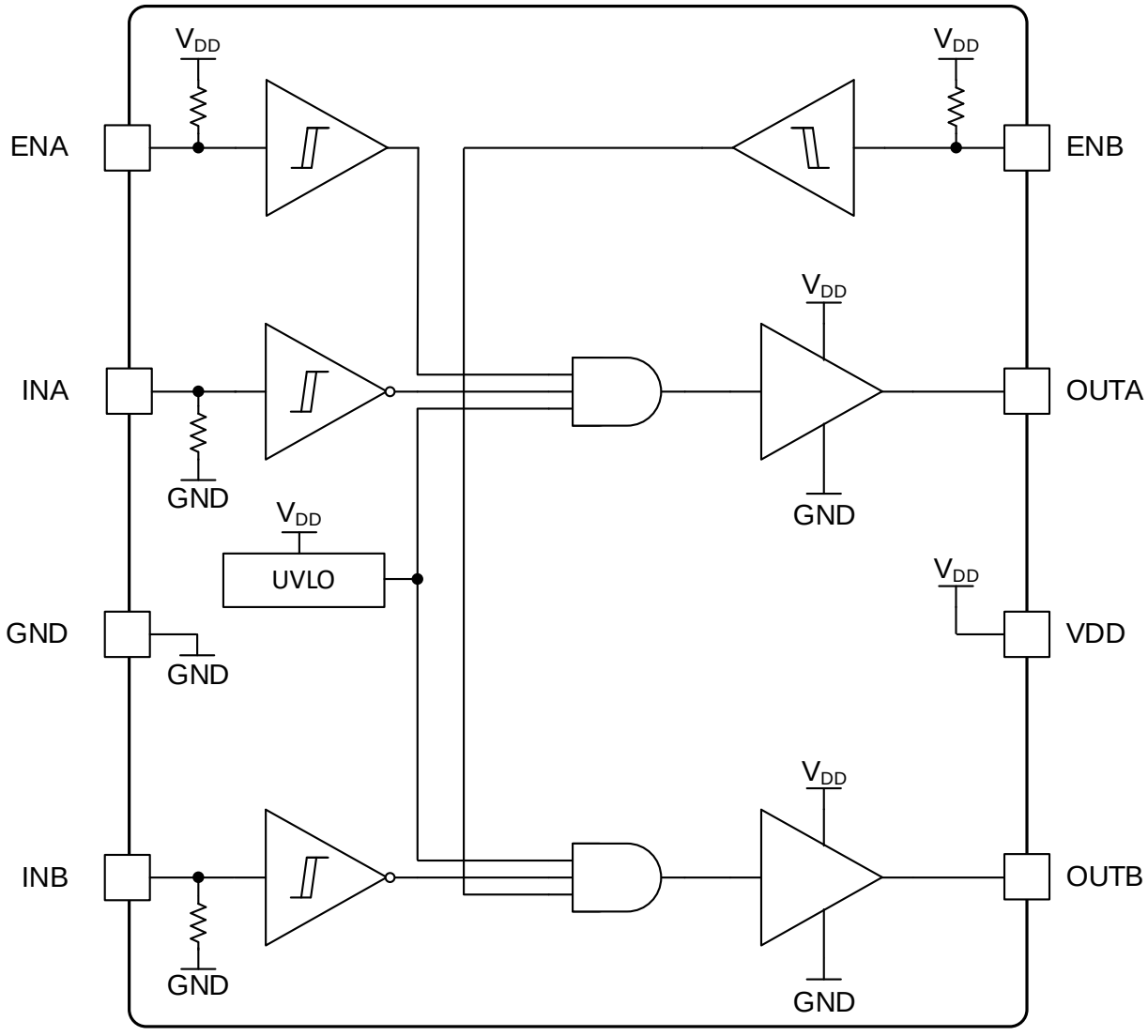


Figure 22 Functional Block Diagram

Feature Description

Low Propagation Delay Driver Outputs

The low-propagation-delay design allows the device to achieve industrial leading low propagation delay between inputs and outputs. The low delay enhances driver performance in high frequency switching regulators. Matching between two channels are optimized to support parallel driving. 3PEAK recommends tying IN1 and IN2 locally together with high input slew rate, to avoid shoot-through between the two well-matched channels. Capacitors are not recommended on IN1 and IN2 nodes when used in parallel.

Supply and UVLO

The device monitors supply voltage with under-voltage lock-out (UVLO). When supply voltage is below UVLO threshold, the outputs are held low in UVLO to avoid glitches during power rising and falling.

The device quiescent current and operating current are measured as shown in Figure 5. The current is related to internal quiescent current consumption as well as output current. The output current can be calculated using external transistor gate charge times switching frequency f_{sw}.

Channel Input

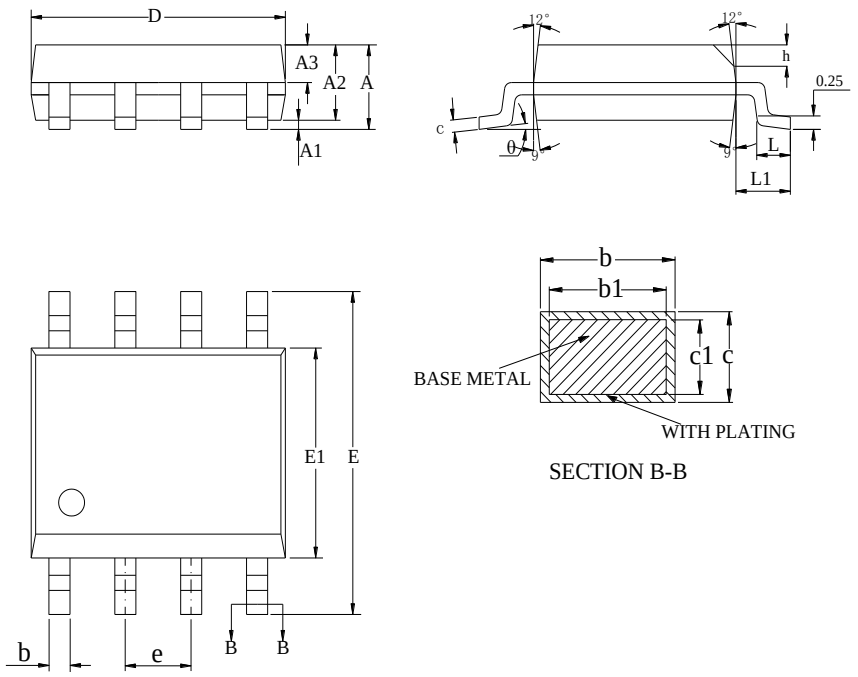
The input of TPM2752x gate drivers supports TTL and CMOS input with threshold voltage independent of supply voltage. The threshold is also designed as temperature independent to support wide range of ambient temperature. Wide hysteresis enhances system level noise immunity. The integrated pull-down resistors set the device in low state when inputs are floating.
Inputs can withstand DC −5V, to improve robustness on ground bouncing.

Output Stage

The TPM2752x output stage is able to deliver high current sourcing and sinking up to 5-A with low propagation delay. The delay matching between dual channels are also optimized within 1-ns.
In the case of higher output driving capabilities needed, TPM2752x could allow paralleling the dual channel to achieve higher driving current. In this case, it is recommended to use high slew rate on IN1 and IN2 and connect IN1 and IN2 together to avoid shoot through between channels.

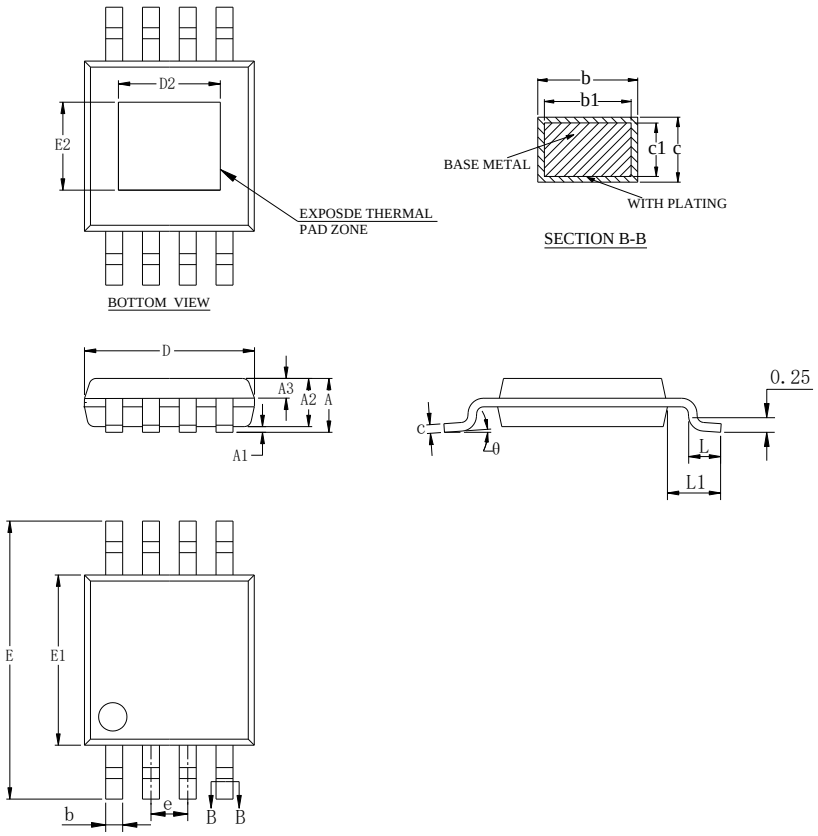
Package Outline Dimensions

SOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05 REF		
θ	0	—	8°

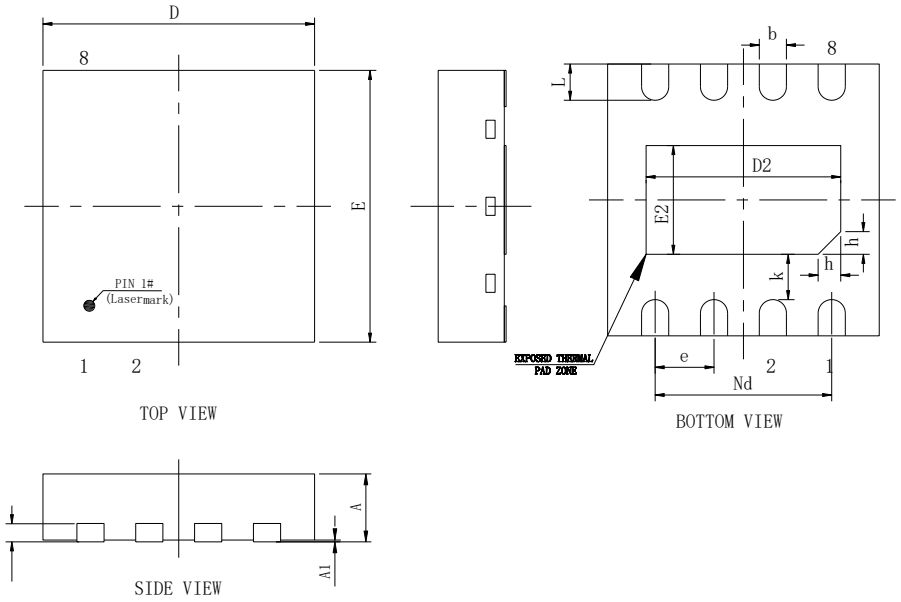
EMSOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

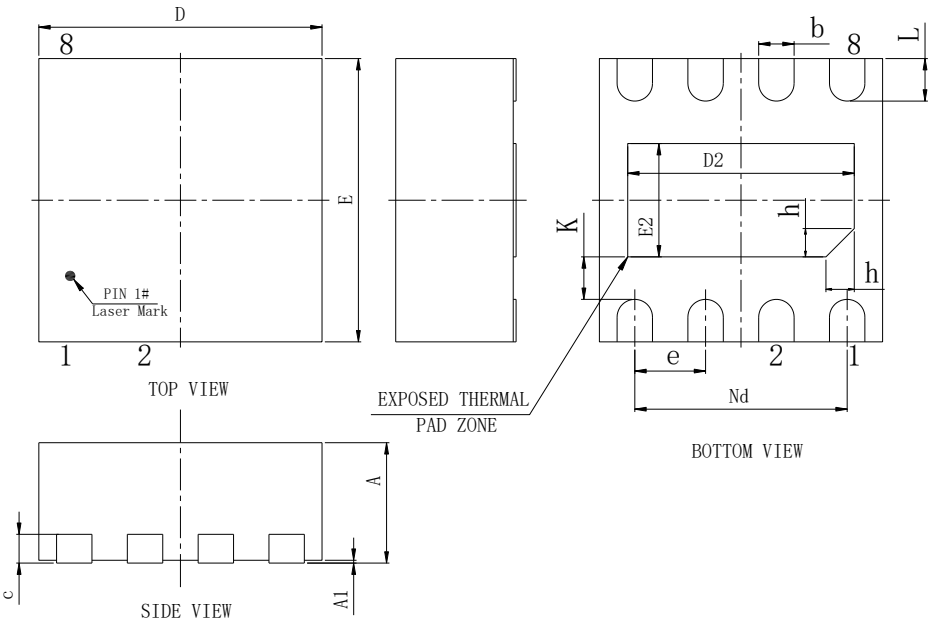
L/F Size (mil) \ Size(mm)	D2	E2
71*71	1.80REF	1.55REF

DFN3X3-8

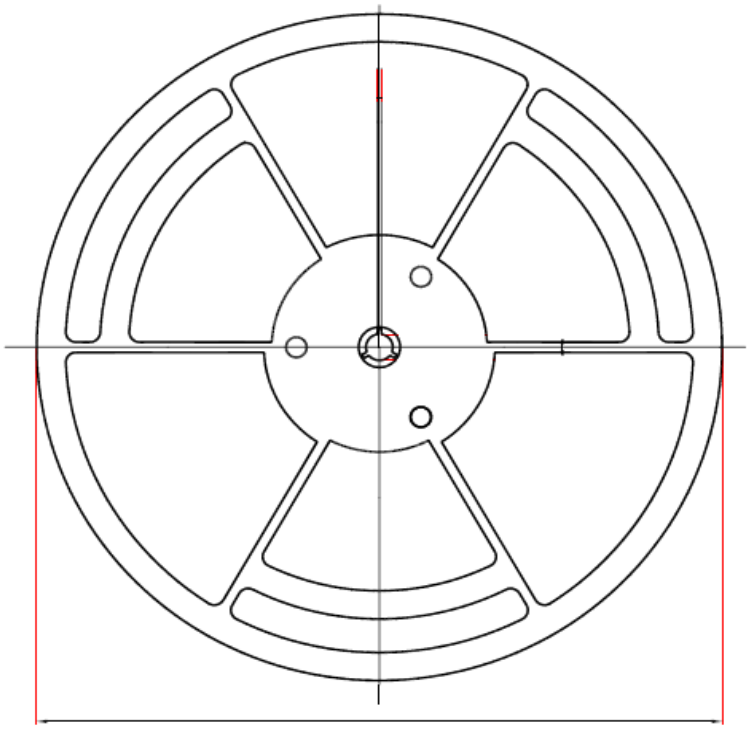


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.25	0.30	0.35
c	0.203REF		
D	2.90	3.00	3.10
D2	2.05	2.15	2.25
Nd	1.95BSC		
E	2.90	3.00	3.10
E2	1.10	1.20	1.30
e	0.65BSC		
K	0.50REF		
L	0.35	0.40	0.45
h	0.20	0.25	0.30

DFN2X2-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	1.95	2.00	2.05
D2	1.55	1.60	1.65
N d	1.50BSC		
e	0.50BSC		
E	1.95	2.00	2.05
E2	0.75	0.80	0.85
L	0.25	0.30	0.35
K	0.25	0.30	0.35
h	0.20REF		



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0(mm)	Pin1 Quadrant
TPM27523-SO1R	SOP-8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TPM27524-SO1R	SOP-8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TPM27525-SO1R	SOP-8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TPM27526-SO1R	SOP-8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TPM27524-DF4R	DFN2X2-8	180.0	13.1	2.3	2.3	1.1	4.0	8.0	Q1
TPM27524-EV1R	EMSOP-8	330.0	17.6	5.2	3.3	1.5	8.0	12.0	Q1
TPM27524-DF6R	DFN3X3-8	330.0	17.6	3.3	3.3	1.1	8.0	12.0	Q1