SGM8212-1/SGM8212-2
Low Noise, High Voltage Operational Amplifiers

GENERAL DESCRIPTION

The SGM8212-1/2 are low noise operational amplifiers which can operate from ±1.35V to ±18V dual power supplies or from 2.7V to 36V single supply. These devices are available in micro-packages and offer low offset and wide bandwidth with low quiescent current. The single and dual versions all have identical specifications for maximum design flexibility.

The SGM8212-1/2 can operate with full rail-to-rail input 100mV beyond the rail, but with reduced performance within 2V of the top rail.

The single SGM8212-1 is available in Green SOT-553-5, SOT-23-5 and SOIC-8 packages. The dual SGM8212-2 is available in Green SOIC-8 and TDFN-3×3-8L packages. The SGM8212-1/2 are specified over the extended -40℃ to +125℃ temperature range.

FEATURES

- **Support Single or Dual Power Supplies: 2.7V to 36V or ±1.35V to ±18V**
- **Low Noise: 15nV/$\sqrt{Hz}$ at 1kHz**
- **Input Offset Voltage: 1.8mV (MAX)**
- **Rail-to-Rail Input and Output**
- **Gain-Bandwidth Product: 2.5MHz**
- **Unity-Gain Stable**
- **Phase Margin: 60° for G = 1 and C_L = 10pF**
- **Low Quiescent Current: 475μA/Amplifier**
- **High CMRR: 98dB (TYP)**
- **Low Input Bias Current: 5pA (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM8212-1 Available in Green SOT-553-5, SOT-23-5 and SOIC-8 Packages
  SGM8212-2 Available in Green SOIC-8 and TDFN-3×3-8L Packages

APPLICATIONS

Tracking Amplifiers in Power Modules
Merchant Power Supplies
Transducer Amplifiers
Bridge Amplifiers
Temperature Measurements
Strain Gauge Amplifiers
Precision Integrators
Battery-Powered Instruments
Test Equipment

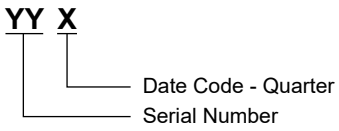
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8212-1	SOT-553-5	-40℃ to +125℃	SGM8212-1XKB5G/TR	MFX	Tape and Reel, 4000
	SOT-23-5	-40℃ to +125℃	SGM8212-1XN5G/TR	R12XX	Tape and Reel, 3000
	SOIC-8	-40℃ to +125℃	SGM8212-1XS8G/TR	SGM 82121XS8 XXXXX	Tape and Reel, 4000
SGM8212-2	SOIC-8	-40℃ to +125℃	SGM8212-2XS8G/TR	SGM 82122XS8 XXXXX	Tape and Reel, 4000
	TDFN-3×3-8L	-40℃ to +125℃	SGM8212-2XTDB8G/TR	SGM 82122DB XXXXX	Tape and Reel, 4000

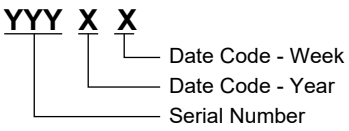
MARKING INFORMATION

NOTE: X = Date Code. XX = Date Code. XXXXX = Date Code, Trace Code and Vendor Code.

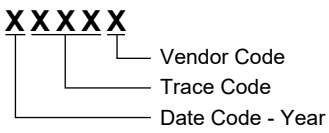
SOT-553-5



SOT-23-5



SOIC-8/TDFN-3×3-8L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 40V
Input/Output Voltage Range..... $(-V_S)$ - 0.3V to $(+V_S)$ + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM (SGM8212-1) 2500V
HBM (SGM8212-2) 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

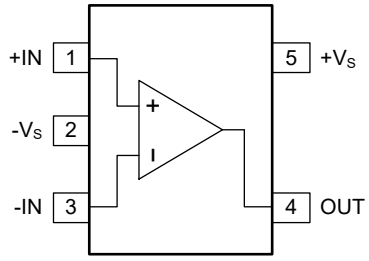
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

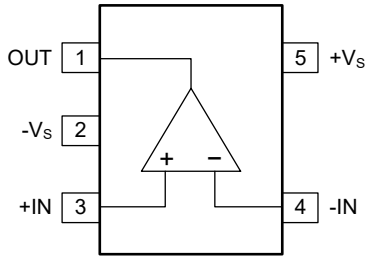
PIN CONFIGURATIONS

SGM8212-1 (TOP VIEW)



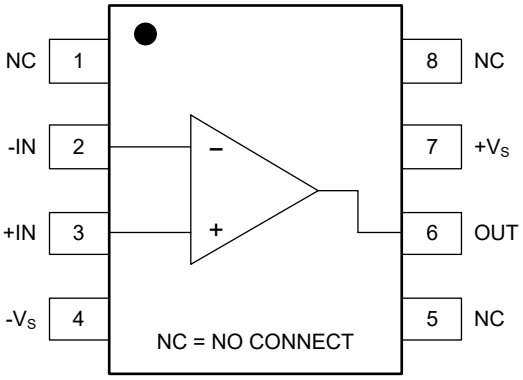
SOT-553-5

SGM8212-1 (TOP VIEW)



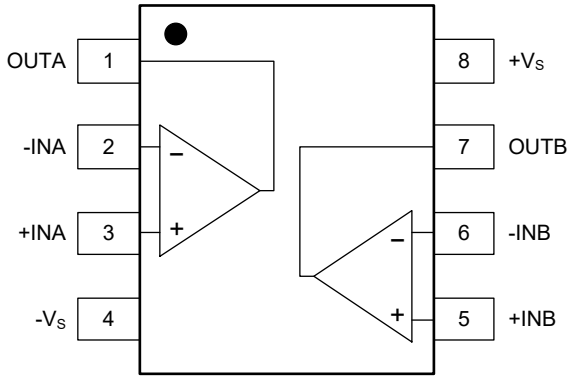
SOT-23-5

SGM8212-1 (TOP VIEW)



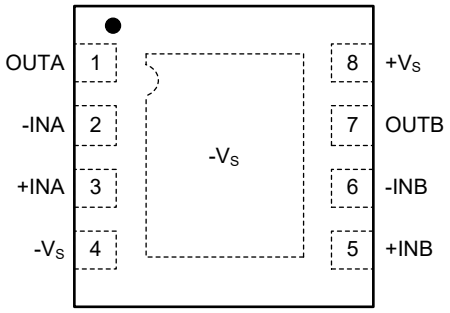
SOIC-8

SGM8212-2 (TOP VIEW)



SOIC-8

SGM8212-2 (TOP VIEW)



TDFN-3×3-8L

NOTE: For the TDFN-3×3-8L package, connect the exposed pad to $-V_S$ or leave it unconnected.

ELECTRICAL CHARACTERISTICS

(At T_A = +25℃, V_S = ±1.35V to ±18V, R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V_{OS}	V_{CM} = 0V	+25℃		0.4	1.8	mV
			Full			2	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		1.1		μV/℃
Input Bias Current	I_B	V_{CM} = 0V	+25℃		±5	±120	pA
Input Offset Current	I_{OS}	V_{CM} = 0V	+25℃		±5	±120	pA
Maximum Differential Input Voltage	$\lvert V_{ID}\rvert$		Full			V_S	V
Maximum Input Difference Bias Current	$\lvert I_{ID}\rvert$	V_S = ±18V, V_{ID} = ±18V	+25℃		2	3	μA
			Full			4	
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S)$ - 0.1		$(+V_S)$ + 0.1	V
Common Mode Rejection Ratio	CMRR	V_S = ±2V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ + 0.1V	+25℃	63	80		dB
			Full	60			
		V_S = ±2V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ - 2V	+25℃	78	94		
			Full	75			
		V_S = ±18V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ + 0.1V	+25℃	83	98		
			Full	80			
		V_S = ±18V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ - 2V	+25℃	100	115		
			Full	97			
Open-Loop Voltage Gain	A_{OL}	V_S = ±2V, $(-V_S)$ + 0.35V < V_{OUT} < $(+V_S)$ - 0.35V	+25℃	103	130		dB
			Full	100			
		V_S = ±18V, $(-V_S)$ + 0.35V < V_{OUT} < $(+V_S)$ - 0.35V	+25℃	123	140		
			Full	120			
Output Characteristics							
Output Voltage Swing from Rail	V_{OUT}	V_S = ±18V	+25℃		110	150	mV
			Full			240	
Output Short-Circuit Current	I_{SC}	V_S = ±18V	+25℃	±16	±30		mA
Power Supply							
Operating Voltage Range	V_S		Full	2.7		36	V
Quiescent Current/Amplifier	I_Q	I_{OUT} = 0A	+25℃		475	600	μA
			Full			680	
Power Supply Rejection Ratio	PSRR	V_S = 4V to 36V	+25℃	103	120		dB
			Full	100			

ELECTRICAL CHARACTERISTICS (continued)

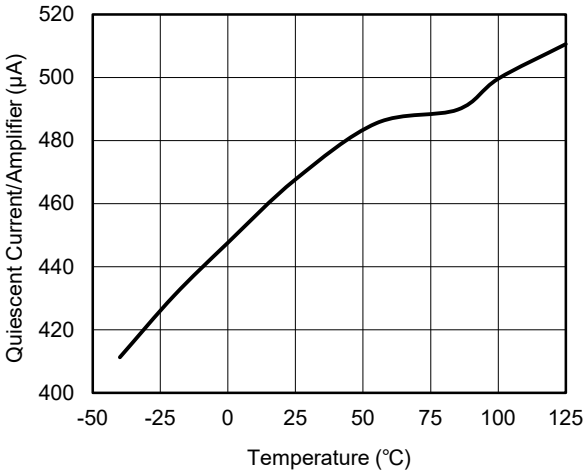
(At T_A = +25℃, V_S = ±1.35V to ±18V, R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Dynamic Performance							
Gain-Bandwidth Product	GBP	C_L = 10pF	+25℃		2.5		MHz
Phase Margin	φ_O	C_L = 10pF	+25℃		60		°
Slew Rate	SR	V_S = ±2V to ±18V, G = +1	+25℃		1.5		V/μs
Settling Time to 0.1%	t_S	V_S = ±18V, G = +1, 10V step	+25℃		15		μs
Overload Recovery Time	ORT	V_{IN} × G > V_S	+25℃		2		μs
Total Harmonic Distortion + Noise	THD+N	V_S = 36V, V_{OUT} = $3V_{RMS}$, f = 1kHz, G = +1	+25℃		0.0002		%
Noise							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		2.5		μV_{P-P}
Input Voltage Noise Density	e_n	f = 100Hz	+25℃		25		$nV/\sqrt{Hz}$
		f = 1kHz	+25℃		15		
Input Current Noise Density	i_n	f = 1kHz	+25℃		300		$fA/\sqrt{Hz}$

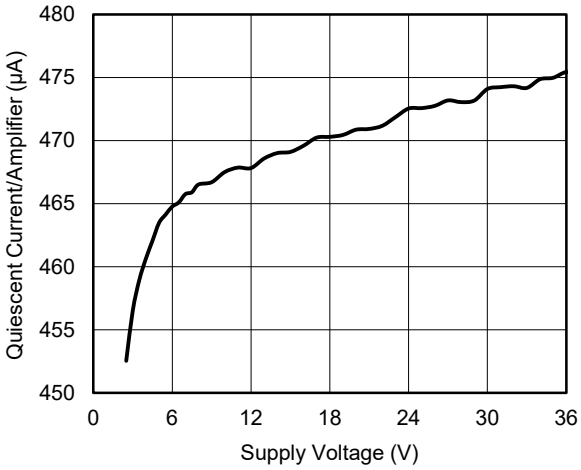
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = ±18V, R_L = 10kΩ, unless otherwise noted.

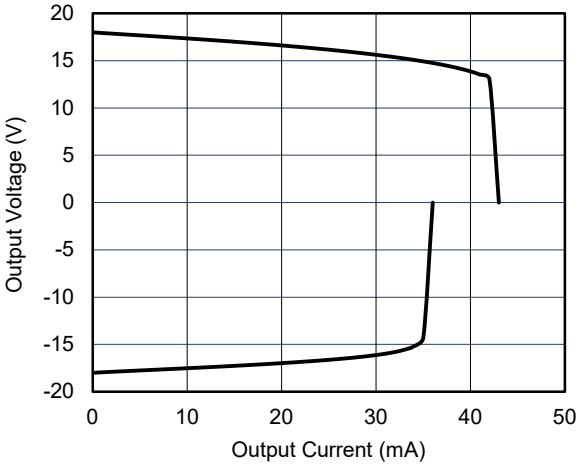
Quiescent Current vs. Temperature



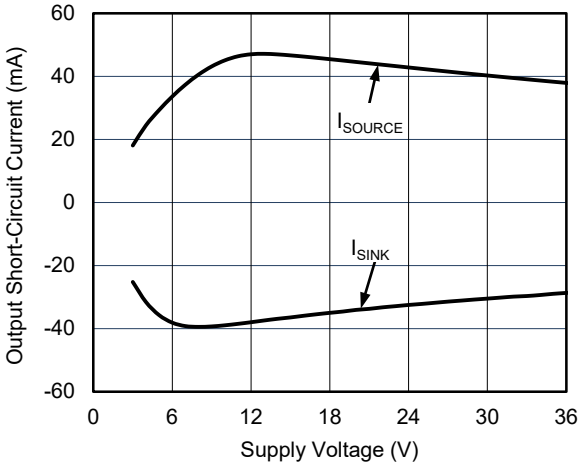
Quiescent Current vs. Supply Voltage



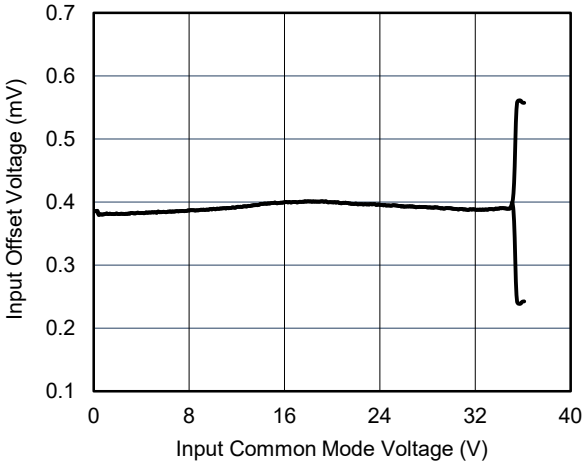
Output Voltage vs. Output Current



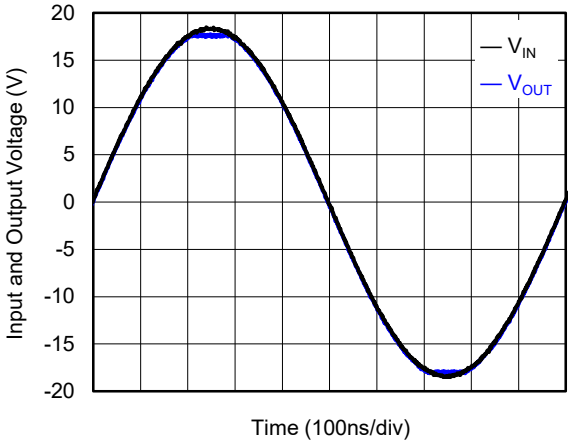
Output Short-Circuit Current vs. Supply Voltage



Input Offset Voltage vs. Input Common Mode Voltage



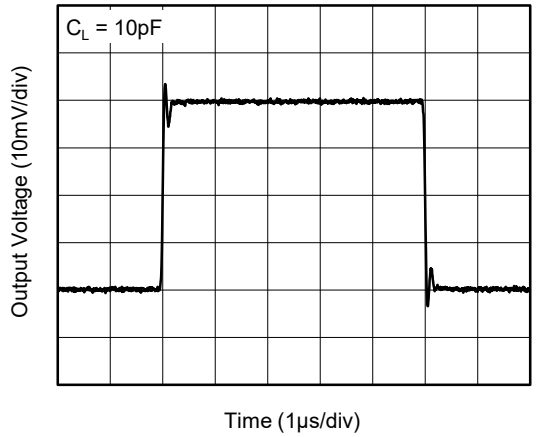
No Phase Reversal



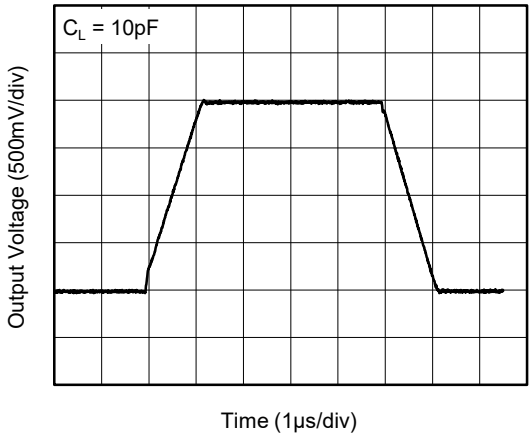
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±18V, R_L = 10kΩ, unless otherwise noted.

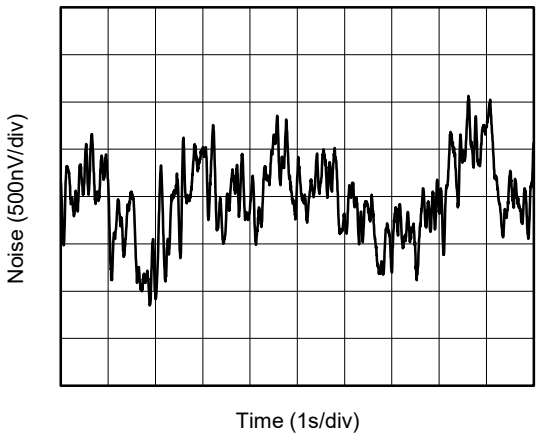
Small-Signal Step Response



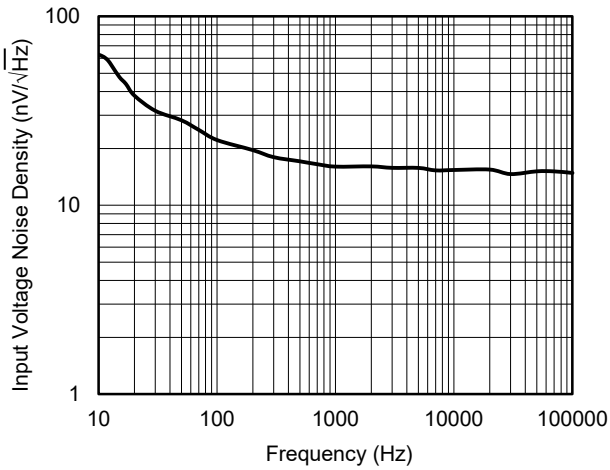
Large-Signal Step Response



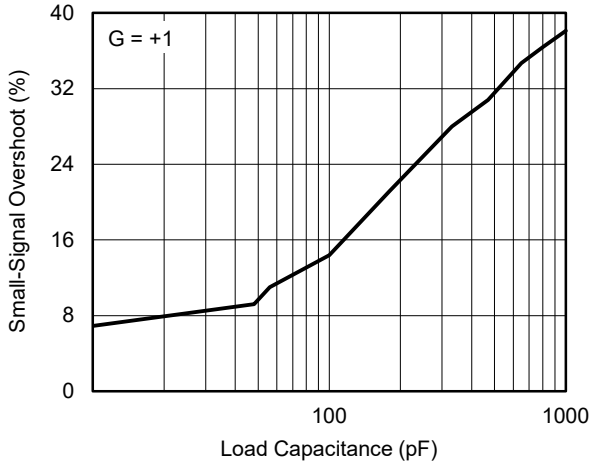
0.1Hz to 10Hz Input Voltage Noise



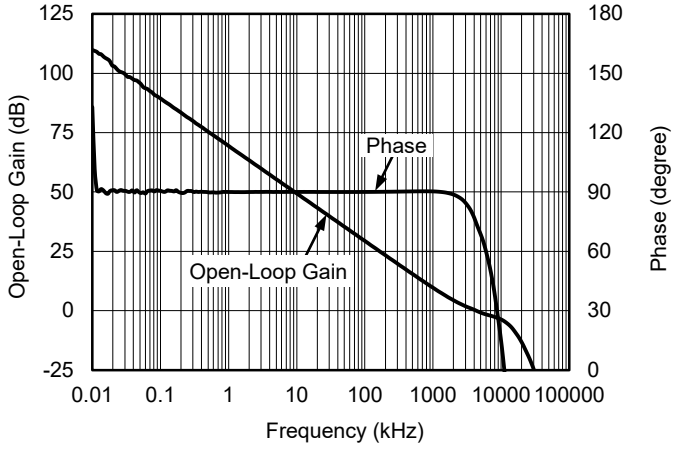
Input Voltage Noise Density vs. Frequency



Small-Signal Overshoot vs. Capacitive Load



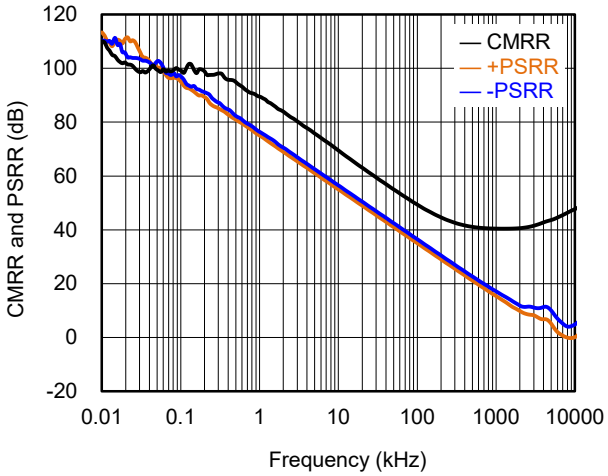
Open-Loop Gain and Phase vs. Frequency



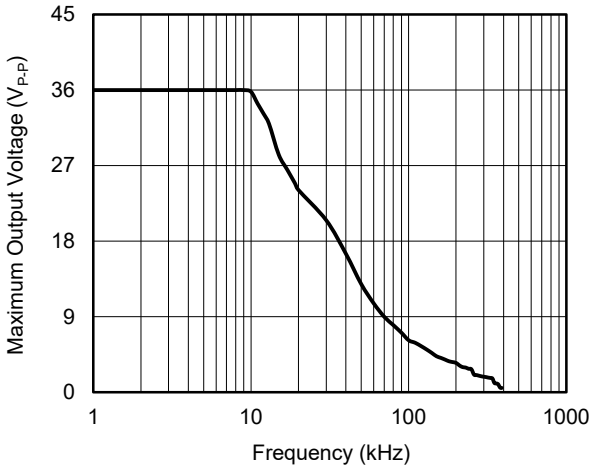
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±18V, R_L = 10kΩ, unless otherwise noted.

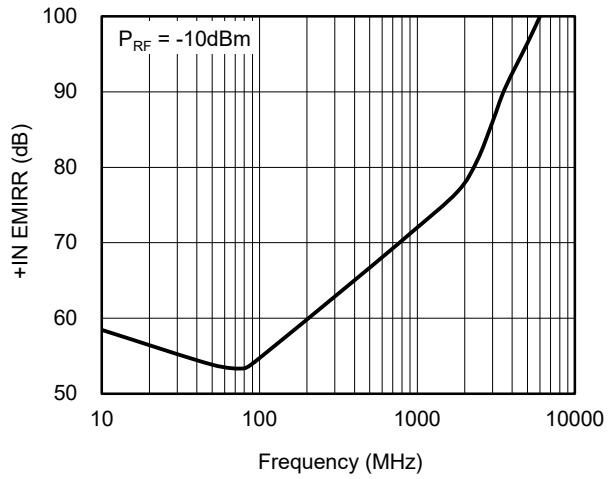
CMRR and PSRR vs. Frequency



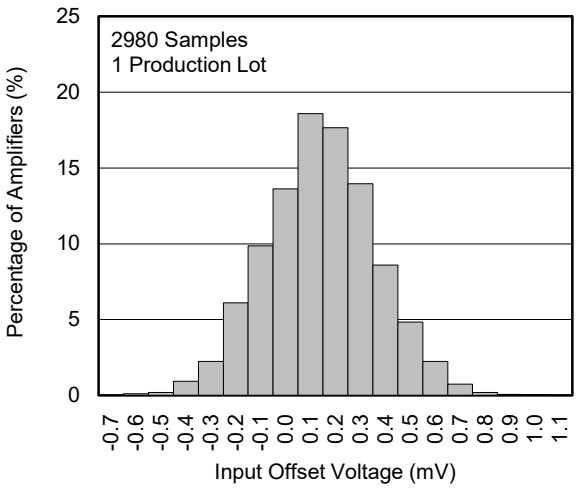
Maximum Output Voltage vs. Frequency



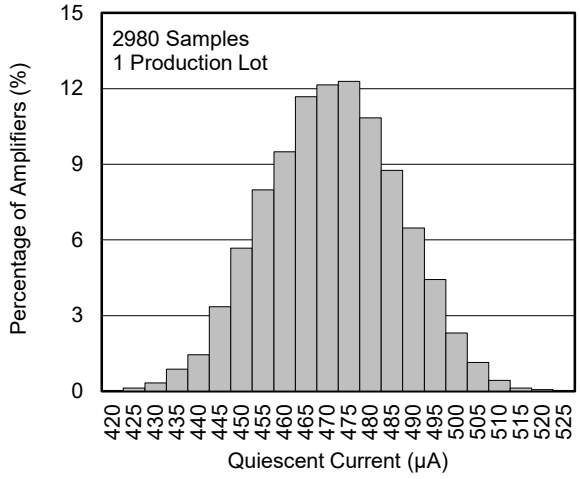
+IN EMIRR vs. Frequency



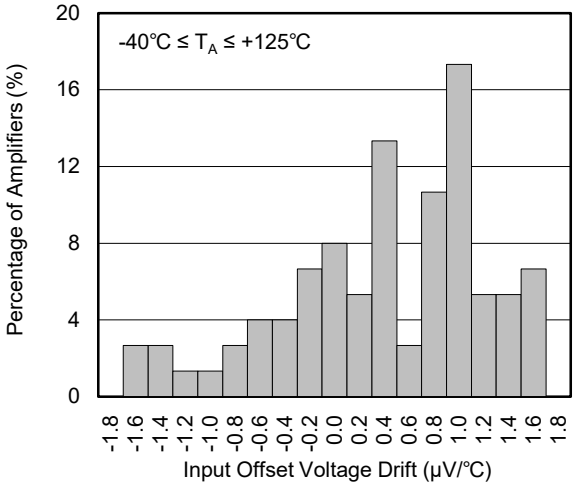
Input Offset Voltage Production Distribution



Quiescent Current Production Distribution



Input Offset Voltage Drift Distribution



APPLICATION NOTES

Rail-to-Rail Input

The input common mode voltage range of the SGM8212-1/2 extends 100mV beyond the supply rails for the full supply voltage range of 2.7V to 36V. Diodes between the inputs and the supply rails keep the input voltage from exceeding the rails.

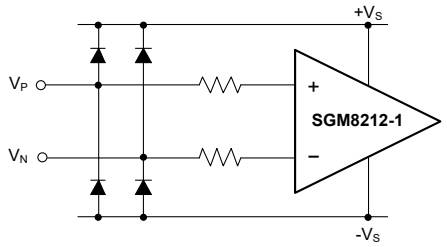


Figure 1. Equivalent Input Circuit

Input Protection

The SGM8212-1/2 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power supply pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10mA. Figure 2 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

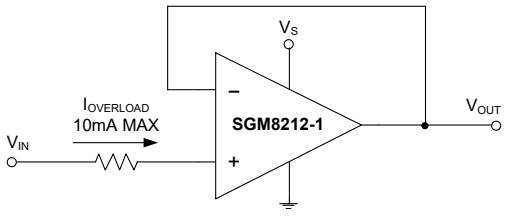


Figure 2. Input Current Protection

Rail-to-Rail Output

The minimum output voltage will be within millivolts of ground for single-supply operation where the load is referenced to ground ($-V_S$). With a 36V supply and the load tied to ground, the typical output swings from 0.11V to 35.89V.

Driving Capacitive Loads

The SGM8212-1/2 are unity-gain stable for capacitive load up to 300pF. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load (Figure 3). Note that this alternative results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD}.

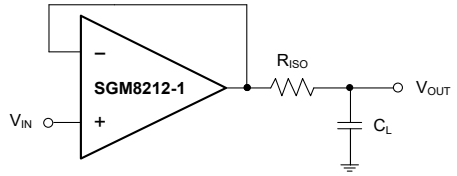


Figure 3. Using Isolation Resistor to Improve Stability when Driving Heavy Capacitive Load

Power Supply Bypassing and Layout

Power supply pins are actually inputs to the amplifiers. Care must be taken to provide the amplifiers with a clean, low noise DC voltage source.

Power supply bypassing is employed to provide a low impedance path to ground for noise and undesired signals at all frequencies. This cannot be achieved with a single capacitor type; but with a variety of capacitors in parallel, the bandwidth of power supply bypassing can be greatly extended. The bypass capacitors have two functions:

1. Provide a low impedance path for noise and undesired signals from the supply pins to ground.

2. Provide local stored charge for fast switching conditions and minimize the voltage drop at the supply pins during transients. This is typically achieved with large electrolytic capacitors.

APPLICATION NOTES (continued)

Good quality ceramic chip capacitors should be used and always kept as close as possible to the amplifier package. A parallel combination of a 0.1μF ceramic and a 10μF electrolytic covers a wide range of rejection for unwanted noise. The 10μF capacitor is less critical for high frequency bypassing, and in most cases, one per supply line is sufficient. The values of capacitors are circuit-dependent and should be determined by the system's requirements.

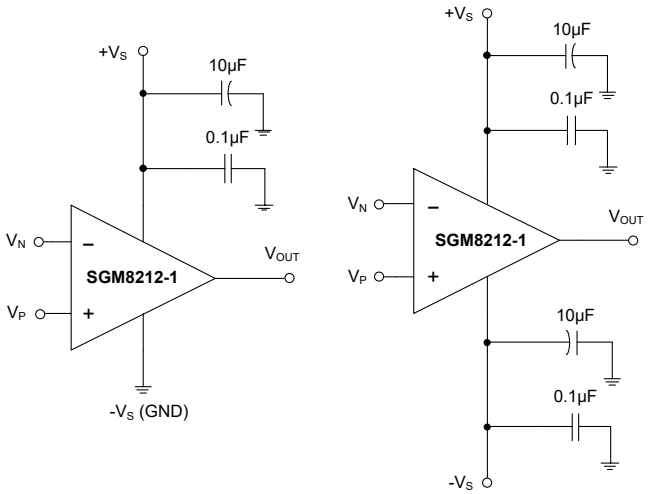


Figure 4. Amplifier with Bypass Capacitors

Grounding

Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes.

A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.

Input-to-Output Coupling

To minimize capacitive coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace. This helps reduce unwanted positive feedback.

TYPICAL APPLICATION CIRCUITS

Difference Amplifier

The circuit shown in Figure 5 performs the difference function. If the resistor ratios are equal ($R_4/R_3 = R_2/R_1$), then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

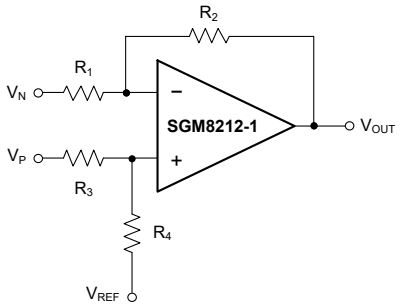


Figure 5. Difference Amplifier

High Input Impedance Difference Amplifier

The circuit in Figure 6 performs the same function as that in Figure 5 but with a high input impedance.

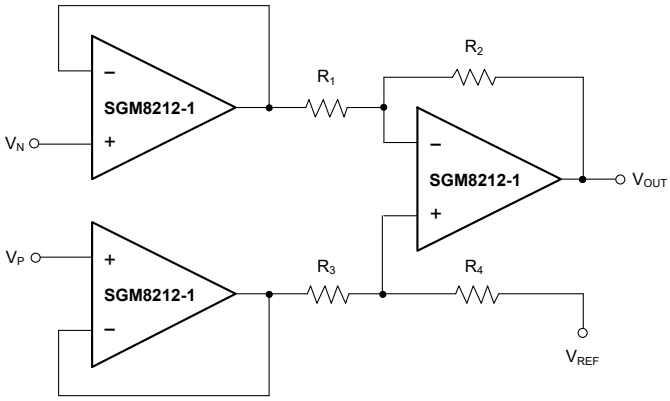


Figure 6. High Input Impedance Difference Amplifier

Active Low-Pass Filter

The low-pass filter shown in Figure 7 has a DC gain of $(-R_2/R_1)$ and the -3dB corner frequency is $1/2\pi R_2C$. Make sure the filter bandwidth is within the bandwidth of the amplifier. Feedback resistors with large values can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistor values as low as possible and consistent with output loading consideration.

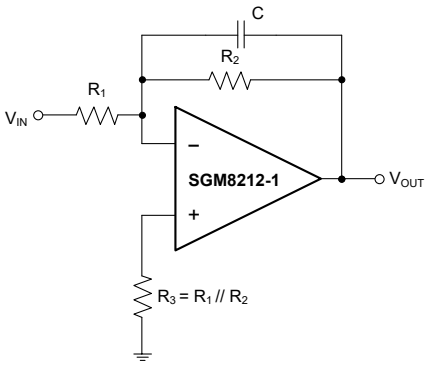


Figure 7. Active Low-Pass Filter

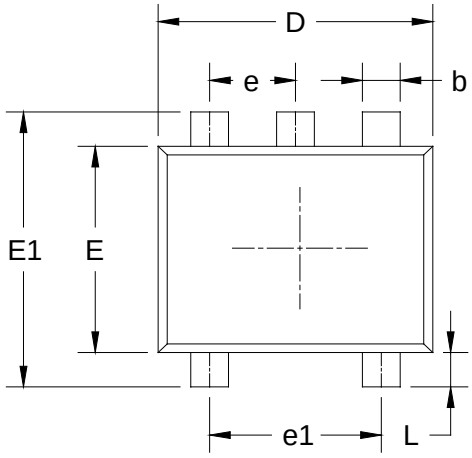
REVISION HISTORY

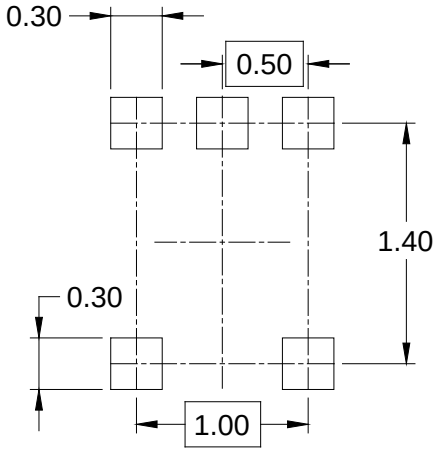
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2020) to REV.A	Page
Changed from product preview to production data	All

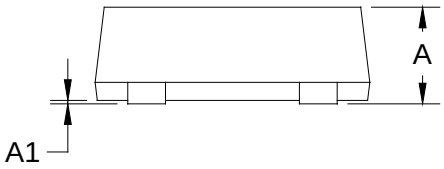
PACKAGE OUTLINE DIMENSIONS

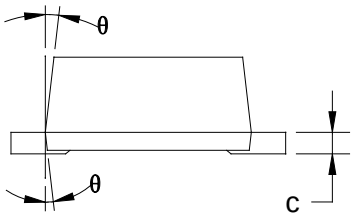
SOT-553-5





RECOMMENDED LAND PATTERN (Unit: mm)

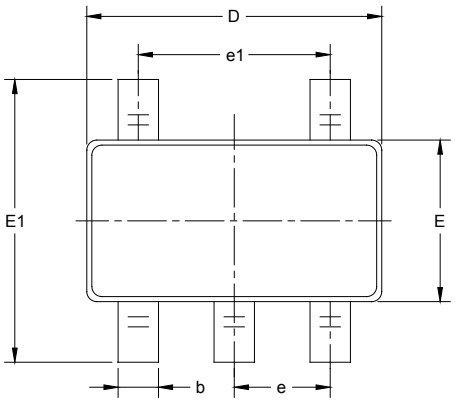


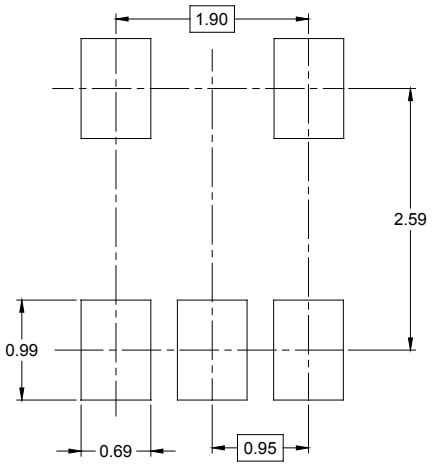


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.160	0.004	0.006
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
e	0.500 TYP		0.020 TYP	
e1	1.000 TYP		0.040 TYP	
L	0.100	0.300	0.004	0.012
θ	7° REF		7° REF	

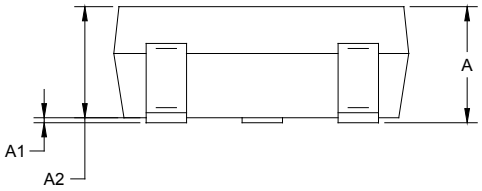
PACKAGE OUTLINE DIMENSIONS

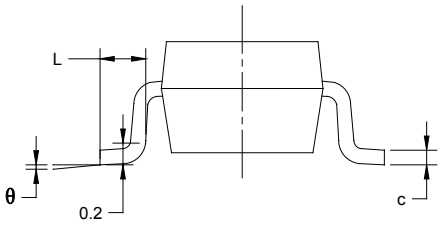
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)

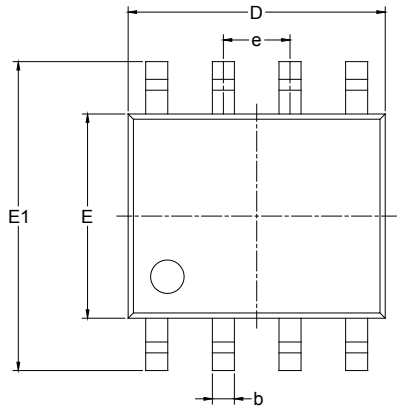


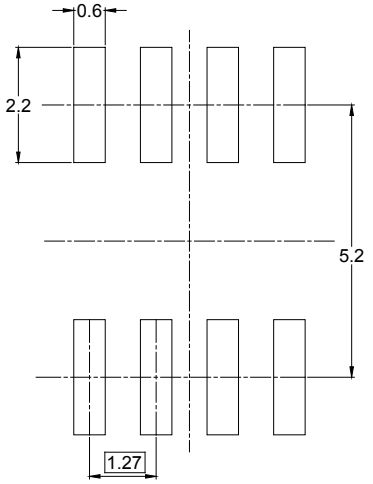


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

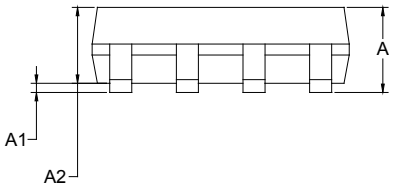
PACKAGE OUTLINE DIMENSIONS

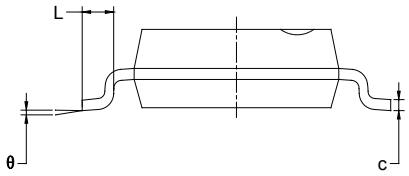
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

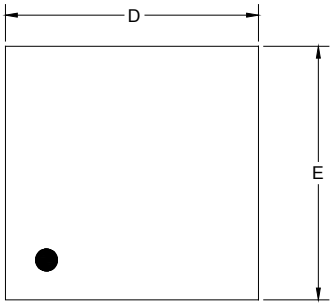




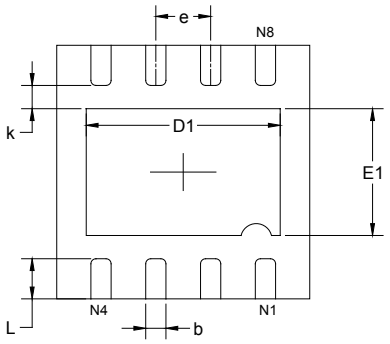
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

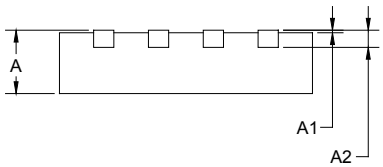
TDFN-3×3-8L



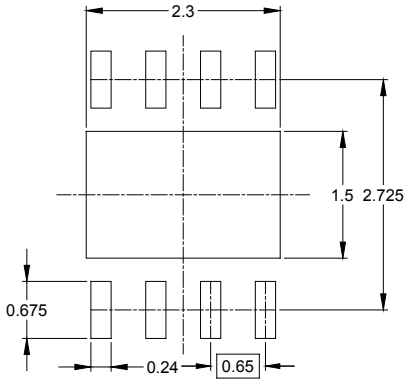
TOP VIEW



BOTTOM VIEW



SIDE VIEW

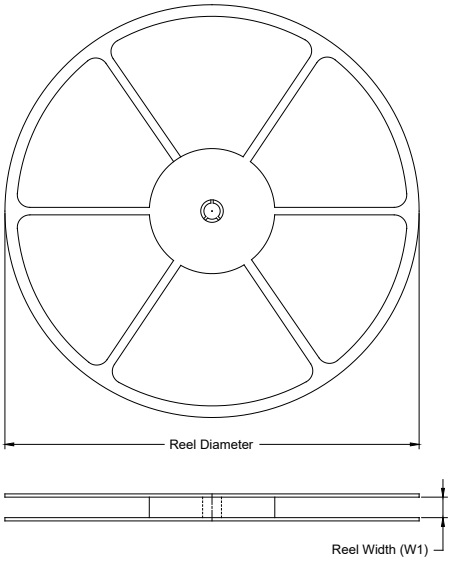


RECOMMENDED LAND PATTERN (Unit: mm)

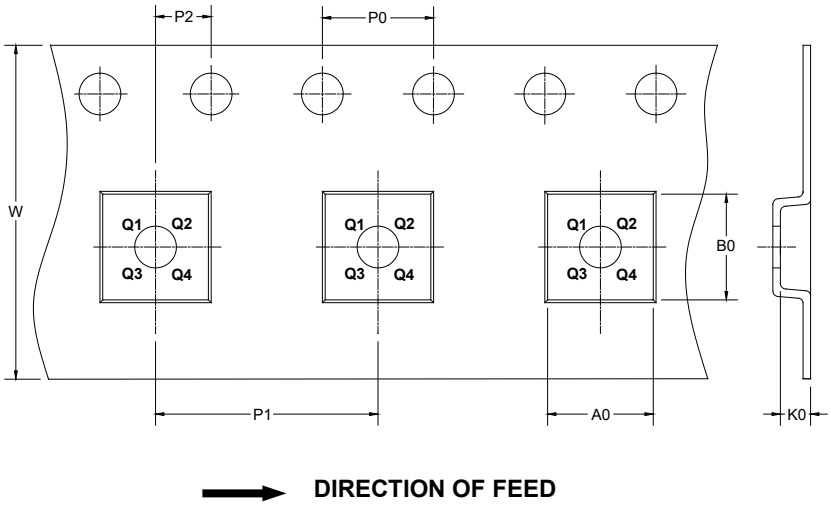
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.200	2.400	0.087	0.094
E	2.900	3.100	0.114	0.122
E1	1.400	1.600	0.055	0.063
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.650 TYP		0.026 TYP	
L	0.375	0.575	0.015	0.023

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



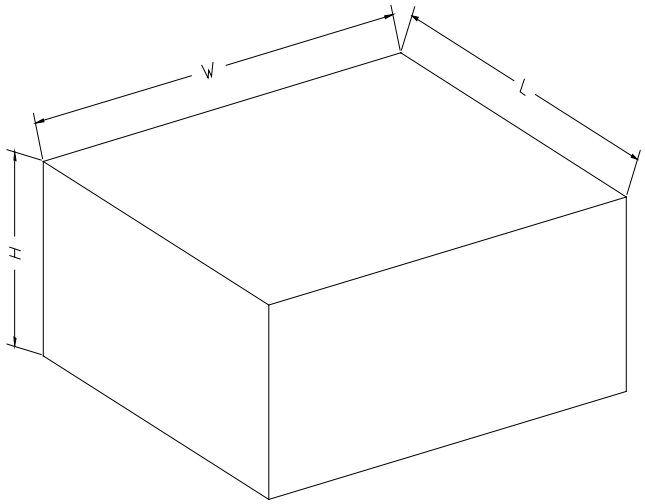
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-553-5	7″	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TDFN-3×3-8L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002