

# Precision, 20 MHz, CMOS, Rail-to-Rail Input/Output Operational Amplifiers

Data Sheet

## AD8615/AD8616/AD8618

### FEATURES

- Low offset voltage: 65  $\mu\text{V}$  maximum
- Single-supply operation: 2.7 V to 5.0 V
- Low noise: 8 nV/ $\sqrt{\text{Hz}}$
- Wide bandwidth: >20 MHz
- Slew rate: 12 V/ $\mu\text{s}$
- High output current: 150 mA
- No phase reversal
- Low input bias current: 1 pA
- Low supply current: 2 mA
- Unity-gain stable

### APPLICATIONS

- Barcode scanners
- Battery-powered instrumentation
- Multipole filters
- Sensors
- ASIC input or output amplifiers
- Audio
- Photodiode amplification

### GENERAL DESCRIPTION

The AD8615/AD8616/AD8618 are single/dual/quad, rail-to-rail, input and output, single-supply amplifiers featuring very low offset voltage, wide signal bandwidth, and low input voltage and current noise. The parts use a patented trimming technique that achieves superior precision without laser trimming. The AD8615/AD8616/AD8618 are fully specified to operate from 2.7 V to 5 V single supplies.

The combination of >20 MHz bandwidth, low offset, low noise, and low input bias current makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. AC applications benefit from the wide bandwidth and low distortion. The AD8615/AD8616/AD8618 offer the highest output drive capability of the DigiTrim® family, which is excellent for audio line drivers and other low impedance applications.

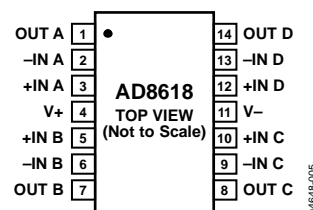
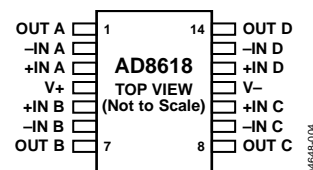
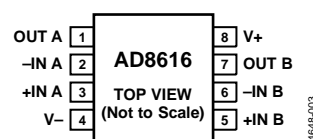
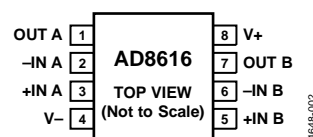
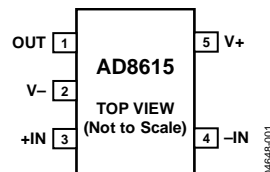
Applications for the parts include portable and low powered instrumentation, audio amplification for portable devices, portable phone headsets, bar code scanners, and multipole filters. The ability to swing rail-to-rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in single-supply systems.

Rev. G

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### PIN CONFIGURATIONS



The AD8615/AD8616/AD8618 are specified over the extended industrial temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ). The AD8615 is available in 5-lead TSOT-23 package. The AD8616 is available in 8-lead MSOP and narrow SOIC surface-mount packages; the MSOP version is available in tape and reel only. The AD8618 is available in 14-lead SOIC and TSSOP packages.

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## REVISION HISTORY

### 6/14—Rev. F to Rev. G

Changes to Input Overvoltage Protection Section.....	11
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### 3/14—Rev. E to Rev. F

Changes to Differential Input Voltage Parameter, Table 3.....	5
Updated Outline Dimensions .....	15
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### 9/08—Rev. D to Rev. E

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### 5/08—Rev. C to Rev. D

Changes to Layout .....	1
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### 6/05—Rev. B to Rev. C

Change to Table 1 .....	3
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### 1/05—Rev. A to Rev. B

Added AD8615 .....	Universal
Changes to Figure 12.....	8
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### 4/04—Rev. 0 to Rev. A

Added AD8618 .....	Universal
Updated Outline Dimensions .....	16

### 1/04—Revision 0: Initial Version

## SPECIFICATIONS

$V_S = 5\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage, AD8616/AD8618	$V_{OS}$	$V_S = 3.5\text{ V}$ at $V_{CM} = 0.5\text{ V}$ and $3.0\text{ V}$		23	60	$\mu\text{V}$
Offset Voltage, AD8615				23	100	$\mu\text{V}$
		$V_{CM} = 0\text{ V}$ to $5\text{ V}$		80	500	$\mu\text{V}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			800	$\mu\text{V}$
Offset Voltage Drift, AD8616/AD8618	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	7	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Drift, AD8615				3	10	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$			0.2	1	$\text{pA}$
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			50	$\text{pA}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			550	$\text{pA}$
Input Offset Current	$I_{OS}$			0.1	0.5	$\text{pA}$
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			50	$\text{pA}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			250	$\text{pA}$
Input Voltage Range			0		5	$\text{V}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$ to $4.5\text{ V}$	80	100		$\text{dB}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V}$ to $5\text{ V}$	105	1500		$\text{V}/\text{mV}$
Input Capacitance	$C_{DIFF}$			2.5		$\text{pF}$
	$C_{CM}$			6.7		$\text{pF}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$	4.98	4.99		$\text{V}$
		$I_L = 10\text{ mA}$	4.88	4.92		$\text{V}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.7			$\text{V}$
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$		7.5	15	$\text{mV}$
		$I_L = 10\text{ mA}$		70	100	$\text{mV}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			200	$\text{mV}$
Output Current	$I_{OUT}$			$\pm 150$		$\text{mA}$
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		3		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$	70	90		$\text{dB}$
Supply Current per Amplifier	$I_{SY}$	$V_O = 0\text{ V}$		1.7	2	$\text{mA}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			2.5	$\text{mA}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		12		$\text{V}/\mu\text{s}$
Settling Time	$t_s$	To 0.01%		<0.5		$\mu\text{s}$
Gain Bandwidth Product	GBP			24		$\text{MHz}$
Phase Margin	$\phi_m$			63		Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		2.4		$\mu\text{V}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		7		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$
Channel Separation	$C_S$	$f = 10\text{ kHz}$		-115		$\text{dB}$
		$f = 100\text{ kHz}$		-110		$\text{dB}$

$V_S = 2.7\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage, AD8616/AD8618	$V_{OS}$	$V_S = 3.5\text{ V}$ at $V_{CM} = 0.5\text{ V}$ and $3.0\text{ V}$		23	65	$\mu\text{V}$
Offset Voltage, AD8615				23	100	$\mu\text{V}$
		$V_{CM} = 0\text{ V}$ to $2.7\text{ V}$		80	500	$\mu\text{V}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			800	$\mu\text{V}$
Offset Voltage Drift, AD8616/AD8618	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	7	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Drift, AD8615				3	10	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$			0.2	1	$\text{pA}$
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			50	$\text{pA}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			550	$\text{pA}$
Input Offset Current	$I_{OS}$			0.1	0.5	$\text{pA}$
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			50	$\text{pA}$
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			250	$\text{pA}$
Input Voltage Range			0		2.7	$\text{V}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$ to $2.7\text{ V}$	80	100		$\text{dB}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V}$ to $2.2\text{ V}$	55	150		$\text{V/mV}$
Input Capacitance	$C_{DIFF}$ $C_{CM}$			2.5		$\text{pF}$ $\text{pF}$
				7.8		$\text{pF}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.65	2.68		$\text{V}$ $\text{V}$
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		11	25	$\text{mV}$ $\text{mV}$
Output Current	$I_{OUT}$			$\pm 50$		$\text{mA}$
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		3		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$	70	90		$\text{dB}$
Supply Current per Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.7	2	$\text{mA}$ $\text{mA}$
					2.5	$\text{mA}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		12		$\text{V}/\mu\text{s}$
Settling Time	$t_S$	To 0.01%		<0.3		$\mu\text{s}$
Gain Bandwidth Product	GBP			23		$\text{MHz}$
Phase Margin	$\phi_m$			42		Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n$ p-p	0.1 Hz to 10 Hz		2.1		$\mu\text{V}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		7		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$
Channel Separation	$C_S$	$f = 10\text{ kHz}$		-115		$\text{dB}$
		$f = 100\text{ kHz}$		-110		$\text{dB}$

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to $V_S$
Differential Input Voltage	$\pm 6$ V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^{\circ}\text{C}$
Junction Temperature	$150^{\circ}\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5-Lead TSOT-23 (UJ)	207	61	$^{\circ}\text{C}/\text{W}$
8-Lead MSOP (RM)	210	45	$^{\circ}\text{C}/\text{W}$
8-Lead SOIC (R)	158	43	$^{\circ}\text{C}/\text{W}$
14-Lead SOIC (R)	120	36	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP (RU)	180	35	$^{\circ}\text{C}/\text{W}$

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

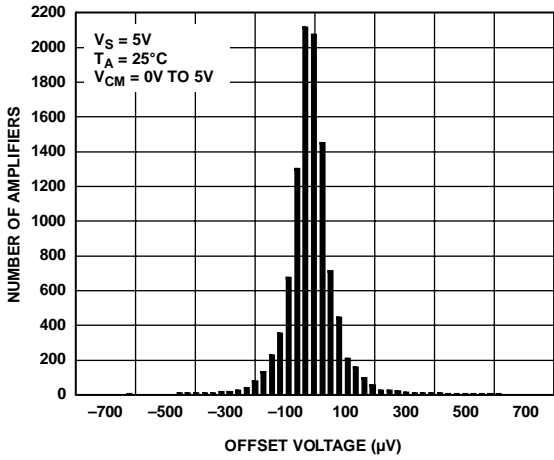


Figure 6. Input Offset Voltage Distribution

04648-008

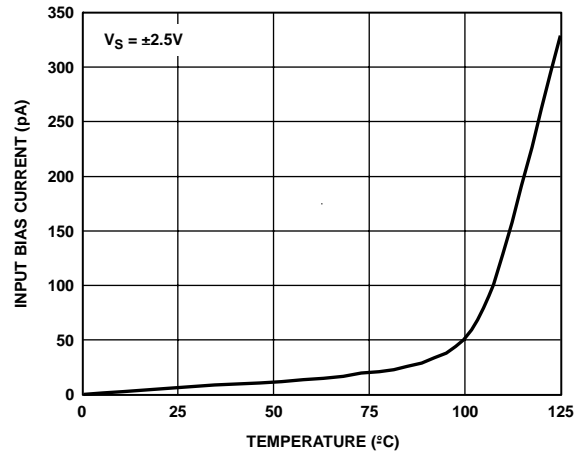


Figure 9. Input Bias Current vs. Temperature

04648-009

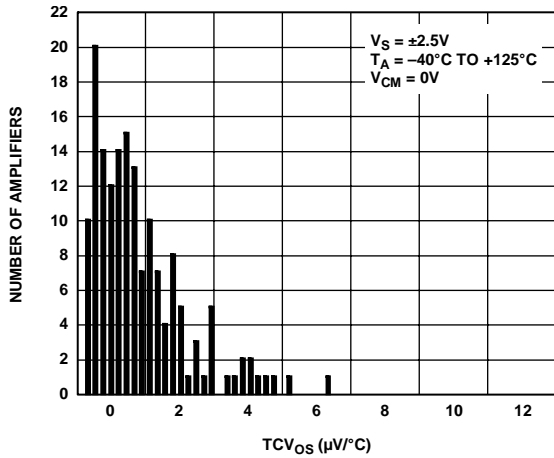


Figure 7. Offset Voltage Drift Distribution

04648-007

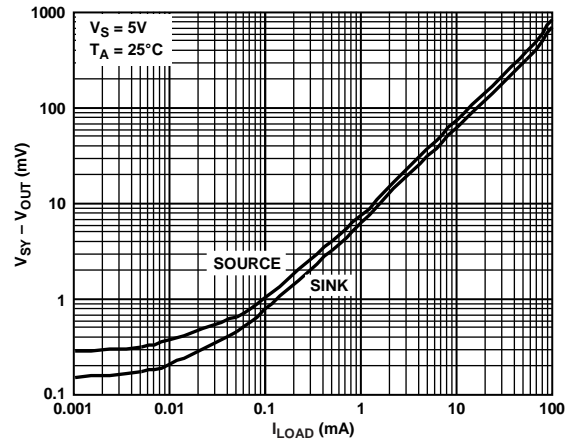


Figure 10. Output Voltage to Supply Rail vs. Load Current

04648-010

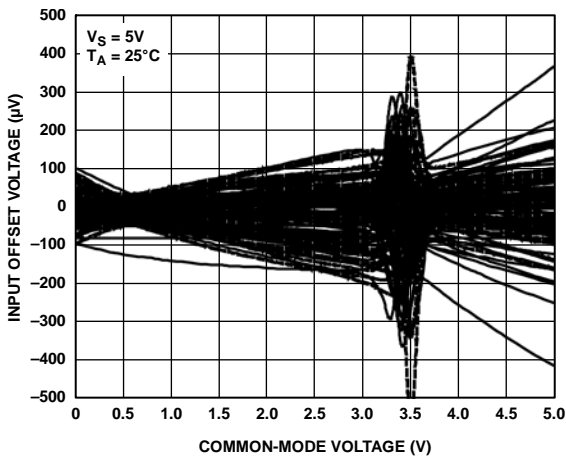


Figure 8. Input Offset Voltage vs. Common-Mode Voltage (200 Units, Five Wafer Lots Including Process Skews)

04648-006

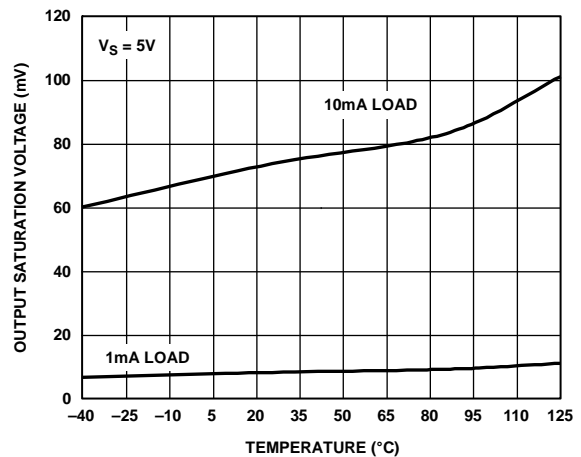


Figure 11. Output Saturation Voltage vs. Temperature

04648-011

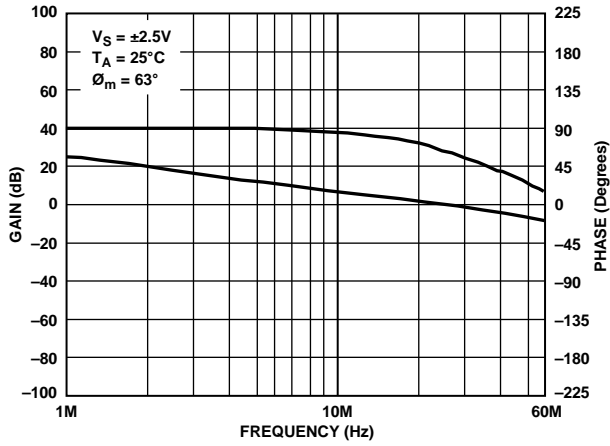


Figure 12. Open-Loop Gain and Phase vs. Frequency

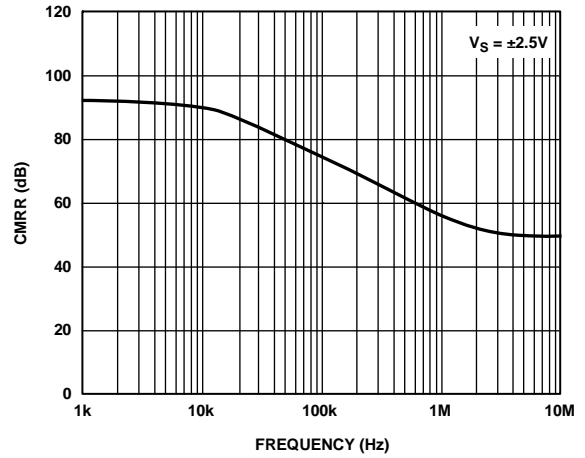


Figure 15. CMRR vs. Frequency

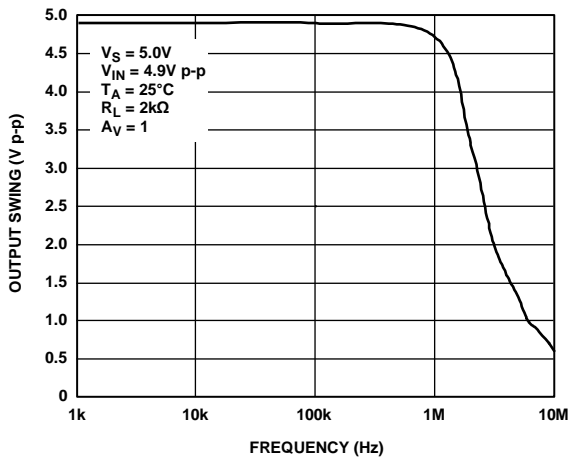


Figure 13. Closed-Loop Output Voltage Swing vs. Frequency

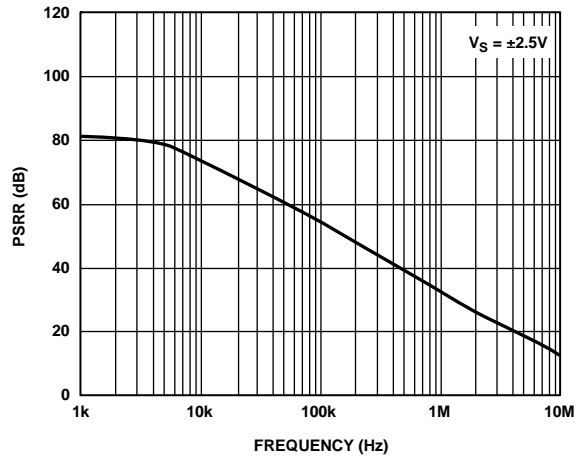


Figure 16. PSRR vs. Frequency

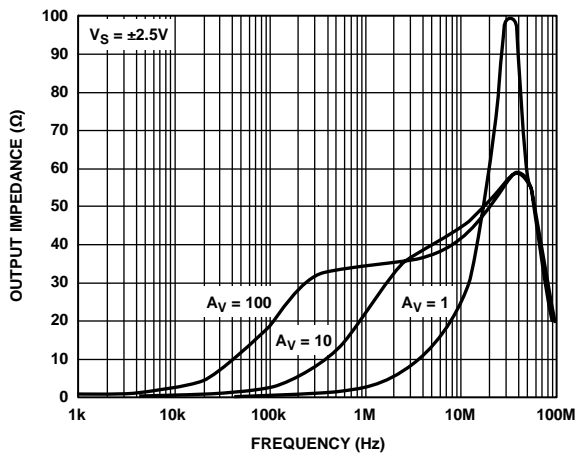


Figure 14. Output Impedance vs. Frequency

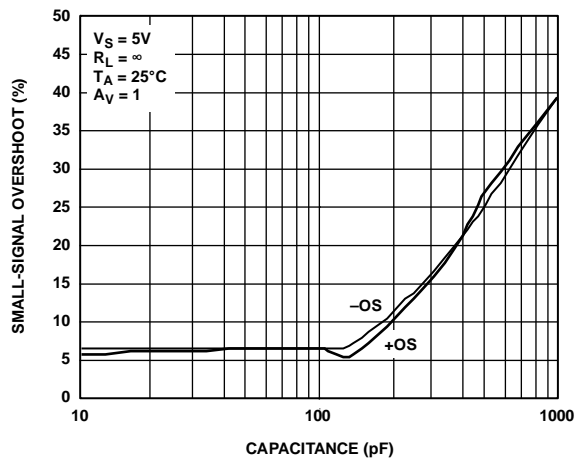


Figure 17. Small-Signal Overshoot vs. Load Capacitance

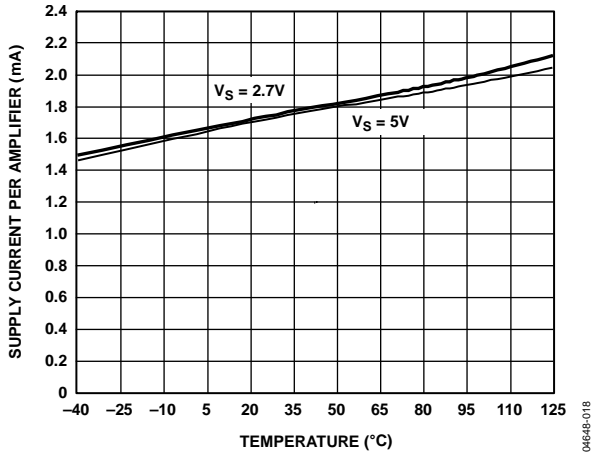


Figure 18. Supply Current vs. Temperature

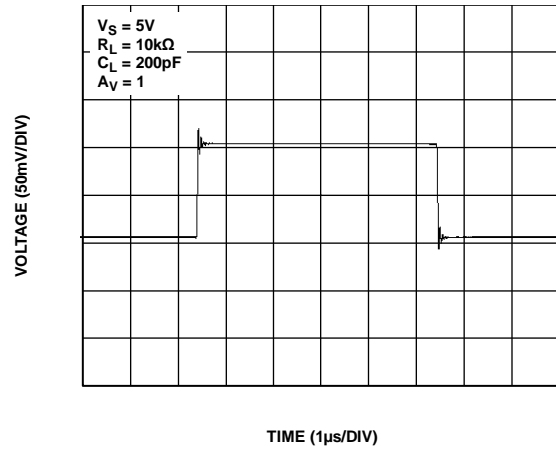


Figure 21. Small Signal Transient Response

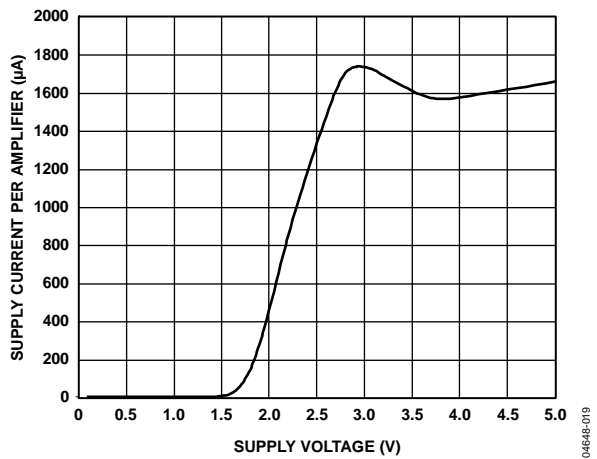


Figure 19. Supply Current per Amplifier vs. Supply Voltage

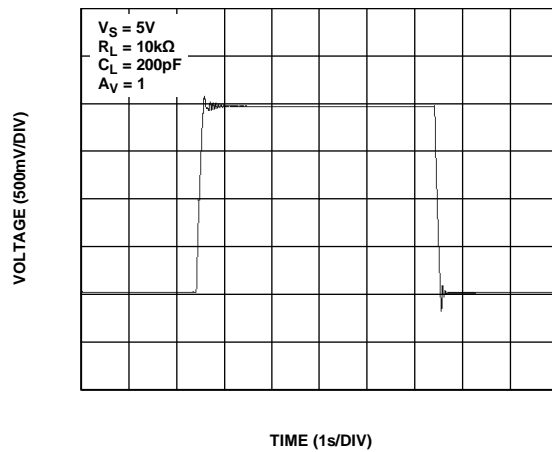


Figure 22. Large Signal Transient Response

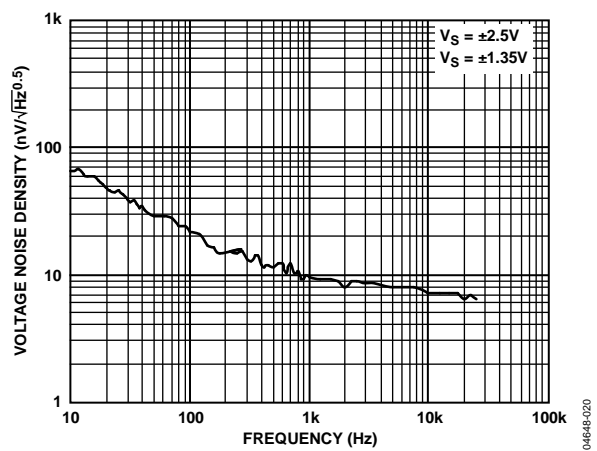


Figure 20. Voltage Noise Density vs. Frequency

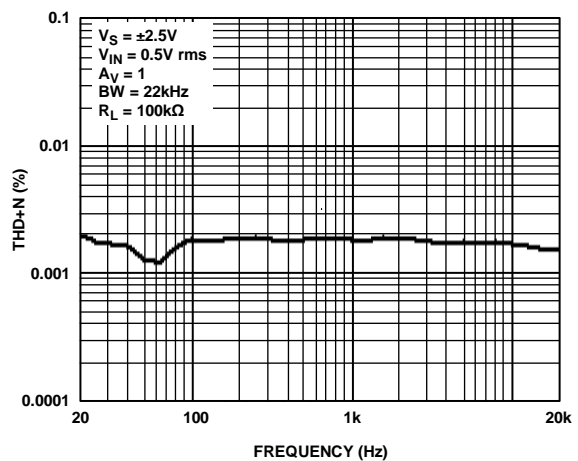


Figure 23. THD + N vs. Frequency



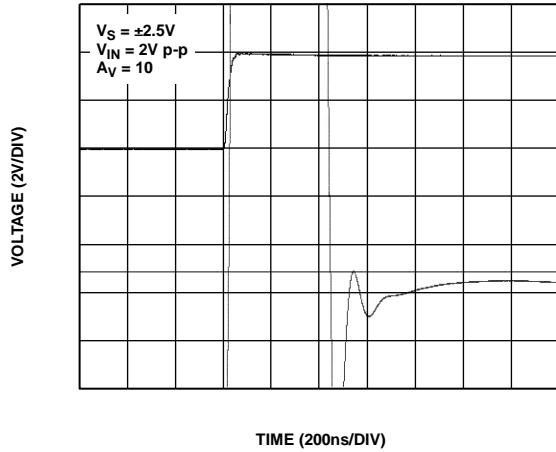


Figure 24. Settling Time

04648-024

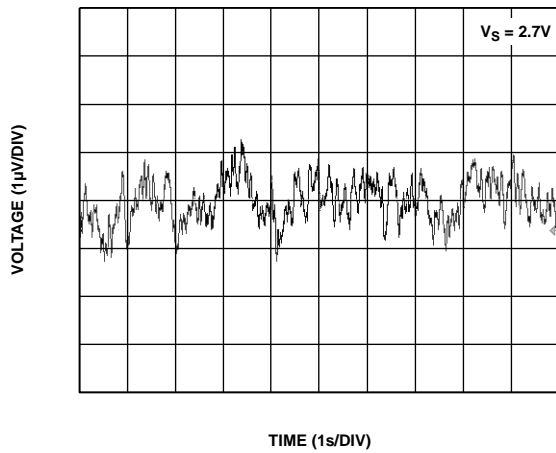


Figure 25. 0.1 Hz to 10 Hz Input Voltage Noise

04648-025

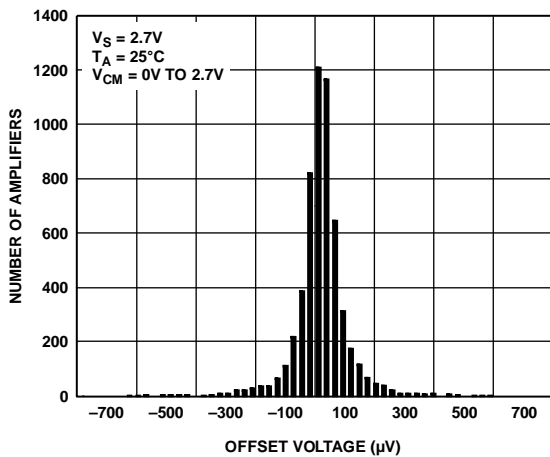


Figure 26. Input Offset Voltage Distribution

04648-026

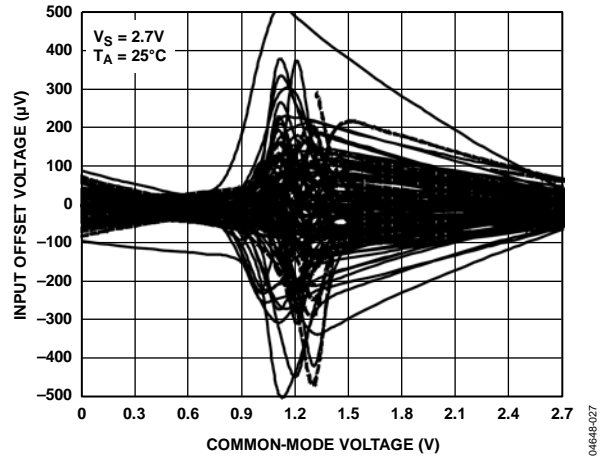


Figure 27. Input Offset Voltage vs. Common-Mode Voltage (200 Units, Five Wafer Lots Including Process Skews)

04648-027

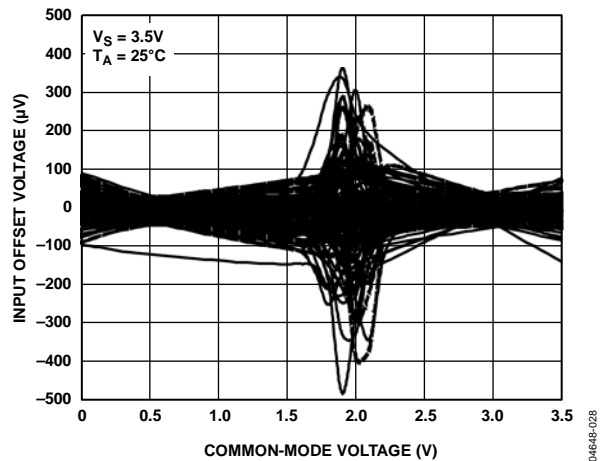


Figure 28. Input Offset Voltage vs. Common-Mode Voltage (200 Units, Five Wafer Lots Including Process Skews)

04648-028

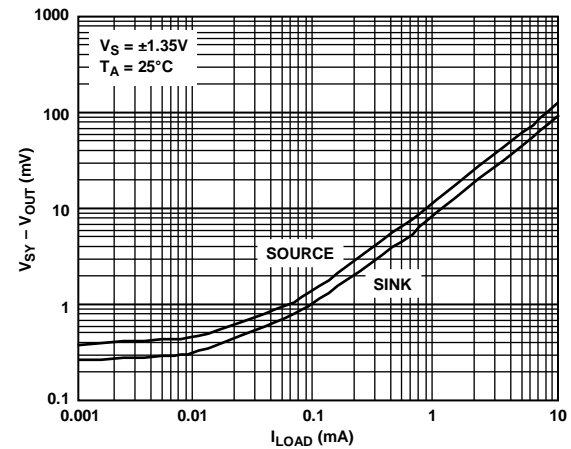


Figure 29. Output Voltage to Supply Rail vs. Load Current

04648-029

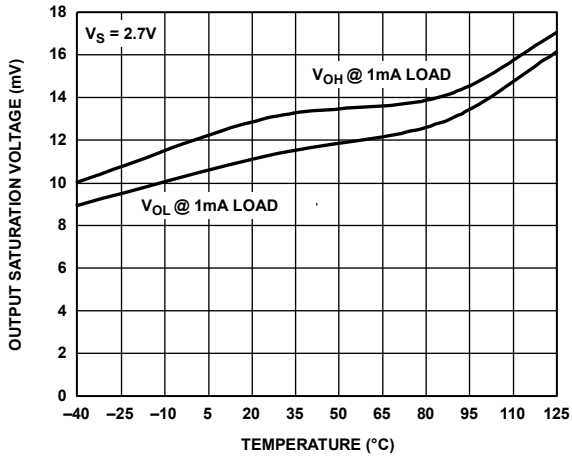


Figure 30. Output Saturation Voltage vs. Temperature

04648-030

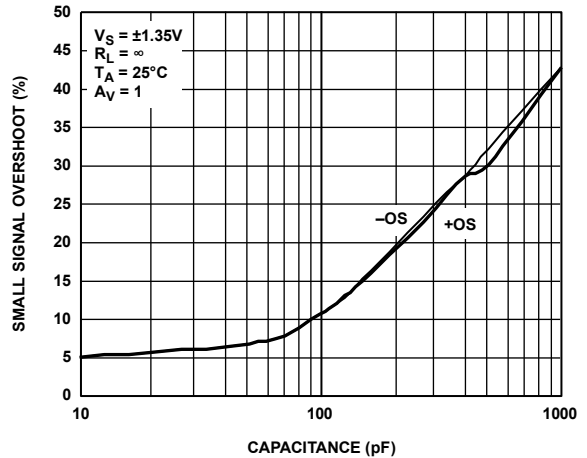


Figure 33. Small Signal Overshoot vs. Load Capacitance

04648-033

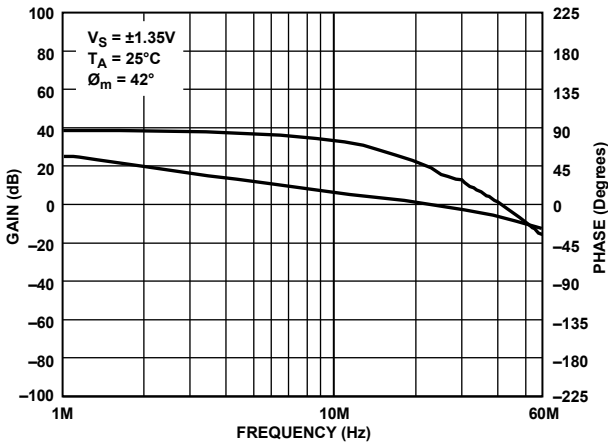


Figure 31. Open-Loop Gain and Phase vs. Frequency

04648-031

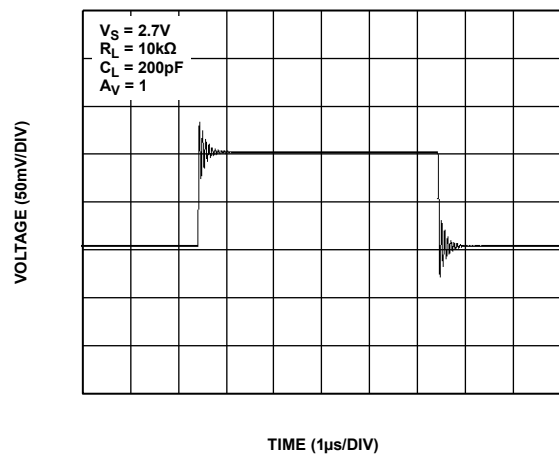


Figure 34. Small Signal Transient Response

04648-034

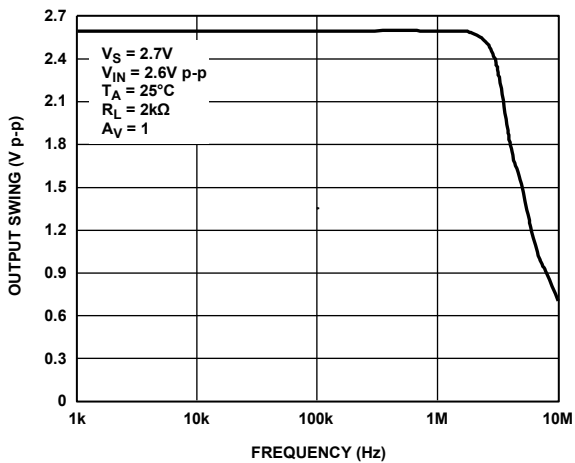


Figure 32. Closed-Loop Output Voltage Swing vs. Frequency

04648-032

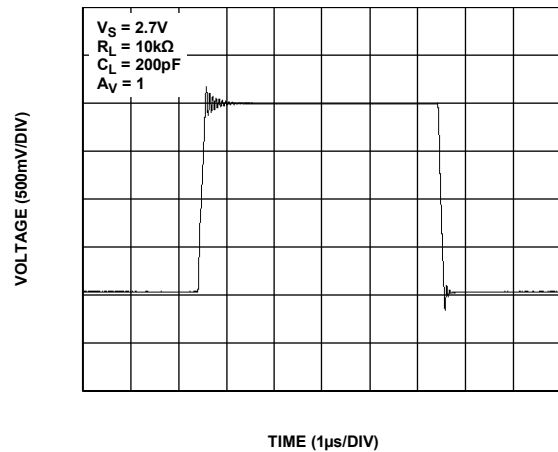


Figure 35. Large Signal Transient Response

04648-035

## APPLICATIONS INFORMATION

### INPUT OVERVOLTAGE PROTECTION

If the voltage applied at either input exceeds the supplies, place external resistors in series with the inputs. The resistor values can be determined by the equation

$$\frac{V_{IN} - V_{SY}}{R_S} < 5 \text{ mA}$$

The extremely low input bias current allows the use of larger resistors, which allows the user to apply higher voltages at the inputs. The use of these resistors adds thermal noise, which contributes to the overall output voltage noise of the amplifier.

For example, a 10 kΩ resistor has less than 13 nV/√Hz of thermal noise and less than 10 nV of error voltage at room temperature.

### OUTPUT PHASE REVERSAL

The AD8615/AD8616/AD8618 are immune to phase inversion, a phenomenon that occurs when the voltage applied at the input of the amplifier exceeds the maximum input common mode.

Phase reversal can cause permanent damage to the amplifier and can create lock ups in systems with feedback loops.

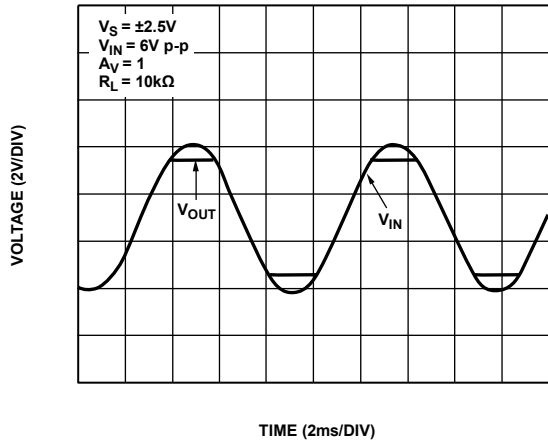


Figure 36. No Phase Reversal

### DRIVING CAPACITIVE LOADS

Although the AD8615/AD8616/AD8618 are capable of driving capacitive loads of up to 500 pF without oscillating, a large amount of overshoot is present when operating at frequencies above 100 kHz. This is especially true when the amplifier is configured in positive unity gain (worst case). When such large capacitive loads are required, the use of external compensation is highly recommended.

This reduces the overshoot and minimizes ringing, which in turn improves the frequency response of the AD8615/AD8616/AD8618. One simple technique for compensation is the snubber, which consists of a simple RC network. With this circuit in place, output swing is maintained and the amplifier is stable at all gains.

Figure 38 shows the implementation of the snubber, which reduces overshoot by more than 30% and eliminates ringing that can cause instability. Using the snubber does not recover the loss of bandwidth incurred from a heavy capacitive load.

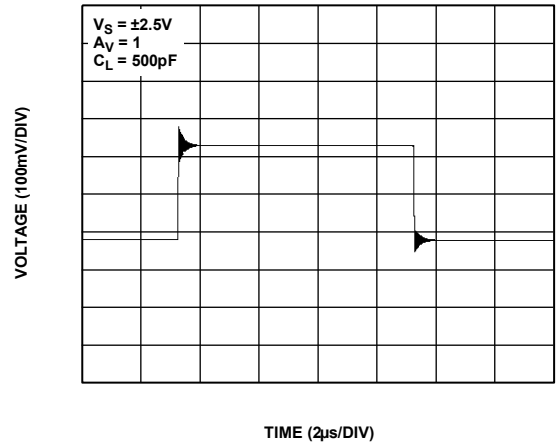


Figure 37. Driving Heavy Capacitive Loads Without Compensation

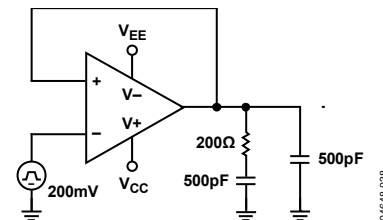


Figure 38. Snubber Network

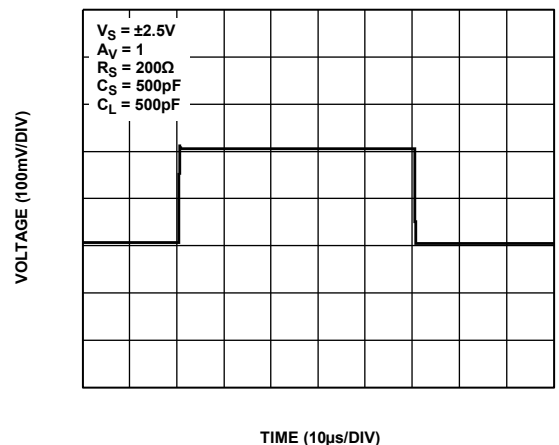


Figure 39. Driving Heavy Capacitive Loads Using the Snubber Network

**OVERLOAD RECOVERY TIME**

Overload recovery time is the time it takes the output of the amplifier to come out of saturation and recover to its linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 40 and Figure 41 show the positive and negative overload recovery times of the AD8616. In both cases, the time elapsed before the AD8616 comes out of saturation is less than 1  $\mu$ s. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion to the output signal.

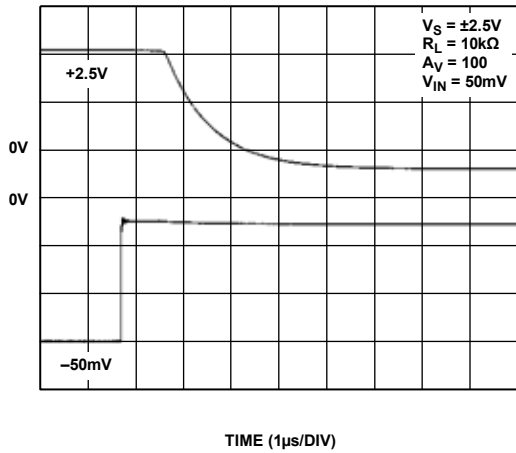


Figure 40. Positive Overload Recovery

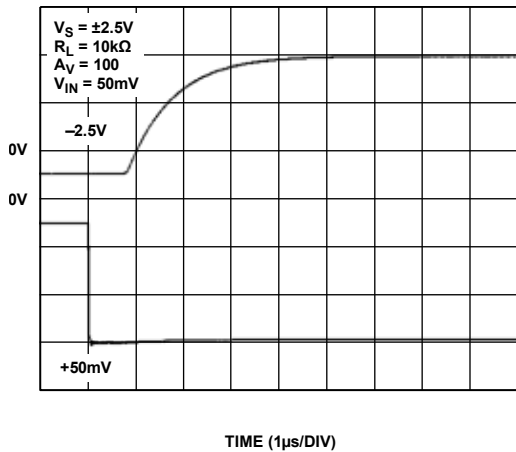


Figure 41. Negative Overload Recovery

**D/A CONVERSION**

The AD8616 can be used at the output of high resolution DACs. The low offset voltage, fast slew rate, and fast settling time make the part suitable to buffer voltage output or current output DACs.

Figure 42 shows an example of the AD8616 at the output of the AD5542. The AD8616's rail-to-rail output and low distortion help maintain the accuracy needed in data acquisition systems and automated test equipment.

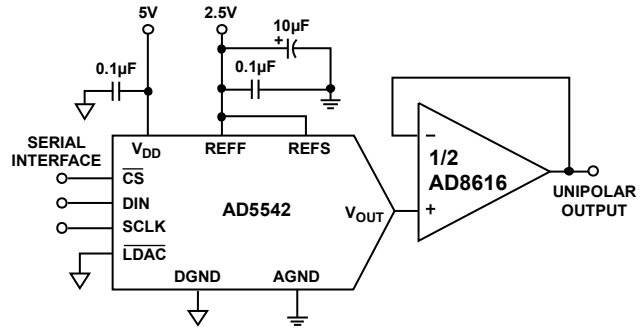


Figure 42. Buffering DAC Output

**LOW NOISE APPLICATIONS**

Although the AD8618 typically has less than 8 nV/ $\sqrt{\text{Hz}}$  of voltage noise density at 1 kHz, it is possible to reduce it further. A simple method is to connect the amplifiers in parallel, as shown in Figure 43. The total noise at the output is divided by the square root of the number of amplifiers. In this case, the total noise is approximately 4 nV/ $\sqrt{\text{Hz}}$  at room temperature. The 100  $\Omega$  resistor limits the current and provides an effective output resistance of 50  $\Omega$ .

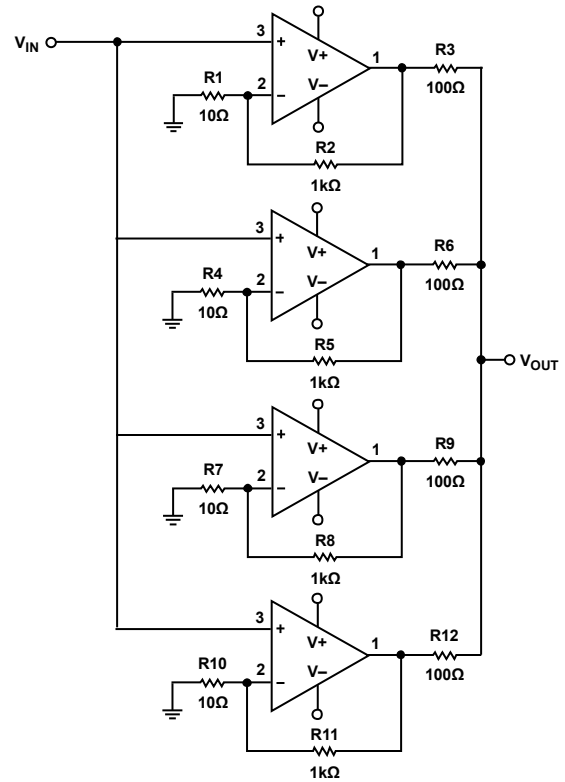


Figure 43. Noise Reduction

**HIGH SPEED PHOTODIODE PREAMPLIFIER**

The AD8615/AD8616/AD8618 are excellent choices for I-to-V conversions. The very low input bias, low current noise, and high unity-gain bandwidth of the parts make them suitable, especially for high speed photodiode preamplifiers.

In high speed photodiode applications, the diode is operated in a photoconductive mode (reverse biased). This lowers the junction capacitance at the expense of an increase in the amount of dark current that flows out of the diode.

The total input capacitance, C1, is the sum of the diode and op amp input capacitances. This creates a feedback pole that causes degradation of the phase margin, making the op amp unstable. Therefore, it is necessary to use a capacitor in the feedback to compensate for this pole.

To get the maximum signal bandwidth, select

$$C2 = \sqrt{\frac{C1}{2\pi R2 f_u}}$$

where  $f_u$  is the unity-gain bandwidth of the amplifier.

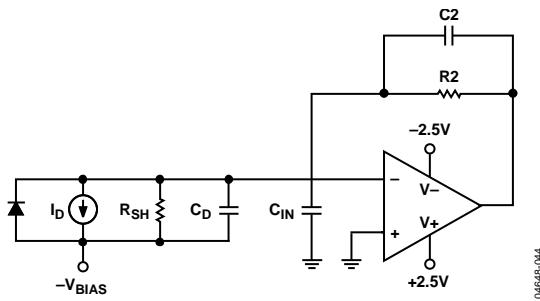


Figure 44. High Speed Photodiode Preamplifier

**ACTIVE FILTERS**

The low input bias current and high unity-gain bandwidth of the AD8616 make it an excellent choice for precision filter design.

Figure 45 shows the implementation of a second-order, low-pass filter. The Butterworth response has a corner frequency of 100 kHz and a phase shift of 90°. The frequency response is shown in Figure 46.

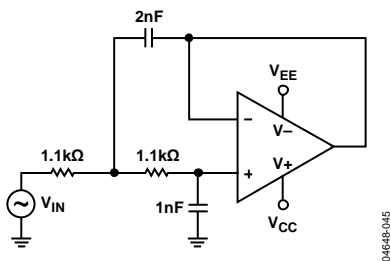


Figure 45. Second-Order, Low-Pass Filter

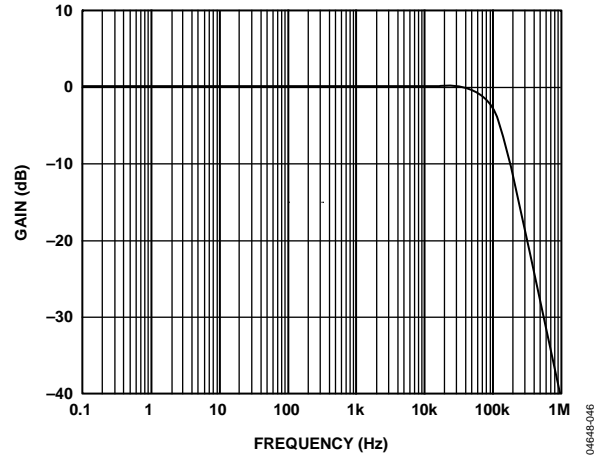


Figure 46. Second-Order Butterworth, Low-Pass Filter Frequency Response

**POWER DISSIPATION**

Although the AD8615/AD8616/AD8618 are capable of providing load currents up to 150 mA, the usable output, load current, and drive capability are limited to the maximum power dissipation allowed by the device package.

In any application, the absolute maximum junction temperature for the AD8615/AD8616/AD8618 is 150°C. This should never be exceeded because the device could suffer premature failure. Accurately measuring power dissipation of an integrated circuit is not always a straightforward exercise; Figure 47 is a design aid for setting a safe output current drive level or selecting a heat sink for the package options available on the AD8616.

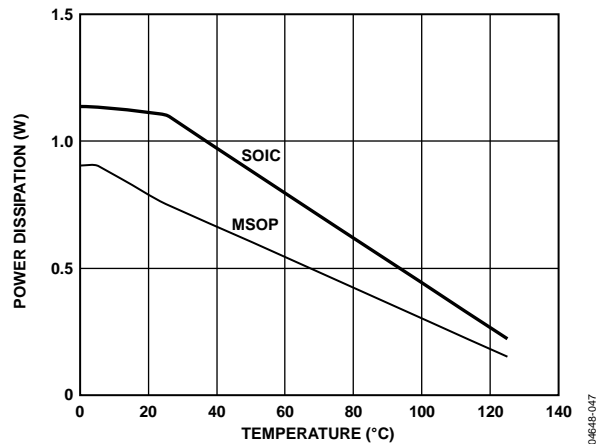


Figure 47. Maximum Power Dissipation vs. Ambient Temperature

These thermal resistance curves were determined using the AD8616 thermal resistance data for each package and a maximum junction temperature of 150°C.

The following formula can be used to calculate the internal junction temperature of the [AD8615/AD8616/AD8618](#) for any application:

$$T_J = P_{DISS} \times \theta_{JA} + T_A$$

where:

$T_J$  = junction temperature

$P_{DISS}$  = power dissipation

$\theta_{JA}$  = package thermal resistance, junction-to-case

$T_A$  = ambient temperature of the circuit

To calculate the power dissipated by the [AD8615/AD8616/AD8618](#), use the following:

$$P_{DISS} = I_{LOAD} \times (V_S - V_{OUT})$$

where:

$I_{LOAD}$  = output load current

$V_S$  = supply voltage

$V_{OUT}$  = output voltage

The quantity within the parentheses is the maximum voltage developed across either output transistor.

### POWER CALCULATIONS FOR VARYING OR UNKNOWN LOADS

Often, calculating power dissipated by an integrated circuit to determine if the device is being operated in a safe range is not as simple as it may seem. In many cases, power cannot be directly measured. This may be the result of irregular output waveforms or varying loads. Indirect methods of measuring power are required.

There are two methods to calculate power dissipated by an integrated circuit. The first is to measure the package temperature and the board temperature. The second is to directly measure the circuit's supply current.

### Calculating Power by Measuring Ambient Temperature and Case Temperature

The two equations for calculating the junction temperature are

$$T_J = T_A + P \theta_{JA}$$

where:

$T_J$  = junction temperature

$T_A$  = ambient temperature

$\theta_{JA}$  = the junction-to-ambient thermal resistance

$$T_J = T_C + P \theta_{JC}$$

where:

$T_C$  is case temperature.

$\theta_{JA}$  and  $\theta_{JC}$  are given in the data sheet.

The two equations for calculating P (power) are

$$T_A + P \theta_{JA} = T_C + P \theta_{JC}$$

$$P = (T_A - T_C) / (\theta_{JC} - \theta_{JA})$$

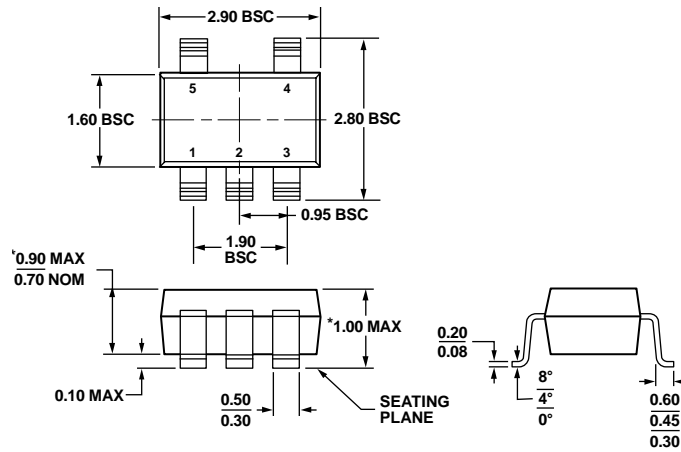
Once the power is determined, it is necessary to recalculate the junction temperature to ensure that the temperature was not exceeded.

The temperature should be measured directly on and near the package but not touching it. Measuring the package can be difficult. A very small bimetallic junction glued to the package can be used, or an infrared sensing device can be used, if the spot size is small enough.

### Calculating Power by Measuring Supply Current

If the supply voltage and current are known, power can be calculated directly. However, the supply current can have a dc component with a pulse directed into a capacitive load, which can make the rms current very difficult to calculate. This difficulty can be overcome by lifting the supply pin and inserting an rms current meter into the circuit. For this method to work, make sure the current is delivered by the supply pin being measured. This is usually a good method in a single-supply system; however, if the system uses dual supplies, both supplies may need to be monitored.

OUTLINE DIMENSIONS

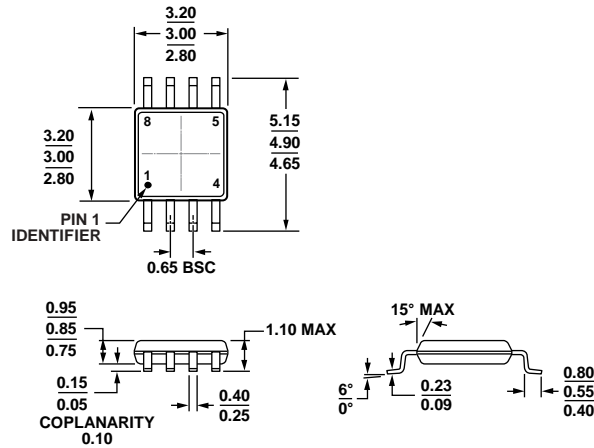


\*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 48. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)

Dimensions shown in millimeters

091508-A

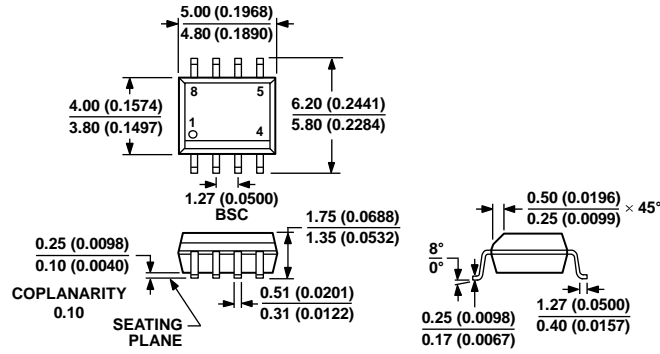


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 49. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

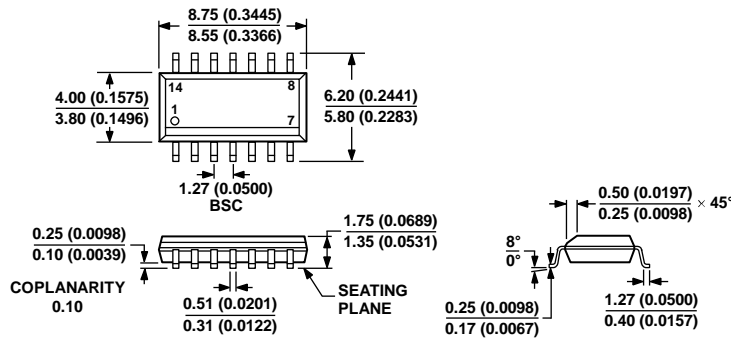
1007-2009-B



COMPLIANT TO JEDEC STANDARDS MS-012-A A  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 50. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body (R-8)  
 Dimensions shown in millimeters and (inches)

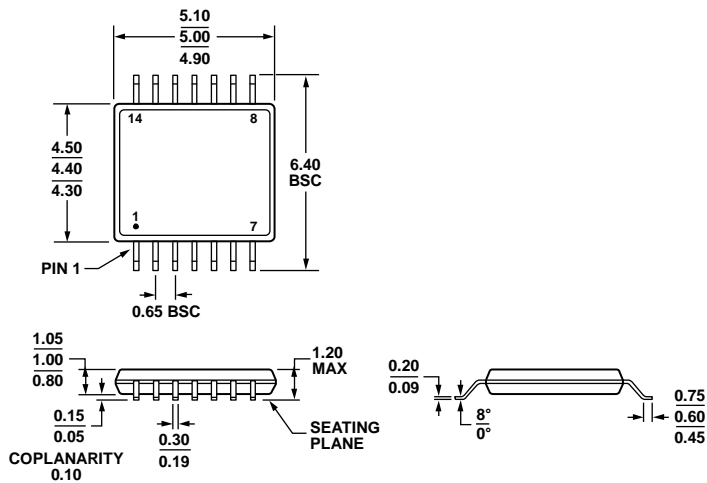
012407-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 51. 14-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body (R-14)  
 Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 52. 14-Lead Thin Shrink Small Outline Package [TSSOP]  
 (RU-14)  
 Dimensions shown in millimeters

061909-A



**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
AD8615AUJZ-R2	-40°C to +125°C	5-Lead TSOT-23	UJ-5	BAK
AD8615AUJZ-REEL	-40°C to +125°C	5-Lead TSOT-23	UJ-5	BAK
AD8615AUJZ-REEL7	-40°C to +125°C	5-Lead TSOT-23	UJ-5	BAK
AD8616ARMZ	-40°C to +125°C	8-Lead MSOP	RM-8	AOK
AD8616ARMZ-REEL	-40°C to +125°C	8-Lead MSOP	RM-8	AOK
AD8616AR	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8616ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8616ARZ-REEL	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8616ARZ-REEL7	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8618ARZ	-40°C to +125°C	14-Lead SOIC_N	R-14	
AD8618ARZ-REEL	-40°C to +125°C	14-Lead SOIC_N	R-14	
AD8618ARZ-REEL7	-40°C to +125°C	14-Lead SOIC_N	R-14	
AD8618ARUZ	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8618ARUZ-REEL	-40°C to +125°C	14-Lead TSSOP	RU-14	

<sup>1</sup> Z = RoHS Compliant Part.