

# CMOS Low Voltage 2.5 $\Omega$ Dual SPDT Switch

Data Sheet

ADG736

## FEATURES

- 1.8 V to 5.5 V single supply
- Automotive temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- 2.5  $\Omega$  (typical) on resistance
- Low on resistance flatness
- $-3$  dB bandwidth  $> 200$  MHz
- Rail-to-rail operation
- 10-lead MSOP package
- Fast switching times
  - $t_{\text{ON}}$ : 16 ns
  - $t_{\text{OFF}}$ : 8 ns
- Typical power consumption ( $< 0.01$   $\mu\text{W}$ )
- TTL-/CMOS-compatible
- Qualified for automotive applications

## APPLICATIONS

- USB 1.1 signal switching circuits
- Cell phones
- PDA's
- Battery-powered systems
- Communications systems
- Sample-and-hold systems
- Audio signal routing
- Audio and video switching
- Mechanical reed relay replacement

## GENERAL DESCRIPTION

The ADG736 is a monolithic device comprising two independently selectable CMOS single pole, double throw (SPDT) switches. These switches are designed using a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents, and wide input signal bandwidth.

The on resistance profile is very flat over the full analog signal range. This ensures excellent linearity and low distortion when switching audio signals. Fast switching speed also makes the part suitable for video signal switching.

The ADG736 operates from a single 1.8 V to 5.5 V supply, making it ideally suited to portable and battery-powered instruments.

Each switch conducts equally well in both directions when on, and each has an input signal range that extends to the power supplies. The ADG736 exhibits break-before-make switching action.

The ADG736 is available in a 10-lead MSOP package.

## FUNCTIONAL BLOCK DIAGRAM

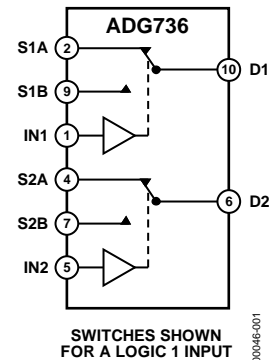


Figure 1.

## PRODUCT HIGHLIGHTS

- 1.8 V to 5.5 V Single-Supply Operation. The ADG736 offers high performance, including low on resistance and fast switching times. It is fully specified and guaranteed with 3 V and 5 V supply rails.
- Very Low  $R_{\text{ON}}$  (4.5  $\Omega$  Maximum at 5 V, 8  $\Omega$  Maximum at 3 V). At a supply voltage of 1.8 V,  $R_{\text{ON}}$  is typically 35  $\Omega$  over the temperature range.
- Low On Resistance Flatness.
- $-3$  dB Bandwidth  $> 200$  MHz.
- Low Power Dissipation. CMOS construction ensures low power dissipation.
- Fast  $t_{\text{ON}}/t_{\text{OFF}}$ .
- Break-Before-Make Switching Action.
- 10-Lead MSOP Package.

## Rev. D

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

## TABLE OF CONTENTS

Features .....	1	Pin Configuration and Function Descriptions.....	6
Applications.....	1	Typical Performance Characteristics .....	7
Functional Block Diagram .....	1	Test Circuits.....	9
General Description .....	1	Terminology .....	10
Product Highlights .....	1	Applications Information .....	11
Revision History .....	2	Outline Dimensions .....	12
Specifications.....	3	Ordering Guide .....	12
Absolute Maximum Ratings.....	5	Automotive Products.....	12
ESD Caution.....	5		

## REVISION HISTORY

### 2/12—Rev. C to Rev. D

Added Automotive Information (Throughout) .....	1
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

### 12/07—Rev. B to Rev. C

Updated Temperature Range (Throughout) .....	1
Changes to Features Section.....	1
Changes to Figure 4 and Figure 5.....	7
Changes to Ordering Guide .....	12

### 1/07—Rev. A to Rev. B

Updated Format.....	Universal
Changes to Leakage Currents .....	3
Changes to Leakage Currents .....	4
Changes to Ordering Guide .....	12
Updated Outline Dimensions .....	12

### 11/03—Rev. 0 to Rev. A

Renumbered Figures and TPCs.....	Universal
Change to Title.....	1
Changes to Applications .....	1
Changes to Absolute Maximum Ratings .....	4
Changes to Ordering Guide .....	4
Changes to Test Circuit 3.....	7
Changes to Outline Dimensions.....	8

## SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ . All specifications  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise noted.

Table 1.

Parameter	B Version			Unit	Test Conditions/Comments
	25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	2.5			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$ ; see Figure 10
	4	4.5	7	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.1	0.4	0.4	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$
				$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5	1.2	1.5	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$
				$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (Off)	$\pm 0.01$		1	nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; see Figure 11
Channel On Leakage $I_D$ , $I_S$ (On)	$\pm 0.01$		5	nA typ	$V_S = V_D = 1\text{ V or }4.5\text{ V}$ ; see Figure 12
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$		2.4	2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.1$	$\pm 0.1$	$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
				$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	12	16	16	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
				ns max	$V_S = 3\text{ V}$ ; see Figure 13
$t_{OFF}$	5	8	8	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
				ns max	$V_S = 3\text{ V}$ ; see Figure 13
Break-Before-Make Time Delay, $t_D$	7	1	1	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
				ns min	$V_{S1} = V_{S2} = 3\text{ V}$ ; see Figure 14
Off Isolation	-62			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 15
Channel-to-Channel Crosstalk	-62			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 16
Bandwidth (-3 dB)	200			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 17
$C_S$ (Off)	9			pF typ	
$C_D$ , $C_S$ (On)	32			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001	1.0	1.0	$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or 5 V
				$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design; not subject to production test.

$V_{DD} = 3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ . All specifications  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	B Version			Unit	Test Conditions/Comments
	25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	5	5.5		$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$ ; see Figure 10
		8	12	$\Omega$ max	See Figure 10
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.1			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$
		0.4	0.4	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )		2.5	2.5	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (Off)	$\pm 0.01$		1	nA typ	$V_{DD} = 3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3\text{ V}$ ; see Figure 11
Channel On Leakage $I_D$ , $I_S$ (On)	$\pm 0.01$		5	nA typ	$V_S = V_D = 1\text{ V or }3\text{ V}$ ; see Figure 12
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$		2.0	2.4	V min	
Input Low Voltage, $V_{INL}$		0.4	0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\pm 0.1$	$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	14			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		20	20	ns max	$V_S = 2\text{ V}$ ; see Figure 13
$t_{OFF}$	6			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		10	10	ns max	$V_S = 2\text{ V}$ ; see Figure 13
Break-Before-Make Time Delay, $t_D$	7			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		1	1	ns min	$V_{S1} = V_{S2} = 2\text{ V}$ ; see Figure 14
Off Isolation	-62			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 15
Channel-to-Channel Crosstalk	-62			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 16
Bandwidth (-3 dB)	200			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 17
$C_S$ (Off)	9			pF typ	
$C_D$ , $C_S$ (On)	32			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 3.3\text{ V}$ Digital inputs = 0 V or 3 V
		1.0	1.0	$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design; not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +6 V
Analog, Digital Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% duty cycle maximum)
Operating Temperature Range	
Automotive	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
MSOP Package, Power Dissipation	315 mW
$\theta_{JA}$ Thermal Impedance	205°C/W
Lead Temperature (Soldering, 10 sec)	300°C
IR Reflow (Peak Temperature, <20 sec)	235°C
Lead-Free Reflow Soldering	
Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec
ESD	2 kV

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

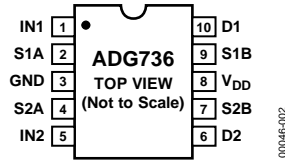


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input.
2	S1A	Source Terminal. May be an input or output.
3	GND	Ground (0 V) Reference.
4	S2A	Source Terminal. May be an input or output.
5	IN2	Logic Control Input.
6	D2	Drain Terminal. May be an input or output.
7	S2B	Source Terminal. May be an input or output.
8	V <sub>DD</sub>	Most Positive Power Supply Potential.
9	S1B	Source Terminal. May be an input or output.
10	D1	Drain Terminal. May be an input or output.

Table 5. Truth Table

Logic	Switch A	Switch B
0	Off	On
1	On	Off

### TYPICAL PERFORMANCE CHARACTERISTICS

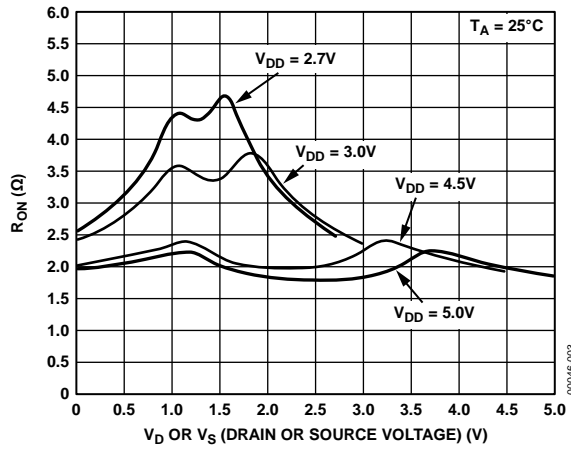


Figure 3. On Resistance as a Function of  $V_D$  or  $V_S$  Single Supplies

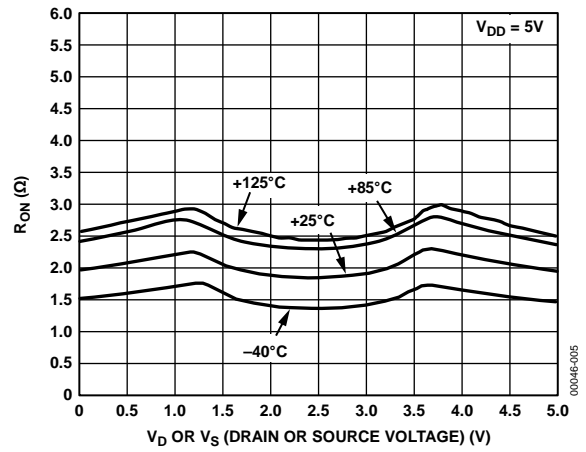


Figure 5. On Resistance as a Function of  $V_D$  or  $V_S$  for Different Temperatures  
 $V_{DD} = 5V$

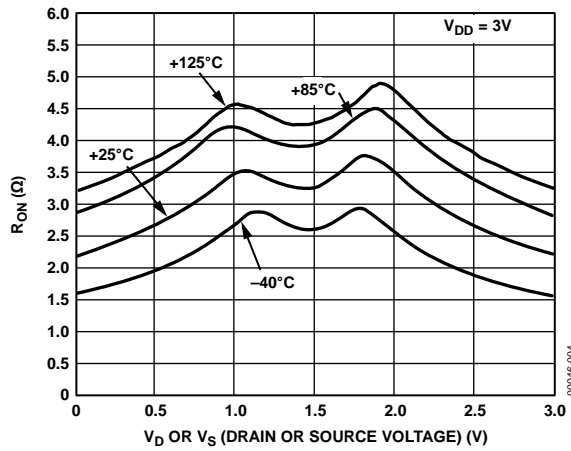


Figure 4. On Resistance as a Function of  $V_D$  or  $V_S$  for Different Temperatures  
 $V_{DD} = 3V$

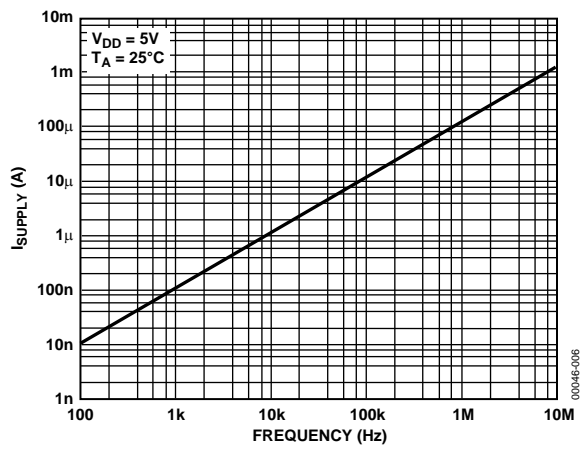


Figure 6. Supply Current vs. Input Switching Frequency

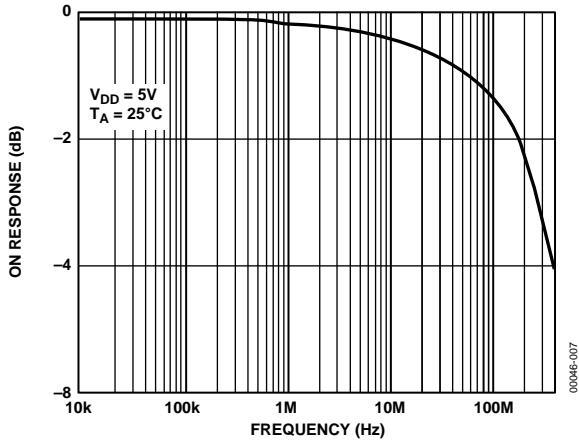


Figure 7. Bandwidth

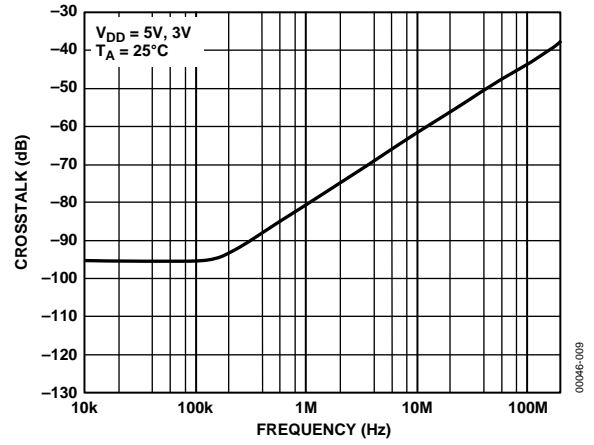


Figure 9. Crosstalk vs. Frequency

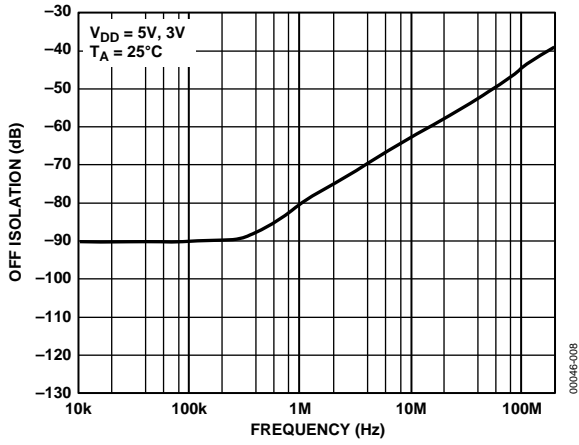


Figure 8. Off Isolation vs. Frequency



TEST CIRCUITS

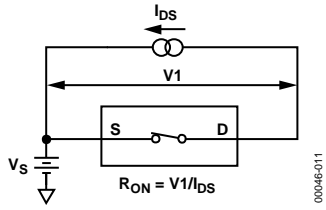


Figure 10. On Resistance

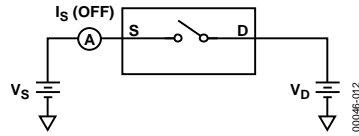


Figure 11. Off Leakage

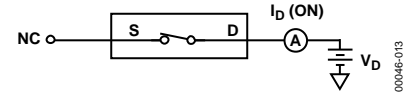


Figure 12. On Leakage

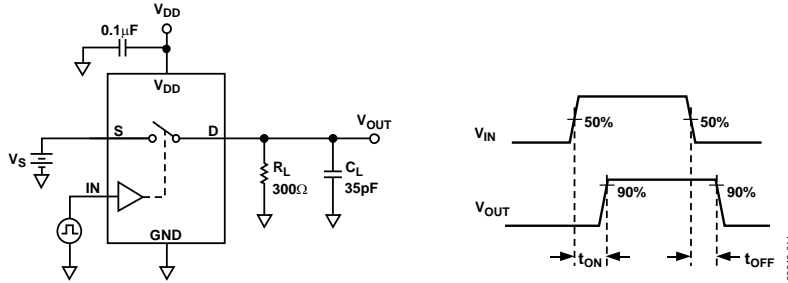


Figure 13. Switching Times

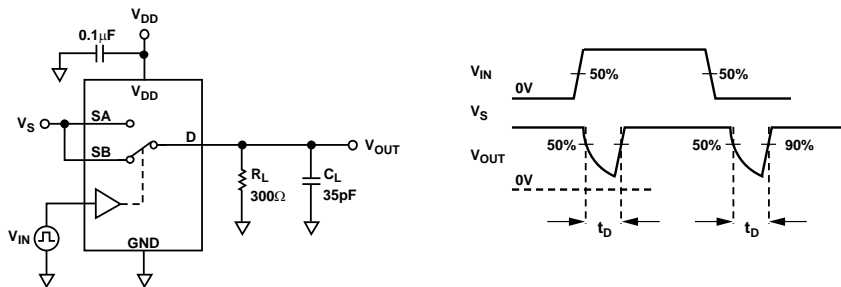


Figure 14. Break-Before-Make Time Delay,  $t_D$

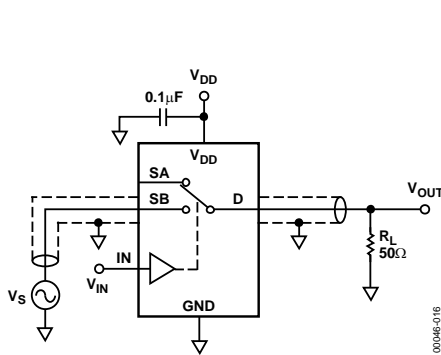


Figure 15. Off Isolation

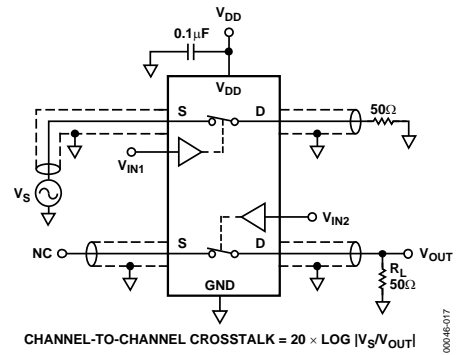


Figure 16. Channel-to-Channel Crosstalk

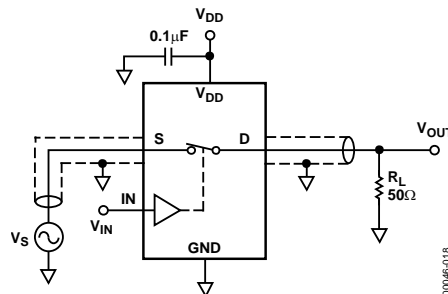


Figure 17. Bandwidth

## TERMINOLOGY

 **$R_{ON}$** 

Ohmic resistance between Terminal D and Terminal S.

 **$\Delta R_{ON}$** 

On resistance match between any two channels; that is,  $R_{ON}$  maximum –  $R_{ON}$  minimum.

 **$R_{FLAT (ON)}$** 

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

 **$I_S$  (Off)**

Source leakage current with the switch off.

 **$I_D, I_S$  (On)**

Channel leakage current with the switch on.

 **$V_D$  ( $V_S$ )**

Analog voltage on Terminal D and Terminal S.

 **$C_S$  (Off)**

Off switch source capacitance.

 **$C_D, C_S$  (On)**

On switch capacitance.

 **$t_{ON}$** 

Delay between applying the digital control input and the output switching on. See Figure 13.

 **$t_{OFF}$** 

Delay between applying the digital control input and the output switching off. See Figure 13.

 **$t_D$** 

Off time or on time measured between the 90% points of both switches, when switching from one address state to another. See Figure 14.

**Crosstalk**

A measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.

**Off Isolation**

A measure of unwanted signal coupling through an off switch.

**Bandwidth**

The frequency at which the output is attenuated by –3 dB.

**On Response**

The frequency response of the on switch.

**On Loss**

The voltage drop across the on switch, seen on the on response vs. frequency plot (see Figure 7) as how many decibels (dB) the signal is away from 0 dB at very low frequencies.

APPLICATIONS INFORMATION

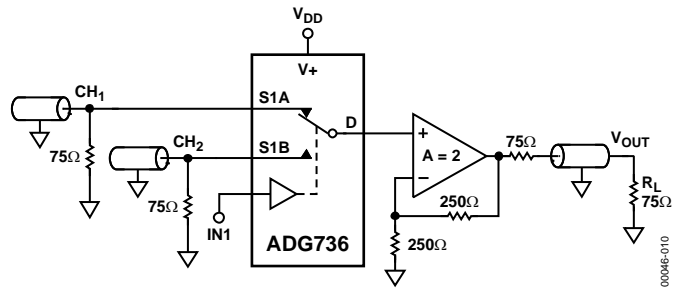


Figure 18. Using the ADG736 to Select Between Two Video Signals

