

# SGMOP07E

## 600kHz, Low Noise, High Voltage, Precision Operational Amplifier

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### GENERAL DESCRIPTION

The SGMOP07E is a low noise, low offset voltage and high voltage operational amplifier, which can be designed into a wide range of applications. The SGMOP07E has a high gain-bandwidth product of 600kHz, a slew rate of 3V/ $\mu$ s and a quiescent current of 0.75mA at wide power supply range.

The SGMOP07E is designed to provide optimal performance in low noise systems. It provides rail-to-rail output swing into heavy loads.

The single SGMOP07E is available in a Green SOIC-8 package. It is specified over the extended -40°C to +125°C temperature range.

### FEATURES

- Rail-to-Rail Output
- Low Bias Current:  $\pm 1$ nA (TYP)
- High Open-Loop Gain: 130dB at  $V_S = \pm 15$ V
- High PSRR: 135dB
- Gain-Bandwidth Product: 600kHz
- Low Noise: 8.5nV/ $\sqrt{\text{Hz}}$  at 1kHz
- Supply Voltage Range:  
3.6V to 36V or  $\pm 1.8$ V to  $\pm 18$ V
- Input Common Mode Voltage Range:  
 $(-V_S) + 1.5$ V to  $(+V_S) - 2$ V
- Low Quiescent Current: 0.75mA (TYP)
- -40°C to +125°C Operating Temperature Range
- Available in a Green SOIC-8 Package

### APPLICATIONS

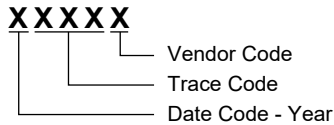
Sensors  
Audio  
Active Filters  
A/D Converters  
Communications  
Test Equipment  
Cellular and Cordless Phones  
Laptops and PDAs  
Photodiode Amplification

**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMOP07E	SOIC-8	-40°C to +125°C	SGMOP07EXS8G/TR	SGM OP07EXS8 XXXXX	Tape and Reel, 4000

**MARKING INFORMATION**

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

- Supply Voltage, +V<sub>S</sub> to -V<sub>S</sub> ..... 40V
- Input Common Mode Voltage Range  
..... (-V<sub>S</sub>) - 0.3V to (+V<sub>S</sub>) + 0.3V
- Package Thermal Resistance @ T<sub>A</sub> = +25°C
- SOIC-8, θ<sub>JA</sub>..... 105°C/W
- SOIC-8, θ<sub>JB</sub>..... 57°C/W
- SOIC-8, θ<sub>JC</sub>..... 43.5°C/W
- Junction Temperature.....+150°C
- Storage Temperature Range .....-65°C to +150°C
- Lead Temperature (Soldering, 10s).....+260°C
- ESD Susceptibility
- HBM.....2000V
- MM.....250V
- CDM ..... 1000V

**RECOMMENDED OPERATING CONDITIONS**

- Supply Voltage Range .....3.6V to 36V
- Operating Temperature Range .....-40°C to +125°C

**OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

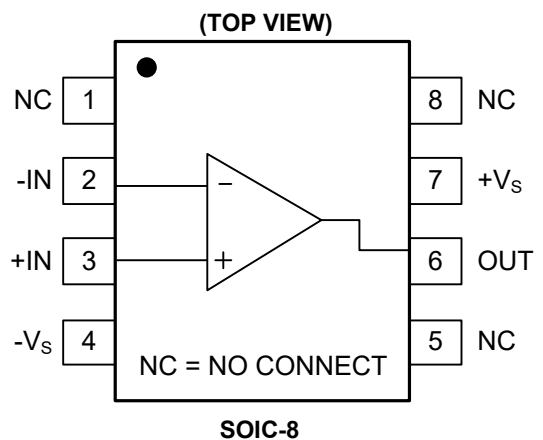
**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

**PIN CONFIGURATION**



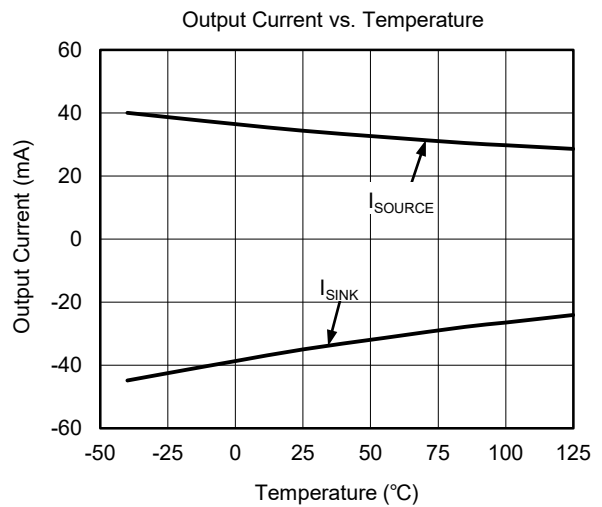
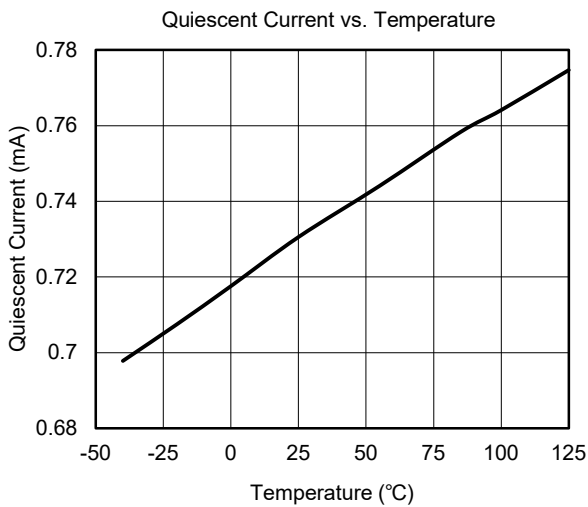
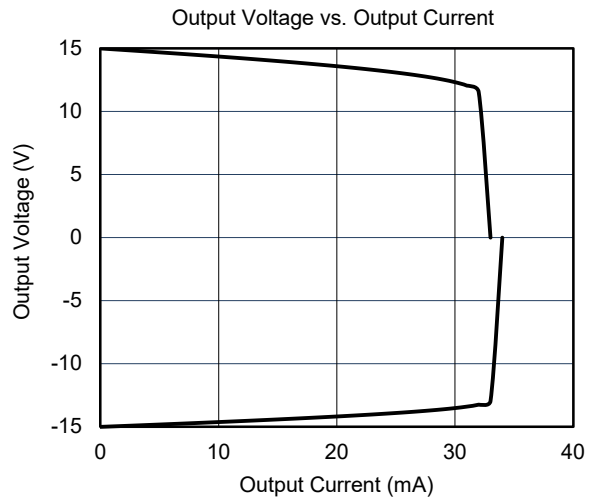
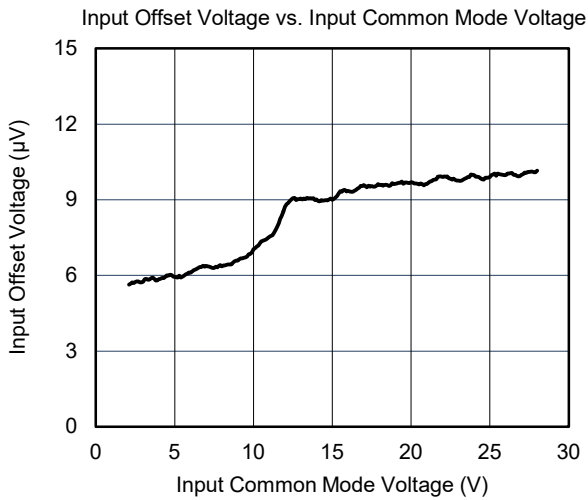
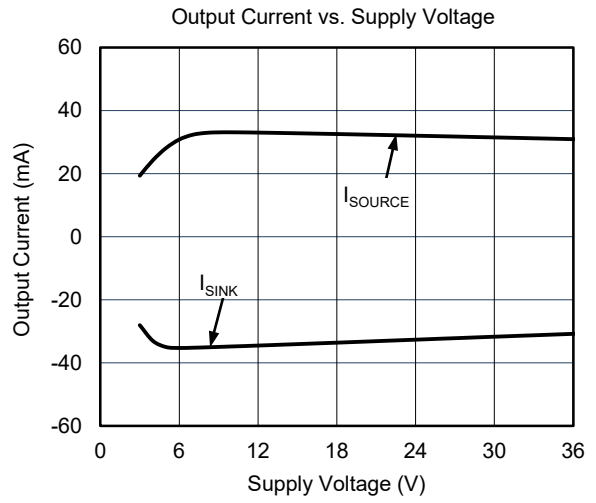
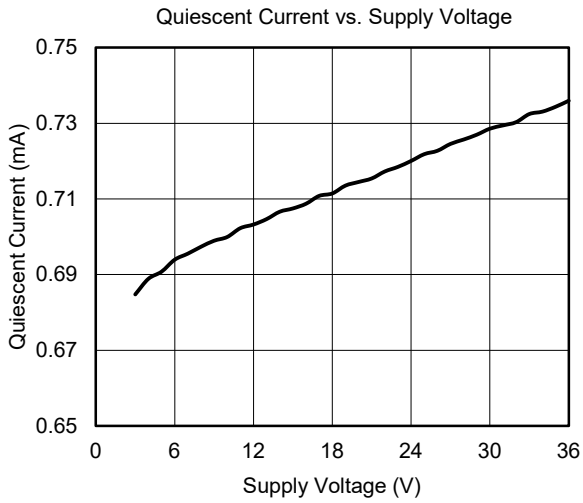
**ELECTRICAL CHARACTERISTICS**

(At T<sub>A</sub> = +25°C, V<sub>S</sub> = ±5V to ±15V, V<sub>CM</sub> = 0V, V<sub>OUT</sub> = 0V and R<sub>L</sub> = 2kΩ connected to 0V, Full = -40°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>Input Characteristics</b>							
Input Offset Voltage	V <sub>OS</sub>		+25°C		35	150	μV
			Full			220	
Input Bias Current	I <sub>B</sub>		+25°C		±1	±12	nA
			Full			±45	
Input Offset Current	I <sub>OS</sub>		+25°C		±1	±12	nA
			Full			±35	
Input Common Mode Voltage Range	V <sub>CM</sub>		Full	(-V <sub>S</sub> ) + 1.5		(+V <sub>S</sub> ) - 2	V
Common Mode Rejection Ratio	CMRR	(-V <sub>S</sub> ) + 1.5V ≤ V <sub>CM</sub> ≤ (+V <sub>S</sub> ) - 2V	+25°C	120	140		dB
			Full	115			
Open-Loop Voltage Gain	A <sub>OL</sub>	V <sub>S</sub> = ±5V, V <sub>OUT</sub> = ±2.5V, R <sub>L</sub> = 10kΩ	+25°C	115	135		dB
			Full	112			
		V <sub>S</sub> = ±15V, V <sub>OUT</sub> = ±10V, R <sub>L</sub> = 10kΩ	+25°C	120	135		
			Full	117			
		V <sub>S</sub> = ±5V, V <sub>OUT</sub> = ±2.5V, R <sub>L</sub> = 2kΩ	+25°C	110	124		
			Full	106			
		V <sub>S</sub> = ±15V, V <sub>OUT</sub> = ±10V, R <sub>L</sub> = 2kΩ	+25°C	120	130		
			Full	112			
Input Offset Voltage Drift	ΔV <sub>OS</sub> /ΔT		Full		0.3		μV/°C
<b>Output Characteristics</b>							
Output Voltage Swing from Rail	V <sub>OUT</sub>	V <sub>S</sub> = ±15V, R <sub>L</sub> = 10kΩ	+25°C		90	120	mV
			Full			165	
		V <sub>S</sub> = ±15V, R <sub>L</sub> = 2kΩ	+25°C		450	600	
			Full			820	
Output Short-Circuit Current	I <sub>SC</sub>	V <sub>S</sub> = ±15V	+25°C	±21	±34		mA
<b>Power Supply</b>							
Operating Voltage Range	V <sub>S</sub>		Full	3.6		36	V
Quiescent Current	I <sub>Q</sub>	I <sub>OUT</sub> = 0mA	+25°C		0.75	0.9	mA
			Full			1	
Power Supply Rejection Ratio	PSRR	V <sub>S</sub> = 3V to 38V	+25°C	123	135		dB
			Full	120			
<b>Dynamic Performance</b>							
Gain-Bandwidth Product	GBP	V <sub>OUT</sub> = 100mV <sub>P-P</sub> , C <sub>L</sub> = 10pF	+25°C		600		kHz
Slew Rate	SR		+25°C		3		V/μs
Settling Time to 0.1%	t <sub>S</sub>	V <sub>IN</sub> = 1V Step, G = +1	+25°C		3.5		μs
Overload Recovery Time		V <sub>IN</sub> × G = V <sub>S</sub>	+25°C		1.5		μs
Phase Margin	φ <sub>O</sub>	V <sub>OUT</sub> = 100mV <sub>P-P</sub> , C <sub>L</sub> = 10pF	+25°C		60		°
Total Harmonic Distortion + Noise	THD+N	V <sub>IN</sub> = 1V <sub>RMS</sub> , G = +1, f = 1kHz	+25°C		0.0008		%
<b>Noise</b>							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25°C		300		nV <sub>P-P</sub>
Input Voltage Noise Density	e <sub>n</sub>	f = 1kHz	+25°C		8.5		nV/√Hz
Input Current Noise Density	i <sub>n</sub>	f = 1kHz	+25°C		1.5		pA/√Hz

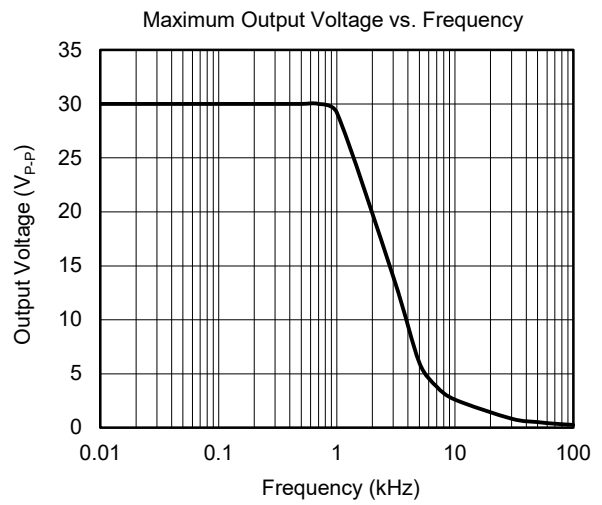
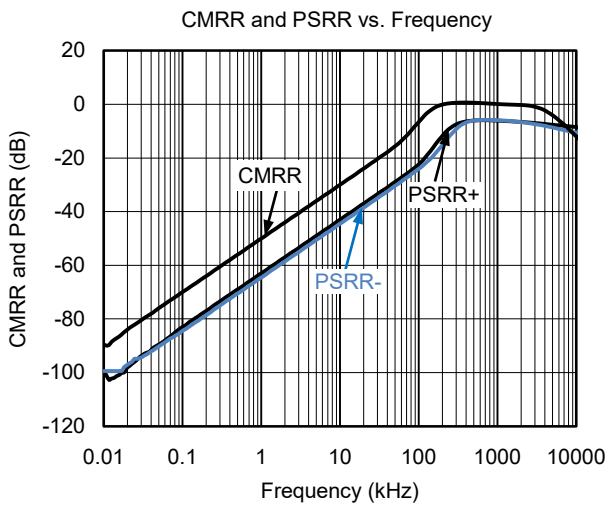
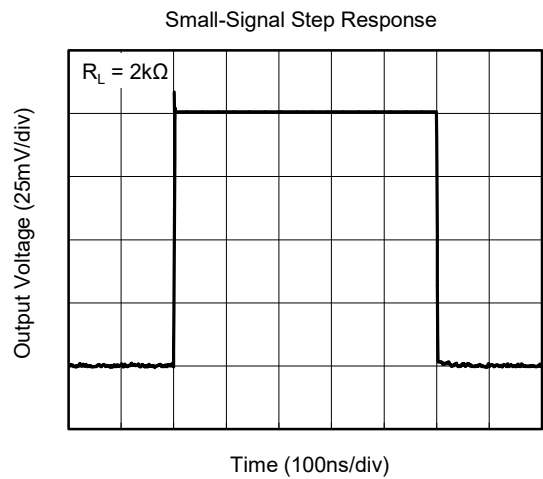
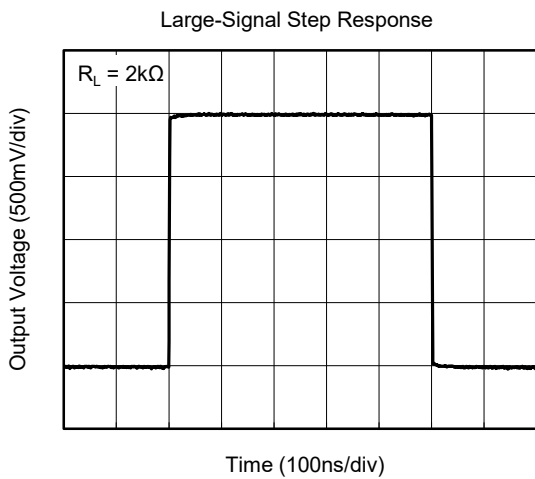
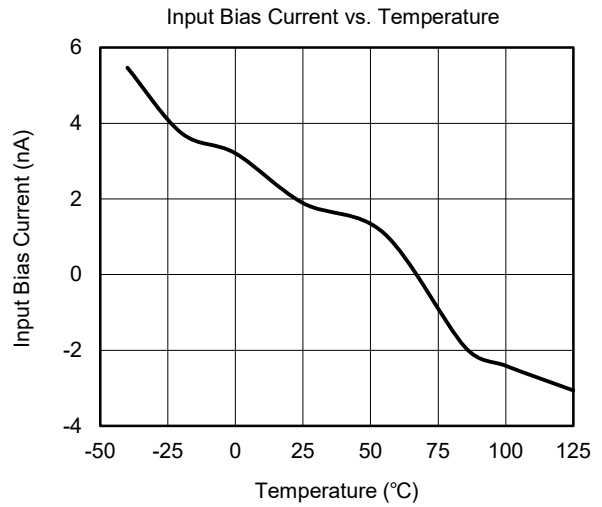
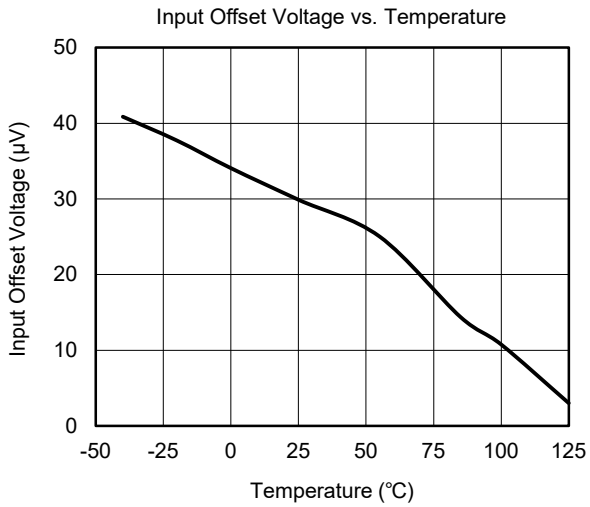
**TYPICAL PERFORMANCE CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$  and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



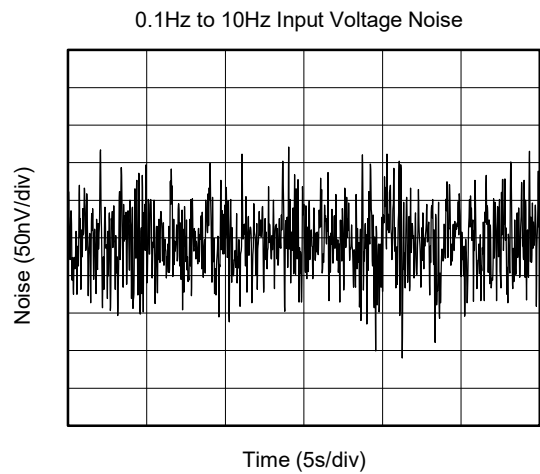
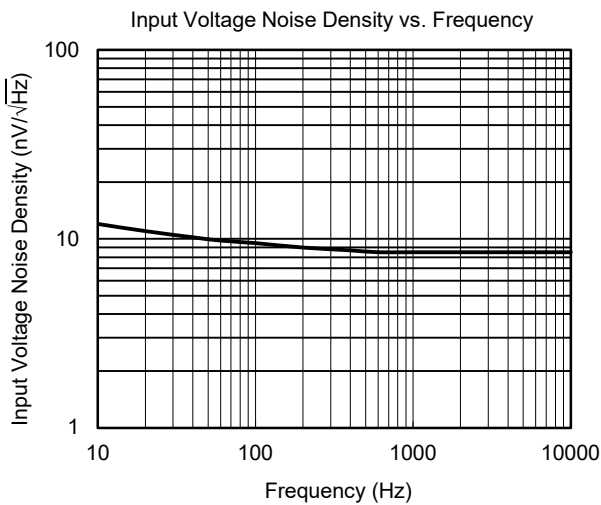
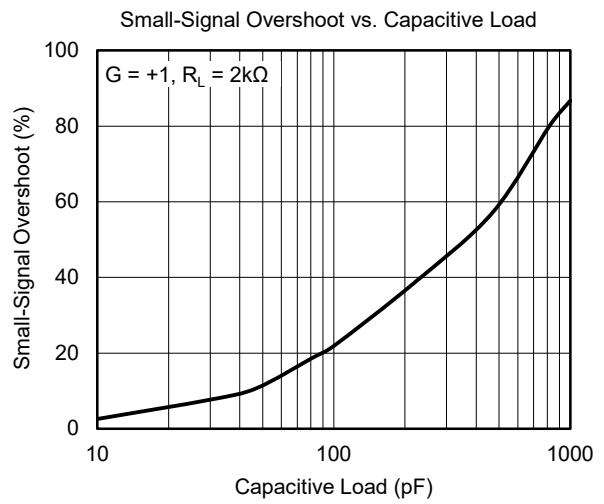
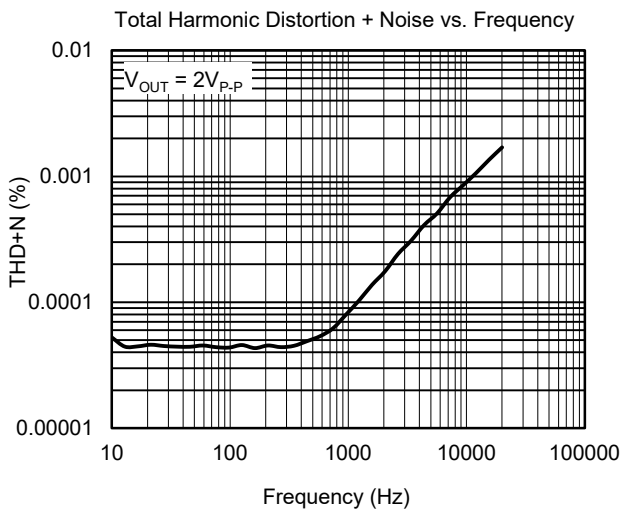
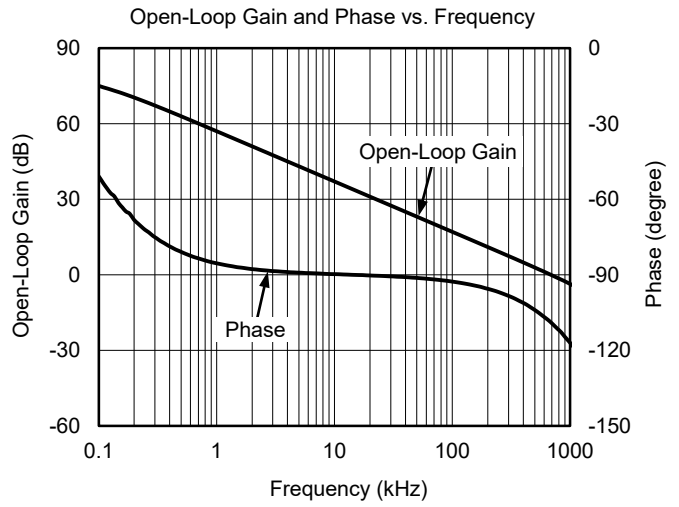
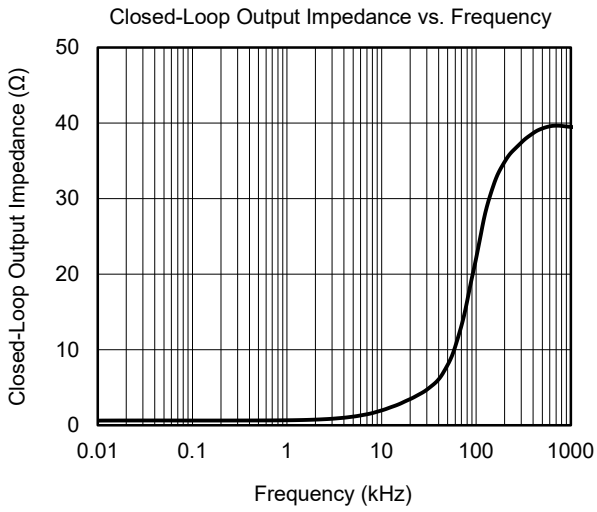
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$  and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



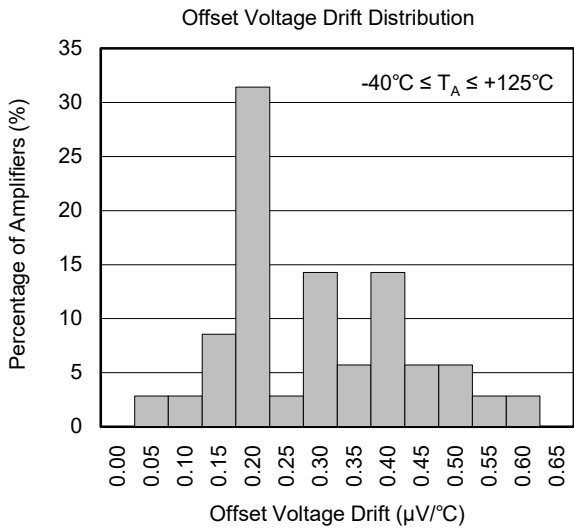
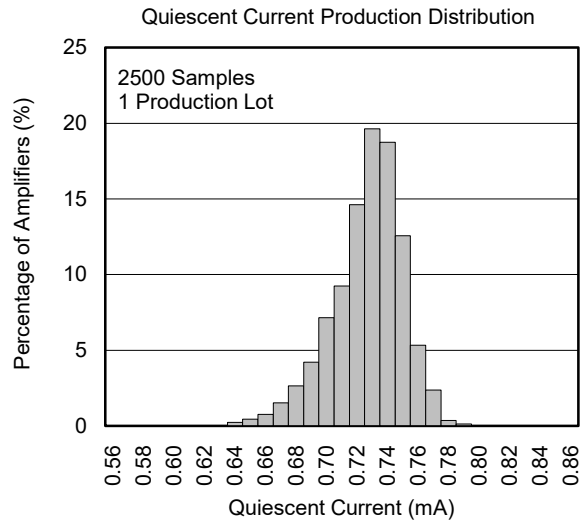
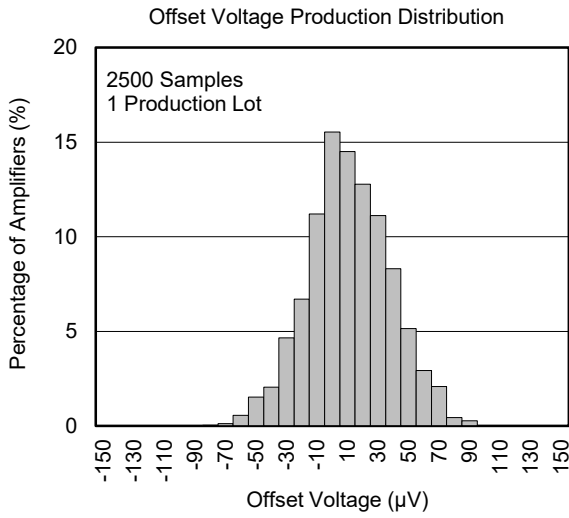
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$  and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$  and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



**APPLICATION NOTES**

**Power Supply Bypassing and Layout**

The SGMOP07E operates from either a single 3.6V to 36V supply or dual  $\pm 1.8V$  to  $\pm 18V$  supplies. For single-supply operation, bypass the power supply  $+V_S$  with a  $0.1\mu F$  ceramic capacitor which should be placed close to the  $+V_S$  pin. For dual-supply operation, both the  $+V_S$  and the  $-V_S$  supplies should be bypassed to ground with separate  $0.1\mu F$  ceramic capacitors.  $10\mu F$  tantalum capacitor can be added for better performance.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the operational amplifier's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible.

For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency current loop area small to minimize the EMI (electromagnetic interference).

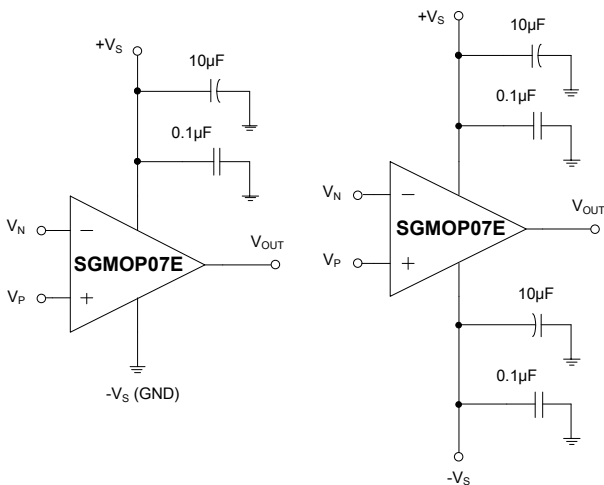


Figure 1. Amplifier with Bypass Capacitors

**Grounding**

A ground plane layer is important for SGMOP07E circuit design. The length of the current path in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

**Input-to-Output Coupling**

To minimize capacitive coupling, the input and output signal traces should not be in parallel. This helps reduce unwanted positive feedback.

**Differential Amplifier**

The circuit shown in Figure 2 performs the difference function. If the resistor ratios are equal ( $R_4/R_3 = R_2/R_1$ ), then  $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$ .

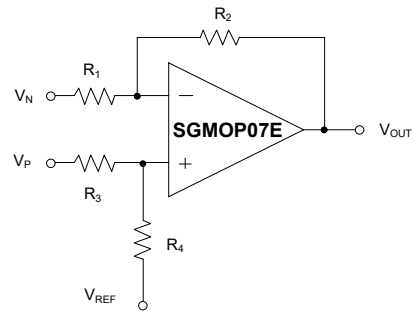


Figure 2. Differential Amplifier

**Instrumentation Amplifier**

The circuit in Figure 3 performs the same function as that in Figure 2 but with a high input impedance.

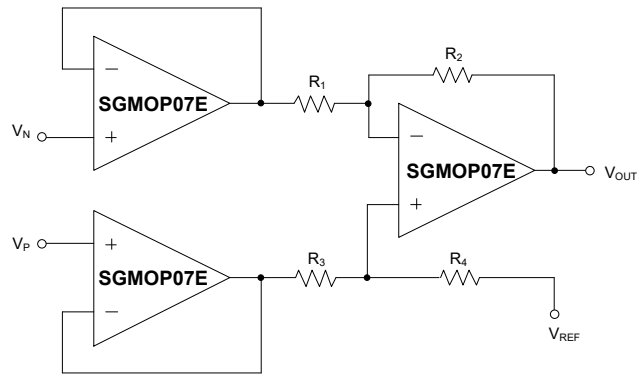


Figure 3. Instrumentation Amplifier

**Active Low-Pass Filter**

The low-pass filter shown in Figure 4 has a DC gain of  $(-R_2/R_1)$  and the  $-3dB$  corner frequency is  $1/2\pi R_2 C$ . Make sure the filter bandwidth is within the bandwidth of the amplifier. Feedback resistors with large values can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistor values as low as possible and consistent with output loading consideration.

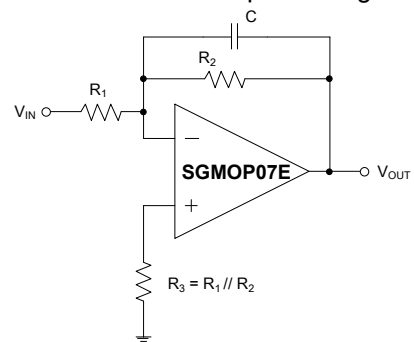


Figure 4. Active Low-Pass Filter



**REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>NOVEMBER 2020 – REV.A to REV.A.1</b>	<b>Page</b>
Updated Marking Information section.....	2
Updated Absolute Maximum Ratings section.....	2

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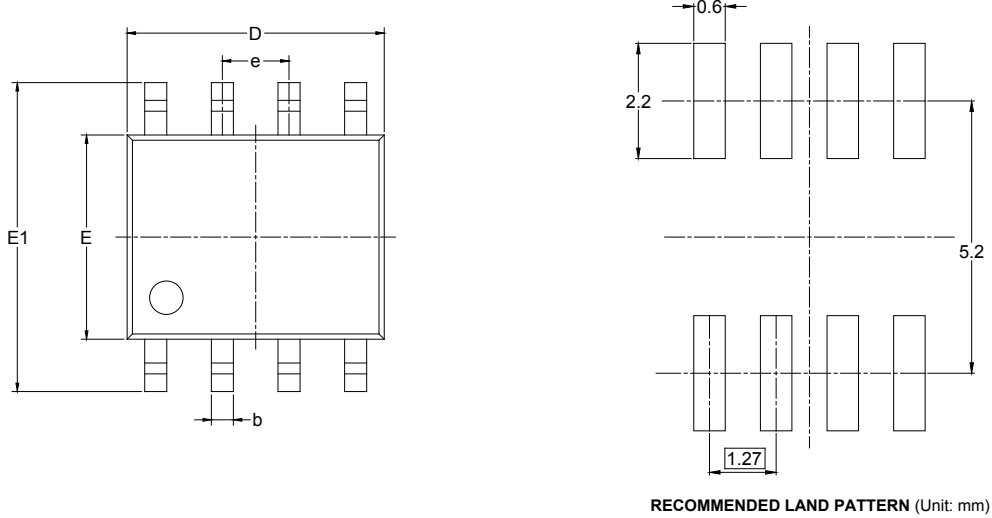
<b>Changes from Original (DECEMBER 2017) to REV.A</b>	<b>Page</b>
Changed from product preview to production data.....	All

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# PACKAGE INFORMATION

## PACKAGE OUTLINE DIMENSIONS

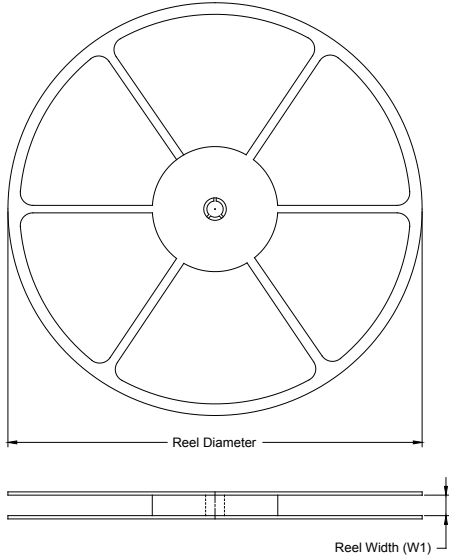
### SOIC-8



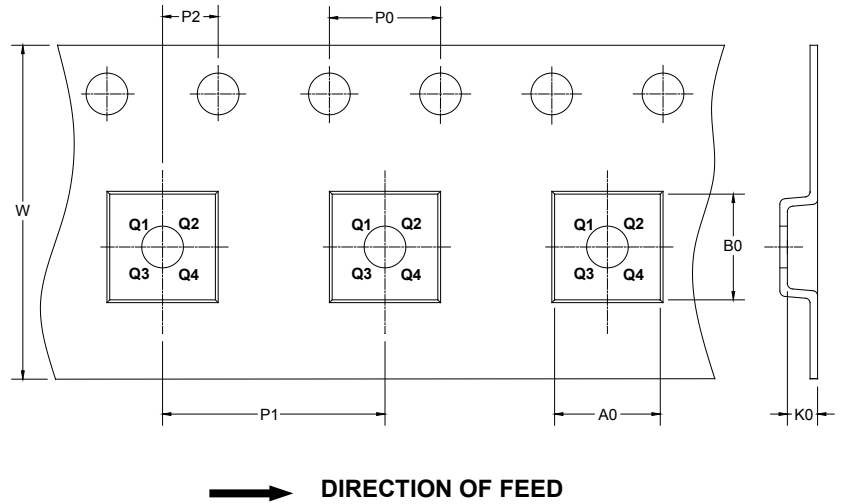
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

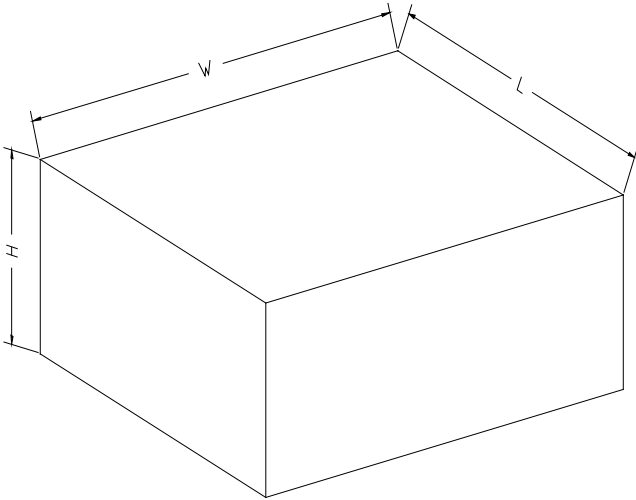
**KEY PARAMETER LIST OF TAPE AND REEL**

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002