

## Features

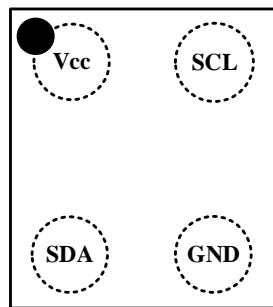
- Compatible with all I<sup>2</sup>C bidirectional data transfer protocol
- Memory array:
  - 128 Kbits (8 Kbytes) of EEPROM
  - Page size: 64 bytes
- Single supply voltage and high speed:
  - 1MHz@1.8V
- Random and sequential Read modes
- Write:
  - Byte Write within 3 ms
  - Page Write within 3 ms
- Partial Page Writes Allowed
- Software data Protection
- Slave Address Configurable
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
- WLCSP4 Package

## Description

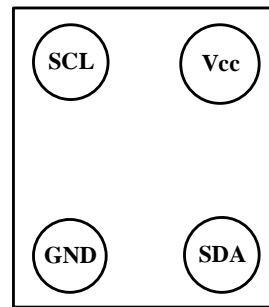
- The BL24SA128B provides 131,072 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 16,384 words of 8 bits each.
- The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

## Pin Configuration

### WLCSP 4 Ball Pitch 0.4mm\*0.5mm

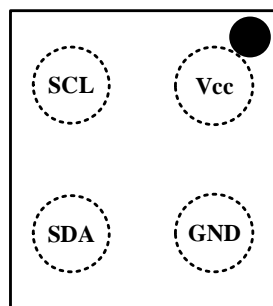


**Marking side  
(Top view)**

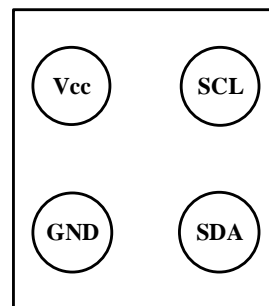


**Pads side  
(Bottom view)**

### WLCSP 4 Ball Pitch 0.4mm\*0.4mm



**Marking side  
(Top view)**



**Pads side  
(Bottom view)**

### Pin Descriptions

Pin Name	Type	Functions
SDA	I/O	Serial Data
SCL	I	Serial Clock Input
GND	P	Ground
Vcc	P	Power Supply

Table 1

### Block Diagram

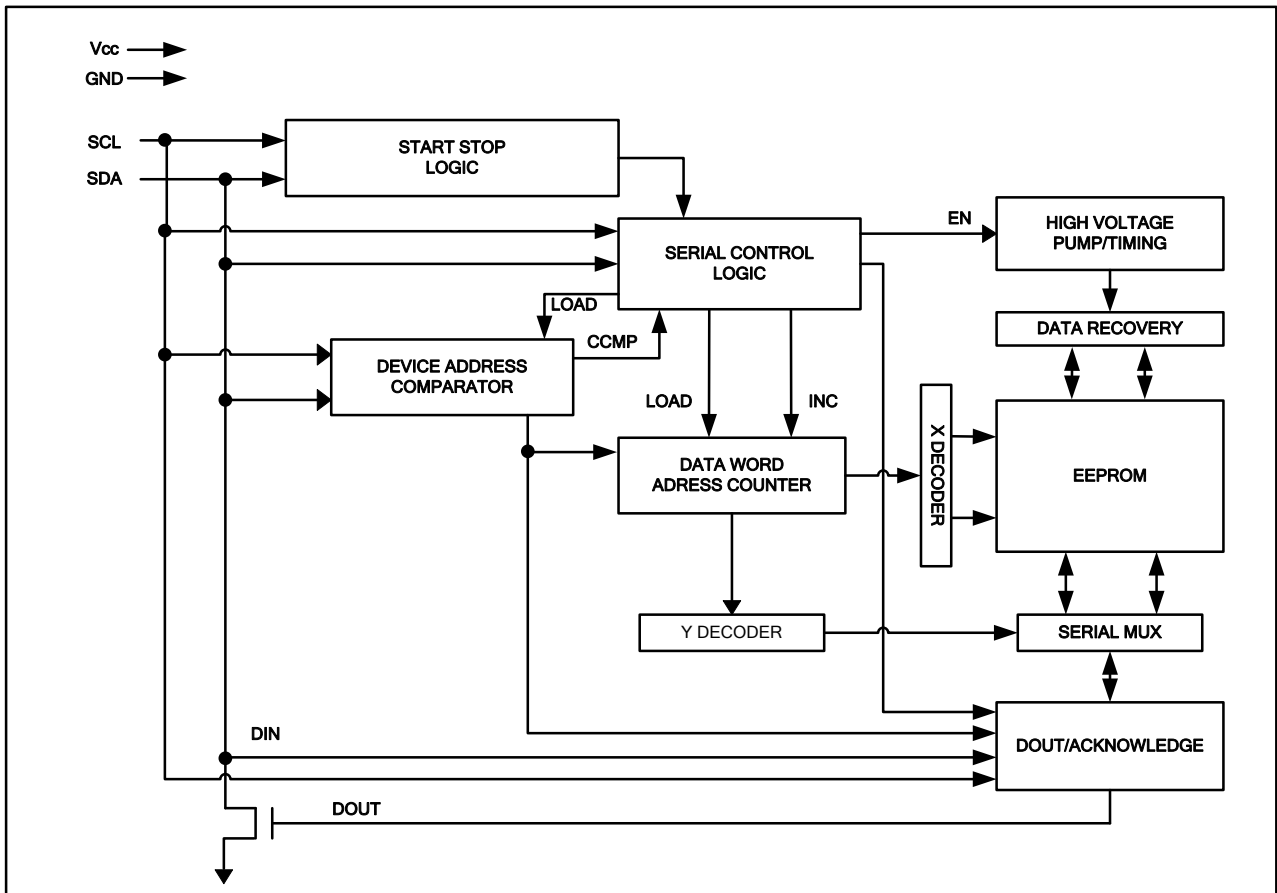


Figure 1

**SERIAL DATA (SDA):** The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

## Functional Description

### 1. Memory Organization

BL24SA128B, 128k SERIAL EEPROM: Internally organized with 256 pages of 64 bytes each, the 128k requires a 14-bit data word address for random word addressing.

### 2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The BL24SA128B features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Lock SDA high in each cycle while SCL is high.
3. Create a start condition.

Figure 2. Data Validity

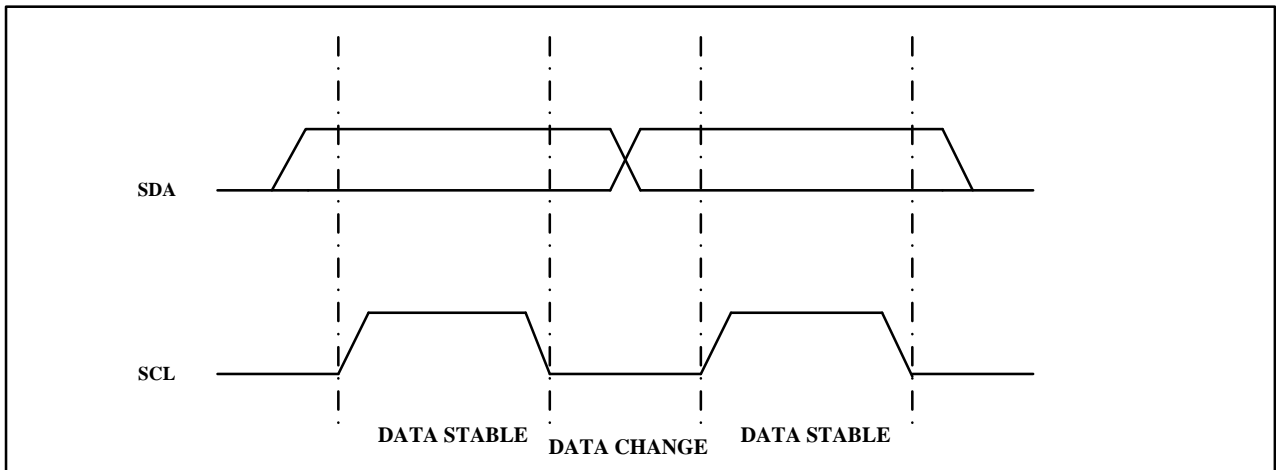


Figure 3. Start and Stop Definition

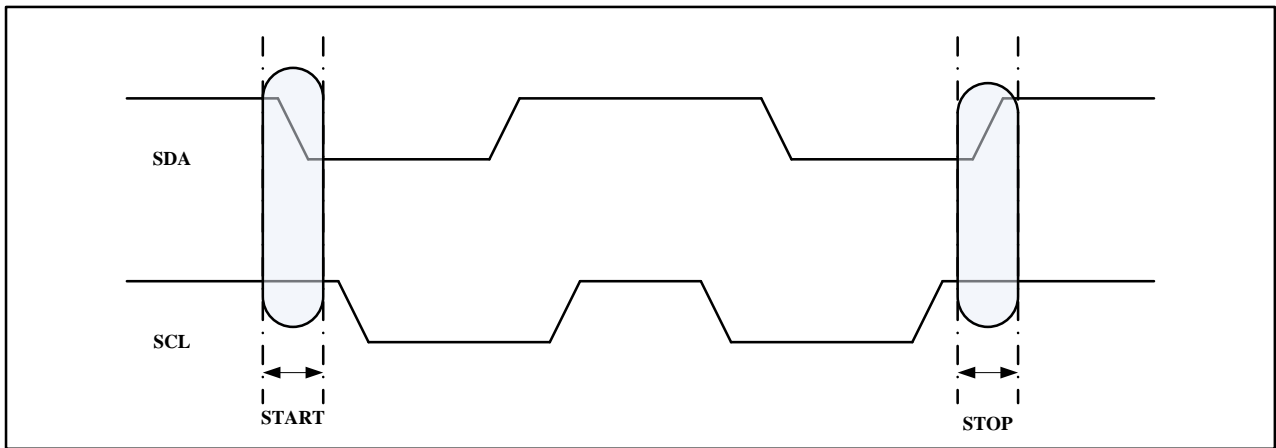
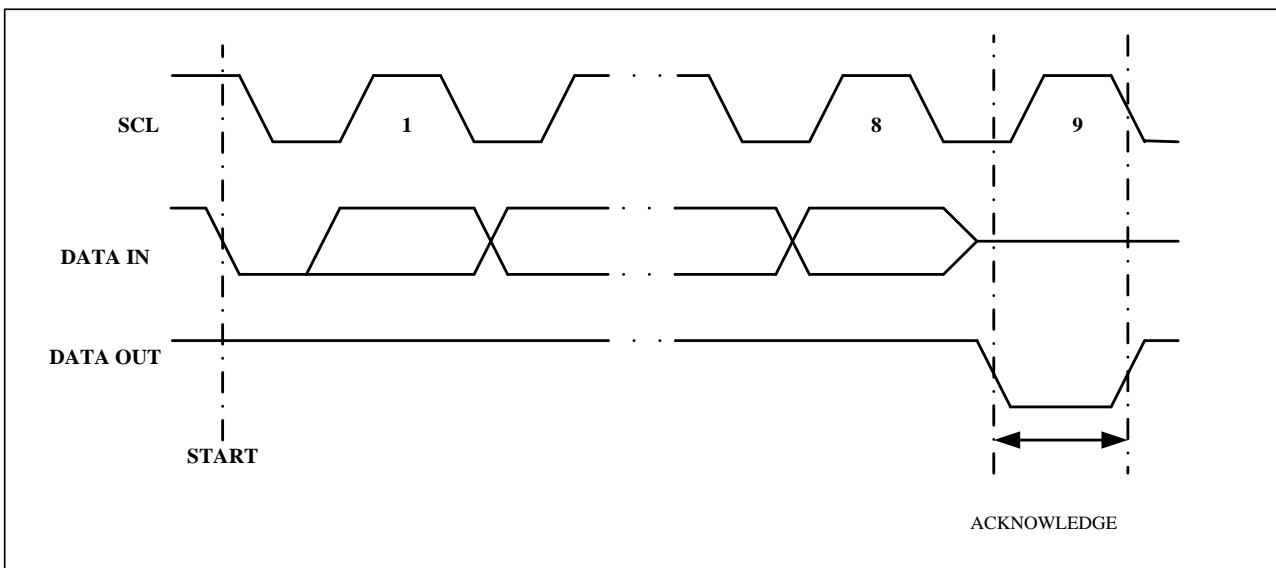
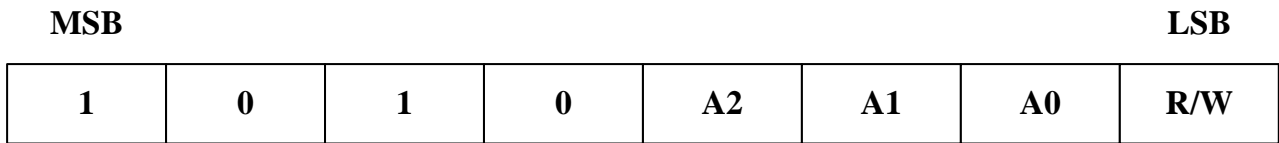


Figure 4. Output Acknowledge



### 3. Device Addressing

The 128k EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)



**Figure 5. Device Address**

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The fifth, sixth and seventh bits of the device address can be configured, default to 000b.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

BL24SA128B consists of a series of products with different fab-out default device address.

Part Number	A2	A1	A0
BL24SA128B	0	0	0
BL24SA128BA2	0	0	1
BL24SA128BA4	0	1	0
BL24SA128BA6	0	1	1
BL24SA128BA8	1	0	0
BL24SA128BAA	1	0	1
BL24SA128BAC	1	1	0
BL24SA128BAE	1	1	1

Table 2



### 5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

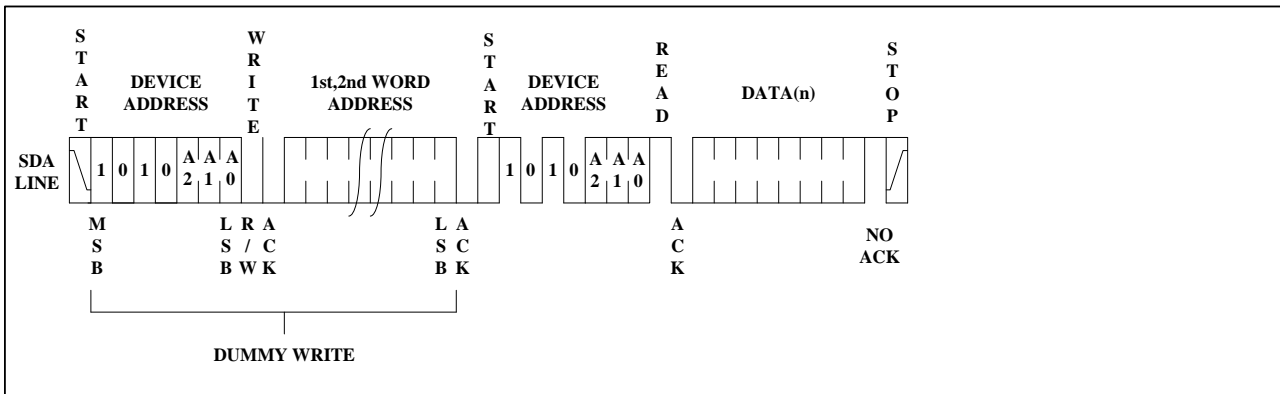
**CURRENT ADDRESS READ:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 9**).



**Figure 9. Current Address Read**

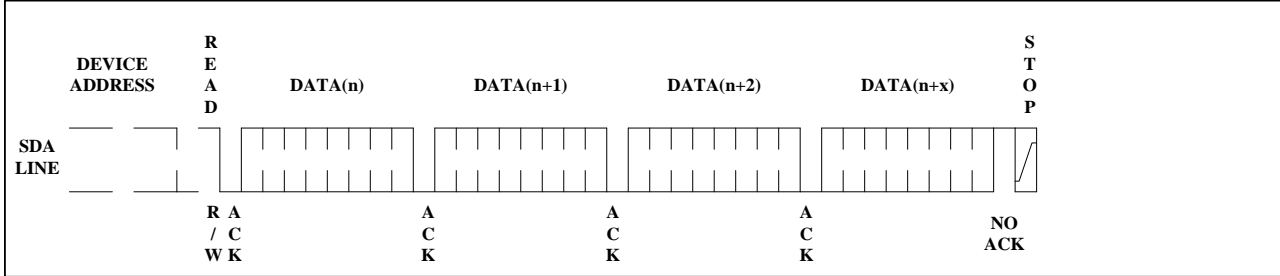
**RANDOM READ:**

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**).



**Figure 10. Random Read**

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 11**).



**Figure 11. Sequential Read**



## 6. Software write protection configuration

By writing specific values in a register (Table 3) located at address 11xx.xxxx.xxxx.xxxx<sub>b</sub>, the memory array can be write-protected by blocks.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write	★	★	★	★	Partial Write protect activation	Size of write protected block	Size of write protected block	★
Read	0	0	0	0				0

Table 3

Notes:

Bit 7 – 4 and bit 0 are don't care bits.

Bit 3 enables or disables the partial write protection.

Bit 3=0: the whole memory can be written (no write protection)

Bit 3=1: the concerned block is write-protected

Bits 2 and 1 define the size of the memory block to be protected against write instructions:

Bit 2, Bit 1= 0, 0: the upper quarter of memory is write-protected

Bit 2, Bit 1= 0, 1: the upper half memory is write-protected

Bit 2, Bit 1= 1, 0: the upper 3/4 of memory are write-protected

Bit 2, Bit 1= 1, 1: the whole memory and the device addressing config register are write-protected

The device is delivered with the Write Protect register set to 0 (00h).

## 7. Device Addressing configuration

By writing specific values in a register (Table 4) located at address 10xx.xxxx.xxxx.xxxx<sub>b</sub>, the device address can be reconfigured.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write	★	★	★	★	★	A2	A1	A0
Read	0	0	0	0	0			

Table 4

Note:

While the SWR register (Table 3) set to "0x0E", bit3, bit 2, bit 1= 1, 1, 1, the device addressing config register (Table 4) is write-protected.

## 8. Electrical Characteristics

Absolute Maximum Stress Ratings:

- DC Supply Voltage . . . . . -0.3V to +6.5V
- Input / Output Voltage . . . . . GND-0.3V to VCC+0.3V
- Operating Ambient Temperature . . . . . -40°C to +85°C
- Storage Temperature . . . . . -65°C to +150°C

Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40°C to +85°C, VCC = +1.7V to +3.6V (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	VCC1	1.7	-	3.6	V	-
Supply Current VCC=1.8V	ICC1	-	0.14	0.3	mA	READ at 400KHZ
Supply Current VCC=1.8V	ICC2	-	0.28	0.5	mA	WRITE at 400KHZ
Supply Current VCC=1.8V	ISB1	-	0.03	0.5	μA	VIN=VCC or VSS
Input Leakage Current	IL1	-	0.10	1.0	μA	VIN=VCC or VSS
Output Leakage Current	ILO	-	0.05	1.0	μA	VOUT=VCC or VSS
Input Low Level	VIL1	-0.3	-	VCC×0.3	V	VCC=1.7V to 5.5V
Input High Level	VIH1	VCC×0.7	-	VCC+0.3	V	VCC=1.7V to 5.5V
Output Low Level VCC=1.7V	VOL1	-	-	0.2	V	IOL=0.15mA
Output Low Level VCC=5.0V	VOL2	-	-	0.4	V	IOL=3.0mA

Table 5

### Pin Capacitance

Applicable over recommended operating range from TA = 25°C, f = 1.0 MHz, VCC = +1.7V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance (SDA)	CI/O	-	-	8	pF	VI0=0V
Input Capacitance (A0, A1, A2, SCL)	CIN	-	-	6	pF	VIN=0V

Table 6

**AC Electrical Characteristics**

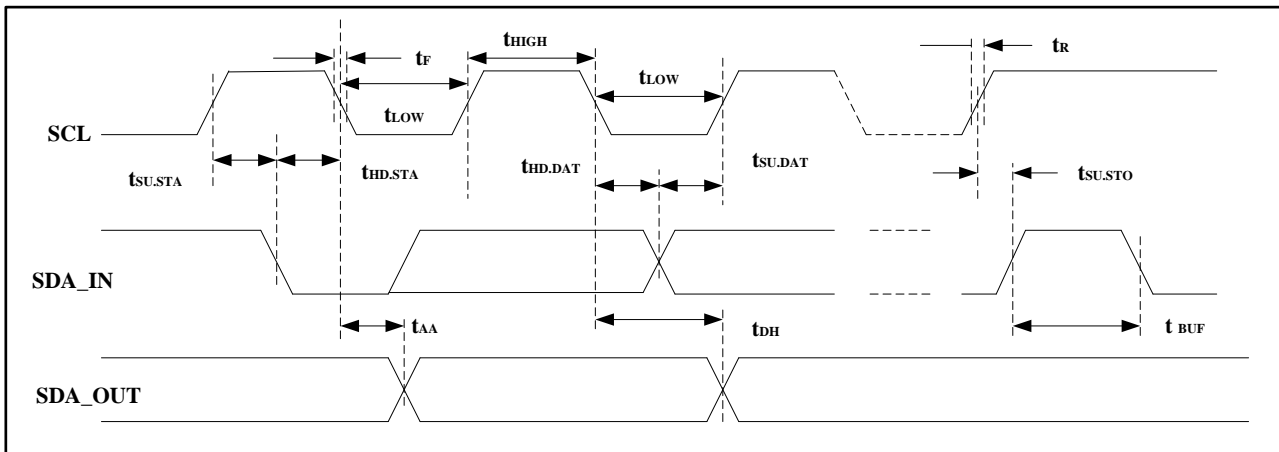
Applicable over recommended operating range from TA = -40°C to +85°C, VCC = +1.7V to +3.6V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Frequency, SCL	f <sub>SCL</sub>	-	-	400	-	-	1000	KHZ
Clock Pulse Width Low	t <sub>LOW</sub>	1.3	-	-	0.5	-	-	μ s
Clock Pulse Width High	t <sub>HIGH</sub>	0.6	-	-	0.26	-	-	μ s
Noise Suppression Time	t <sub>I</sub>	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t <sub>AA</sub>	-	-	0.9	-	-	0.45	μ s
Time the bus must be free before a new transmission can start	t <sub>BUF</sub>	1.3	-	-	0.5	-	-	μ s
Start Hold Time	t <sub>HD:STA</sub>	0.6	-	-	0.25	-	-	μ s
Start Setup Time	t <sub>SU:STA</sub>	0.6	-	-	0.25	-	-	μ s
Data In Hold Time	t <sub>HD:DAT</sub>	0	-	-	0	-	-	μ s
Data in Setup Time	t <sub>SU:DAT</sub>	100	-	-	100	-	-	ns
Input Rise Time(1)	t <sub>R</sub>	-	-	0.3	-	-	0.12	μ s
Input Fall Time(1)	t <sub>F</sub>	-	-	0.3	-	-	0.12	μ s
Stop Setup Time	t <sub>SU:STO</sub>	0.6	-	-	0.25	-	-	μ s
Data Out Hold Time	t <sub>DH</sub>	50	-	-	50	-	-	ns
Write Cycle Time	t <sub>WR</sub>	-	1.9	3	-	1.9	3	ms
5.0V, 25°C, Byte Mode(1)	Endurance	1M	-	-	1M	-	-	Write Cycle

**Table 7****Notes:**

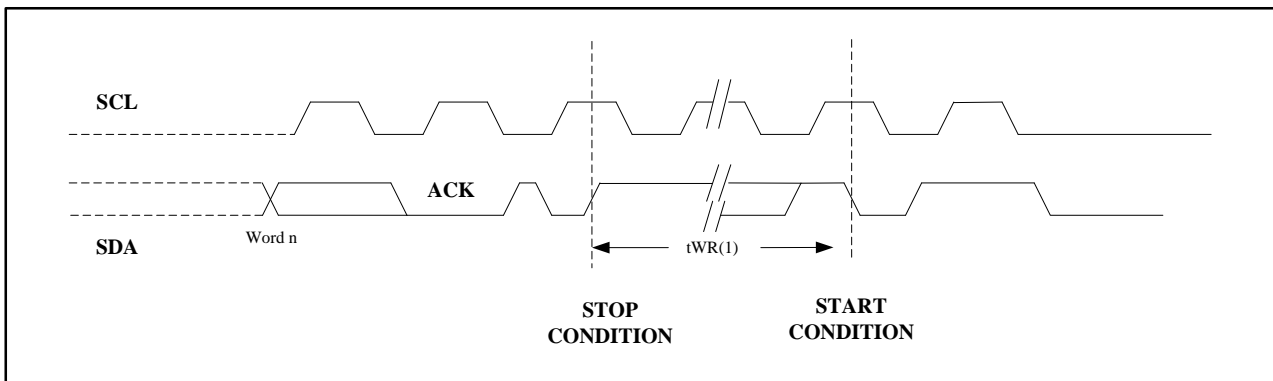
1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:  
 RL (connects to VCC): 1.3 k  
 Input pulse voltages: 0.3 VCC to 0.7 VCC  
 Input rise and fall time: 50 ns  
 Input and output timing reference voltages: 0.5 VCC  
 The value of RL should be concerned according to the actual loading on the user's system.

**Bus Timing**



**Figure 12. SCL: Serial Clock, SDA: Serial Data I/O**

**Write Cycle Timing**



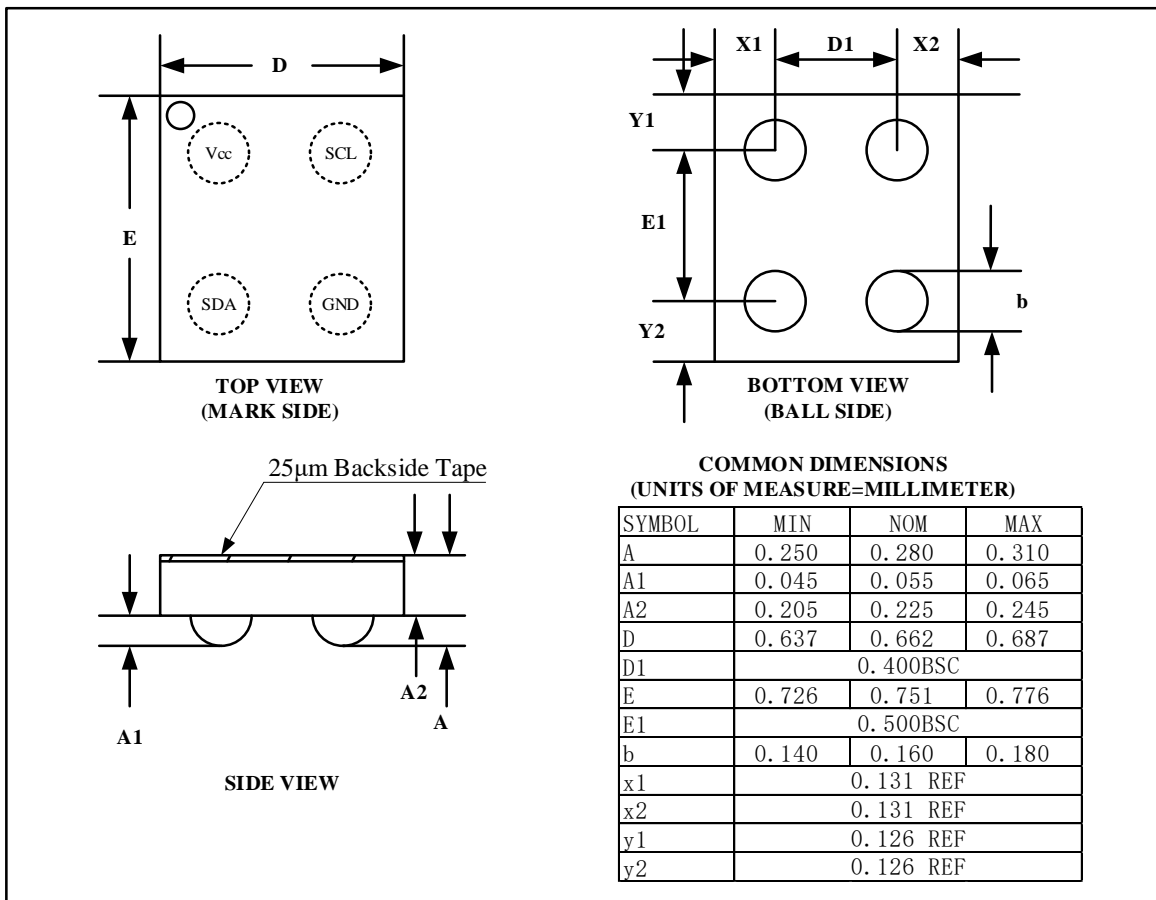
**Figure 13. SCL: Serial Clock, SDA: Serial Data I/O**

**Notes:**

The write cycle time  $t_{WR}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

**Package Information**

**WLCSP 4 Ball Pitch 0.4mm\*0.5mm**



**Figure 14**

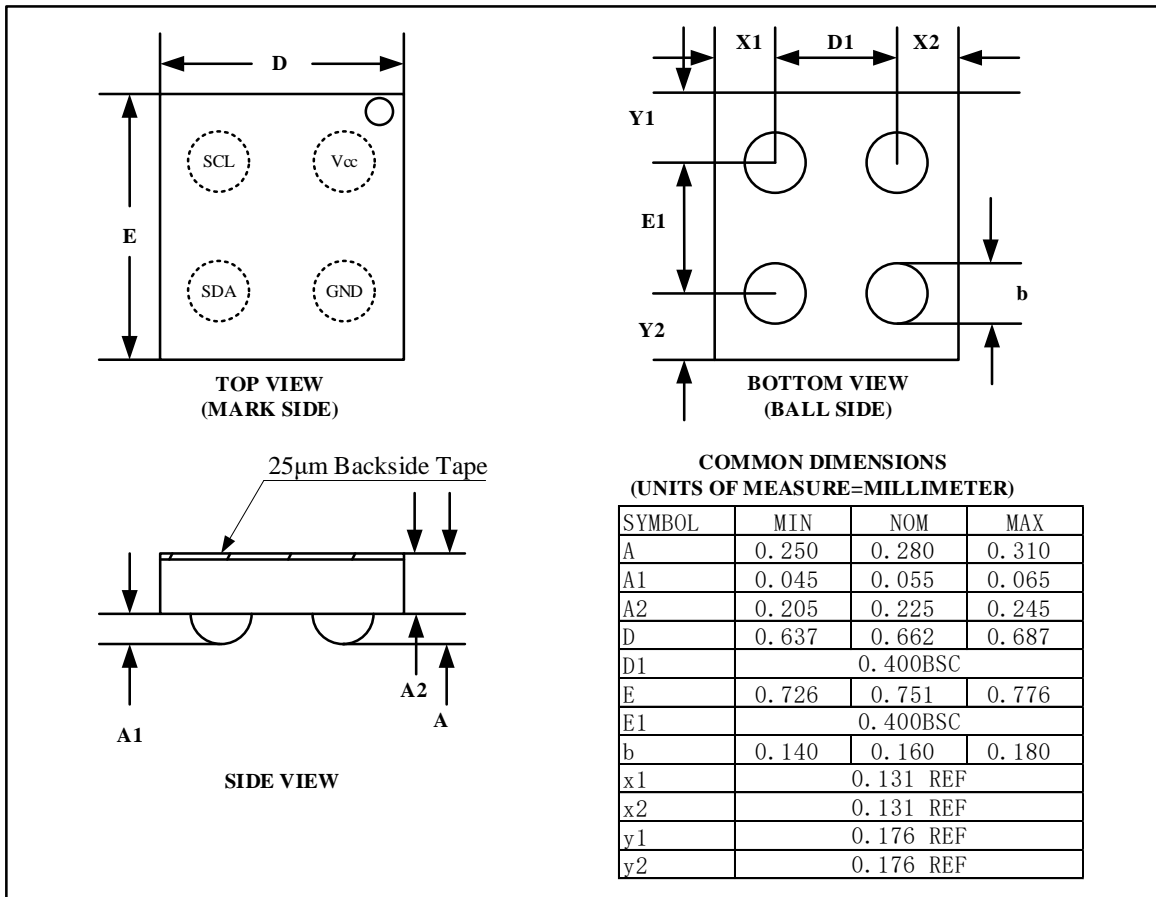
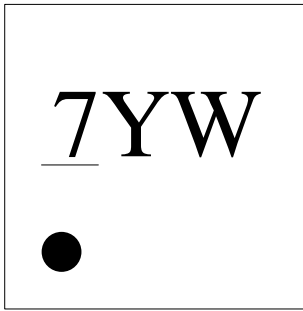


Figure 15

### Marking Diagram

WLCSP 4 Ball Pitch 0.4mm\*0.5mm



1 PIN MARK

Y: The last digits of the year

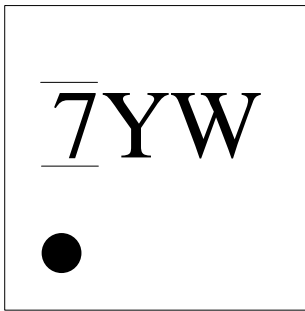
W: week code.

Y	1	...	3	4	5	...	9	0
Year	2011	...	2013	2014	2015	...	2019	2020

W	A	...	Y	Z	a	...	y	z
Week	1	...	25	26	27	...	51	52

Part Number	Mark
BL24SA128B-CS	<u>7</u> YW
BL24SA128BA2-CS	<u>7</u> YW
BL24SA128BA4-CS	<u>7</u> <u>Y</u> W
BL24SA128BA6-CS	<u>7</u> <u>Y</u> W
BL24SA128BA8-CS	<u>7</u> YW
BL24SA128BAA-CS	<u>7</u> YW
BL24SA128BAC-CS	<u>7</u> <u>Y</u> W
BL24SA128BAE-CS	<u>7</u> <u>Y</u> W

**WLCSP 4 Ball Pitch 0.4mm\*0.4mm**



**1 PIN MARK**

Y: The last digits of the year

W: week code.

Y	1	...	3	4	5	...	9	0
Year	2011	...	2013	2014	2015	...	2019	2020

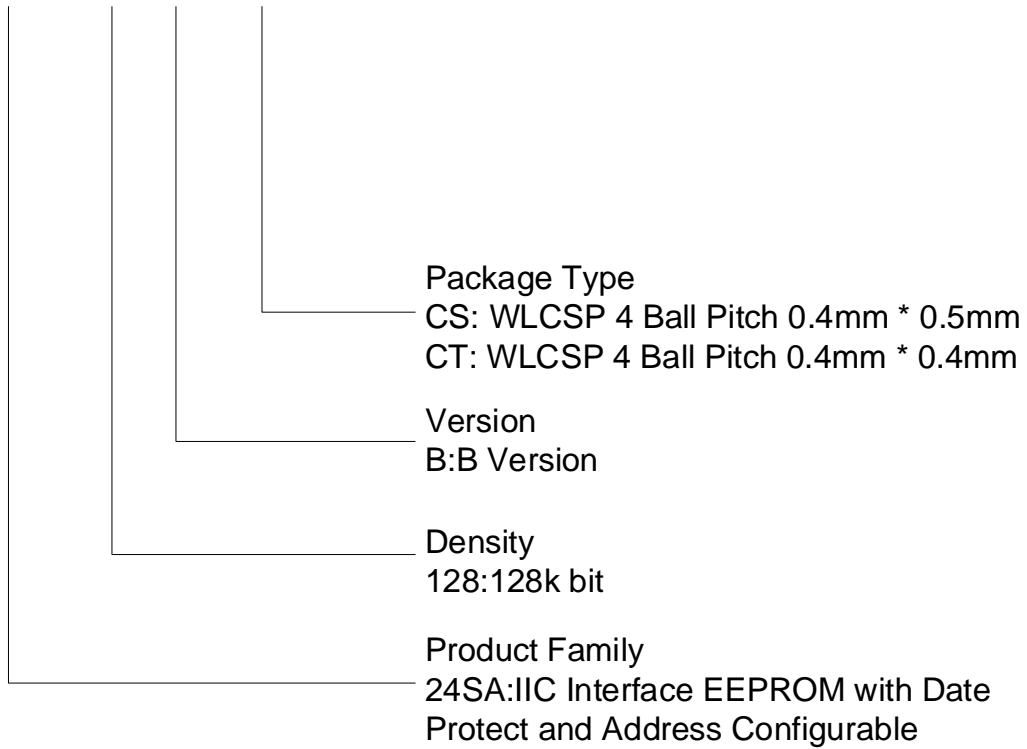
W	A	...	Y	Z	a	...	y	z
Week	1	...	25	26	27	...	51	52

Part Number	Mark
BL24SA128B-CT	<u>7</u> YW
BL24SA128BA2-CT	<u>7</u> YW
BL24SA128BA4-CT	<u>7</u> YW
BL24SA128BA6-CT	<u>7</u> YW
BL24SA128BA8-CT	<u>7</u> YW
BL24SA128BAA-CT	<u>7</u> YW
BL24SA128BAC-CT	<u>7</u> YW
BL24SA128BAE-CT	<u>7</u> YW



**Ordering Information**

BL 24SA 128 B - CS



Device	Package	Shipping (Qty/Packing)
BL24SA128B	WLCSP-4, 0.662*0.751 (Pb-Free/Halogen Free)	5000/Tape &Reel

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**Revision history**

<b>Version 1.00 BL24SA128B</b>	<b>12/5/2017</b>
Initial Version	
<b>Version 1.01 BL24SA128B</b>	<b>7/5/2018</b>
Add Marking Diagram Add WLCSP 4 Ball Pitch 400um*400um package information	
<b>Version 1.02 BL24SA128B</b>	<b>9/15/2018</b>
Modify Text and Structure of documents	
<b>Version 1.03 BL24SA128B</b>	<b>3/15/2019</b>
Modify software write protection configuration Modify the MAX frequency condition from 3.6V to 1.7V	
<b>Version 1.04 BL24SA128B</b>	<b>4/25/2019</b>
Modify WLCSP 4 Ball Pitch 0.4mm*0.4mm Package Information	
<b>Version 1.05 BL24SA128B</b>	<b>7/10/2019</b>
Modify WLCSP 4 Ball Pitch 0.4mm*0.4mm Marking Information	
<b>Version 1.06 BL24SA128B</b>	<b>8/18/2019</b>
Update ESD Characteristics Information Update Ordering Information	
<b>Version 1.07 BL24SA128B</b>	<b>6/4/2020</b>
Update the software write protection description	