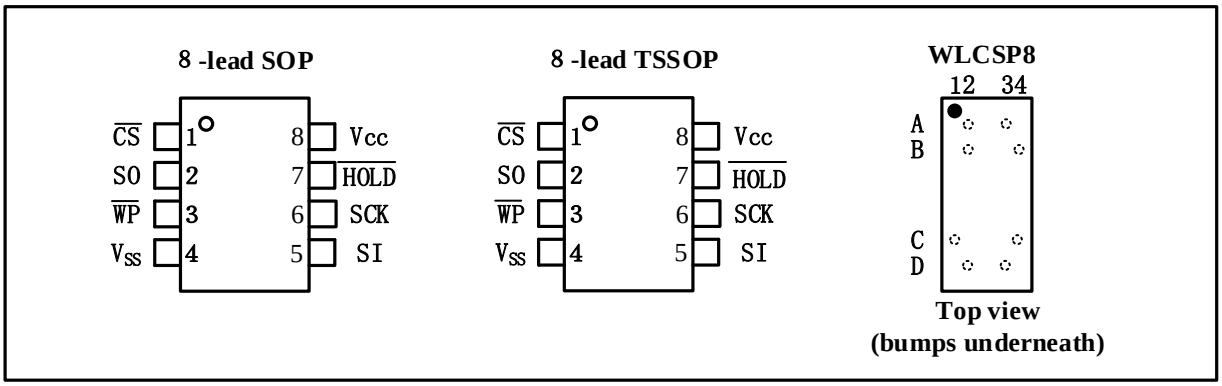
Features

- Serial Peripheral Interface (SPI) data transfer protocol
- Memory array:
  - 2M bits (256 Kbytes) of EEPROM
  - Page size: 256 bytes
  - Additional Write lockable page
- Single supply voltage and high speed:
  - 5 MHz (2.8V - 5.5V)
- Random and sequential Read modes
- Write:
  - Byte Write within 6 ms
  - Page Write within 6 ms
  - Partial Page Writes Allowed
- Write Protect: quarter, half or whole memory array
- Operating temperature range: from -40℃ to 85℃
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
  - HBM 8000V
- 8-lead SOP/TSSOP and WLCSP8 packages

Description

- The BL25CM2A devices are Electrically Erasable Programmable Memory (EEPROM) organized as 262144 x 8 bits, accessed through the SPI bus.
- The BL25CM2A can operate with a supply range from 2.8V to5.5V. These devices are guaranteed over the -40 °C/+85 °C temperature range.
- The BL25CM2A offers an additional page, named the Identification Page (256 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Pin Configuration



Pin Descriptions

Pin Name	Type	Functions
$\overline{CS}$	I	Chip Select
SO	O	Serial Data Output
$\overline{WP}$	I	Write Protect
V_{SS}	P	Ground
V_{CC}	P	Power Supply
$\overline{HOLD}$	I	Hold
SCK	I	Serial Clock
SI	I	Serial Data Input

Table1

Position	A	B	C	D
1	-	-	SCK	-
2	V_{CC}	$\overline{HOLD}$	-	SI
3	$\overline{CS}$	-	-	V_{SS}
4	-	SO	$\overline{WP}$	-

Table2

Block Diagram

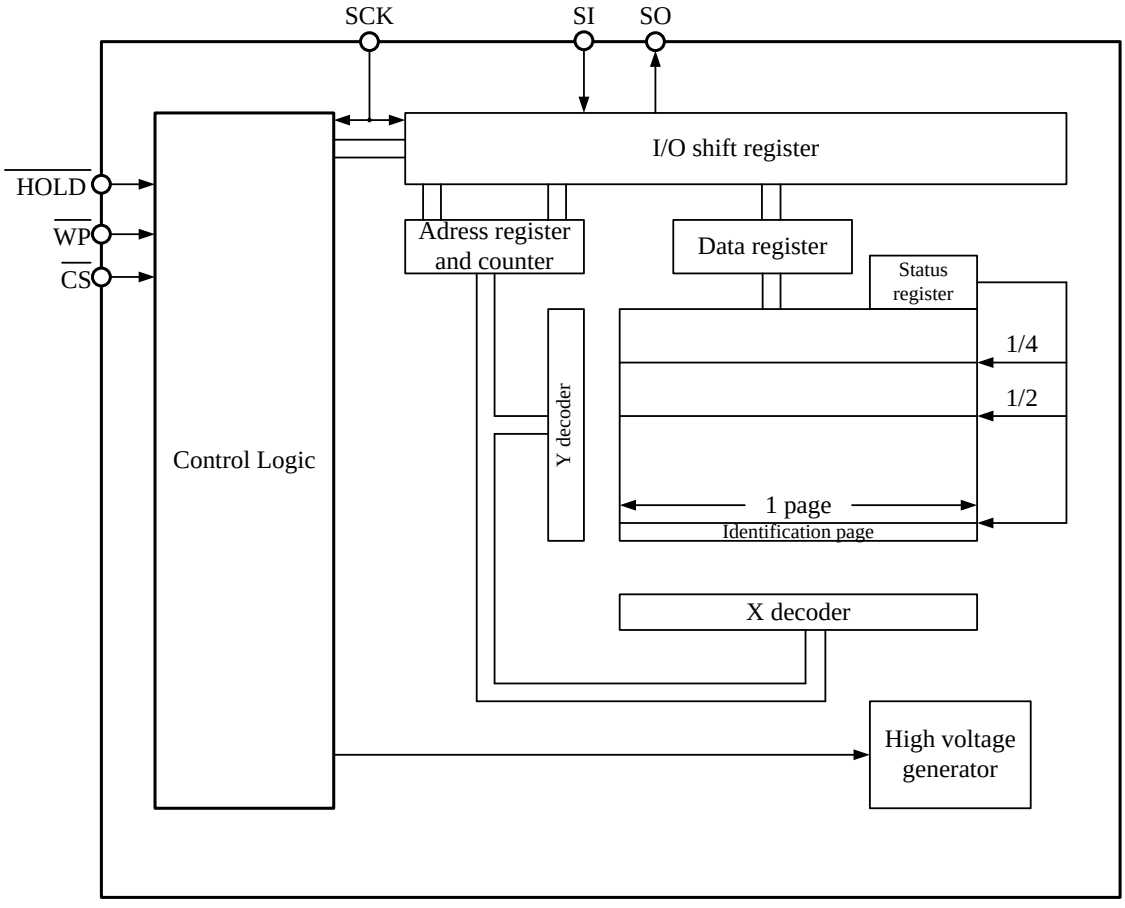


Figure 1

Serial Data Input (SI):

The SPI Serial data input (SI) is used to serially receive write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) input pin.

Serial Data Output (SO): The SPI Serial data output (SO) is used to read data or status from the device on the falling edge of CLK.

Serial Clock (SCK): The SPI Serial Clock Input (SCK) pin provides the timing for serial input and output operations.

Chip Select ($\overline{CS}$): The SPI Chip Select ($\overline{CS}$) pin enables and disables device operation. When ($\overline{CS}$) is high, the device is deselected and the Serial Data Output (SO) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal write cycle is in progress. When ($\overline{CS}$) is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, ($\overline{CS}$) must transition from high to low before a new instruction will be accepted.

Hold ($\overline{HOLD}$): The $\overline{HOLD}$ pin allows the device to be paused while it is actively selected. When $\overline{HOLD}$ is brought low, while $\overline{CS}$ is low, the SO pin will be at high impedance and signals on the SI and SCK pins will be ignored (don’ t care). When $\overline{HOLD}$ is brought high, device operation can resume. The $\overline{HOLD}$ function can be useful when multiple devices are sharing the same SPI signals. The $\overline{HOLD}$ pin is active low.

Write Protect ($\overline{WP}$): The Write Protect ($\overline{WP}$) pin is used in conjunction with the Status Register Write Disable (SRWD) Bit to prevent the Status Registers from being written. Write Protect ($\overline{WP}$) pin and Status Register Write Disable (SRWD) Bit enable the device to be put in the Hardware Protected mode (when Status Register Write Disable (SRWD) Bit is set to 1, and Write Protect ($\overline{WP}$) pin is driven low).

Functional Description

The BL25CM2A device supports the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8−bit instruction register. The instruction set and associated op−codes are listed in Table 3.

Reading data stored in the BL25CM2A is accomplished by simply providing the READ command and an address. Writing to the BL25CM2A, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the $\overline{CS}$ input pin, the BL25CM2A will accept any one of the six instructions op−codes listed in Table 3 and will ignore all other possible 8−bit combinations. The communication protocol follows the timing from Figure 11.

The BL25CM2A features an additional Identification Page (256 bytes) which can be accessed for Read and Write operations when the IPL bit from the Status Register is set to “1”. The user can also

choose to make the Identification Page permanent write protected by setting the LIP bit from the Status Register (LIP= "1").

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

Table3

1. Status Register

The Status Register, as shown in Table 4, contains a number of status and control bits.

7	6	5	4	3	2	1	0
SRWD	IPL	t_{WC}	LIP	BP1	BP0	WEL	$\overline{\text{READY}}$

Table 4

$\overline{\text{READY}}$: The $\overline{\text{READY}}$ bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

BP0,BP1: The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non−volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 5. The protected blocks then become read−only.

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	30000h−3FFFFh	Quarter Array Protection
1	0	20000h−3FFFFh	Half Array Protection
1	1	00000h−3FFFFh	Full Array Protection

Table 5

t_{WC} : The t_{WC} (Write Cycle Time) bit is set by the user with the WRSR command and is volatile. When set to 0, the device is in a standard write mode with optimum ICC write, when set to 1 the device is in a fast write mode.

Note: The fast write mode is recommended to be used only with VCC > 2.8 V.

SRWD : The SRWD (Status Register Write Disable) bit acts as an enable for the $\overline{\text{WP}}$ pin. Hardware write protection is enabled when the $\overline{\text{WP}}$ pin is low and the SRWD bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non−block protected memory can be written. Hardware write protection is disabled when the $\overline{\text{WP}}$ pin is high or the SRWD bit is 0. The SRWD bit, $\overline{\text{WP}}$ pin and WEL bit combine

to either permit or inhibit Write operations, as detailed in Table 6.

SRWD	WP	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

Table 6

IPL : The IPL (Identification Page Latch) bit determines whether the additional Identification Page (IPL = 1) or main memory array (IPL = 0) can be accessed both for Read and Write operations. The IPL bit is set by the user with the WRSR command and is volatile. The IPL bit is automatically reset after read/write operations.

LIP : The LIP bit is set by the user with the WRSR command and is non-volatile. When set to 1, the Identification Page is permanently write protected (locked in Read-only mode).

Note: The IPL and LIP bits cannot be set to 1 using the same WRSR instruction. If the user attempts to set ("1") both the IPL and LIP bit in the same time, these bits cannot be written and therefore they will remain unchanged.

2. Write Operations

The BL25CM2A device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

Write Enable and Write Disable :The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN instruction to the BL25CM2A. Care must be taken to take the $\overline{CS}$ input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 2. The WREN instruction must be sent prior to any WRITE or WRSR instruction.

The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 3. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

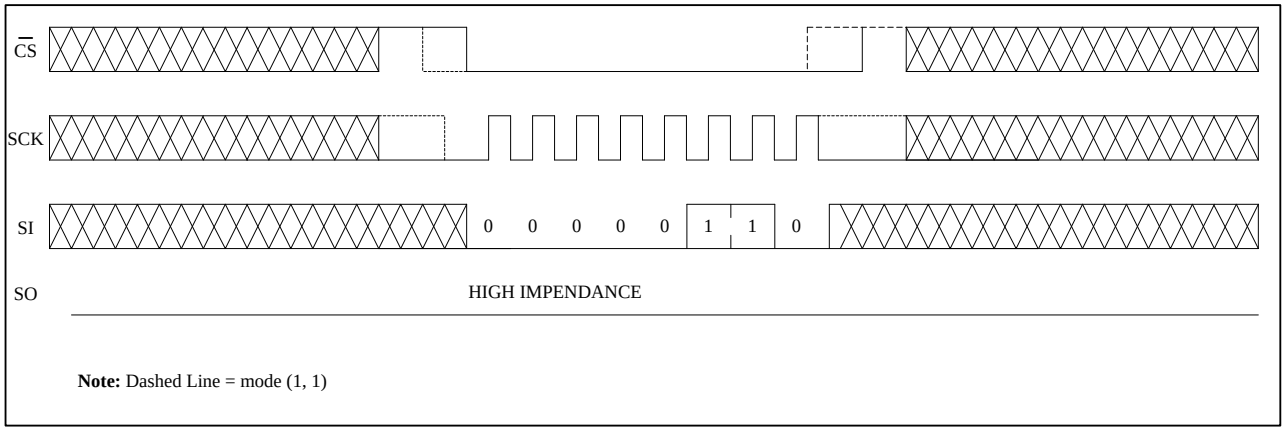


Figure 2

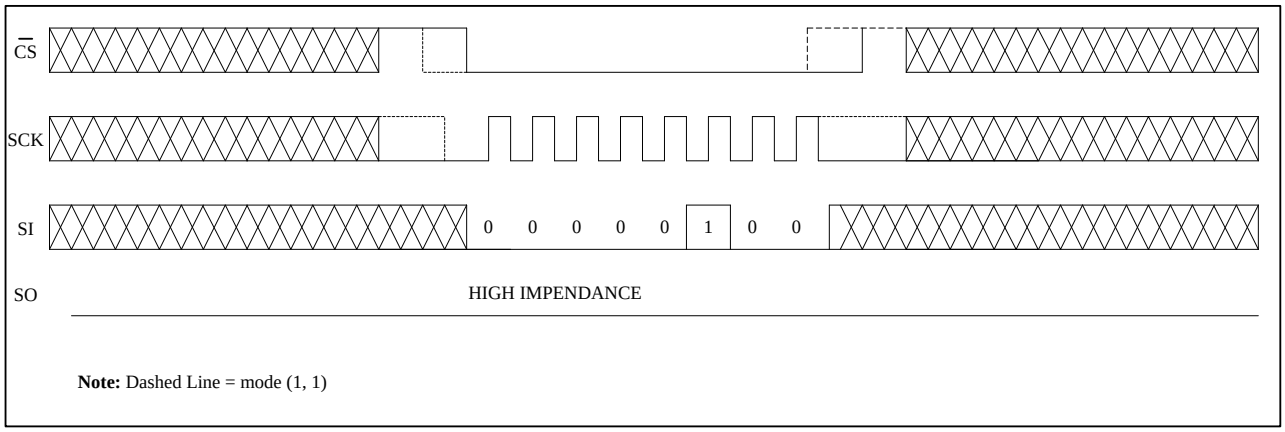


Figure 3

Byte Write: Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 24–bit address and a data byte as shown in Figure 4. Only 18 significant address bits are used by the BL25CM2A. The rest are don't care bits, as shown in Table 7. Internal programming will start after the low to high $\overline{CS}$ transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The $\overline{READY}$ bit will indicate if the internal write cycle is in progress ($\overline{READY}$ high), or the device is ready to accept commands ($\overline{READY}$ low).

Page Write: After sending the first data byte to the BL25CM2A, the host may continue sending data, up to a total of 256 bytes, according to timing shown in Figure 5. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will "roll over" to the first byte in the page, thus possibly overwriting previously loaded data. Following completion of the write cycle, the BL25CM2A is automatically returned to the write disable state.

Write Identification Page: The additional 256-byte Identification Page (IP) can be written with user data using the same Write commands sequence as used for Page Write to the main memory array (Figure 5). The IPL bit from the Status Register must be set (IPL = 1) using the WRSR instruction, before attempting to write to the IP. Prior to any write to the Identification Page, the Write Enable Latch must be set (WEL=1) by sending the WREN instruction.

The address bits [A23:A8] are Don't Care and the [A7:A0] bits define the byte address within the Identification Page. In addition, the Byte Address must point to a location outside the protected area defined by the BP1, BP0 bits from the Status Register. When the full memory array is write protected (BP1, BP0 = 1,1), the write instruction to the IP is not accepted and not executed.

Also, the write to the IP is not accepted if the LIP bit from the Status Register is set to 1 (the page is locked in Read-only mode).

Device	Address Significant Bits	Address Don't Care Bits	# Address Clock Pulses
Main Memory Array	A17 − A0	A23 – A18	24
Identification Page	A7 − A0	A23 – A8	24

Table 7

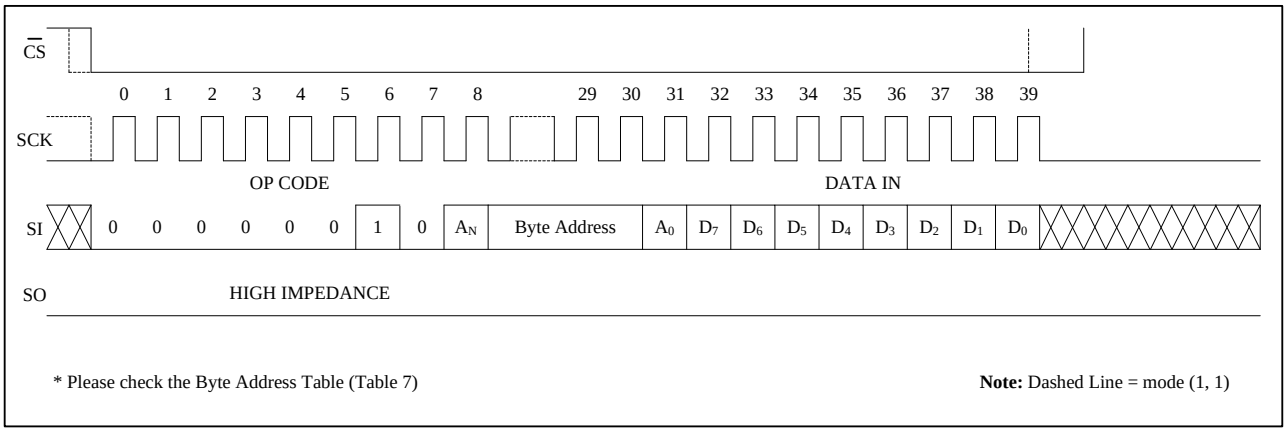


Figure 4

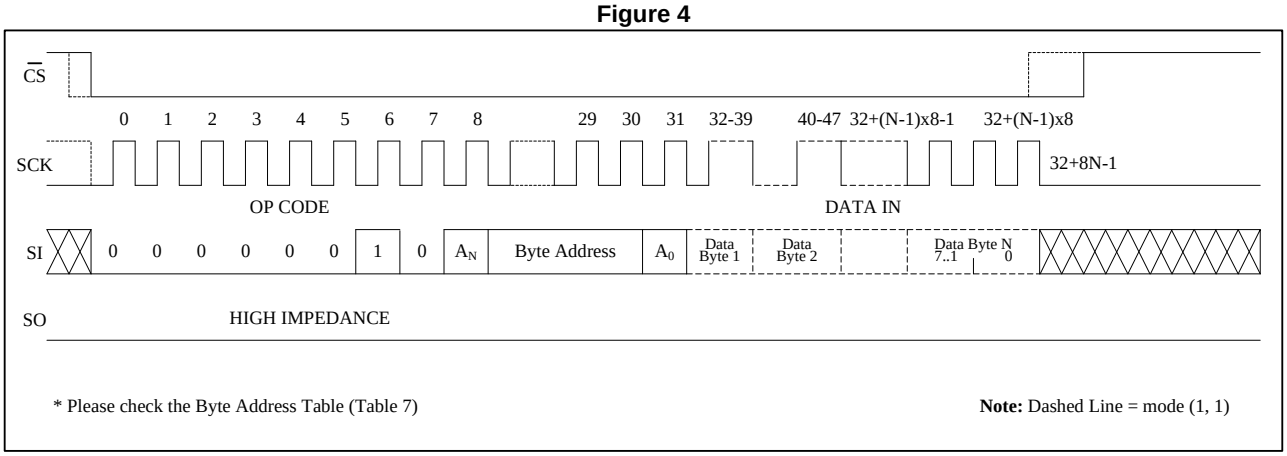


Figure 5

Write Status Register: The Status Register is written by sending a WRSR instruction according to timing shown in Figure 6. Only bits 2, 3, 4, 5, 6 and 7 can be written using the WRSR command.

Write Protection: The Write Protect ($\overline{WP}$) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When $\overline{WP}$ is low and the SRWD bit is set to "1", write operations to the Status Register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the Status Register. The $\overline{WP}$ pin function is blocked when the SRWD bit is set to "0". The $\overline{WP}$ input timing is shown in Figure 7.

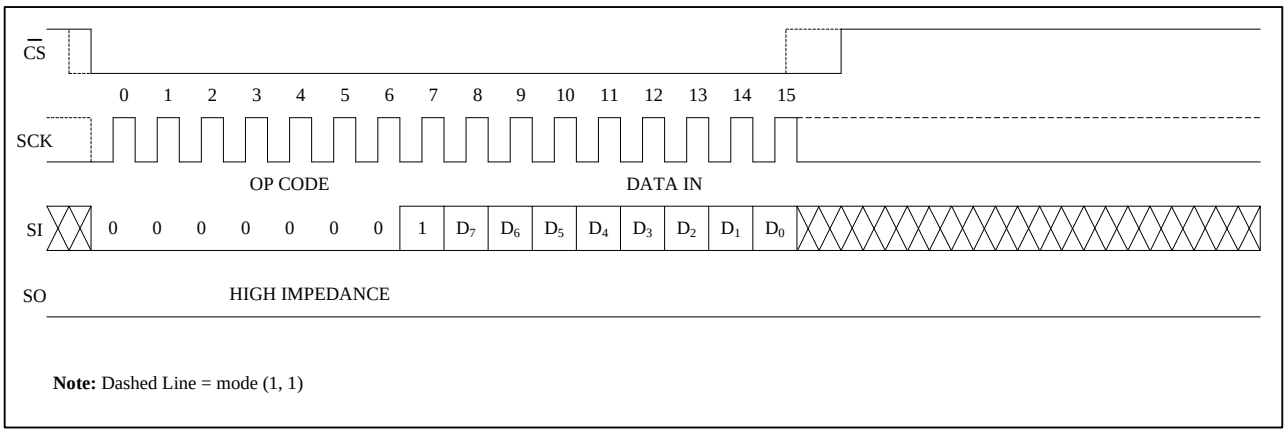


Figure 6

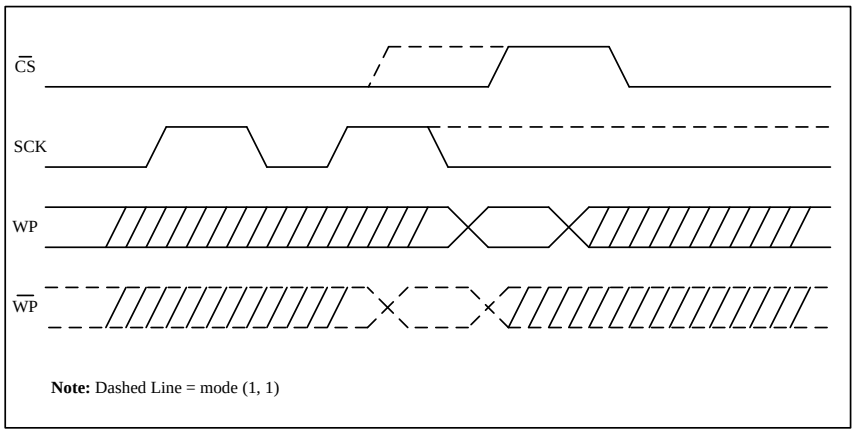


Figure 7

3. Read Operations

Read from Memory Array: To read from memory, the host sends a READ instruction followed by a 24−bit address (see Table 7 for the number of significant address bits).After receiving the last address bit, the BL25CM2A will respond by shifting out data on the SO pin (as shown in Figure 8). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter "rolls over" to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Read Identification Page: Reading the additional 256-byte Identification Page (IP) is achieved using the same Read command sequence as used for Read from main memory array (Figure 9). The IPL bit from the Status Register must be set (IPL = 1) before attempting to read from the IP. The [A7:A0] are the address significant bits that point to the data byte shifted out on the SO pin. If the $\overline{CS}$ continues to be held low, the internal address register defined by [A7:A0] bits is automatically incremented and the next data byte from the IP is shifted out. The byte address must not exceed the 256-byte page boundary.

Read Status Register: To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the BL25CM2A will shift out the contents of the status register on the SO pin (Figure 9). The status register may be read at any time, including during an internal write cycle.

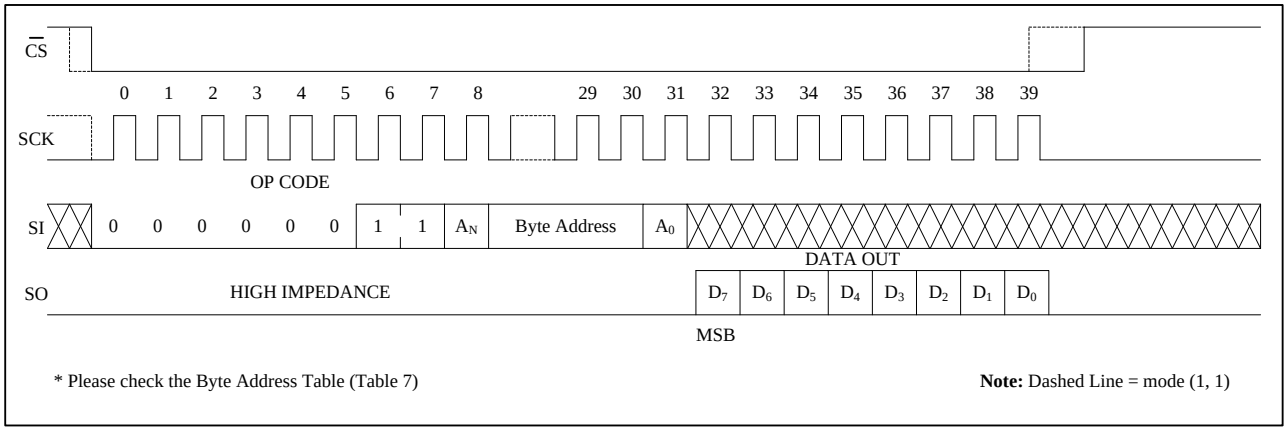


Figure 8

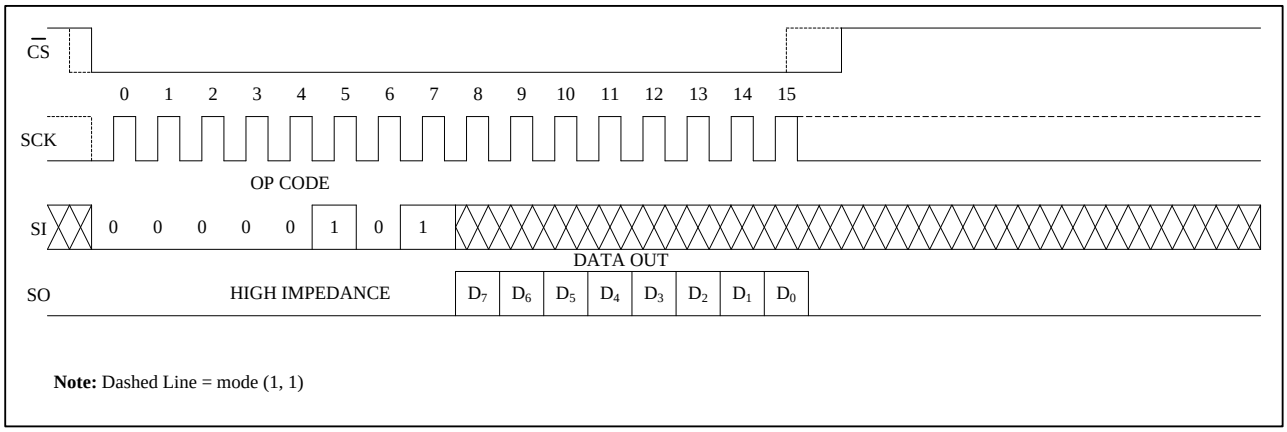


Figure 9

4. Hold Operation

The $\overline{HOLD}$ input can be used to pause communication between host and BL25CM2A. To pause, $\overline{HOLD}$ must be taken low while SCK is low (Figure 10). During the hold condition the device must remain selected ($\overline{CS}$ low). During the pause, the data output pin (SO) is tri−stated (high impedance) and SI transitions are ignored. To resume communication, $\overline{HOLD}$ must be taken high while SCK is low.

5. Design Considerations

The BL25CM2A device incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after VCC exceeds the POR trigger level and will power down into Reset mode when VCC drops below the POR trigger level. This bi−directional POR behavior protects the device against 'brown−out' failure following a temporary loss of power.

The BL25CM2A device powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior to any writes to the device.

After power up, the $\overline{CS}$ pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The $\overline{CS}$ input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid op−code will be ignored and the serial output pin (SO) will remain in the high impedance state.

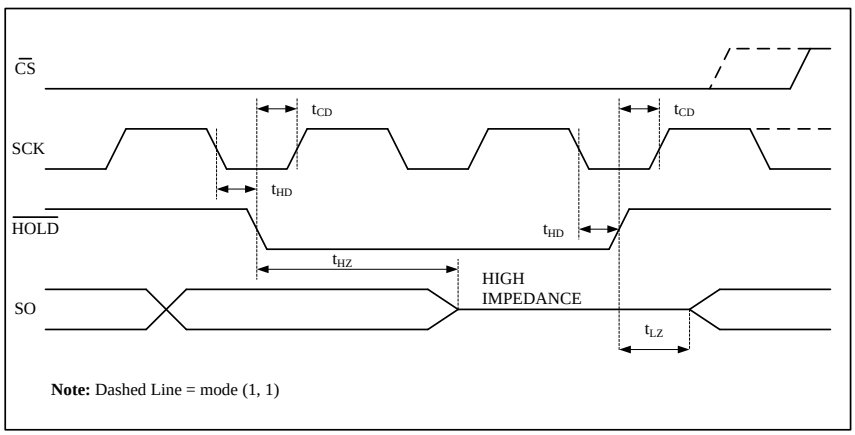


Figure 10

Electrical Characteristics

Absolute Maximum Stress Ratings:

Parameters	Ratings	Units
Operating Temperature	–40 to +85	℃
Storage Temperature	–65 to +150	℃
Voltage on any Pin with Respect to Ground (Note 1)	–0.5 to +6.5	V
VESD（HBM）	8000	V

Table 8

Comments:

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RELIABILITY CHARACTERISTICS (Note 4):

Symbol	Parameter	Min	Units
N_{END} (Notes 2, 3)	Endurance	1,000,000	Program/Erase Cycles
TDR	Data Retention	100	Years

Table 9

D. C. OPERATING CHARACTERISTICS:

(VCC = 2.8V to 5.5 V, TA = −40°C to +85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Supply Current (Read Mode)	Read, SO open / −40°C to +86°C	VCC = 2.8 V, f_{SCK} = 5 MHz	-	3	mA
			VCC = 5.5 V, f_{SCK} = 5 MHz	-	3	mA
I_{CCW}	Supply Current (Write Mode)	Write, $\overline{CS}$ = VCC/ −40°C to +85°C	2.8 V < VCC < 5.5 V	-	3	mA
I_{SB1} (Note 5)	Standby Current	V_{IN} = GND or VCC, $\overline{CS}$ = VCC, $\overline{WP}$ = VCC, HOLD = VCC, VCC = 5.5 V	T_A = −40°C to +85°C	-	5	µA
I_{SB2} (Note 5)	Standby Current	VIN = GND or VCC, $\overline{CS}$ = VCC, $\overline{WP}$ = GND, HOLD = GND, VCC = 5.5 V	T_A = −40°C to +85°C	-	5	µA
I_L	Input Leakage Current	V_{IN} = GND or VCC		-	± 2	µA
I_{LO}	Output Leakage Current	$\overline{CS}$ = VCC VOUT = GND or VCC		-	± 2	µA
V_{IL1}	Input Low Voltage	VCC ⩾ 2.8V		–0.45	0.3 VCC	V
V_{IH1}	Input High Voltage	VCC ⩾ 2.8 V		0.7 VCC	VCC+1	V
V_{OL1}	Output Low Voltage	VCC ⩾ 2.8 V, I_{OL} = 3.0 mA		-	0.4	V
V_{OH1}	Output High Voltage	VCC ⩾ 2.8 V, I_{OH} = −1.6 mA		0.8 VCC	-	V

Table 10

A.C. CHARACTERISTICS:

(VCC = 2.8 V to 5.5 V, TA = −40°C to +85°C, unless otherwise specified.) (Note 6)

Symbol	Parameter	VCC = 2.8 V − 5.5 V		Units
		Min	Max	
f_{SCK}	Clock Frequency	DC	5	MHz
t_{SU}	Data Setup Time	20		ns
t_H	Data Hold Time	20		ns
t_{WH}	SCK High Time	75		ns
t_{WL}	SCK Low Time	75		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z		50	ns
t_{RI} (Note 7)	Input Rise Time		2	μs
t_{FI} (Note 7)	Input Fall Time		2	μs
t_{HD}	$\overline{HOLD}$ Setup Time	0		ns
t_{CD}	$\overline{HOLD}$ Hold Time	10		ns
t_V	Output Valid from Clock Low		75	ns
t_{HO}	Output Hold Time	0		ns
t_{DIS}	Output Disable Time		50	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z		100	ns
t_{CS}	$\overline{CS}$ High Time	80		ns
t_{CSS}	$\overline{CS}$ Setup Time	60		ns
t_{CSH}	$\overline{CS}$ Hold Time	60		ns
t_{CNS}	$\overline{CS}$ Inactive Setup Time	60		ns
t_{CNH}	$\overline{CS}$ Inactive Hold Time	60		ns
t_{WPS}	$\overline{WP}$ Setup Time	20		ns
t_{WPH}	$\overline{WP}$ Hold Time	20		ns
t_{WC} (Notes 9, 10)	Write Cycle Time		6	ms

Table 11

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

POWER−UP TIMING (Notes 7, 8):

Symbol	Parameter	Max	Units
t_{PUR}, t_{PUW}	Power−up to Read / Write Operation	0.1	ms

Table 12

Note:

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than VCC + 0.5 V. During transitions, the voltage on any pin may ndershoot to no less than −1.5 V or overshoot to no more than VCC + 1.5 V, for periods of less than 20 ns.
2. Page Mode, VCC = 5 V, 25°C.
3. The device uses ECC (Error Correction Code) logic with 6 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re−programmed. It is recommended to write by multiple of 4 bytes located at addresses 4N, 4(N+1), 4(N+2), 4(N+3), in order to benefit from the maximum number of write cycles.
4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
5. When not driven, the $\overline{WP}$ and $\overline{HOLD}$ inputs are pulled up to VCC internally. For noisy environments, when the pin is not used, it is recommended the $\overline{WP}$ and $\overline{HOLD}$ input to be tied to VCC, either directly or through a resistor.
6. AC Test Conditions:

   Input Pulse Voltages: 0.3 VCC to 0.7 VCC

   Input rise and fall times: ≤ 10 ns

   Input and output reference voltages: 0.5 VCC

   Output load: current source I_{OL} max/I_{OH} max; CL = 30 pF
7. This parameter is tested initially and after a design or process change that affects the parameter.
8. t_{PUR} and t_{PUW} are the delays required from the time VCC is stable until the specified operation can e initiated.
9. t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.
10. The t_{WC} time can be set by the user to allow faster internal writes (max 10 ms) by setting the t_{WC} bit from the Status Register. The fast write mode is recommended for VCC > 2.5 V.

Bus Timing

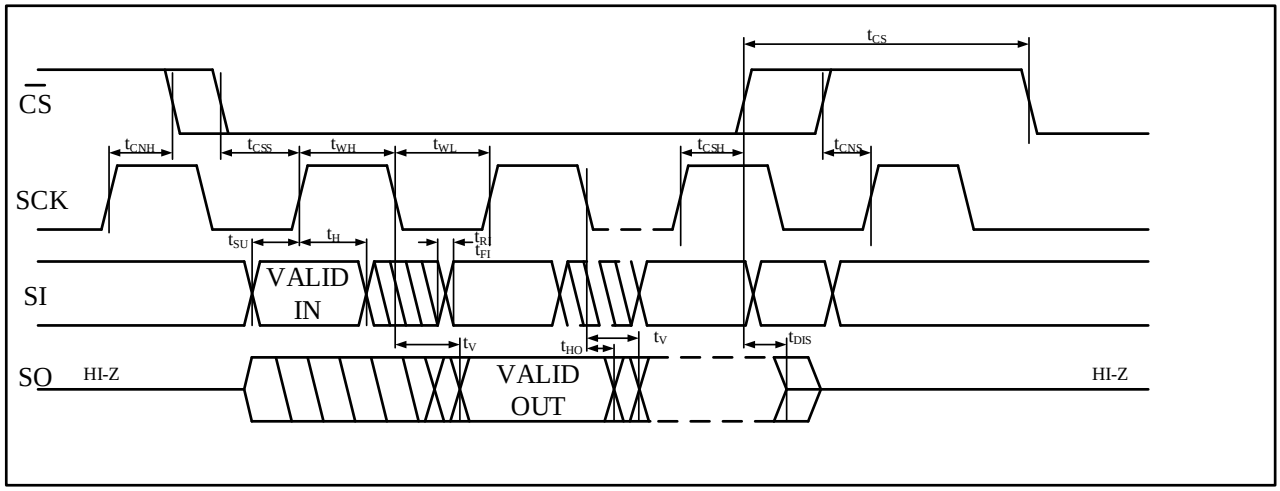
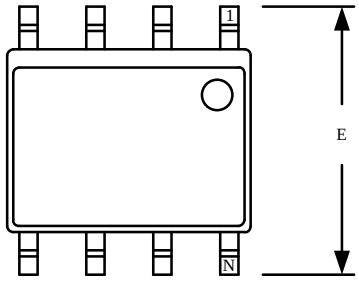
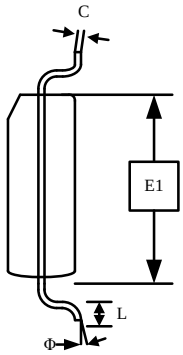


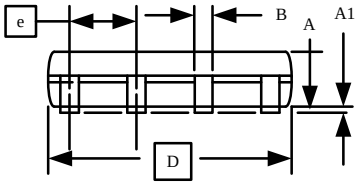
Figure 11

Package Information

SOP







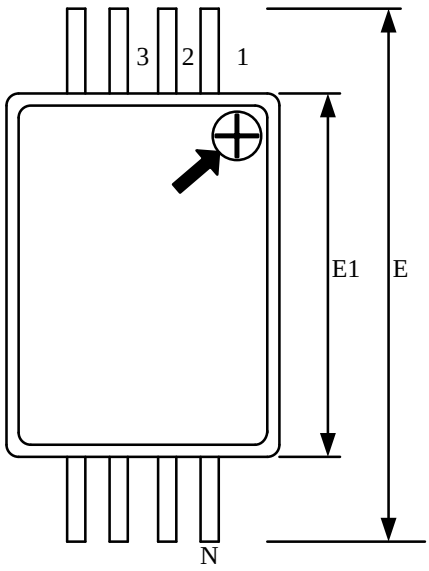
COMMON DIMENSIONS
Unit of Measure=mm

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.23	
B	0.39	–	0.48	
C	0.21	–	0.26	
D	4.70	4.90	5.10	
E1	3.70	3.90	4.10	
E	5.80	6.00	6.20	
e	1.27BSC			
L	0.50	–	0.80	
Φ	0″	–	8″	

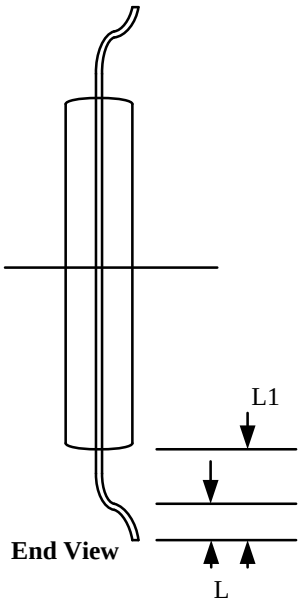
Notes:

These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, data, etc.

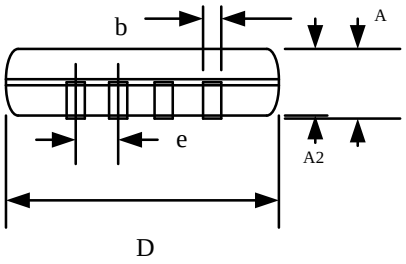
TSSOP



Top View



End View



Side View

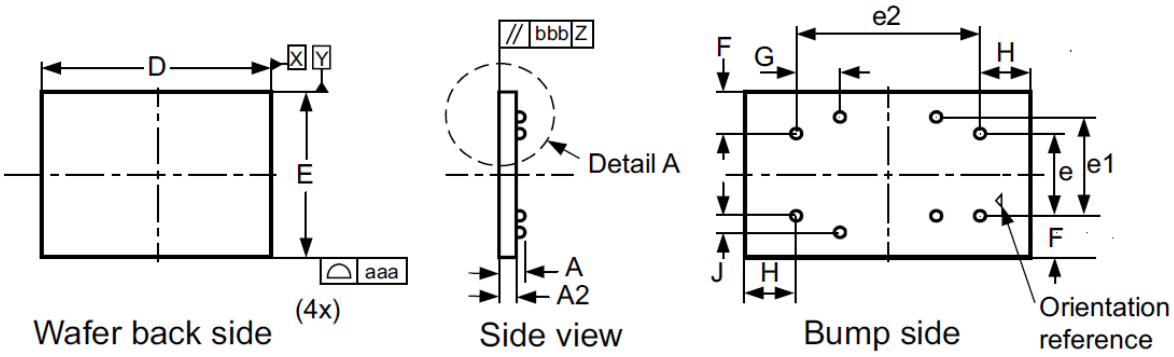
COMMON DIMENSIONS
Unit of Measure=mm

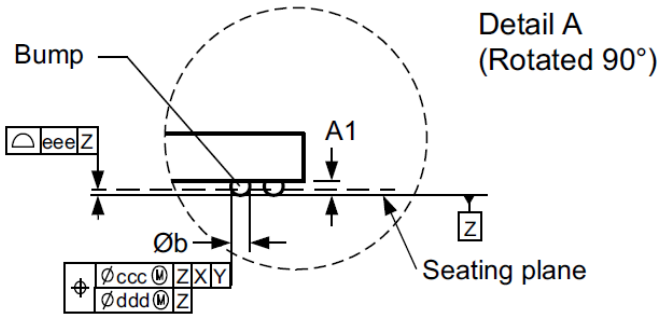
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A2	0.90	1.00	1.05	
b	0.21	–	0.30	4
D	2.90	3.00	3.10	2,5
E	6.20	6.40	6.60	
E1	4.30	4.40	4.50	3,5
e	0.65BSC			
L	0.45	–	0.75	
L1	1.00REF			

Notes:

1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

WLCSP

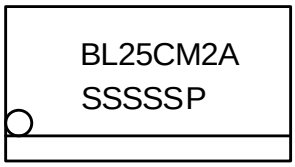




Symbol	millimeters		
	Min	Typ	Max
A	0.49	0.540	0.590
A1	0.165	0.190	0.215
A2	0.325	0.350	0.375
b	0.240	0.270	0.300
D	2.100	2.130	2.160
E	2.880	2.910	2.940
e	-	1.000	-
e1	-	1.200	-
e2	-	2.100	-
F	-	0.565	-
G	-	0.500	-
H	-	0.405	-
J	-	0.200	-

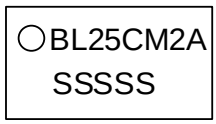
Marking Diagram

SOP



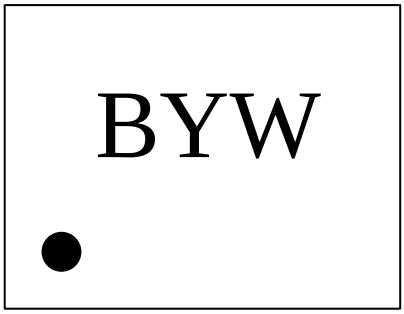
SSSSS : Lot ID

TSSOP



SSSSS : Lot ID

WLCSP8



PIN MARK

Y:The last digits of the year

W:week code.

Y	1	…	3	4	5	…	9	0
Year	2011	…	2013	2014	2015	…	2019	2020

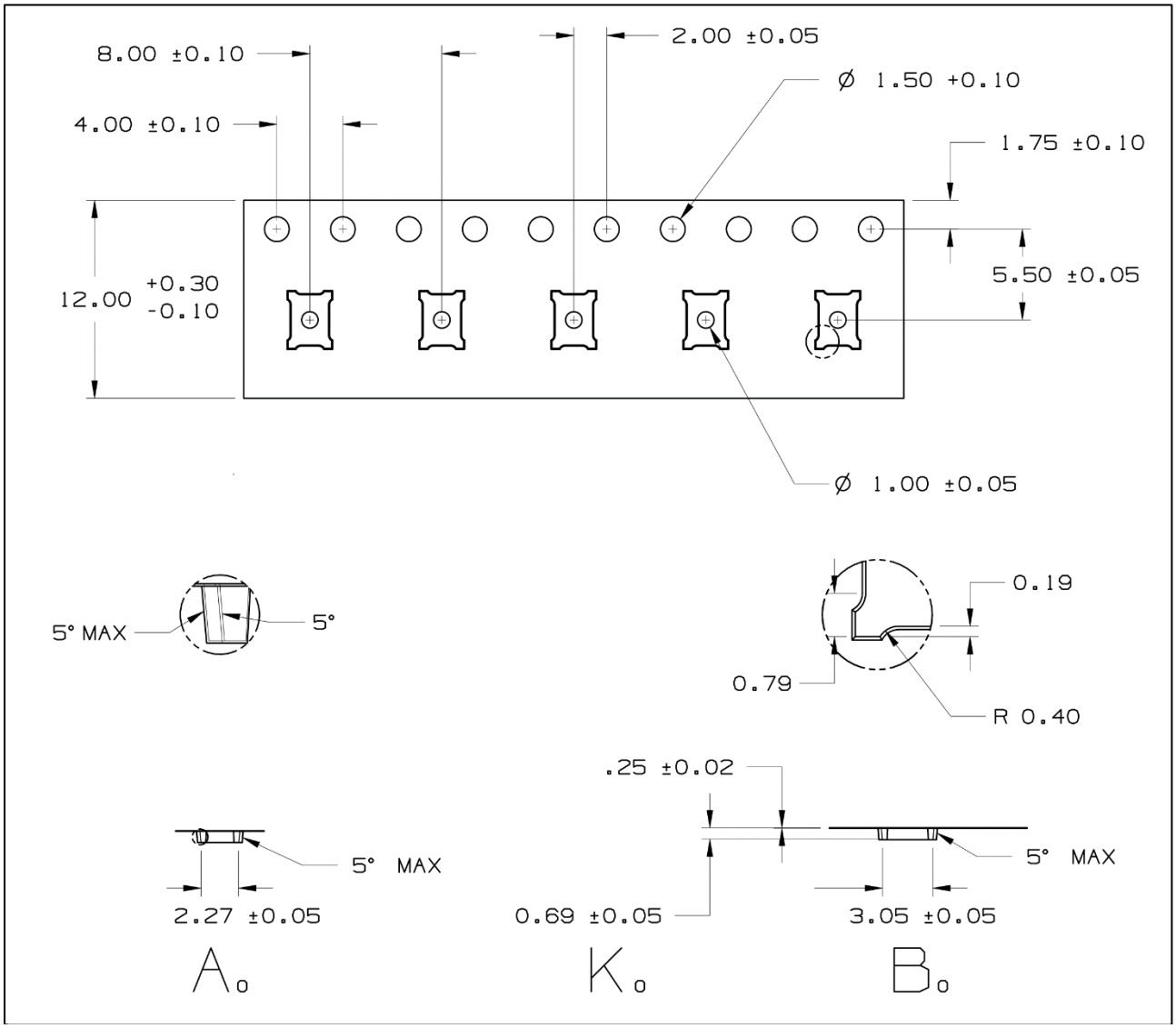
W	A	…	Y	Z	a	…	y	z
Week	1	…	25	26	27	…	51	52

Ordering Information

BL 25C M2 A-PA R C

- Feature
  - S: Standard (default, Pb Free RoHS Std.)
  - C: Green (Halogen Free)
- Packing type
  - R: Tape and Reel
  - T: Tube
- Package Type
  - PA: SOP-8L
  - SF: TSSOP-8L
  - CS: WLCSP
  - DA: PDIP-8L
- Generation
  - A: A Version
- Density
  - M1: 1Mbit
- Product Family
  - 25C: SPI Interface EEPROM

Device	Package	Shipping (Qty/Packing)
BL25CM2A-CS-R	WLCSP-8, 2.130*2.910 (Pb-Free/Halogen Free)	3000/Tape &Reel



Revision history

Version 1.00 BL25CM2A
Initial version
Version 1.01 BL25CM2A
Modify the supply voltage from 2.2-5.5V to 2.6-5.5V Remove UDFN Package information
Version 1.02 BL25CM2A
Modify the supply voltage from 2.6-5.5V to 2.8-5.5V Modify SOP Package Information Add Marking Diagram
Version 1.03 BL25CM2A
Add WLCSP package information