SGM3743
Dual-Channel WLED Driver for Smart Phone

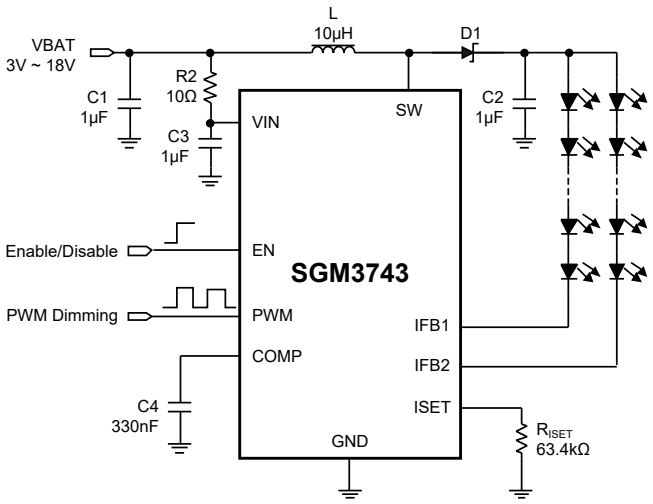
GENERAL DESCRIPTION

The SGM3743 is dual-channel WLED driver which provides highly integrated solutions for single-cell Li-ion battery powered smart phone backlight. The device has a built-in high efficiency boost regulator with integrated 1.5A/40V power MOSFET and supports as low as 3V input voltage. With two high current-matching capability current sink regulators, the device can drive up to 10S2P WLED diodes. The boost output can automatically adjust to the WLED forward voltage and allow very low voltage headroom control, thus to improve LED strings efficiency effectively.

The SGM3743 supports both of the PWM dimming interface and one wire digital dimming interface and can realize 9-bit brightness code programming. The SGM3743 integrates built-in soft-start, over-voltage, over-current protection, and thermal shutdown protection.

The SGM3743 is available in a Green WLCSP -1.32×1.32-9B package and operates over the -40℃ to +85℃ temperature range.

TYPICAL APPLICATION CIRCUIT



FEATURES

- **3V to 18V Input Voltage Range**
- **Integrated 1.5A/40V MOSFET**
- **1.2MHz Switching Frequency**
- **Optimized Rise Time and Fall Time to Control EMI for SW Pin**
- **Dual Current Sinks of up to 30mA Current Each**
- **1% Typical Current Matching and Accuracy**
- **38.5V OVP, 1.2MHz Frequency**
- **Adaptive Boost Output to WLED Voltages**
- **Very Low Voltage Headroom Control (90mV)**
- **Flexible Digital and PWM Brightness Control**
- **One Wire Control Interface**
- **PWM Dimming Control Interface**
- **Up to 9-Bit Dimming Resolution**
- **Up to 90% Efficiency**
- **Built-In Soft-Start Function**
- **Over-Voltage Protection**
- **Built-In WLED Open/Short Protection**
- **Dimming Stable in More than 1:500 PWM Range**
- **PFM Mode at Light Load**
- **Thermal Shutdown**
- **Support 4.7μH Inductor Application**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in a Green WLCSP-1.32×1.32-9B Package**

APPLICATIONS

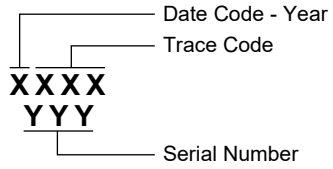
Smart Phones
PDAs, Handheld Computers
GPS Receivers
Backlight for Small and Media Form Factor LCD Display with Single-Cell Battery Input

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3743	WLCSP-1.32×1.32-9B	-40℃ to +85℃	SGM3743YG/TR	XXXX G06	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN ..... 0.3V to 20V
EN, PWM to GND ..... .-0.3V to 6V
COMP, ISET to GND ..... -0.3V to 3V
SW, IFB1, IFB2 to GND ..... -0.3V to 40V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
MM 200V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 3V to 18V
Operating Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range, T_J
..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

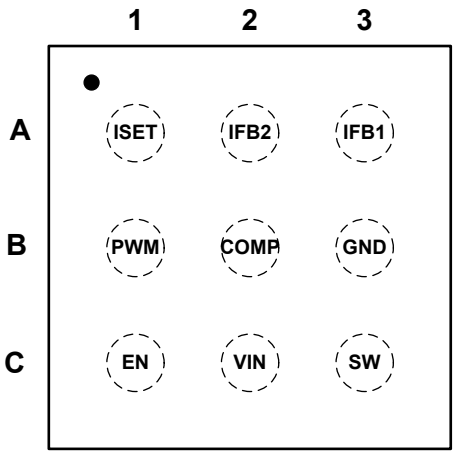
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM3743 (TOP VIEW)



WLCSP-1.32×1.32-9B

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
A1	ISET	I	Full-scale LED Current Set Pin. Connecting a resistor to the pin programs the full-scale LED current.
A2	IFB2	I	Regulated Current Sink Input Pin.
A3	IFB1	I	Regulated Current Sink Input Pin.
B1	PWM	I	PWM Dimming Signal Input.
B2	COMP	O	Output of the Transconductance Error Amplifier. Connect external capacitor to this pin to compensate the boost loop.
B3	GND	O	Ground.
C1	EN	I	Enable Control and One Wire Digital Signal Input.
C2	VIN	I	Supply Input Pin.
C3	SW	I	Drain Connection of the Internal Power MOSFET.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, EN = high, PWM = high, I_{FB} = 20mA, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise specified.)

PARAMETER		SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Power Supply								
Input Voltage Range		V_{IN}		+25℃	3		18	V
Operating Quiescent Current into VIN		I_Q	Device enable, switching 1.2MHz and no load, V_{IN} = 3.6V	+25℃		1.2	1.7	mA
Shutdown Current		I_{SD}	EN = low	+25℃		0.4	1	μA
Under-Voltage Lockout Threshold		UVLO	V_{IN} falling	+25℃		2.25	2.45	V
			V_{IN} rising	+25℃		2.35		
Under-Voltage Lockout Hysterisis		V_{HYS}		+25℃		100		mV
EN and PWM								
EN/PWM Threshold	Logic High Voltage	V_{IH}		Full	1.6			V
	Logic Low Voltage	V_{IL}		Full			0.3	V
EN Pin and PWM Pin Internal Pull-Down Resistor		R_{PD}		+25℃		800		kΩ
PWM Logic Low Width to Shutdown		t_{PWM_SD}	PWM high to low	+25℃	40			ms
EN Logic Low Width to Shutdown		t_{EN_SD}	EN high to low	+25℃	5			ms
PWM Dimming Signal Frequency		f_{PWM}		+25℃	10		100	kHz
Minimum PWM On-Time		$t_{PWM_ON(MIN)}$		+25℃	30			ns
Regulation								
ISET Pin Voltage		V_{ISET_FULL}	Full brightness	Full	1.18	1.213	1.24	V
Current Multiplier		K_{ISET_FULL}	Full brightness	+25℃		1050		
Current Accuracy		I_{FB_AVG}	I_{ISET} = 20μA, D = 100%	+25℃	-3.5	1	3.5	%
$(I_{MAX} – I_{AVG}) / I_{AVG}$		K_M	D = 100%	+25℃		1	2	%
Current Sink Max Output Current		I_{IFB_MAX}	I_{ISET} = 35μA, each IFBx pin	+25℃	30			mA
Power Switch								
Switch MOSFET On-Resistance		$R_{DS(ON)}$	V_{IN} = 3.6V	+25℃		0.35		Ω
			V_{IN} = 3V	+25℃		0.38		
Switch MOSFET Leakage Current		I_{LEAK_SW}	V_{SW} = 35V, T_A = 25℃	+25℃		0.1	1	μA
Oscillator								
Oscillator Frequency		f_S		Full	1000	1200	1350	kHz
Maximum Duty Cycle		D_{MAX}	Measured on the drive signal of switch MOSFET	+25℃		95		%
Boost Voltage Control								
IFBx Feedback Regulation Voltage		V_{IFB_REG}	I_{IFBx} = 20mA, measured on IFBx pin which has a lower voltage	+25℃		90		mV
COMP Pin Sink Current		I_{SINK}		+25℃		12		μA
COMP Pin Source Current		I_{SOURCE}		+25℃		5		μA
Error Amplifier Transconductance		G_{EA}		+25℃		55		μmho
Error Amplifier Output Resistance		R_{EA}		+25℃		100		MΩ
Error Amplifier Crossover Frequency		f_{EA}	5pF connected to COMP pin	+25℃		1.2		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, EN = high, PWM = high, I_{FB} = 20mA, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise specified.)

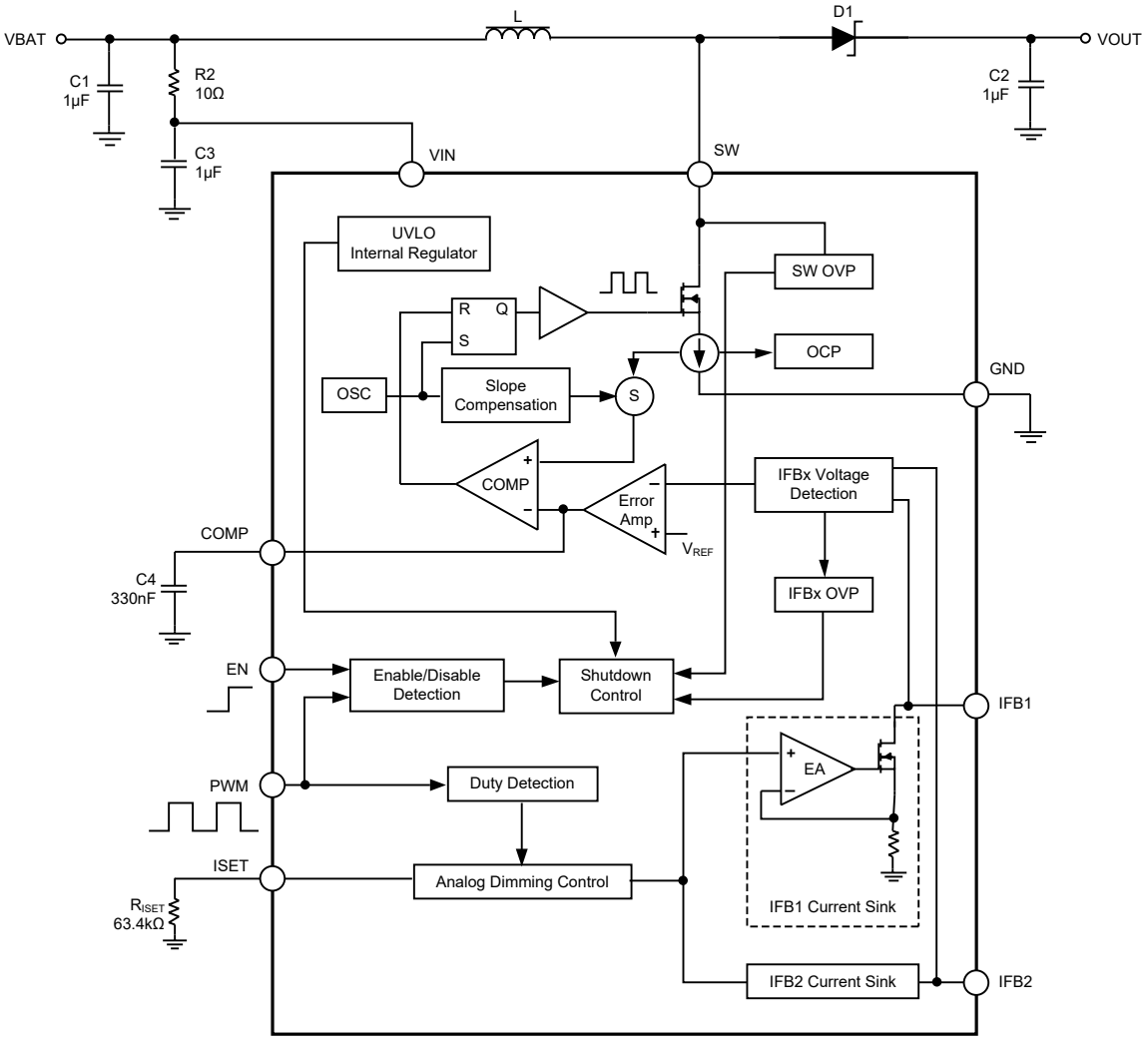
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Protection							
Switch MOSFET Current Limit	I_{LIM}	D = D_{MAX}	+25℃	1.15	1.5	1.75	A
Switch MOSFET Start Up Current Limit	I_{LIM_START}	D = D_{MAX}	+25℃		0.6		A
Time Window for Half Current Limit	t_{HALF_LIM}		+25℃		6		ms
SW Pin Over-Voltage Threshold	V_{OVP_SW}		Full	37.5	38.5	39.7	V
IFBx Pin Over-Voltage Threshold	V_{OVP_IFB}	Measured on IFBx pin	+25℃		4.5		V
Digital One Wire Interface							
One Wire Detection Delay	t_{OW_DELAY}	Measured from EN low to high	+25℃	100			μs
One Wire Detection Time	t_{OW_DET}	EN pin low time	+25℃	260			μs
One Wire Detection Window (1)	t_{OW_WIN}	Measured from EN low to high	+25℃	1			ms
Start Time of Program Stream	t_{START}		+25℃	6			μs
End Time of Program Stream	t_{EOS}		+25℃	6		360	μs
High Time of Low Bit	t_{H_LB}	Logic 0	+25℃	6		180	μs
Low Time of Low Bit	t_{L_LB}	Logic 0	+25℃	2 × t_{H_LB}		360	μs
High Time of High Bit	t_{H_HB}	Logic 1	+25℃	2 × t_{L_HB}		360	μs
Low Time High Bit	t_{L_HB}	Logic 1	+25℃	6		180	μs
Acknowledge Valid Time	$t_{valACKN}$		+25℃			4	μs
Duration of Acknowledge Condition	t_{ACKN}		+25℃			512	μs
Acknowledge Output Voltage Low (2)	V_{ACKNL}	Open drain, $R_{PULL-UP}$ = 15kΩ to V_{IN}	+25℃			0.4	V
Thermal Shutdown							
Thermal shutdown threshold	T_{SHDN}				150		℃
Thermal shutdown hysteresis	T_{HYS}				15		℃

NOTES:

1. To select one wire digital interface, after t_{OW_DELAY} delay from EN low to high, drive EN pin to low for more than t_{OW_DET} before t_{OW_WIN} expires.

2. Acknowledge condition active 0, this condition is only applied when the RFA bit is set to 1. To use this feature, master must have an open drain output, and the data line needs to be pulled up by the master with a resistor load.

FUNCTIONAL BLOCK DIAGRAM

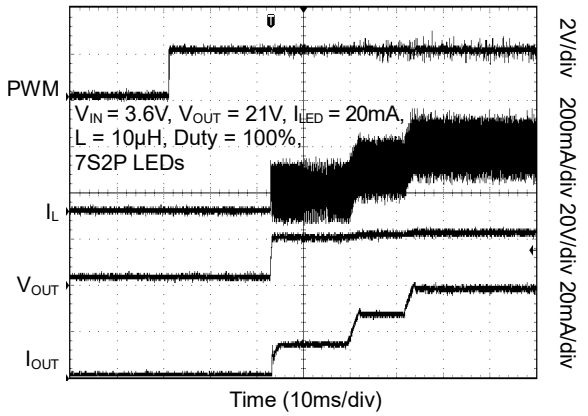


RECOMMENDED COMPONENTS OF TEST CIRCUITS

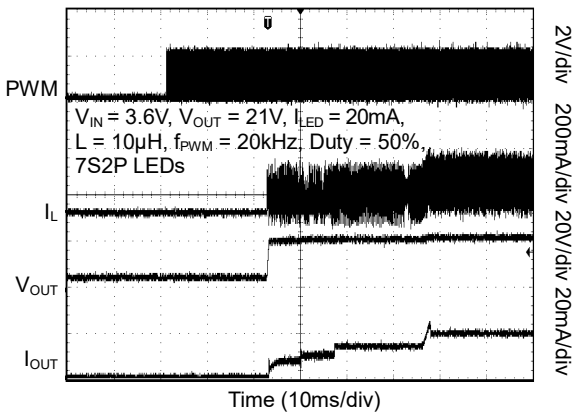
	COMPONENT		COMPONENT
INDUCTOR	10μH/CD75NP-100KC	**CAPACITOR**	1μF/C2012X7R1H105KT
DIODE	MBR0540		

TYPICAL PERFORMANCE CHARACTERISTICS

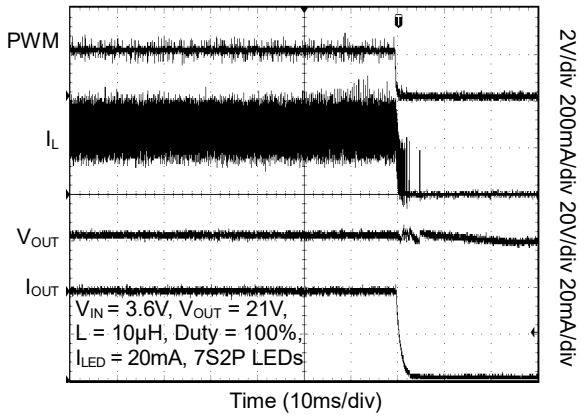
Start-Up



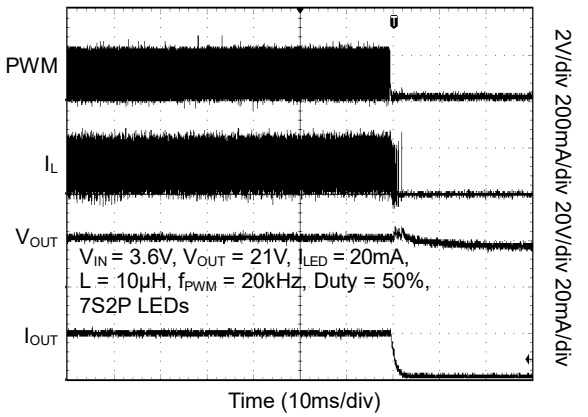
Start-Up



Shutdown

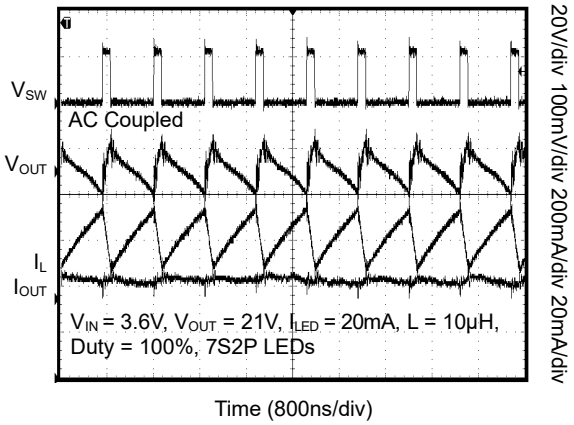


Shutdown

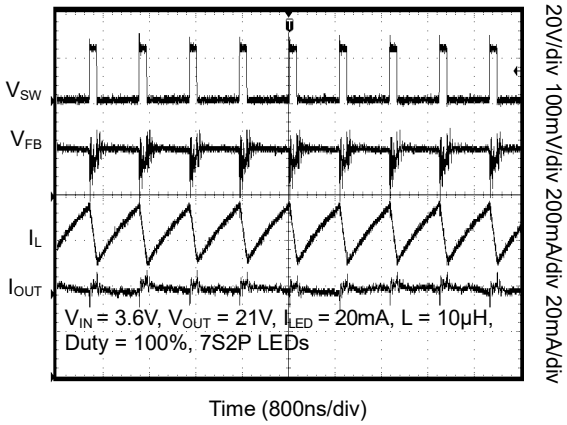


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

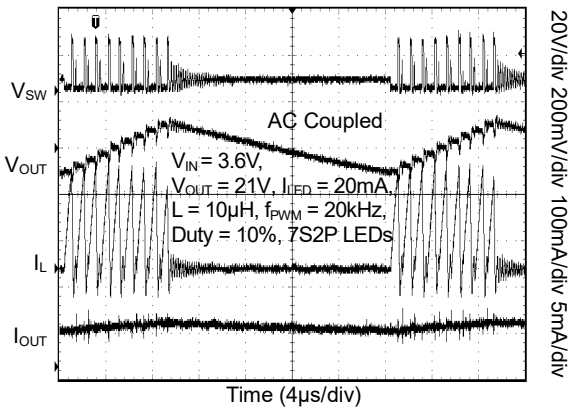
Switching Waveform



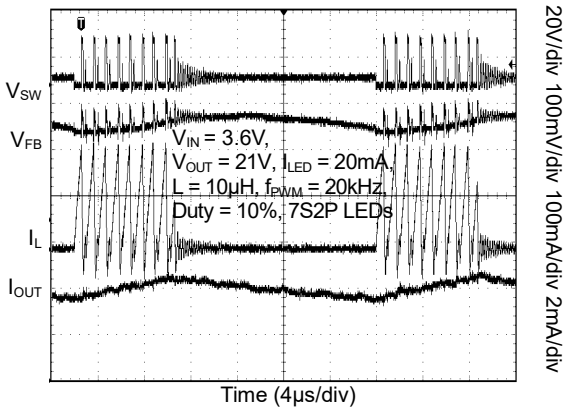
Switching Waveform



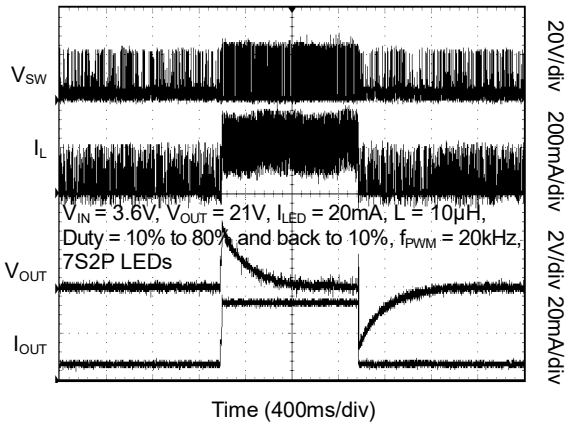
Switching Waveform



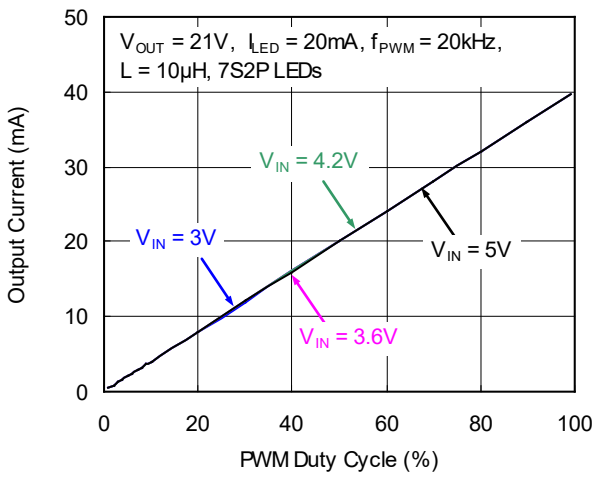
Switching Waveform



Dimming Transient Waveform

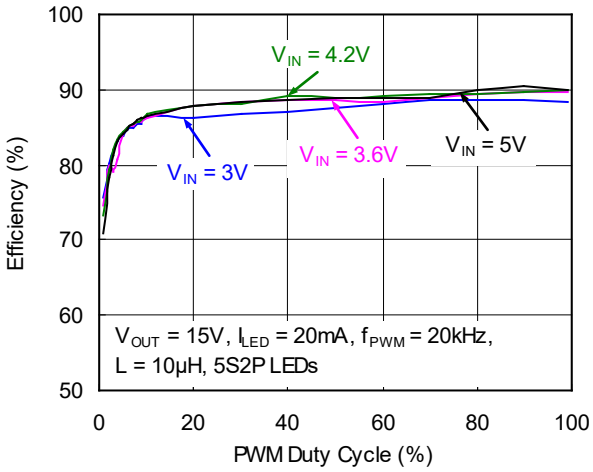


Dimming Linearity



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Efficiency vs. PWM Duty Cycle



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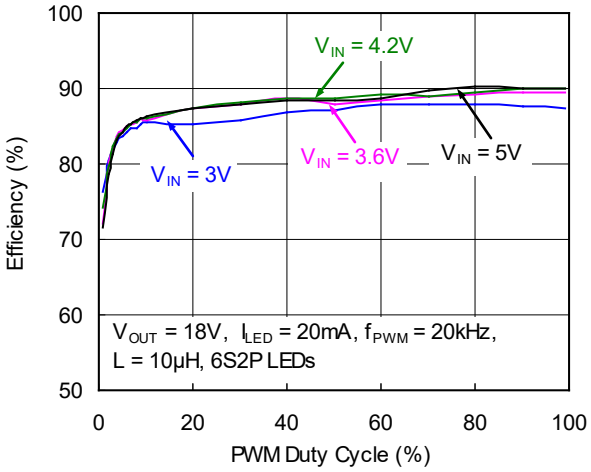

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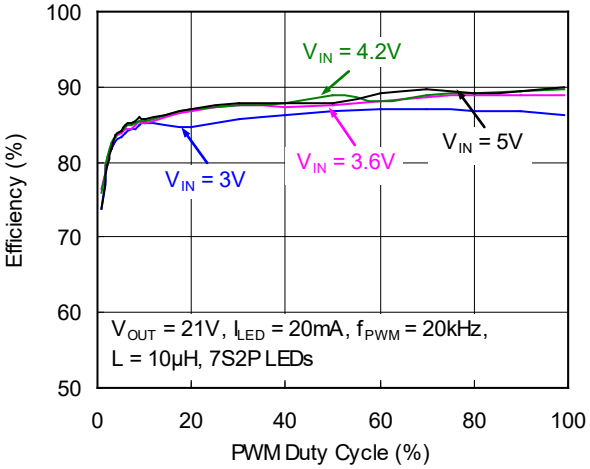
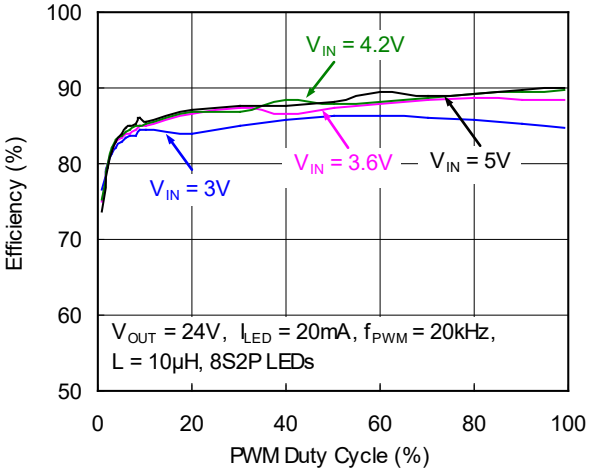
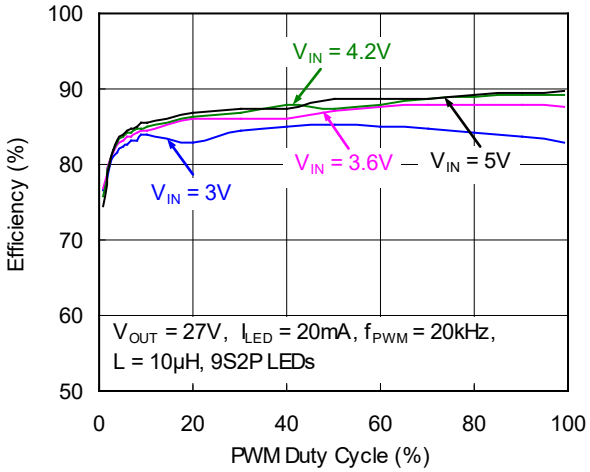


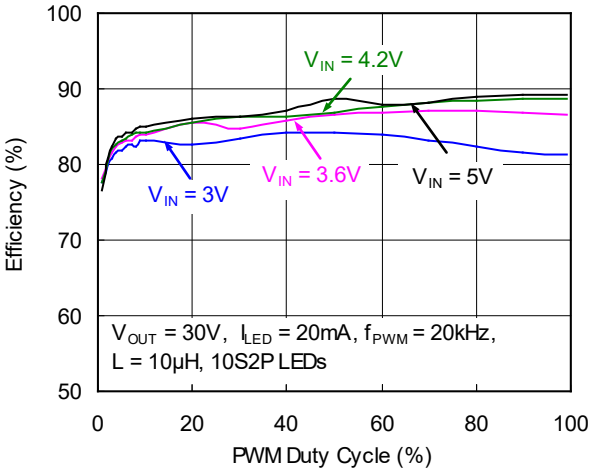
Efficiency vs. PWM Duty Cycle



Efficiency vs. PWM Duty Cycle



Efficiency vs. PWM Duty Cycle



DETAILED DESCRIPTION

Normal Operation

In order to provide high brightness backlighting for big size or high resolution smart phone panels, more and more white LED diodes are used. Having all LED diodes in a string improves overall current matching; however, the output voltage of a boost converter will be limited when input voltage is low, and normally the efficiency will drop when output voltage goes very high. Thus the LED diodes are arranged in two parallel strings.

The SGM3743 is a high efficiency, dual-channel white LED driver for such smart phone backlighting applications. Two current sink regulators of high current-matching capability are integrated in the SGM3743 to support dual LED strings connection and to improve the current balance and protect the LED diodes when either LED string is open or short.

SGM3743 has integrated all of the key function blocks to power and control up to 20 white LED diodes. It includes a 40V/1.5A boost converter, two current sink regulators and protection circuit for over-current, over-voltage and thermal shutdown protection.

Boost Converter

The boost converter of the SGM3743 integrates 40V/1.5A low side switch MOSFET and has a fixed switching frequency of 1.2MHz. The control architecture is based on traditional current-mode PWM control. For operation see the Functional Block Diagram. Two current sinks regulate the dual-channel current and the boost output is automatically set by regulating IFBx pin’s voltage. The output of error amplifier and the sensed current of switch MOSFET are applied to a control comparator to generate the boost switching duty cycle; slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%.

The forward voltages of two LED strings are normally different due to the LED diode forward voltage inconsistency, thus the IFB1 and IFB2 voltages are normally different. The SGM3743 can select out the IFBx pin which has a lower voltage than the other and regulates its voltage to a very low value (90mV typical), which is enough for the two current sinks' headroom. In this way, the output voltage of the boost converter is automatically set and adaptive to LED strings' forward voltages, and the power dissipation of the current sink regulators can be reduced remarkably with this very low headroom voltage.

IFBx Pin Unused

If only one channel is needed, a user can easily disable the unused channel by connecting its IFBx pin to ground. If both IFBx pins are connected to ground, the IC will not start up.

Enable and Start Up

In order to enable the IC from shutdown mode, three conditions have to be met:

1. POR (Power On Reset, that is, VIN voltage is higher than UVLO threshold);
2. Logic high on EN pin;
3. PWM signal (logic high or PWM pulses) on PWM pin.

When these conditions are all met, an internal LDO linear regulator is enabled to provide supply to internal circuits and the IC can start up.

The SGM3743 supports two dimming interfaces: One wire digital interface and PWM interface. SGM3743 begins an one wire digital detection window after startup to detect which interface is selected. If the one wire digital interface is needed, signals of a specific pattern should be input into EN pin during the one wire digital detection window; otherwise, PWM dimming interface will be enabled (see details in One Wire Digital Interface).

After the one wire digital detection window, the SGM3743 checks the status of IFBx pins. If one IFBx pin is detected to connect to ground, the corresponding channel will be disabled and removed from the control loop. Then the soft-start begins and the boost converter starts switching. If both IFBx pins are shorted to ground, the SGM3743 will not start up.

Either pulling EN pin low for more than 5ms or pulling PWM pin low for more than 40ms can disable the device and the SGM3743 enters into shutdown mode.

DETAILED DESCRIPTION (continued)

Soft-Start

Soft-start is implemented internally to prevent voltage over-shoot and in-rush current. After the IFBx pin status detection, the COMP pin voltage starts ramp up and the boost starts switching. During the beginning 6ms (t_{HALF_LIM}) of the switching, the peak current of the switch MOSFET is limited at I_{LIM_START} (0.6A typical) to avoid the input inrush current. After the 6ms, the current limit is changed to I_{LIM} (1.5A typical) to allow the normal operation of the boost converter.

Full-Scale Current Program

The dual channels of the SGM3743 can provide up to 30mA current each. No matter either one wire digital interface or PWM interface is selected, the full-scale current (current when dimming duty cycle is 100%) of each channel should be programmed by an external resistor R_{ISET} at ISET pin according to Equation 1.

$$I_{FB_FULL} = \frac{V_{ISET_FULL}}{R_{ISET}} \times K_{ISET_FULL} \quad (1)$$

where

I_{FB_FULL}, full-scale current of each channel

K_{ISET_FULL} = 1050 (Current multiple when dimming duty cycle = 100%)

V_{ISET_FULL} = 1.213V (ISET pin voltage when dimming duty cycle = 100%)

R_{ISET} = ISET pin resistor

Brightness Control

The SGM3743 controls the DC current of the dual channels to realize the brightness dimming. The DC current control is normally referred to as analog dimming mode. When the DC current of LED diode is reduced, the brightness is dimmed.

The SGM3743 can receive either the PWM signals at the PWM pin (PWM interface) or digital commands at the EN pin for brightness dimming. If the one wire digital interface is selected, the PWM pin should be kept high; if PWM interface is selected, the EN pin should be kept high.

One Wire Digital Interface

The EN pin features a simple digital interface to allow digital brightness control. The digital dimming interface can save the processor power and battery life as it does not require PWM signals all the time, and the processor can enter idle mode if possible. In order to enable the one wire digital interface, the following conditions must be satisfied and the specific digital pattern on the EN pin must be recognized by the IC every time the SGM3743 starts up from shutdown mode.

1. VIN voltage is higher than UVLO threshold and PWM pin is pulled high.

2. Pull EN pin from low to high to enable the SGM3743. At this moment, the one wire digital detection window starts.

3. After one wire digital detection delay time (t_{OW_DELAY}, 100μs), drive EN to low for more than one wire digital detection time (t_{OW_DET}, 260μs).

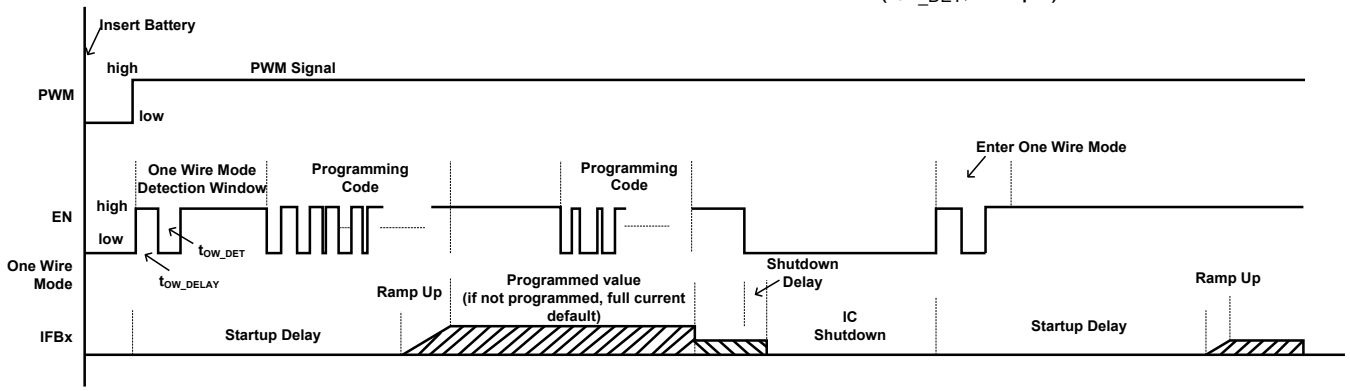


Figure 1. One Wire Digital Interface Detection

DETAILED DESCRIPTION (continued)

The third step must be finished before the one wire digital detection window (t_{OW_WIN}, 1ms) expires, and once this step is finished, the one wire digital interface is enabled and the one wire digital communication can start. Refer to the Figure 1 for a graphical explanation.

The SGM3743 supports 9-bit brightness code programming. By the one wire digital interface, a master can program the 9-bit code D8 (MSB) to D0 (LSB) to any of 511 steps with a single command. The default code value of D8 ~ D0 is “111111111” when the device is first enabled, and the programmed value will be stored in an internal register and set the dual-channel current according to Equation 2. The code will be reset to default value when the IC is shut down or disabled.

$$I_{FBx} = I_{FB_FULL} \times \frac{Code}{511} \quad (2)$$

where

I_{FB_FULL}: the full-scale LED current set by the R_{ISET} at ISET pin.

Code: the 9-bit brightness code D8~D0 programmed by one wire digital interface.

When the one wire digital interface at EN pin is selected, the PWM pin can be connected to either VIN pin or a GPIO (refer to Additional Application Circuits). If PWM pin is connected to VIN pin, EN pin alone can enable and disable the IC: pulling EN pin low for more than 5ms disables the IC; if PWM pin is connected to a GPIO, both PWM and EN signals should be high to enable the IC, and either pulling EN pin low for more than 5ms or pulling PWM pin low for more than 40ms disables the IC.

One Wire Programming

One wire is a simple but flexible one pin interface to configure the current of the dual channels. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor and the IC is the slave. Figure 2 and Table 1 give an overview of the protocol used by SGM3743. A command consists of 24 bits, including an 8-bit device address byte and a 16-bit data byte. All of the 24 bits should be transmitted together each time, and the LSB bit should be transmitted first. The device’s address byte DA7 (MSB) ~ DA0 (LSB) is fixed to 0x8F. The data byte includes 9 bits D8 (MSB) ~ D0 (LSB) for brightness information and an RFA bit. The RFA bit set to "1" indicates the Request for Acknowledge condition. The Acknowledge condition is only applied when the protocol is received correctly. The advantage of one wire compared with other one pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7kBit/sec and up to 160kBit/sec.

DETAILED DESCRIPTION (continued)

Table 1. One Wire Digital Interface Bit Description

Byte	Bit Number	Name	Transmission Direction	Description
Device Address Byte (0x8F)	23 (MSB)	DA7	IN	DA7 = 1, MSB of device address
	22	DA6		DA6 = 0
	21	DA5		DA5 = 0
	20	DA4		DA4 = 0
	19	DA3		DA3 = 1
	18	DA2		DA2 = 1
	17	DA1		DA1 = 1
	16	DA0		DA0 = 1, LSB of device address
Data Byte	15	Bit 15	IN	No information. Write 0 to this bit.
	14	Bit 14		No information. Write 0 to this bit.
	13	Bit 13		No information. Write 0 to this bit.
	12	Bit 12		No information. Write 0 to this bit.
	11	Bit 11		No information. Write 0 to this bit.
	10	RFA		Request for acknowledge. If set to 1, IC will pull low the data line when it receives the command well. This feature can only be used when the master has an open drain output stage and the data line needs to be pulled high by the master with a pull-up resistor; otherwise, acknowledge condition is not allowed and don't set this bit to 1.
	9	Bit 9		No information. Write 0 to this bit.
	8	D8		Data bit 8, MSB of brightness code
	7	D7		Data bit 7
	6	D6		Data bit 6
	5	D5		Data bit 5
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0, LSB of brightness code

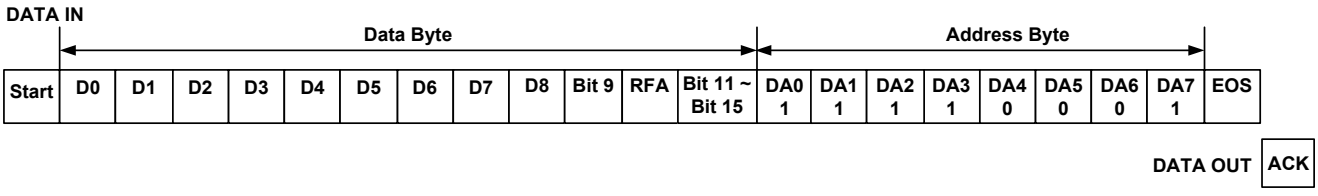


Figure 2. One Wire Digital Interface Protocol Overview

DETAILED DESCRIPTION (continued)

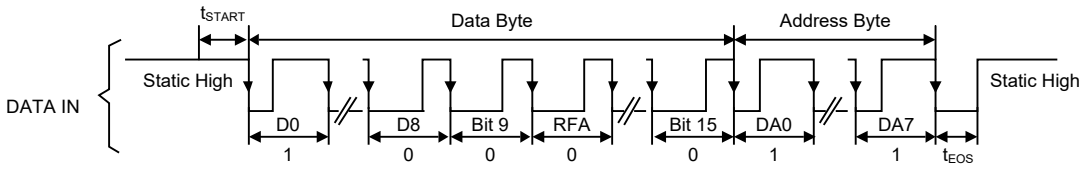


Figure 3. One Wire Digital Timing, with RFA = 0

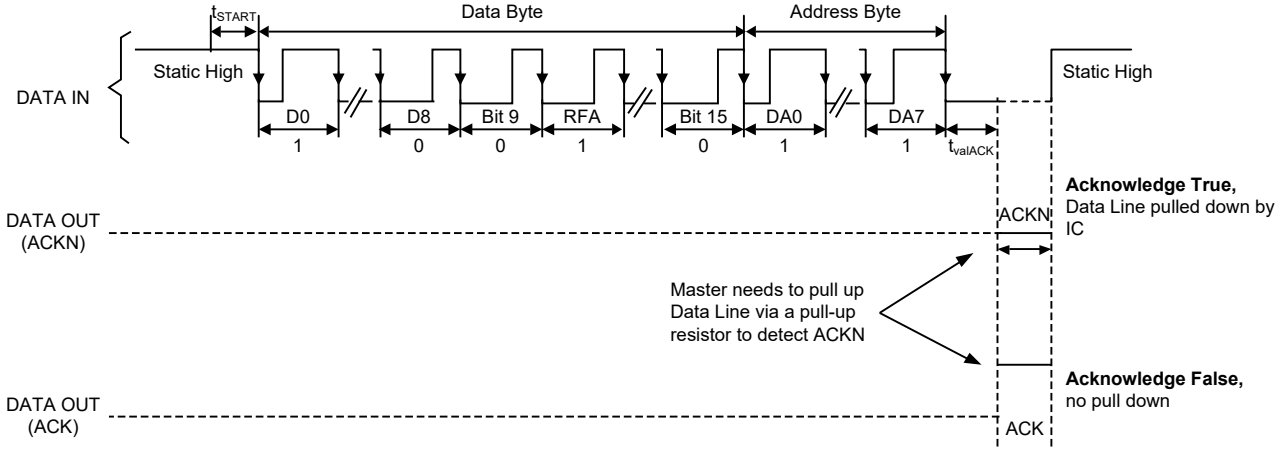


Figure 4. One Wire Digital Timing, with RFA = 1

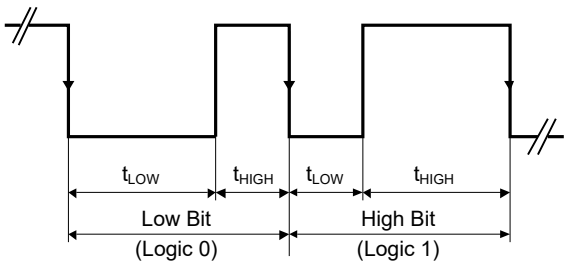


Figure 5. One Wire Digital Interface Bit Coding

DETAILED DESCRIPTION (continued)

The 24-bit command should be transmitted with LSB first and MSB last. Figure 3 shows the protocol without acknowledge request (Bit RFA = 0), Figure 4 with acknowledge request (Bit RFA = 1). Before the command transmission, a start condition must be applied. For this, the EN pin must be pulled high for at least t_{START} (6μs) before the bit transmission starts with the falling edge. If the EN pin is already at high level, no start condition is needed. The transmission of each command is closed with an End of Stream condition for at least t_{EOS} (6μs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH} (refer to Figure 5). It can be simplified to:

Low Bit (Logic 0): $t_{LOW} \geq 2 \times t_{HIGH}$
High Bit (Logic 1): $t_{HIGH} \geq 2 \times t_{LOW}$

The bit detection starts with a falling edge on the EN pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:
• Acknowledge is requested by setting RFA bit to 1.
• The transmitted device address matches with the device address of the IC.
• Total 24 bits are received correctly.

If above conditions are met, after t_{valACK} delay from the moment when the last falling edge of the protocol is detected, an internal ACKN-MOSFET is turned on to pull the EN pin low for the time t_{ACKN}, which is 512μs maximum, then the Acknowledge condition is valid. During the t_{valACK} delay, the master controller keeps the line low; after the delay, it should release the line by outputting high impedance and then detect the acknowledge condition. If it reads back a logic 0, it means the IC has received the command correctly. The EN pin can be used again by the master when the acknowledge condition ends after t_{ACKN} time.

Note that the acknowledge condition can only be requested when the master device has an open drain output. For a push-pull output stage, the use of a series resistor in the EN line to limit the current to 500μA is recommended to for such cases as:
• An accidentally requested acknowledge, or
• To protect the internal ACKN-MOSFET.

PWM Control Interface

The PWM control interface is automatically enabled if the one wire interface fails to be enabled during start up. In this case, the SGM3743 receives PWM dimming signals on the PWM pin to control the backlight brightness. When using PWM interface, the EN pin can be connected to VIN pin or a GPIO (refer to Additional Application Circuits). If EN pin is connected to VIN pin, PWM pin alone is used to enable and disable the IC: pulling PWM pin high or apply PWM signals at PWM pin to enable the IC and pulling PWM pin low for more than 40ms to disable the IC; if EN pin is connected to a GPIO, either pulling EN pin low for more than 5ms or pulling PWM pin low for more than 40ms can disable the IC. Only after both EN and PWM signals are applied, the SGM3743 can start up. Refer to Figure 6 for a graphical explanation.

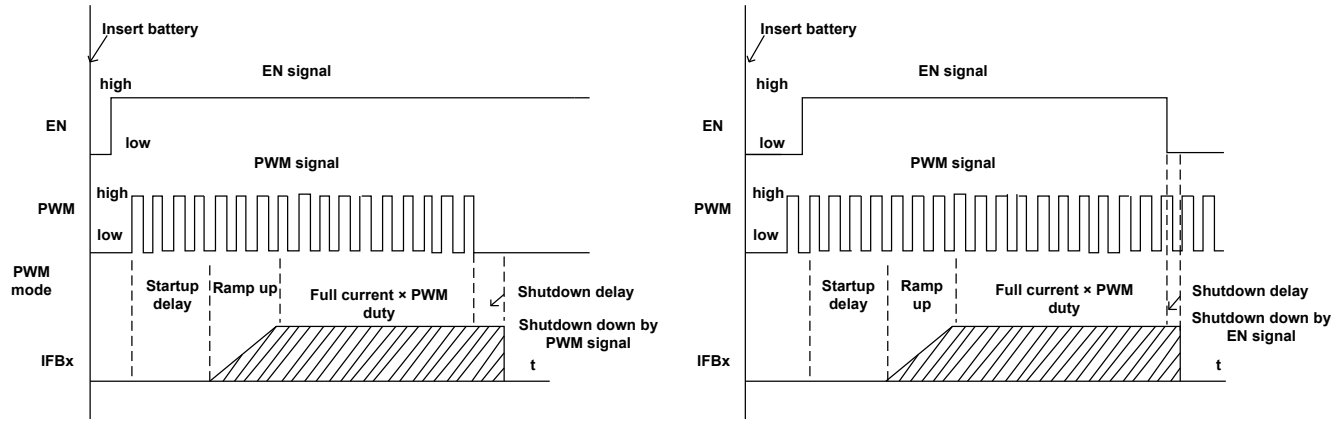


Figure 6. PWM Control Interface Detection

DETAILED DESCRIPTION (continued)

When the PWM pin is constantly high, the dual channel current is regulated to full-scale according to Equation 1. The PWM pin allows PWM signals to reduce this regulation current according to the PWM duty cycle; therefore, it achieves LED brightness dimming. The relationship between the PWM duty cycle and IFBx current is given by Equation 3.

$$I_{FBx} = I_{FB_FULL} \times Duty + 30\mu A \quad (3)$$

Where I_{FBx} is the current of each current sink, I_{FB_FULL} is the full-scale LED current, Duty is the duty cycle information detected from the PWM signals. The PWM frequency is in the range from 10kHz to 100kHz.

Under-Voltage Lockout

An under-voltage lockout circuit prevents the operation of the device at input voltages below under-voltage threshold (2.25V typical). When the input voltage is below the threshold, the device is shut down. If the input voltage rises by under-voltage lockout hysteresis, the IC restarts.

Over-Voltage Protection

Over-voltage protection circuitry prevents IC damage as the result of white LED string disconnection or shortage.

The SGM3743 monitors the voltages at SW pin and IFBx pin during each switching cycle. No matter either SW OVP threshold V_{OVP_SW} or IFBx OVP threshold V_{OVP_FB} is reached due to the LED string open or short issue, the protection circuitry will be triggered. Refer to Figure 7 and Figure 8 for the protection actions.

If one LED string is open, its IFBx pin voltage drops, and the boost output voltage is increased by the control loop as it tries to regulate this lower IFBx voltage to the target value (90mV typical). For the normal string, its current is still under regulation but its IFBx voltage increases along with the output voltage. During the process, either the SW voltage reaches its OVP threshold V_{OVP_SW} or the normal string's IFBx pin voltage reaches the IFBx OVP threshold V_{OVP_FB}, then the protection circuitry will be triggered accordingly.

If both LED strings are open, both IFBx pins' voltages drop to ground, and the boost output voltage is increased by the control loop until reaching the SW OVP threshold V_{OVP_SW}, the SW OVP protection circuitry is triggered. Only VIN POR or EN/PWM pin toggling can restart the IC.

One LED diode short in a string is allowed for the SGM3743. If one LED diode in a string is short, the normal string's IFBx voltage is regulated to about 90mV, and the abnormal string's IFBx pin voltage will be higher. Normally with only one diode short, the higher IFBx pin voltage does not reach the IFBx OVP threshold V_{OVP_FB}, so the protection circuitry will not be triggered.

If more than one LED diodes are short in a string, as the boost loop regulates the normal string's IFBx voltage to 90mV, this abnormal string's IFBx pin voltage is much higher and will reach V_{OVP_FB}, then the protection circuitry is triggered.

The SW OVP protection will also be triggered when the forward voltage drop of an LED string exceeds the SW OVP threshold.

Over-Current Protection

The SGM3743 has a pulse-by-pulse over-current limit. The boost switch turns off when the inductor current reaches this current threshold and it remains off until the beginning of the next switching cycle. This protects the SGM3743 and external component under overload conditions.

Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 150℃ is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15℃.

DETAILED DESCRIPTION (continued)

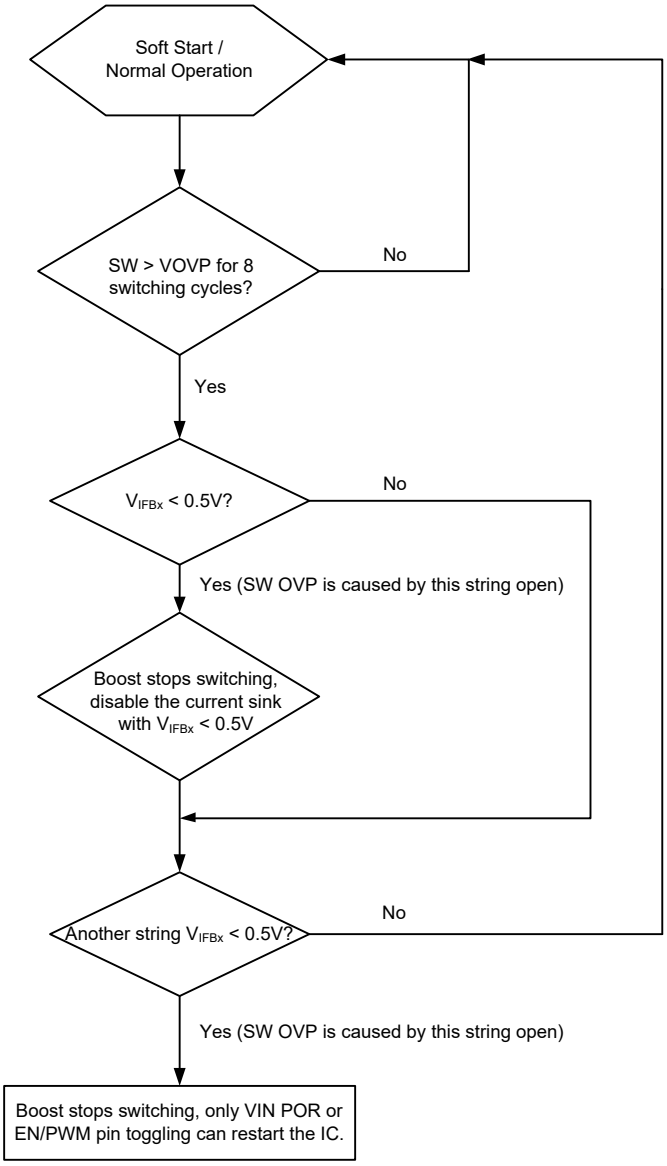


Figure 7. SW OVP Protection Action

DETAILED DESCRIPTION (continued)

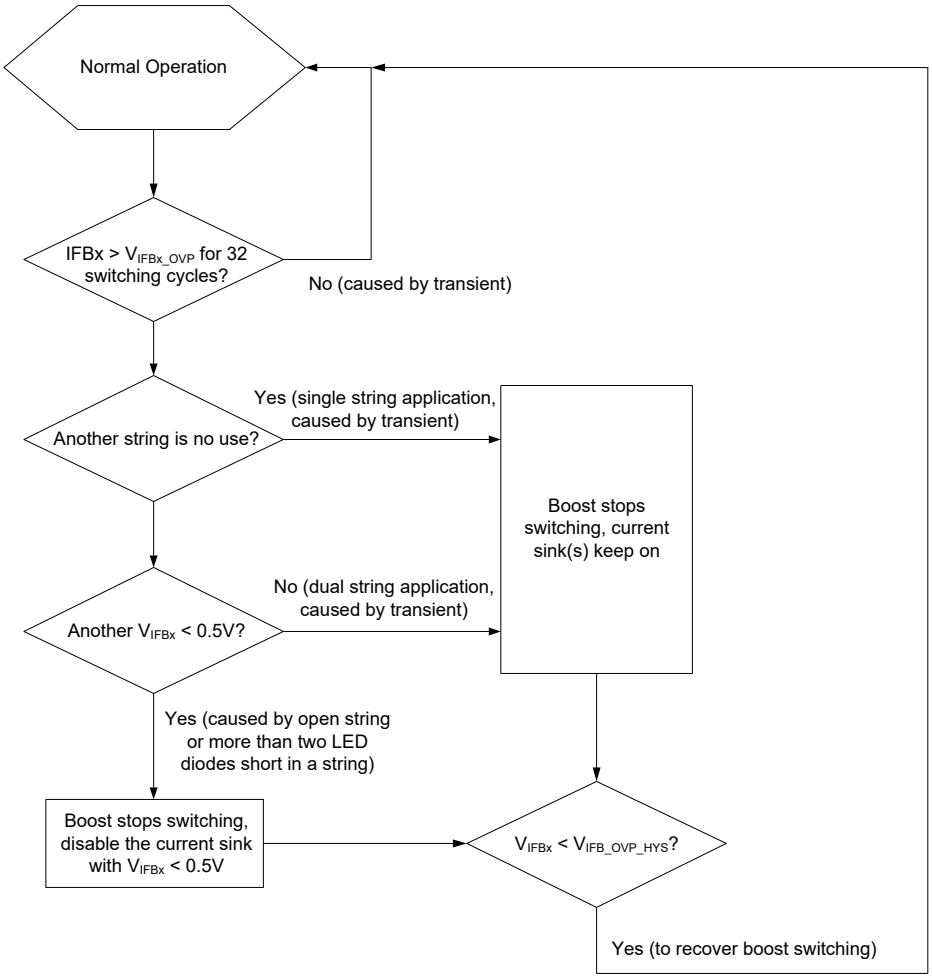


Figure 8. VIFBx OVP Protection Action

APPLICATION INFORMATION

Inductor Selection

Because the selection of inductor affects power supply's steady state operation, transient behavior, loop stability and the boost converter efficiency, the inductor is one of the most important components in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance, and saturation current. The SGM3743 is designed to work with inductor values from 4.7μH to 10μH. A 4.7μH inductor is typically available in a smaller or lower profile package, while a 10μH inductor produces lower inductor ripple. If the boost output current is limited by the over-current protection of the IC, using a 10μH inductor may maximize the controller's output current capability.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. When selecting an inductor, please make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation 4 to Equation 6 to calculate the inductor's peak current. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage and maximum load current of the application. In order to leave enough design margin, the minimum switching frequency (1.2MHz), the inductor value with -30% tolerance, and a low power conversion efficiency, such as 80% or lower are recommended for the calculation.

In a boost regulator, the inductor DC current can be calculated as Equation 4.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (4)$$

where
V_{OUT} = boost output voltage
I_{OUT} = boost output current
V_{IN} = boost input voltage
η = boost power conversion efficiency

The inductor current peak to peak ripple can be calculated as Equation 5.

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times f_S} \quad (5)$$

where
I_{PP} = inductor peak-to-peak ripple
L = inductor value
f_S = boost switching frequency
V_{OUT} = boost output voltage
V_{IN} = boost input voltage

Therefore, the peak current I_P seen by the inductor is calculated with Equation 6.

$$I_P = I_{DC} + \frac{I_{PP}}{2} \quad (6)$$

Select an inductor with saturation current over the calculated peak current. If the calculated peak current is larger than the switch MOSFET current limit I_{LIM}, use a larger inductor, such as 10μH, and make sure its peak current is below I_{LIM}.

APPLICATION INFORMATION (continued)

Boost converter efficiency is dependent on the resistance of its current path, the switching losses associated with the switch MOSFET and power diode and the inductor's core loss. The SGM3743 has optimized the internal switch resistance, however, the overall efficiency is affected a lot by the inductor's DC Resistance (DCR), Equivalent Series Resistance (ESR) at the switching frequency and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR/ESR conduction losses as well as higher core loss. Normally a datasheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, an inductor with lower DCR/ESR is recommended for SGM3743 application. However, there is a trade off among inductor's inductance, DCR/ESR resistance, and its footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones. Table 2 lists some recommended inductors for the SGM3743. Verify whether the recommended inductor can support your target application by the calculations above as well as bench validation.

Table 2. Recommended Inductors

Part Number	L (μH)	DCR Max (mΩ)	Saturation Current (A)	Size (L × W × H mm)	Vendor
LPS4018-472ML	4.7	125	1.9	4 × 4 × 1.8	Coilcraft
LPS4018-682ML	6.8	150	1.3	4 × 4 × 1.8	Coilcraft
LPS4018-103ML	10	200	1.3	4 × 4 × 1.8	Coilcraft
PCMB051B-4R7M	4.7	163	2.7	5.4 × 5.2 × 1.2	Cyntec
PCMB051B-6R8M	6.8	250	2.3	5.4 × 5.2 × 1.2	Cyntec

Schottky Diode Selection

The SGM3743 demands a low forward voltage, high-speed and low capacitance schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. ONSemi MBR0540 and NSR05F40, and Vishay MSS1P4 are recommended for the SGM3743.

Compensation Capacitor Selection

The compensation capacitor C4 (refer to Additional Application Circuits) connected from the COMP pin to GND, is used to stabilize the feedback loop of the SGM3743. A 330nF ceramic capacitor for C4 is suitable for most applications.

Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for the output ripple and loop stability. A 1μF to 2.2μF capacitor is recommended for the loop stability consideration. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Due to its low ESR, V_{RIPPLE_ESR} could be neglected for ceramic capacitors. Assuming a capacitor with zero ESR, the output ripple can be calculated with Equation 7.

$$V_{RIPPLE} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times f_S \times C_{OUT}} \quad (7)$$

Where: V_{RIPPLE} = peak-to-peak output ripple. The additional part of ripple caused by the ESR is calculated using $V_{RIPPLE_ESR} = I_{OUT} \times R_{ESR}$ and can be ignored for ceramic capacitors.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

APPLICATION INFORMATION (continued)

Layout Consideration

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in Additional Application Circuits, needs to be close to the inductor, as well as the VIN pin and GND pin in order to reduce the input ripple seen by the IC. If possible, choose higher capacitance value for it. If the ripple seen at VIN pin is so large that it affects the boost loop stability or internal circuits operation, R2 and C3 are recommended to filter and decouple the noise. In this case, C3 should be placed as close as possible to the VIN and GND pins. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor and schottky diode should be kept as short and wide as possible. The trace between schottky diode and the output capacitor C2 should also be as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the GND pin since there is a large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point close to the GND pin.

ADDITIONAL APPLICATION CIRCUITS

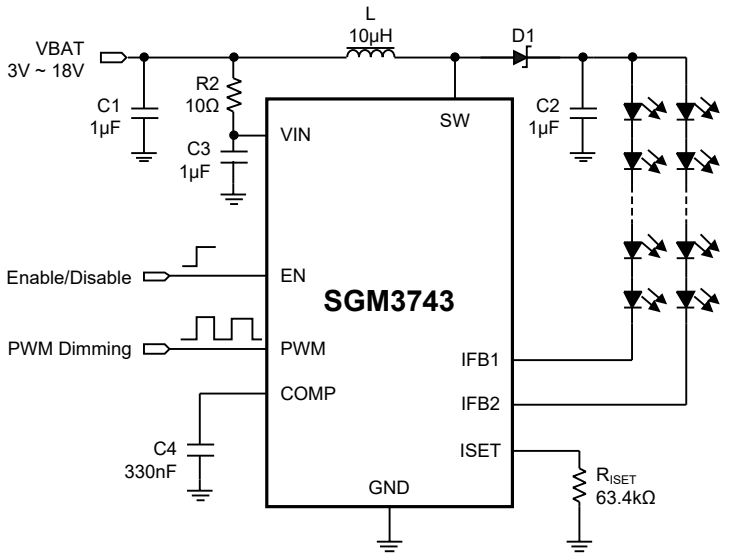


Figure 9. SGM3743 Typical Application (PWM interface enabled, EN pin can be used to enable or disable the IC)

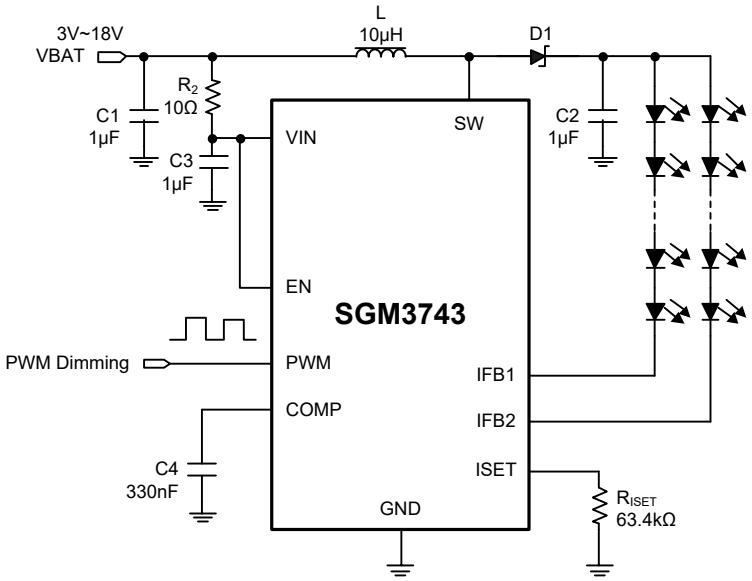


Figure 10. SGM3743 Typical Application
(PWM interface enabled, EN pin connected to VIN, only PWM signal is used to enable or disable the IC)

ADDITIONAL APPLICATION CIRCUITS (continued)

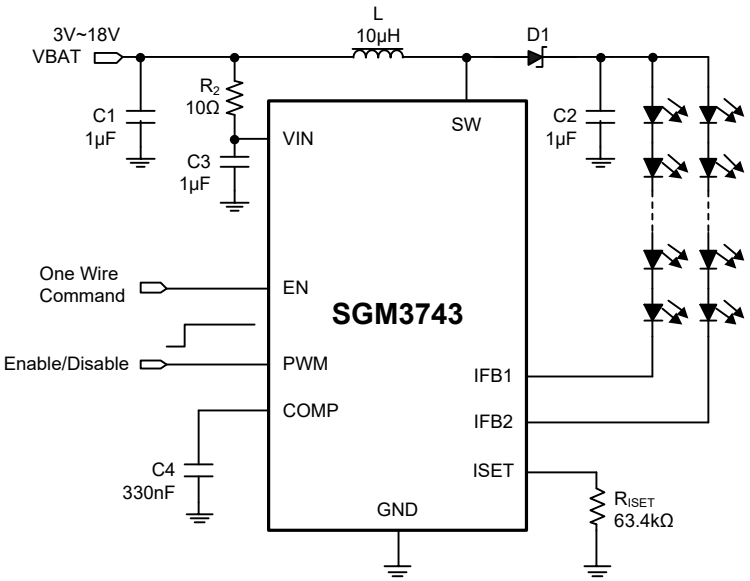


Figure 11. SGM3743 Typical Application
(One wire digital interface enabled, PWM pin can be used to enable or disable the IC)

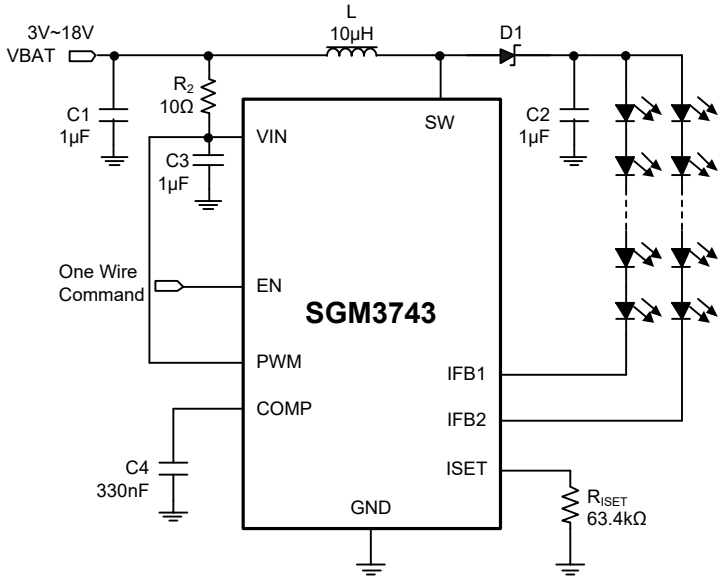


Figure 12. SGM3743 Typical Application
(One wire digital interface enabled, PWM pin connected to VIN, only EN signal is used to enable or disable the IC)

REVISION HISTORY

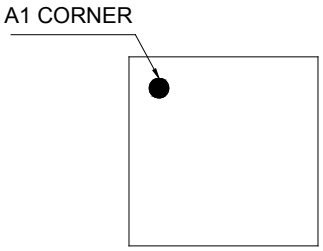
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

FEBRUARY 2021 – REV.A to REV.A.1	Page
Updated Marking Information section	2

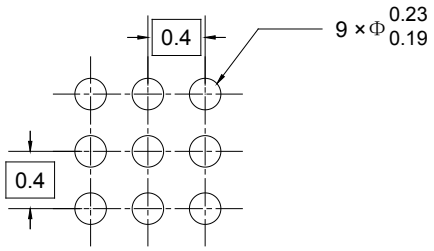
Changes from Original (JUNE 2016) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

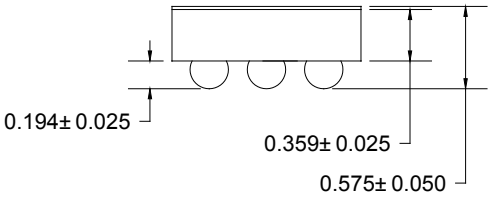
WLCSP-1.32×1.32-9B



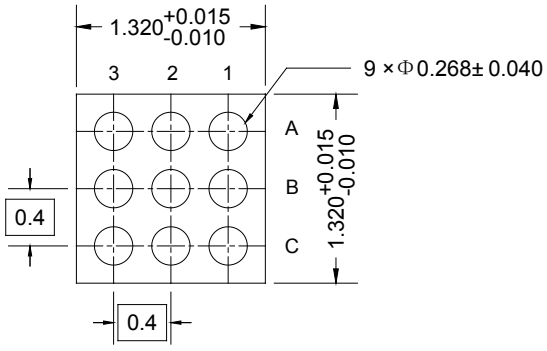
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

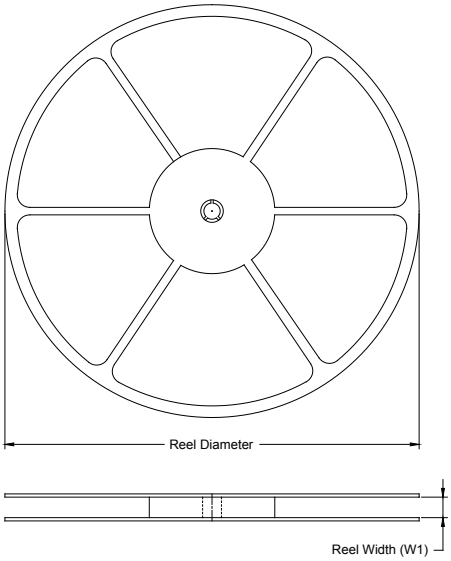


BOTTOM VIEW

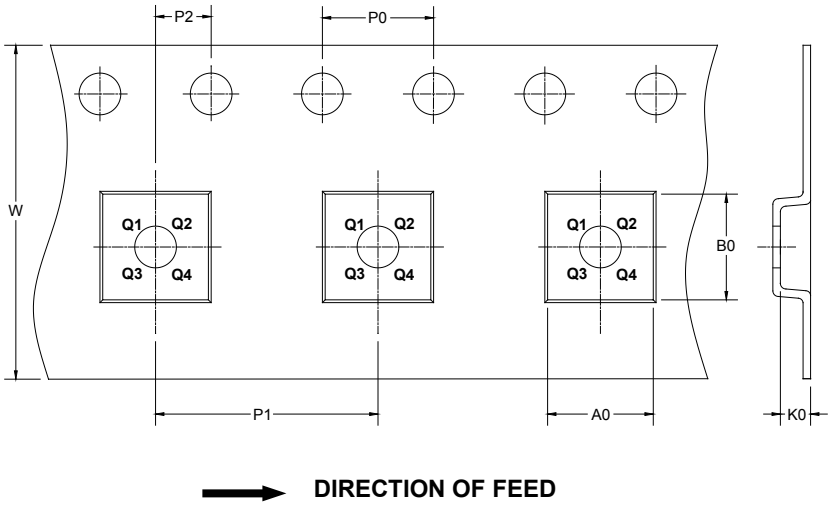
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



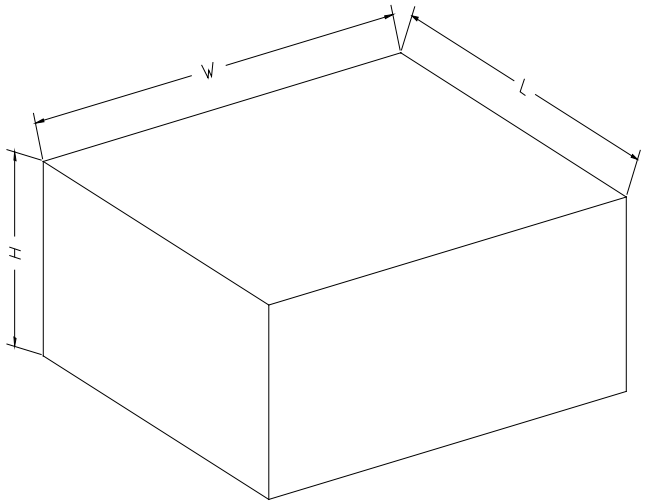
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.32×1.32-9B	7″	9.5	1.38	1.38	0.70	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002