SGM5351-16
16-Bit, Ultra-Low Glitch, Voltage-Output Digital-to-Analog Converter

GENERAL DESCRIPTION

The SGM5351-16 is a low power, single channel, 16-bit, voltage-output DAC. It operates from a 2.7V to 5.5V supply and the monotonicity is guaranteed by design.

The SGM5351-16 sets the output range by using an external reference voltage. It incorporates a power-on reset circuit that ensures the DAC output powers to 0V and remains powered up at this level until a valid write takes place. The SGM5351-16 provides a power-down mode accessed via the serial interface that reduces the current consumption of the device to 450nA (TYP) at 5.5V. The SGM5351-16 consumes 0.27mW (TYP) at 2.7V in normal mode, which reduces to less than 1μW in power-down mode, the low power consumption in normal mode is very suitable for portable battery-operated equipment.

The SGM5351-16 uses a 3-wire serial interface which can be operated at clock rates to 30MHz and is compatible with standard SPI interface.

The SGM5351-16 is available in a Green MSOP-8 package. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Power Supply Range: 2.7V to 5.5V**
- **16-Bit DAC, Monotonicity Guaranteed by Design**
- **6LSB (TYP) Relative Accuracy**
- **Low Power Operation: 100μA at 2.7V**
- **Power-On Reset to Zero-Scale**
- **10μs (TYP) Settling Time**
- **3-Wire Serial Interface with Schmitt Trigger Logic Inputs**
- **Rail-to-Rail Buffered Voltage-Output Operation**
- **Binary Code Input**
- **Power-Down Function**
- **nSYNC Interrupt Facility**
- **Available in a Green MSOP-8 Package**

APPLICATIONS

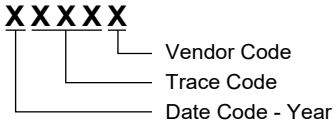
Portable Instrumentation
Programmable Attenuators
Process Control
Closed-Loop Servo-Control
Data Acquisition Systems

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5351-16	MSOP-8	-40℃ to +125℃	SGM5351-16XMS8G/TR	SGMSVP XMS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range ..... -0.3V to 6V
Digital Input Voltage Range ..... -0.3V to V_{CC} + 0.3V
Output Voltage Range ..... -0.3V to V_{CC} + 0.3V
Package Thermal Resistance
MSOP-8, θ_{JA} ..... 168℃/W
MSOP-8, θ_{JC} ..... 65℃/W
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility
HBM.....±4000V
CDM .....±1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range (V_{CC} to GND).....2.7V to 5.5V
Digital Input Voltage Range ($D_{IN/OUT}$, SCLK, and nSYNC)
..... 0V to V_{CC}
Reference Input Voltage Range, V_{REF} ..... 0V to V_{CC}
Output Amplifier Feedback Input, V_{FB} .....V_{OUT}
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

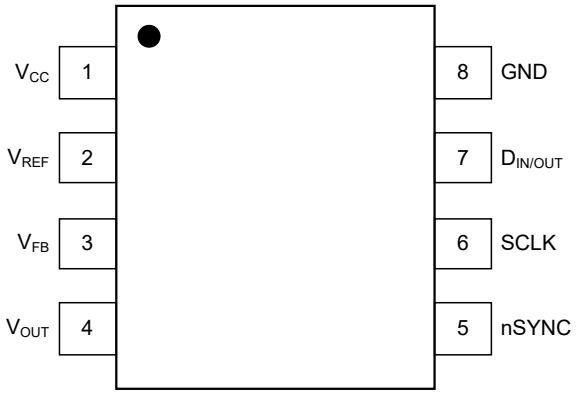
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



MSOP-8

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	V_{CC}	P	Power Supply Pin. It can be operated from 2.7V to 5.5V.
2	V_{REF}	I	Reference Voltage Input Pin.
3	V_{FB}	I	Output Amplifier Feedback Input Pin. Connect to V_{OUT} externally for the voltage-output operation.
4	V_{OUT}	O	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
5	nSYNC	I	Frame Synchronization Input Pin. Active low. When this pin goes low, data is transferred into the input shift register on the falling edges of SCLK. After the 24^{th} falling edge of SCLK, the DAC is updated. If nSYNC is brought high before this edge, the rising edge of nSYNC acts as an interrupt and the write sequence is ignored by the DAC.
6	SCLK	I	Serial Clock Input Pin. Data can be transferred at clock rates to 30MHz Schmitt-Trigger logic input.
7	$D_{IN/OUT}$	I/O	Serial Data Input/Output Pin. Data is clocked into the 24-bit input shift register on the falling edge of SCLK.
8	GND	G	Ground Pin.

NOTE:
1. I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Static Performance (1)						
Resolution			16			Bits
Relative Accuracy		Measured by line passing through codes 485 and 64741 at V_{REF} = 5.4V, codes 970 and 63947 at V_{REF} = 2.5V		6	12	LSB
Differential Nonlinearity	DNL	2.5V ≤ V_{REF} ≤ 5.5V, -40℃ ≤ T_A ≤ +125℃		0.5	1	LSB
Zero-Code Error		Measured by line passing through codes 485 and 64741		0.55	2.5	mV
Full-Scale Error		Measured by line passing through codes 485 and 64741		0.06	0.2	% of FSR
Gain Error		Measured by line passing through codes 485 and 64741		0.05	0.15	% of FSR
Zero-Code Error Drift				4		μV/℃
Gain Temperature Coefficient				1		ppm of FSR/℃
Power-Supply Rejection Ratio	PSRR	R_L = 2kΩ, C_L = 200pF		0.15		mV/V
Output Characteristics (2)						
Output Voltage Range			0		V_{REF}	V
Output Voltage Settling Time		R_L = 2kΩ, C_L = 50pF		10		μs
Slew Rate				1		V/μs
Capacitive Load Stability		R_L = ∞		2		nF
		R_L = 2kΩ		10		
Code Change Glitch Impulse		1LSB change around major carry		20		nV-s
Digital Feedthrough		50kΩ series resistance on digital lines		0.1		nV-s
DC Output Impedance		At mid-code input		0.3		Ω
Short-Circuit Current		V_{CC} = 5V		38		mA
		V_{CC} = 3V		36		
Power-Up Time		Coming out of power-down mode, V_{CC} = 5V		16		μs
		Coming out of power-down mode, V_{CC} = 3V		14		
AC Performance						
Signal-to-Noise Ratio	SNR	BW = 20kHz, V_{CC} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		54		dB
Total Harmonic Distortion	THD	BW = 20kHz, V_{CC} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		-62		dB
Spurious-Free Dynamic Range	SFDR	BW = 20kHz, V_{CC} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		66		dB
Signal-to-Noise and Distortion	SINAD	BW = 20kHz, V_{CC} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		53		dB
Reference Input						
Reference Input Current		V_{REF} = V_{CC} = 5V		21	26	μA
		V_{REF} = V_{CC} = 3.6V		15	22	
Reference Input Range			0		V_{CC}	V
Reference Input Impedance				235		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.7V to 5.5V, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (2)							
Input Current					10		nA
Input Low Voltage	V_{IL}	V_{CC} = 5.5V				1	V
		V_{CC} = 2.7V				0.6	
Input High Voltage	V_{IH}	V_{CC} = 5.5V		2.1			V
		V_{CC} = 2.7V		1.5			
Pin Capacitance					2		pF
Power Requirements							
Supply Voltage	V_{CC}			2.7		5.5	V
Supply Current	I_{CC}	Normal mode, input code = 32768, no load, does not include reference current, V_{IH} = V_{CC}, V_{IL} = GND	V_{CC} = 5.5V		108	150	μA
			V_{CC} = 2.7V		100	130	
		All power-down modes, V_{IH} = V_{CC}, V_{IL} = GND	V_{CC} = 5.5V		0.45	2	
			V_{CC} = 2.7V		0.32	2	
I_{OUT}/I_{CC} Power Efficiency		I_{LOAD} = 2mA, V_{CC} = 5V			95		%
Specified Performance Temperature				-40		125	℃

NOTES:

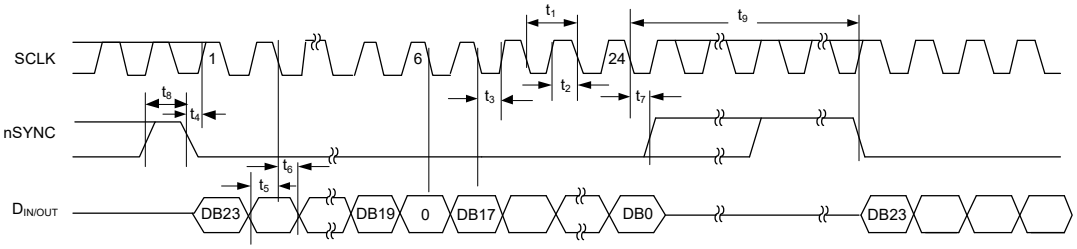
1. Linearity calculated using a reduced codes range of 485 and 64741 at V_{REF} = 5.4V, codes 970 and 63947 at V_{REF} = 2.5V; output unloaded, 100mV headroom between reference and supply.
2. Guaranteed by design. Not production tested.

TIMING CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40℃ to +125℃, unless otherwise noted.) (1) (2)

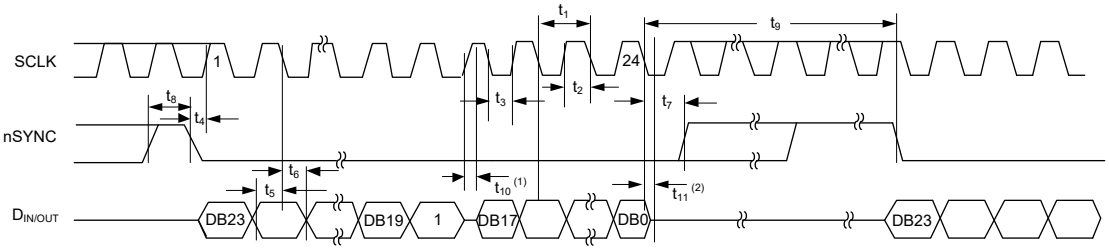
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Cycle Time (3)	t_1	V_{CC} = 2.7V to 3.6V	50			ns
		V_{CC} = 3.6V to 5.5V	33			
SCLK High Time	t_2	V_{CC} = 2.7V to 3.6V	10			ns
		V_{CC} = 3.6V to 5.5V	11			
SCLK Low Time	t_3	V_{CC} = 2.7V to 3.6V	11			ns
		V_{CC} = 3.6V to 5.5V	11			
nSYNC Falling Edge to SCLK Rising Edge Setup Time	t_4	V_{CC} = 2.7V to 3.6V	0			ns
		V_{CC} = 3.6V to 5.5V	0			
Data Setup Time	t_5	V_{CC} = 2.7V to 3.6V	5			ns
		V_{CC} = 3.6V to 5.5V	5			
Data Hold Time	t_6	V_{CC} = 2.7V to 3.6V	5			ns
		V_{CC} = 3.6V to 5.5V	5			
24th SCLK Falling Edge to nSYNC Rising Edge	t_7	V_{CC} = 2.7V to 3.6V	0			ns
		V_{CC} = 3.6V to 5.5V	0			
Minimum nSYNC High Time	t_8	V_{CC} = 2.7V to 3.6V	22			ns
		V_{CC} = 3.6V to 5.5V	26			
24th SCLK Falling Edge to nSYNC Falling Edge	t_9	V_{CC} = 2.7V to 5.5V	100			ns
$D_{IN/OUT}$ Tri-State to Driven	t_{10}	V_{CC} = 2.7V to 5.5V	15			ns
24th SCLK Falling Edge to $D_{IN/OUT}$ Tri-State	t_{11}	V_{CC} = 2.7V to 5.5V	0			ns

NOTES:
1. All input signals are specified with t_R = t_F = 5ns (10% to 90% of V_{CC}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
2. Refer to Figure 1 and Figure 2.
3. Maximum SCLK frequency is 30MHz at V_{CC} = 3.6V to 5.5V and 20MHz at V_{CC} = 2.7V to 3.6V.



NOTE: 1. When DB[18] = 0, this is a write operation, the data DB[17:0] is locked into DAC on each falling edge of SCLK.

Figure 1. Serial Write Operation



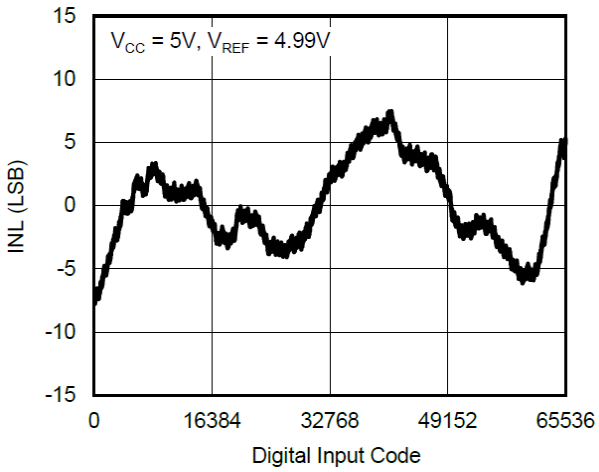
NOTES:
1. When DB[18] = 1, this is a read operation, the data DB[17:0] is read from DAC. On the rising edge of 7th of SCLK, the $D_{IN/OUT}$ is switched from input to output, the data of internal register is put on the bus on each rising edge of SCLK.
2. On the 24th falling edge of SCLK, the $D_{IN/OUT}$ is turned off to Hi-Z.

Figure 2. Serial Read Operation

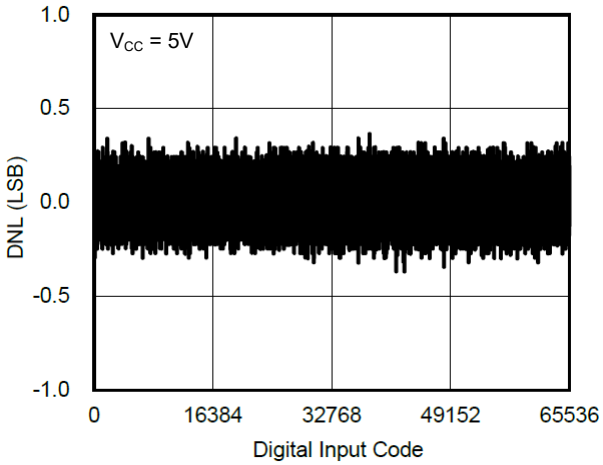
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

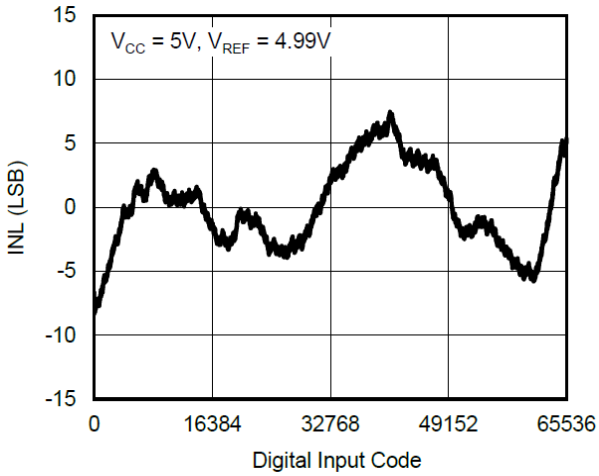
INL vs. Digital Input Code (-40℃)



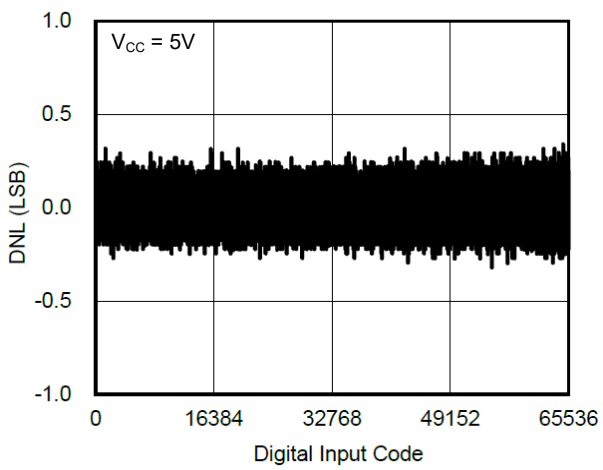
DNL vs. Digital Input Code (-40℃)



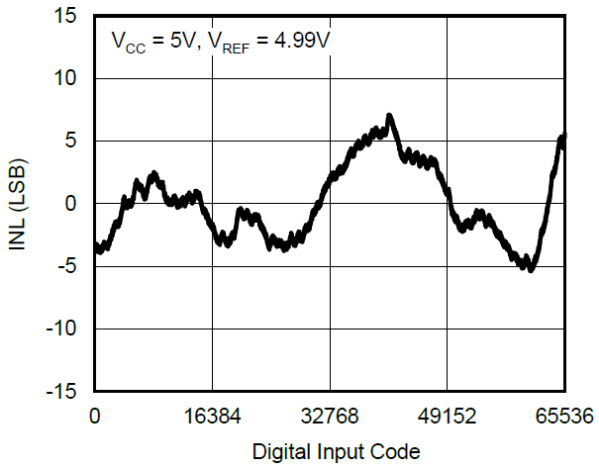
INL vs. Digital Input Code (+25℃)



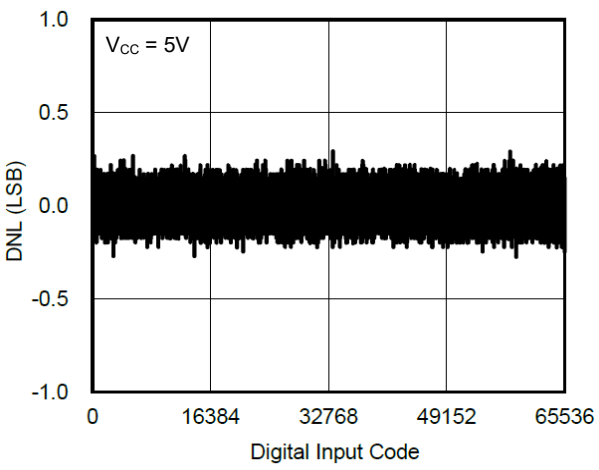
DNL vs. Digital Input Code (+25℃)



INL vs. Digital Input Code (+125℃)



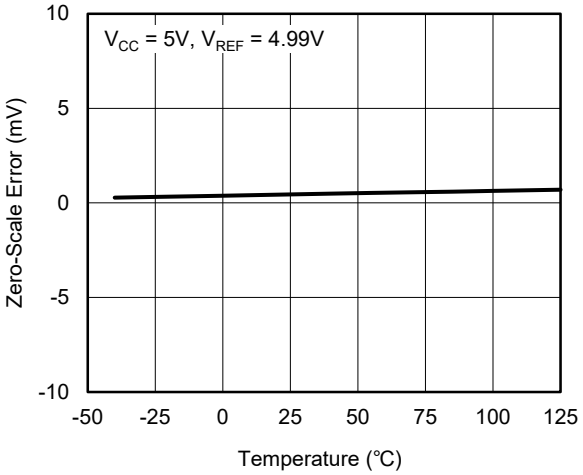
DNL vs. Digital Input Code (+125℃)



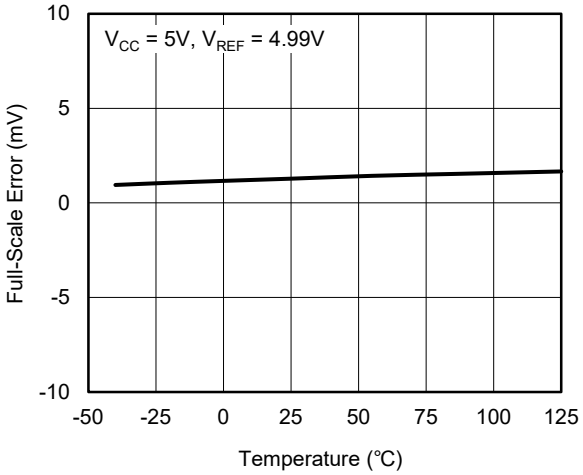
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

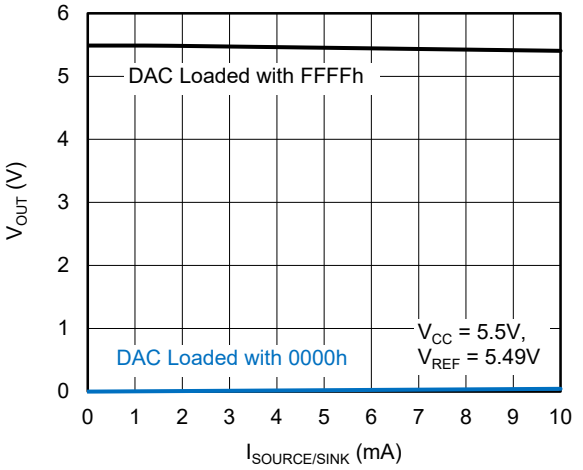
Zero-Scale Error vs. Temperature



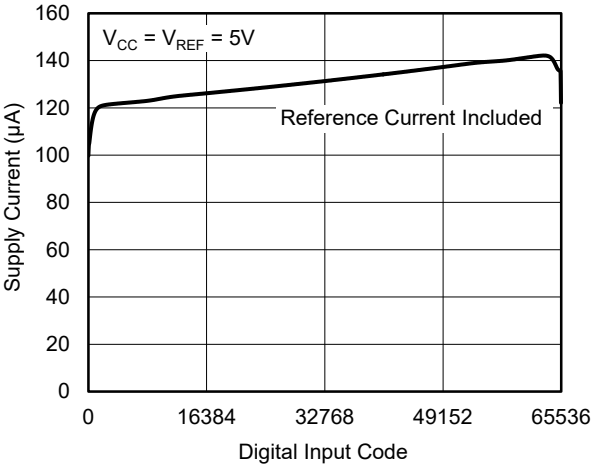
Full-Scale Error vs. Temperature



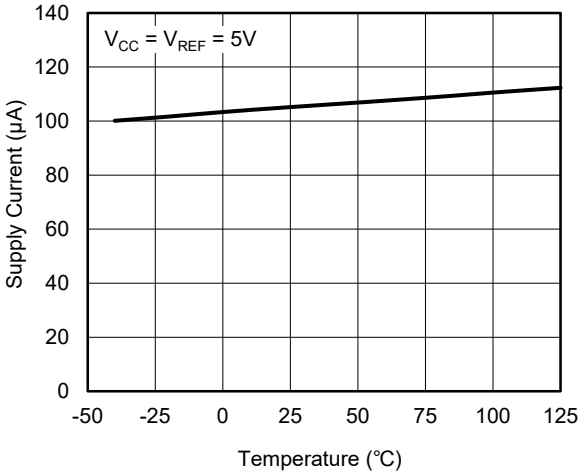
Source and Sink Current Capability



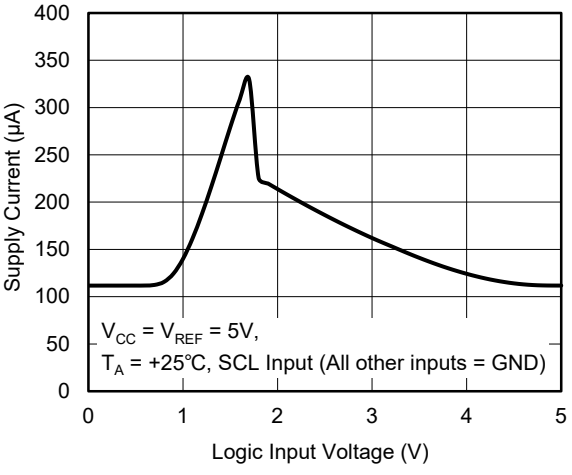
Supply Current vs. Digital Input Code



Supply Current vs. Temperature



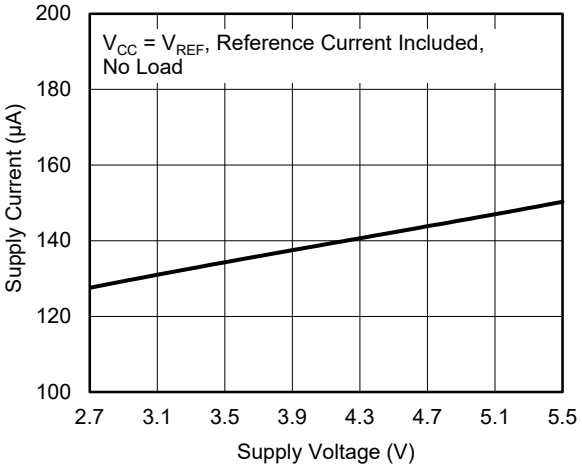
Supply Current vs. Logic Input Voltage



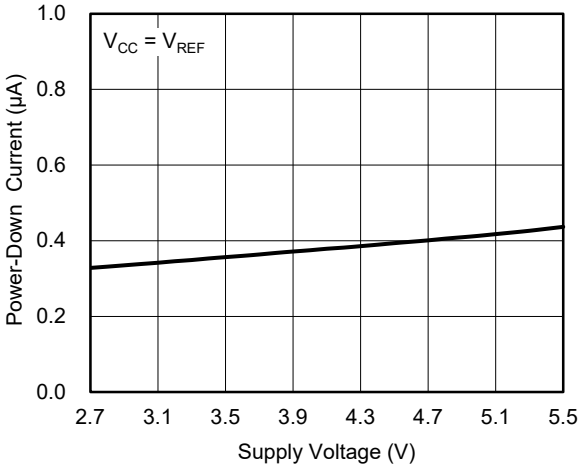
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

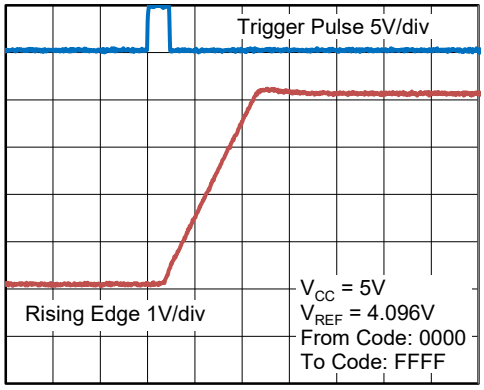
Supply Current vs. Supply Voltage



Power-Down Current vs. Supply Voltage

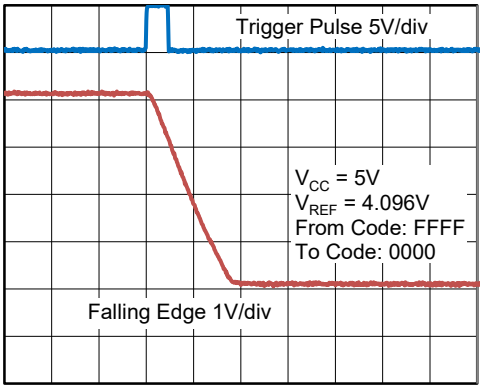


Full-Scale Settling Time, 5V Rising Edge



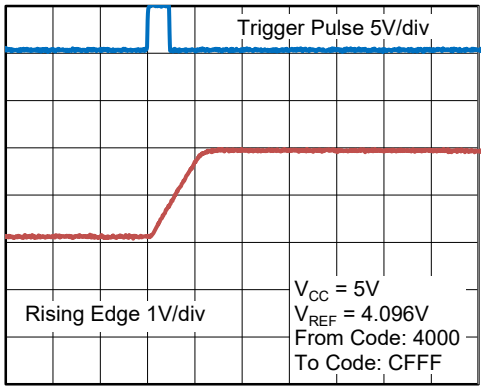
Time (2μs/div)

Full-Scale Settling Time, 5V Falling Edge



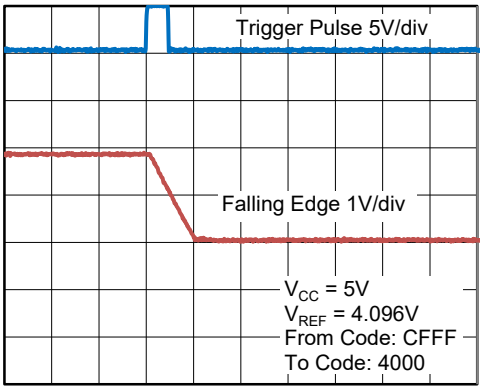
Time (2μs/div)

Half-Scale Settling Time, 5V Rising Edge



Time (2μs/div)

Half-Scale Settling Time, 5V Falling Edge

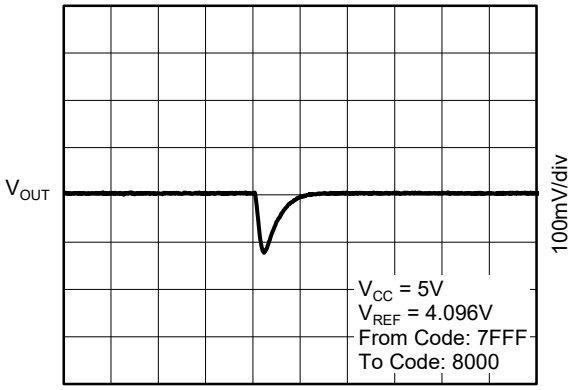


Time (2μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

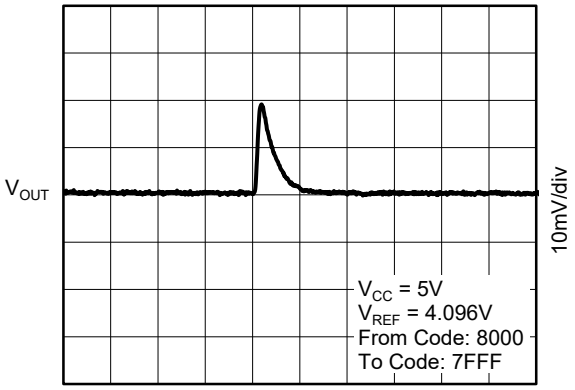
T_A = +25℃, unless otherwise noted.

Glitch Energy: 5V, 1LSB Step, Rising Edge



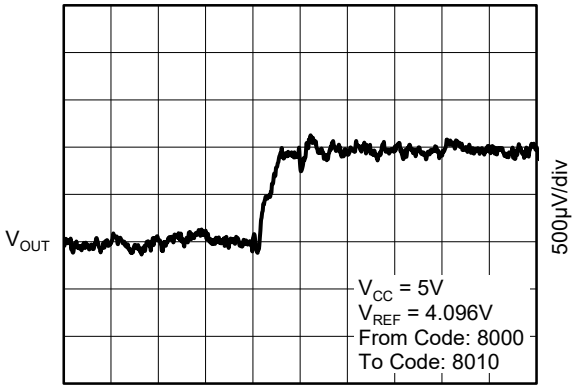
Time (2μs/div)

Glitch Energy: 5V, 1LSB Step, Falling Edge



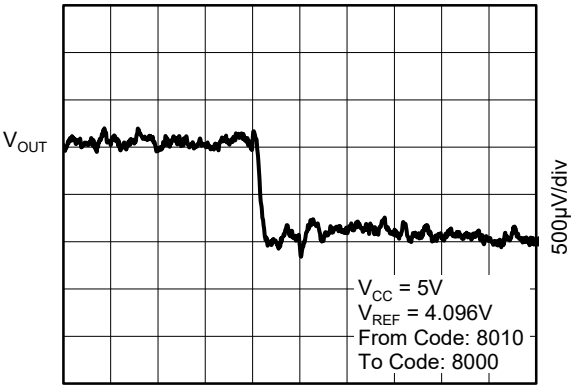
Time (2μs/div)

Glitch Energy: 5V, 16LSB Step, Rising Edge



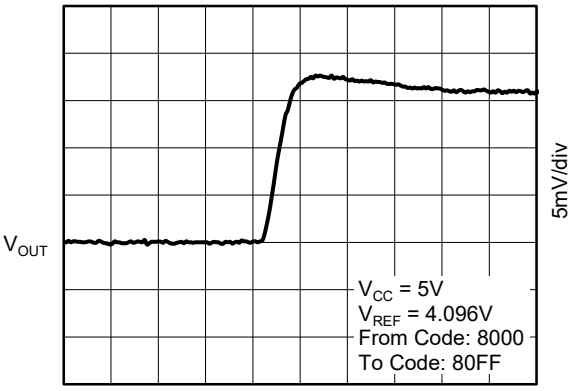
Time (2μs/div)

Glitch Energy: 5V, 16LSB Step, Falling Edge



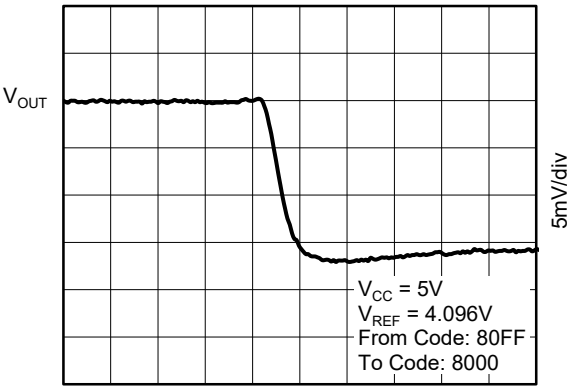
Time (2μs/div)

Glitch Energy: 5V, 256LSB Step, Rising Edge



Time (500ns/div)

Glitch Energy: 5V, 256LSB Step, Falling Edge

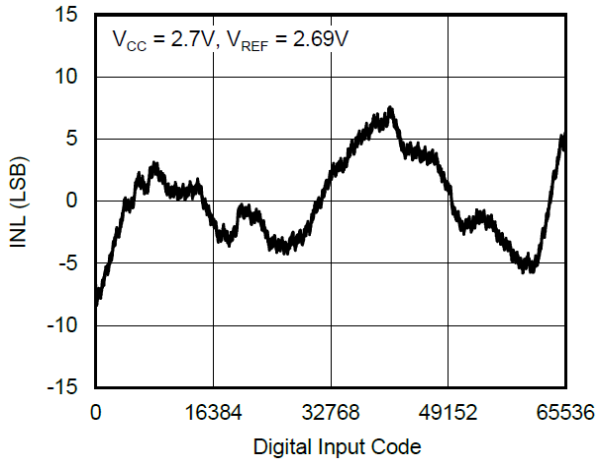


Time (500ns/div)

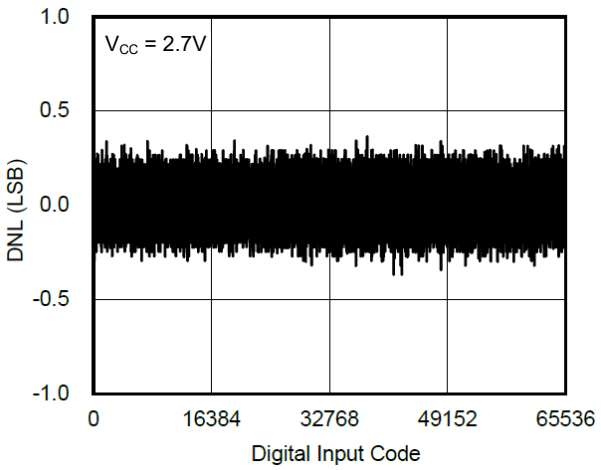
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

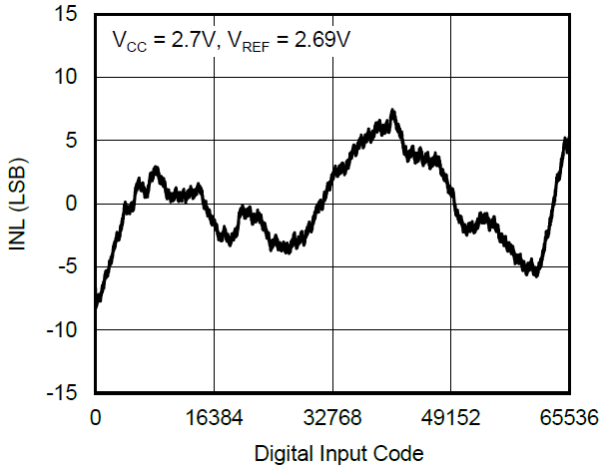
INL vs. Digital Input Code (-40℃)



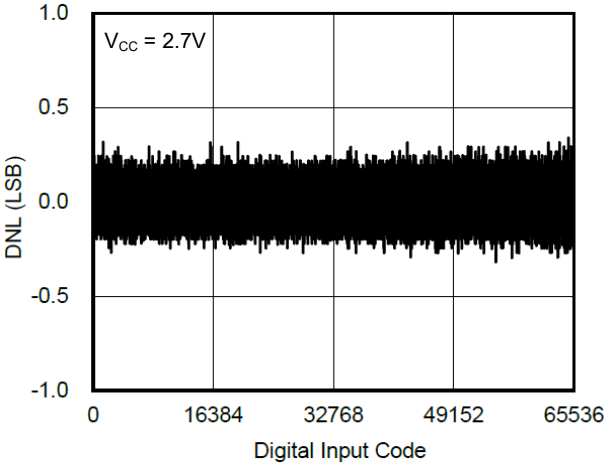
DNL vs. Digital Input Code (-40℃)



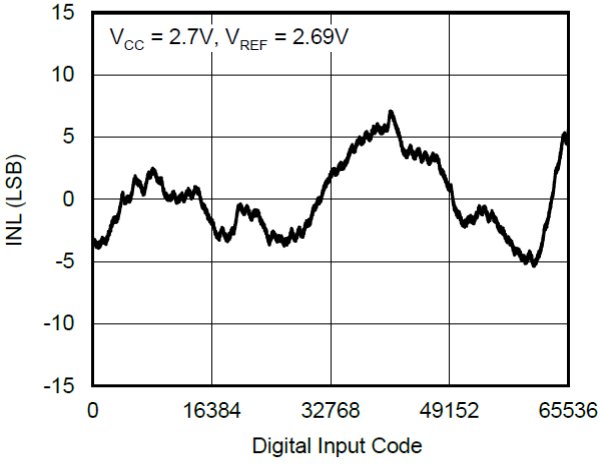
INL vs. Digital Input Code (+25℃)



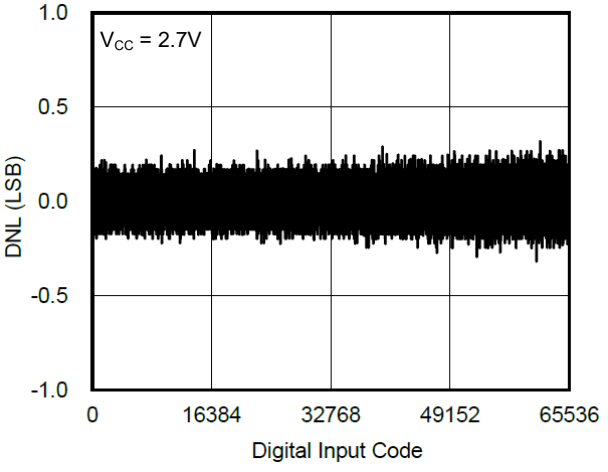
DNL vs. Digital Input Code (+25℃)



INL vs. Digital Input Code (+125℃)



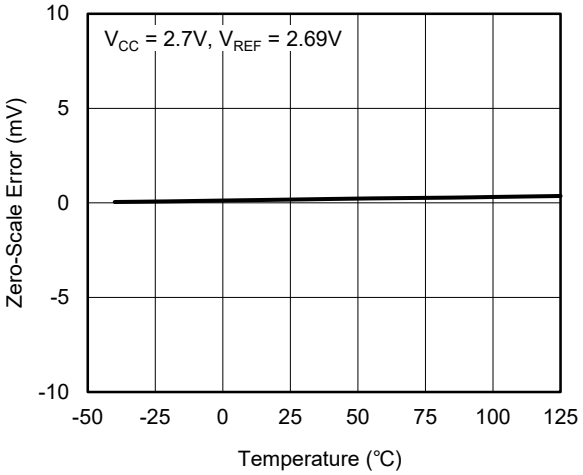
DNL vs. Digital Input Code (+125℃)



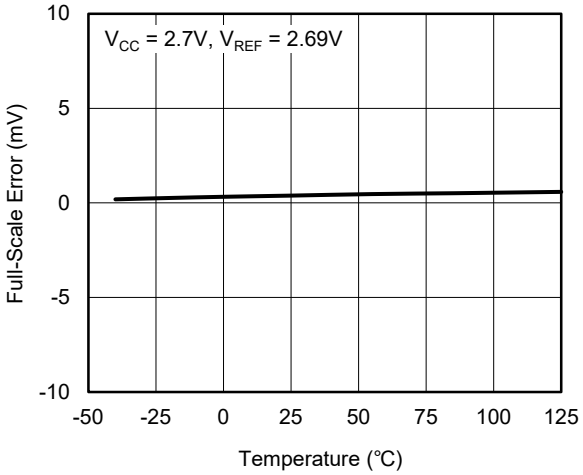
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

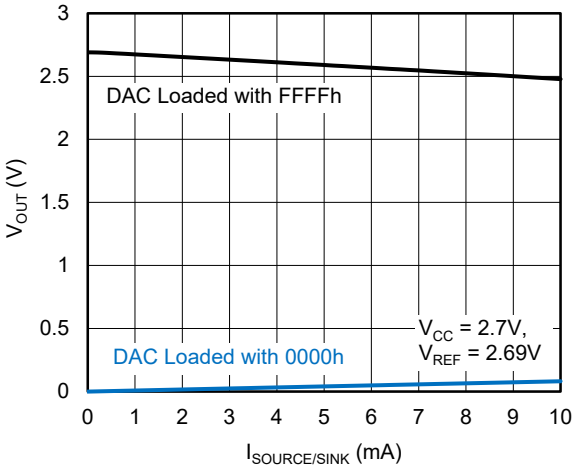
Zero-Scale Error vs. Temperature



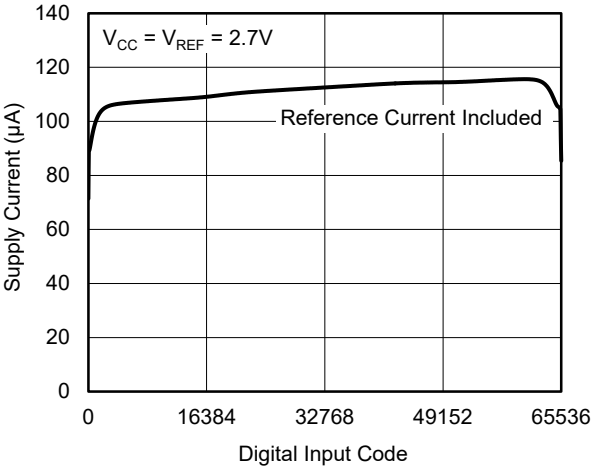
Full-Scale Error vs. Temperature



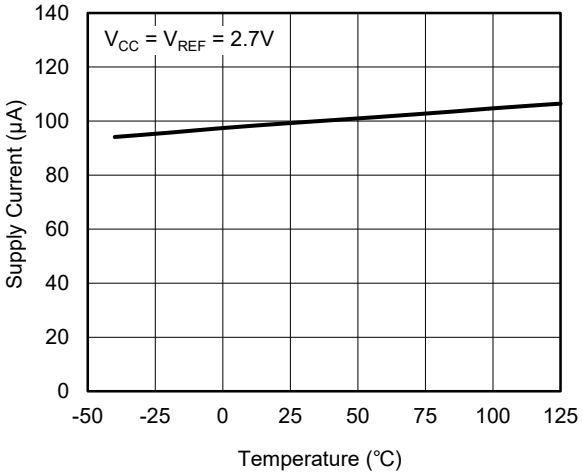
Source and Sink Current Capability



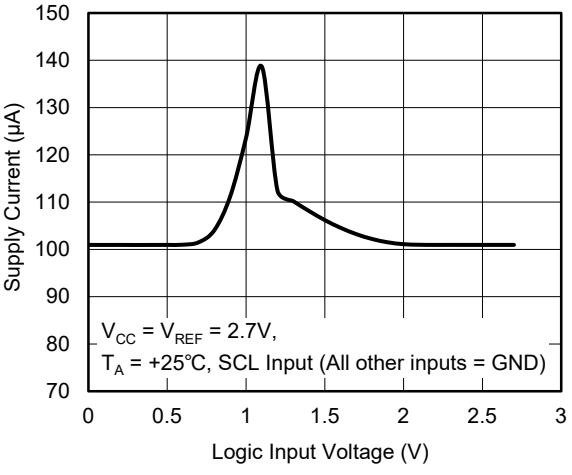
Supply Current vs. Digital Input Code



Supply Current vs. Temperature



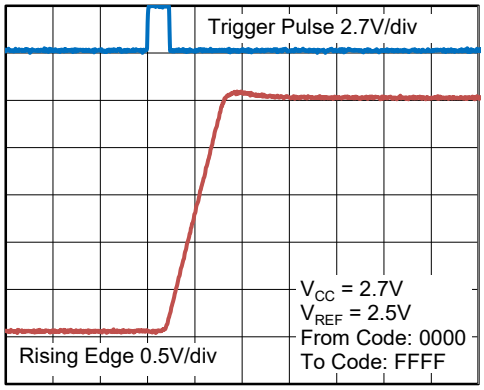
Supply Current vs. Logic Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

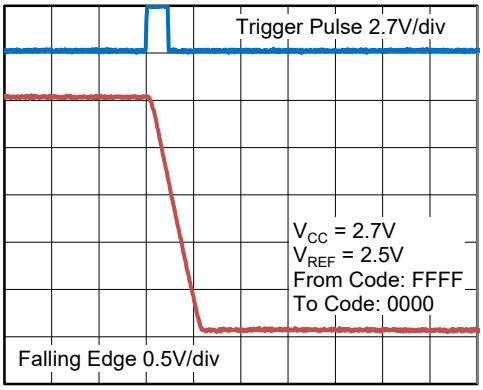
T_A = +25℃, unless otherwise noted.

Full-Scale Settling Time: 2.7V Rising Edge



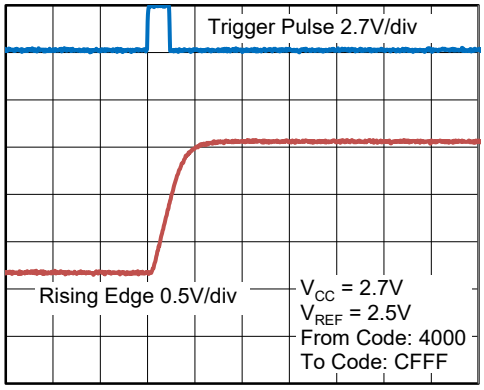
Time (2μs/div)

Full-Scale Settling Time: 2.7V Falling Edge



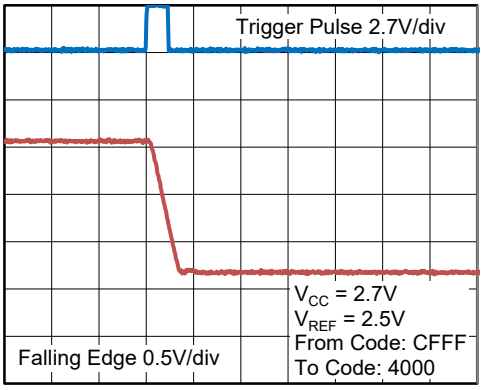
Time (2μs/div)

Half-Scale Settling Time: 2.7V Rising Edge



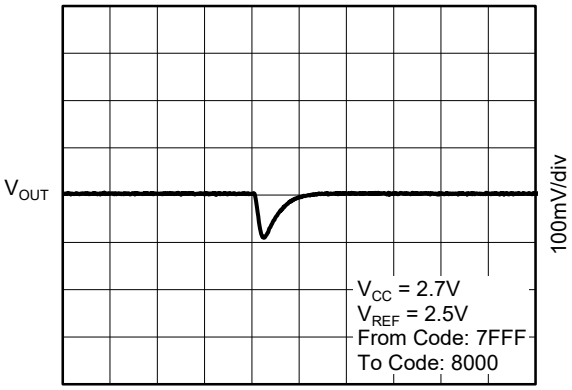
Time (2μs/div)

Half-Scale Settling Time: 2.7V Falling Edge



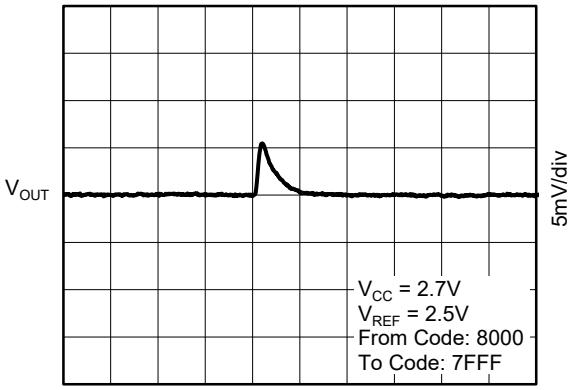
Time (2μs/div)

Glitch Energy: 2.7V, 1LSB Step, Rising Edge



Time (2μs/div)

Glitch Energy: 2.7V, 1LSB Step, Falling Edge

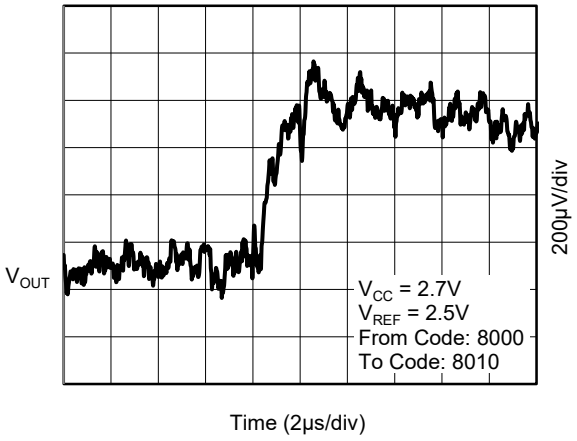


Time (2μs/div)

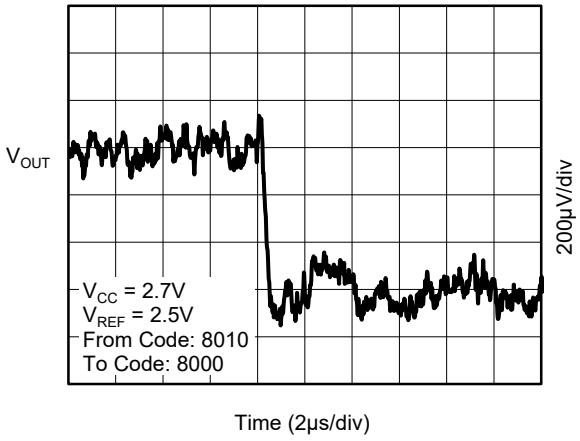
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

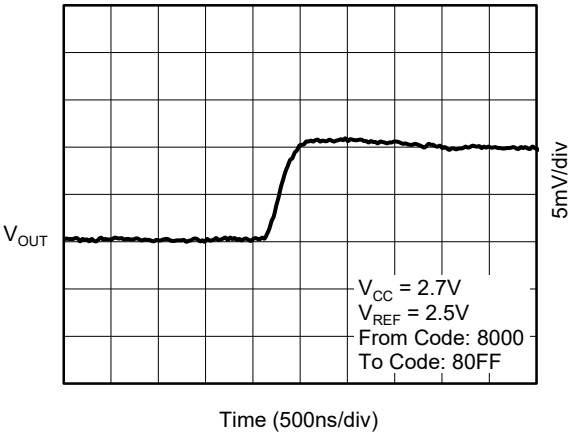
Glitch Energy: 2.7V, 16LSB Step, Rising Edge



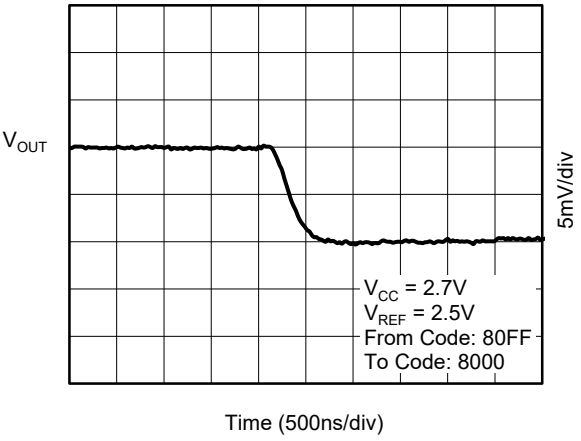
Glitch Energy: 2.7V, 16LSB Step, Falling Edge



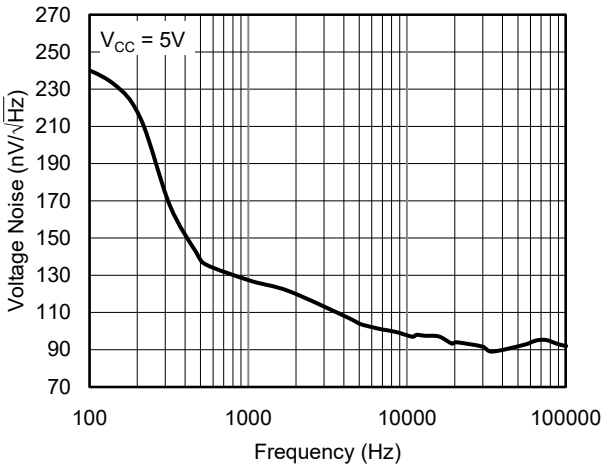
Glitch Energy: 2.7V, 256LSB Step, Rising Edge



Glitch Energy: 2.7V, 256LSB Step, Falling Edge



Output Noise Density



FUNCTIONAL BLOCK DIAGRAM

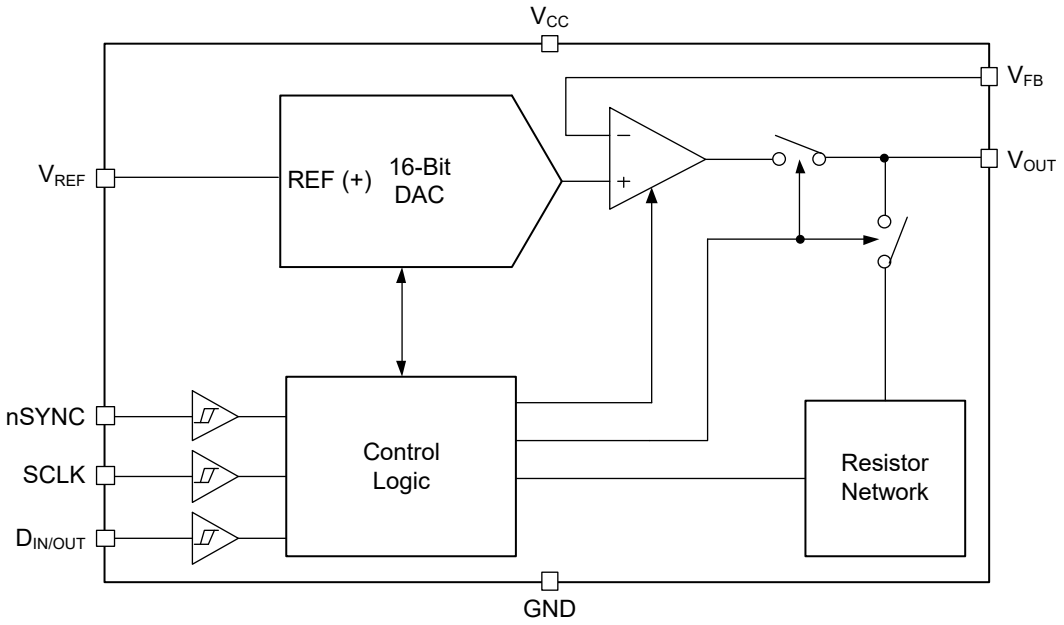


Figure 3. Block Diagram

DETAILED DESCRIPTION

DAC Section

The SGM5351-16 is a resistor string DAC followed by an output buffer amplifier. The input code to the SGM5351-16 is straight binary, so the ideal output voltage can be calculated based on the following equation:

$$V_{OUT} = \frac{D_{IN}}{65536} \times V_{REF} \quad (1)$$

Where:

D_{IN} = Equal decimal code that is loaded to the DAC register, it's from 0 to 65535.

Serial Interface

The 3-wire serial interface (nSYNC, SCLK, and $D_{IN/OUT}$) is compatible with SPI interface standard. The SGM5351-16 supports 3-wire SPI read and write operation. See Figure 1 for an example of a write sequence, and see Figure 2 for an example of a read sequence.

Input Shift Register

The input shift register is 24 bits wide, as shown in Figure 4. The first 5 bits are unused bits. DB[18] is a write or read selection bit. These bits are transferred to the DAC register on the 24th falling edge of SCLK.

nSYNC Interrupt

In a normal write/read sequence, the nSYNC line must be kept low for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if nSYNC goes high before the 24th falling edge, this write/read operation is invalid and ignored. An example is shown in Figure 5.

Power-On Reset

The SGM5351-16 has a power-on reset circuit, which can control the output voltage during power-up. On power-up, the DAC output voltages are 0V.

Power-Down Modes

The SGM5351-16 supports four separate modes of operation. The detailed operating mode is shown in Table 1.

Table 1. Operating Modes

PD1 (DB[17])	PD0 (DB[16])	Operating Mode
Normal Mode		
0	0	Normal operation
Power-Down Modes		
0	1	Output typically 1kΩ to GND
1	0	Output typically 100kΩ to GND
1	1	Hi-Z

Bit Number	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write Data (1)	Unused					0	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Read Data (1)	Unused					1	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

NOTE:

1. When in write data mode, DB[18] = 0, DB[17:0] are the data to be written to DAC; when in read data mode, DB[18] = 1, DB[17:0] are the data to be read out from DAC.

Figure 4. Data Input Register Format

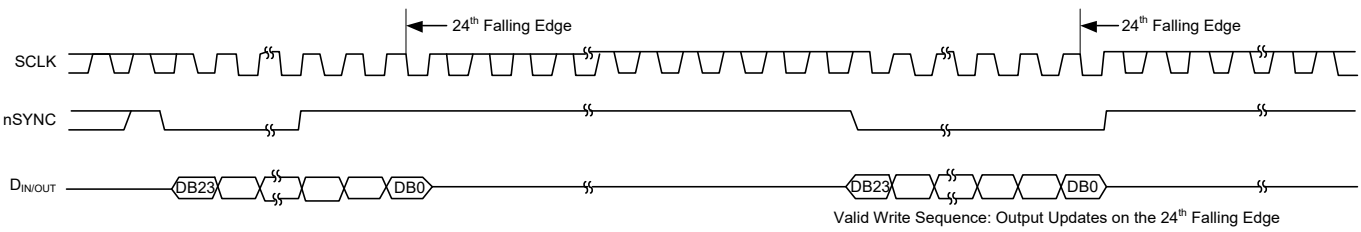


Figure 5. nSYNC Interrupt Facility

REVISION HISTORY

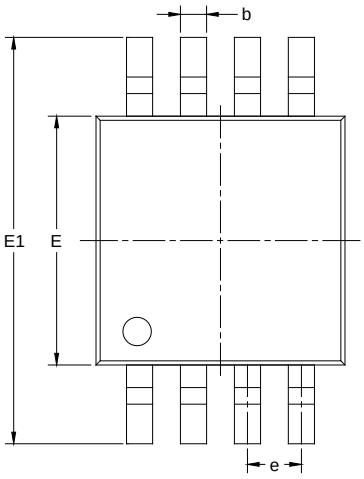
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

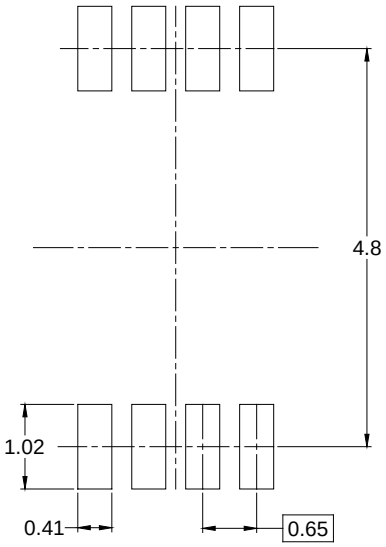
JANUARY 2022 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	4

Changes from Original (DECEMBER 2021) to REV.A	Page
Changed from product preview to production data	All

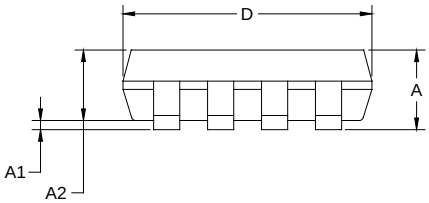
PACKAGE OUTLINE DIMENSIONS

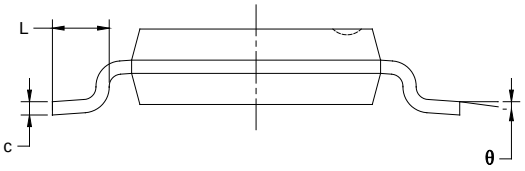
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)



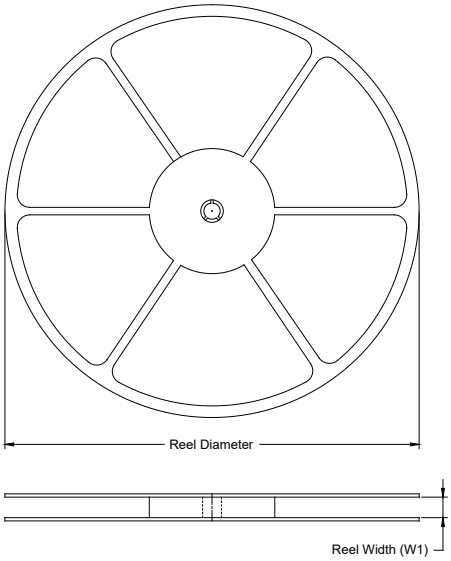


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

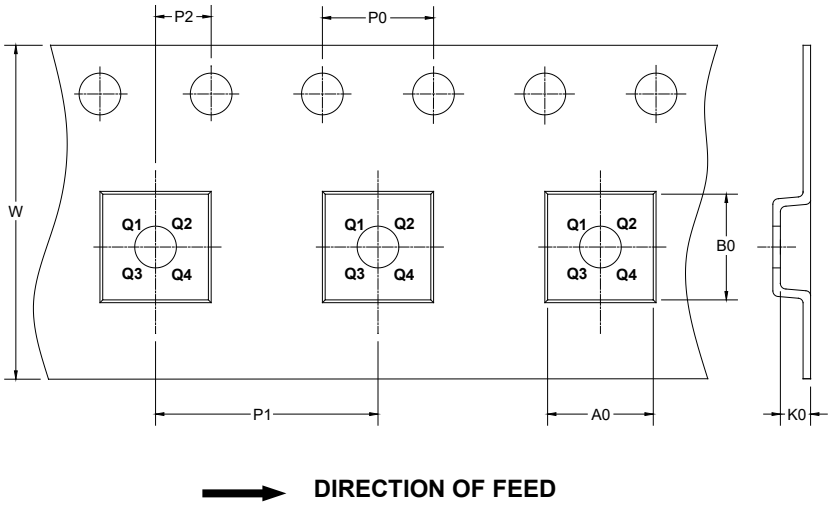
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

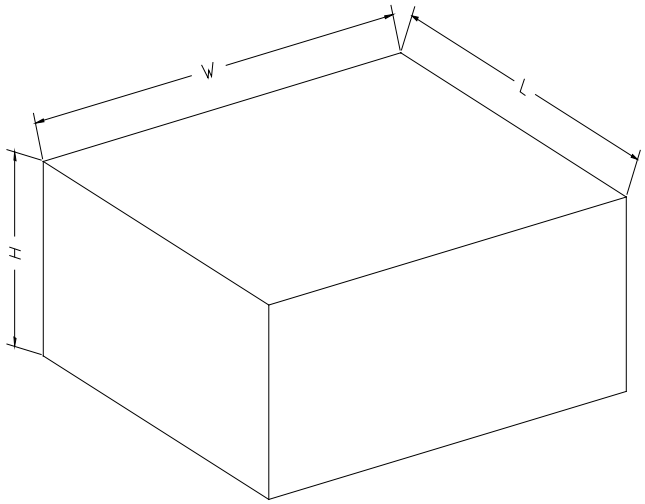
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-8	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002