SGM61020
2A High Efficiency Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61020 is a high efficiency synchronous Buck DC/DC converter with 2A output current capability and adjustable output voltage. The input supply voltage is in the range of 2.5V to 5.5V. Using adaptive off-time peak current control, the efficiency of this device is higher than 80% for loads over 1mA and reaches 95% in the moderate load ranges (5V to 3.3V).

This device operates with a quasi-fixed 1.5MHz pulse width modulation (PWM) mode for moderate or heavy loads. But at light loads, pulse skip modulation is used for power-save mode (PSM). The PSM operating quiescent current is very low, typically 42μA, which is well suitable for battery powered applications to increase standby time. Despite such low quiescent current, the transient response to large load variations is excellent. The device shutdown current is typically 0.02μA.

The SGM61020 provides an adjustable output voltage by an external resistor divider. The device is capable for low dropout operation with 100% duty cycle. Some other features include internal soft-start for limiting startup inrush current, over-current and thermal shutdown protections, enable input and power good output (for P version only).

The SGM61020 is available in Green SOT-23-5 and SOT-563-6 packages and can operate in the -40℃ to +125℃ ambient temperature range.

FEATURES

- **2.5V to 5.5V Input Voltage Range**
- **Adjustable Output Voltage from 0.6V to V_{IN}**
- **Up to 95% Efficiency**
- **Low R_{DSON} Switches (102mΩ/57mΩ)**
- **Power-Save Mode for Light Load Efficiency**
- **42μA (TYP) Operating Quiescent Current**
- **100% Duty Cycle for Low Dropout Operation**
- **1.5MHz PWM Switching Frequency**
- **Power Good Output (SGM61020P Only)**
- **Over-Current Protection**
- **Thermal Shutdown Protection**
- **Input Under-Voltage Lockout (UVLO) Protection**
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM61020: Available in Green SOT-23-5 and SOT-563-6 Packages
  SGM61020P: Available in a Green SOT-563-6 Package

APPLICATIONS

Battery-Powered Applications
Point-of-Load
Processor Power Supplies
Hard Disk Drives (HDD)/Solid State Drives (SSD)

TYPICAL APPLICATION

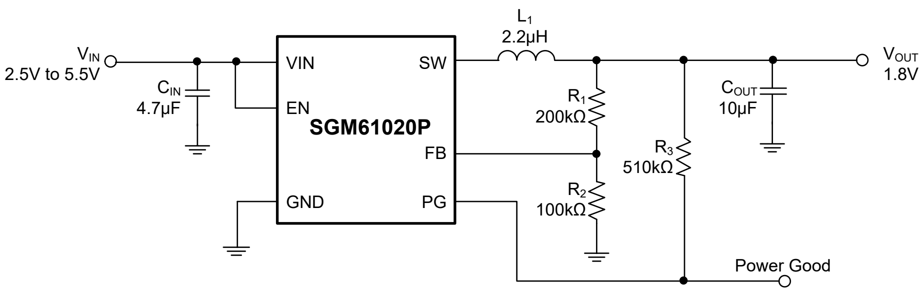


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61020	SOT-23-5	-40℃ to +125℃	SGM61020XN5G/TR	RAAXX	Tape and Reel, 3000
	SOT-563-6	-40℃ to +125℃	SGM61020XKB6G/TR	ZMXX	Tape and Reel, 5000
SGM61020P	SOT-563-6	-40℃ to +125℃	SGM61020PXKB6G/TR	ZNXX	Tape and Reel, 5000

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

MARKING INFORMATION

SOT-23-5

(1) XX = Date Code.

YYY X X

- X — Date Code - Week
- X — Date Code - Year
- YYY — Serial Number

SOT-563-6

(2) XX = Date Code.

YY X X

- X — Date Code - Week
- X — Date Code - Year
- YY — Serial Number

ABSOLUTE MAXIMUM RATINGS

Voltage Range [(1)]

VIN, EN, PG.. -0.3V to 6V

SW (DC) ....-0.3V to V_{IN} + 0.3V

SW (AC, less than 10ns) [(2)]..................................... -2V to 9V

FB .... -0.3V to 5.5V

Package Thermal Resistance

SOT-23-5, θ_{JA} .... 193℃/W

SOT-563-6, θ_{JA} .... 170℃/W

Junction Temperature ....+150℃

Storage Temperature Range........................-65℃ to +150℃

Lead Temperature (Soldering, 10s) ....+260℃

NOTES:
1. All voltage values are with respect to the ground terminal.
2. While switching.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN}.....................................2.5V to 5.5V

Output Voltage Range, V_{OUT} .... 0.6V to V_{IN}

Output Current Range, I_{OUT} ....0 to 2A

Sink Current at PG Pin, I_{SINK_PG} .... 1mA (MAX)

Operating Junction Temperature Range...... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

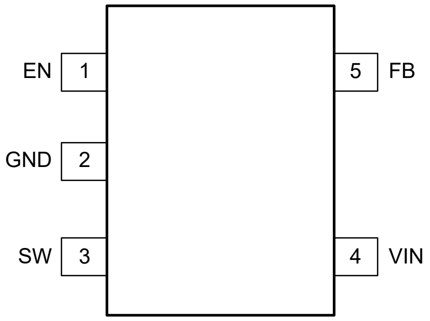
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

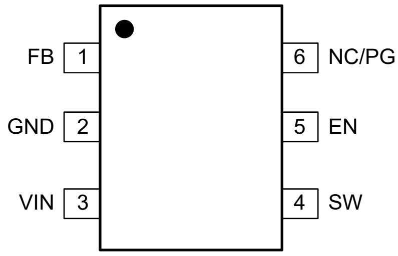
PIN CONFIGURATIONS

SGM61020 (TOP VIEW)



SOT-23-5

SGM61020/SGM61020P (TOP VIEW)



SOT-563-6

PIN DESCRIPTION

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th rowspan="2">I/O</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>SOT-23-5</th><th>SOT-563-6</th></tr>
<tr><td>1</td><td>5</td><td>EN</td><td>I</td><td>Active High Enable Input. Apply a logic low to shut down the device or pull EN up to VIN to enable it. Do not leave EN floating.</td></tr>
<tr><td>2</td><td>2</td><td>GND</td><td>G</td><td>Ground Pin.</td></tr>
<tr><td>3</td><td>4</td><td>SW</td><td>O</td><td>Switching Node Output Pin. Connect to the filter inductor.</td></tr>
<tr><td>4</td><td>3</td><td>VIN</td><td>P</td><td>Power Supply Input. Decouple VIN with at least 4.7μF ceramic capacitor to GND, close to the device. (If the input voltage oscillates, the input capacitance can be increased.)</td></tr>
<tr><td>5</td><td>1</td><td>FB</td><td>I</td><td>Feedback Input. Use a resistor divider to feedback the output voltage to this pin and set the voltage.</td></tr>
<tr><td rowspan="2">—</td><td rowspan="2">6</td><td>NC</td><td>—</td><td>No Connection. This pin can be left open or connected to GND.</td></tr>
<tr><td>PG</td><td>O</td><td>Open-Drain Power Good Output Pin (SGM61020P Only). Pull it up with a resistor to a positive voltage no more than 5.5V. It can be left open if unused.</td></tr>
</table>

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

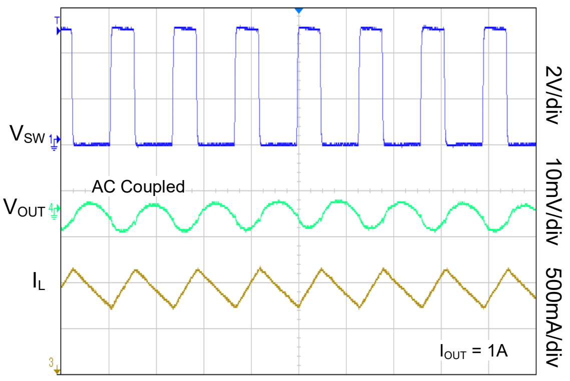
(V_{IN} = 5.0V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Quiescent Current into VIN Pin	I_Q	Not switching		42		μA
Shutdown Current into VIN Pin	I_{SD}	EN = 0V		0.02		μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling		2.3		V
Under-Voltage Lockout Hysteresis	V_{HYS}			100		mV
Thermal Shutdown	T_{JSD}	Junction temperature rising		150		℃
		Junction temperature falling		130		
Logic Interface						
High-Level Threshold at EN Pin	V_{IH}	2.5V ≤ V_{IN} ≤ 5.5V		0.98		V
Low-Level Threshold at EN Pin	V_{IL}	2.5V ≤ V_{IN} ≤ 5.5V		0.85		V
Soft Startup Time	t_{SS}	SGM61020 SOT-23-5 package		800		μs
		SGM61020/P SOT-563-6 package		800		
Output						
Feedback Regulation Voltage	V_{FB}			0.6		V
High-side FET On-Resistance	R_{DSON}	SOT-23-5 package		102		mΩ
		SOT-563-6 package		78		
Low-side FET On-Resistance		SOT-23-5 package		57		mΩ
		SOT-563-6 package		41		
High-side FET Current Limit	I_{LIM}	SGM61020 SOT-23-5 package		3.2		A
		SGM61020/P SOT-563-6 package		3.2		
Switching Frequency	f_{SW}	V_{OUT} = 2.5V		1.5		MHz
SGM61020P Only						
Power Good Threshold	V_{PG}	V_{FB} rising, referenced to V_{FB} nominal		95% × V_{REF}		V
		V_{FB} falling, referenced to V_{FB} nominal		90% × V_{REF}		
Power Good Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA		0.1		V
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V		0.01		μA
Power Good Delay Time	t_{PG_DLY}	V_{FB} falling		43		μs

TYPICAL PERFORMANCE CHARACTERISTICS

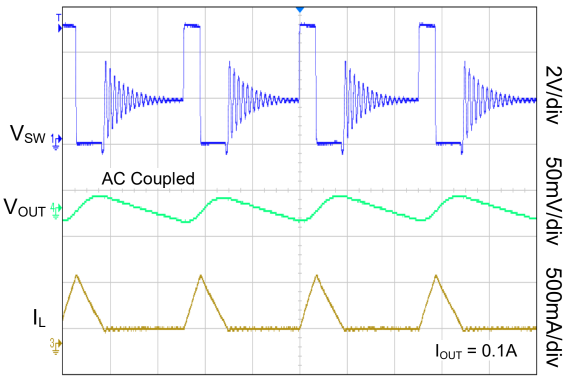
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, C_{OUT} = 10μF, unless otherwise noted.

PWM Operation



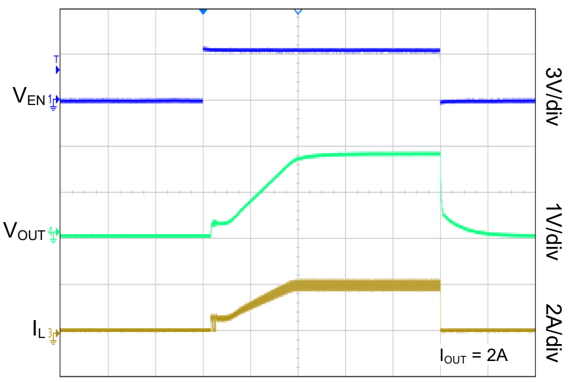
Time (500ns/div)

Power-Save Mode Operation



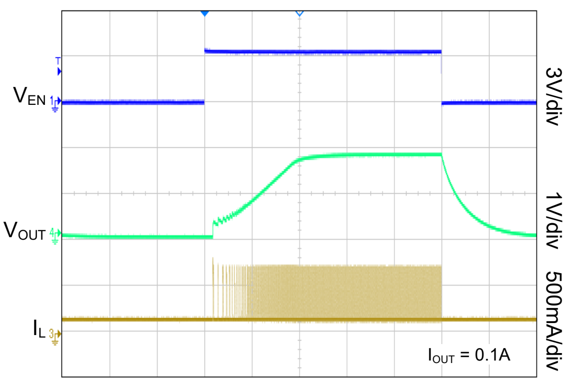
Time (1μs/div)

Startup and Shutdown with Load



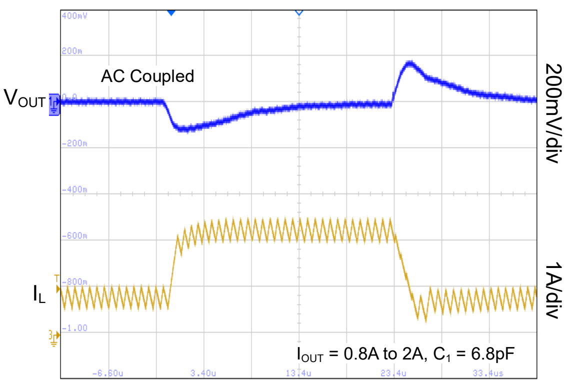
Time (500μs/div)

Startup and Shutdown with Load



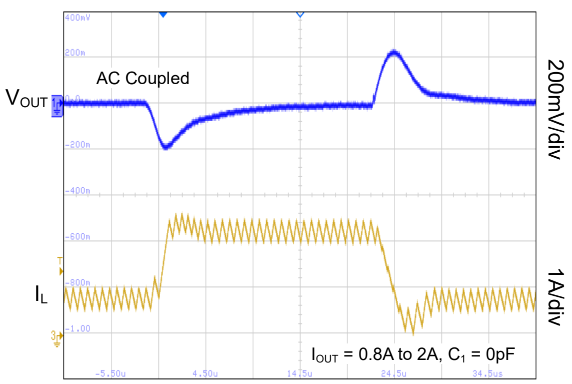
Time (500μs/div)

Load Transient



Time (5μs/div)

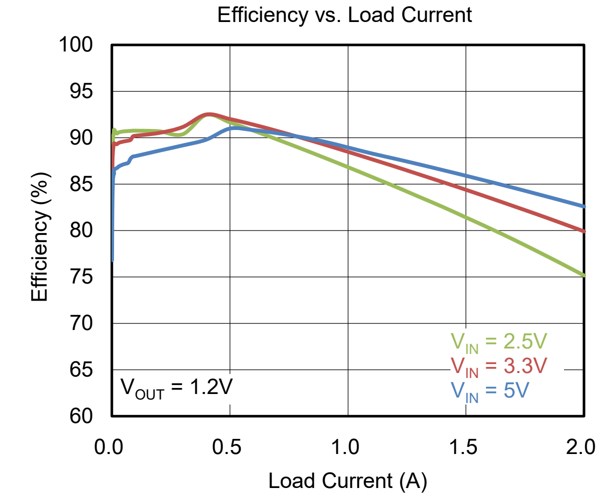
Load Transient

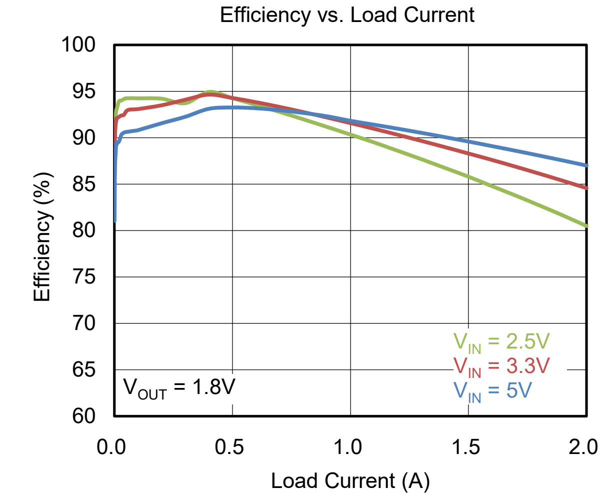


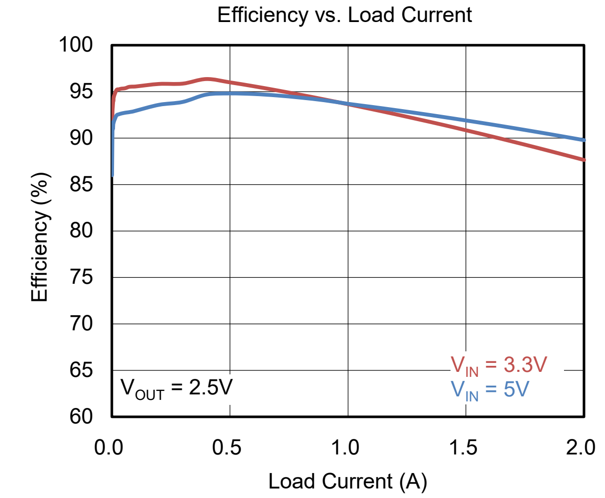
Time (5μs/div)

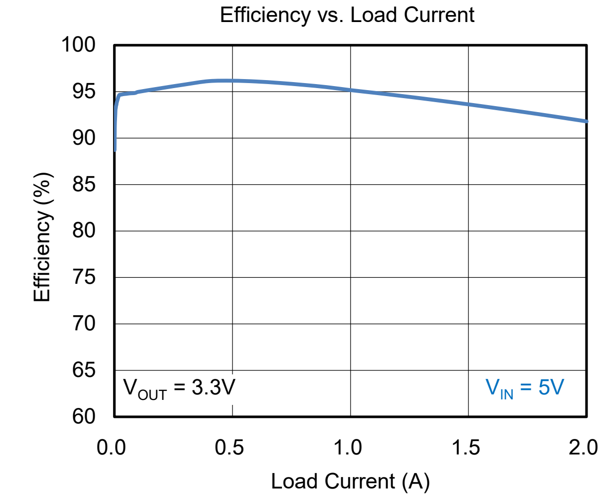
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

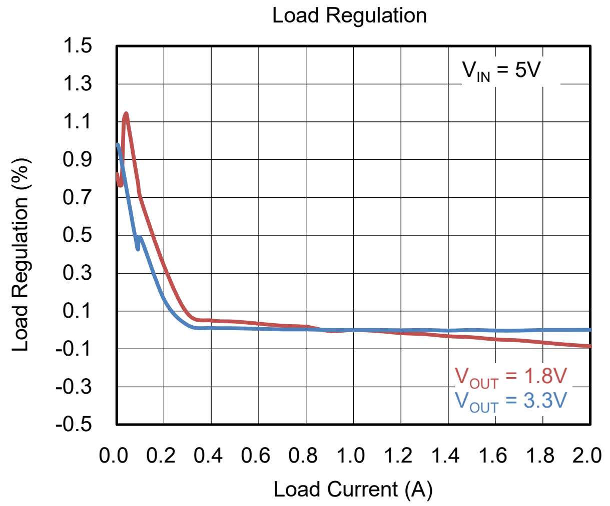
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, DCR = 18mΩ, unless otherwise noted.

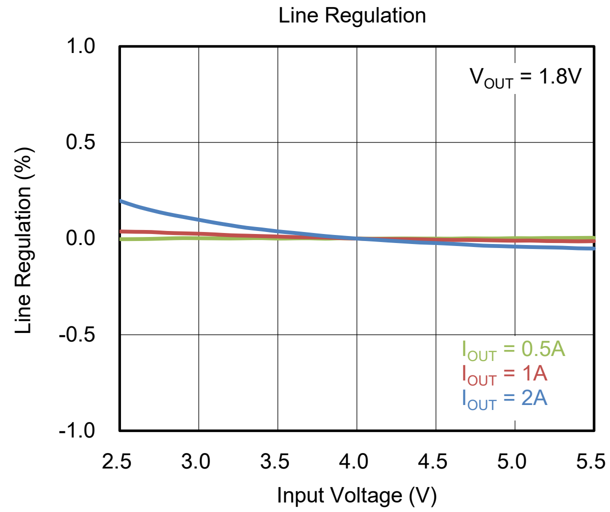






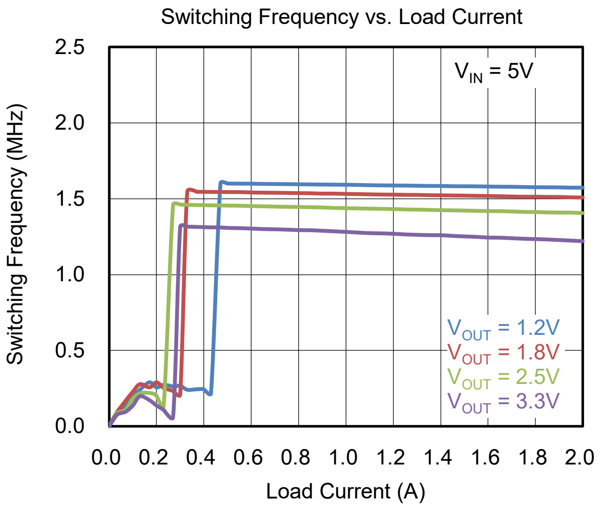


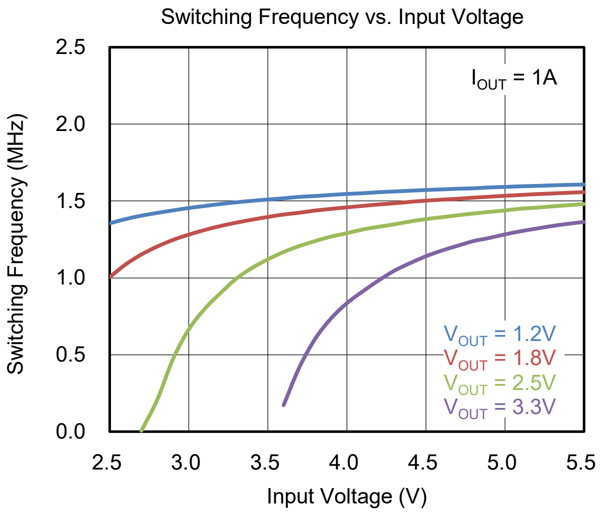




TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, DCR = 18mΩ, unless otherwise noted.





FUNCTIONAL BLOCK DIAGRAM

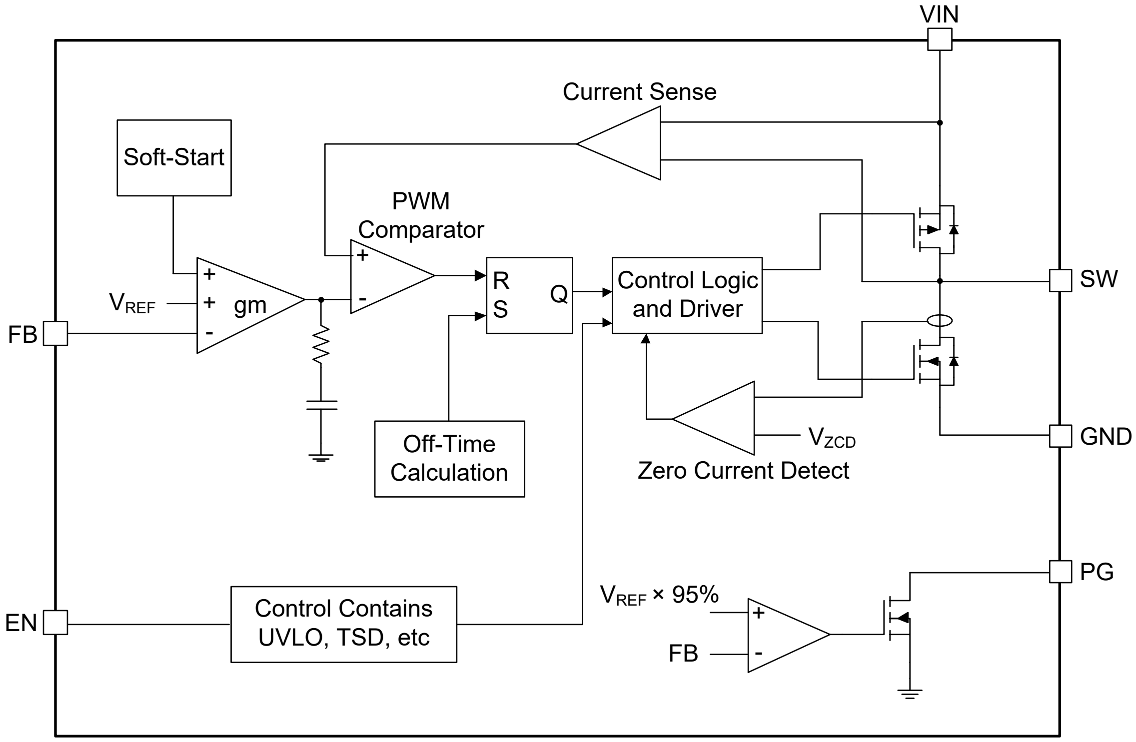


Figure 2. SGM61020/SGM61020P Block Diagram

DETAILED DESCRIPTION

The SGM61020 is a high efficiency Buck switching regulator optimized for handheld battery-powered applications. It operates at a quasi-fixed frequency of 1.5MHz and uses adaptive off-time PWM control for the moderate to heavy load range. This allows using a small inductor and small capacitors for compact designs. At light load condition, this device operates in power-save mode to reduce the switching frequency and losses for longer battery life. The power-save mode quiescent current is 42μA (TYP) while the shutdown current is only 0.02μA (TYP).

Under-Voltage Lockout Protection

When the input voltage is below the UVLO threshold (2.3V, TYP), the device is shut down. If the input voltage rises above the UVLO threshold plus hysteresis, the IC will restart.

Enable Input

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn it off. Connect the EN pin directly to a voltage source that can't be higher than the VIN pin. The EN input should not be left floating.

Power Good Output (SGM61020P Only)

The PG pin is an open-drain output. PG requires a pull-up resistor (e.g. 510kΩ). PG pin is pulled to GND before the output voltage is above 95% of the nominal voltage. After FB voltage reaches 95% of V_{REF}, the PG pin is pulled high immediately. When the FB voltage drops below 90% of V_{REF}, the PG pin will be pulled low after a 43μs delay. Leave the PG pin unconnected when not used.

Table 1. PG Output Logic

Device Conditions		Logic Status	
		High Z	Low
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_A > T_{JSD}$		√
UVLO	$1.4V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 1.4V$	√	

DETAILED DESCRIPTION (continued)

Soft Startup

An 800μs internal soft-start circuit is included to prevent input inrush current and voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage (V_{REF} = 0.6V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61020 is also capable of starting with a pre-biased output capacitor when it is powering up or enabled. When the device is turning on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device may not be able to startup properly. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value.

Power-Save Mode (PSM)

At light load condition, the SGM61020 shifts to the PSM mode and operates with pulse skip modulation to reduce the switching frequency and minimize the losses. It also shuts down most of the internal circuits in PSM. In this mode, one or more PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal again and the switches will turn off. In power-save mode, the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Low Dropout Operation (100% Duty Cycle)

When the input voltage reduces, the on-time increases. When the input voltage is lower than the regulation output voltage, the output voltage drops, and the SGM61020 goes into 100% duty cycle mode. The high-side switch is always on, and the output voltage is determined by the load current times the R_{DSON} composed by the high-side switch and inductor.

Current Limit Protection

Limiting the switch current protects the switch itself and also prevents over-current in the source and the inductor. If the high-side (HS) switch current exceeds the I_{LIM} threshold, HS switch is turned off and the low-side (LS) switch will be turned on to reduce the inductor current and limit the peak.

Note that the measured peak current limit in the closed-loop and open-loop (I_{LIM_OL}) test conditions is slightly different, mainly due to the current comparator propagation delay.

Thermal Shutdown Protection

A thermal shutdown function is implemented to prevent damage caused by excessive heat and power dissipation. Once the junction temperature exceeds +150°C, the device is shut down. The device is released from shutdown automatically when the junction temperature decreases by 20℃.

APPLICATION INFORMATION

In this section, power supply design with the SGM61020 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

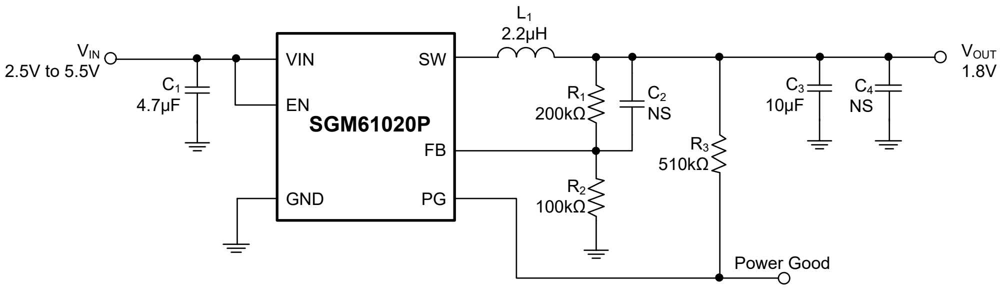


Figure 3. SGM61020P Application Example with 1.8V/2.0A Output

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	2.5V to 5.5V
Output Voltage	1.8V
Output Current	≤ 2A
Output Ripple Voltage	< 30mV

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1	4.7µF, 10V, X7R, 0805, Ceramic P/N: GRM21BR71A475ME51L	Murata
C_2, C_4	NS	Standard
C_3	10µF, 10V, X5R, 0805, Ceramic P/N: GRM21BR71A106ME51L	Murata
L_1	2.2µH Wire Wound, DCR_{MAX} = 39mΩ, $I_{SAT(30\%)}$ = 4.9A, $I_{RMS(40℃)}$ = 3A, 4mm × 4mm × 3mm, P/N: SWPA4030S2R2NT	Sunlord
R_1	Value Depends on V_{OUT}, 200kΩ, 1%, 0603, 1/16W Chip Resistor	Standard
R_2	100kΩ, 1%, 0603, 1/16W Chip Resistor	Standard
R_3	510kΩ, 5%, 0603, 1/16W Chip Resistor	Standard

Input Capacitor Selection (C_{IN})

High frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 4.7µF ceramic capacitor with X5R or better dielectric and 0805 or smaller size is sufficient in most cases. A larger value can be selected to reduce the input current ripple.

Inductor Selection (L)

The important factors for inductor selection are inductance (L), saturation current (I_{SAT}), RMS rating (I_{RMS}), DC resistance (DCR) and dimensions. Use Equation 1 to find the inductor peak current (I_{L_MAX}) and peak-to-peak ripple current (ΔI_L) in static conditions:

$$I_{L\_MAX} = I_{O\_MAX} + \frac{\Delta I_L}{2}$$
$$\Delta I_L = V_{OUT} \times \frac{1-D}{L \times f_{SW}} \quad (1)$$

I_{O_MAX} is the maximum load current, D = V_{OUT}/V_{IN} represents duty cycle and f_{SW} is the switching frequency.

I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Typically, the saturation current above high-side current limit is enough, and a 10% to 30% ripple current is selected to calculate the inductance. Larger inductance values reduce the ripple current but lead to sluggish transient response.

Output Voltage Setting

Use Equation 3 to select the R_1/R_2 resistor divider to set the V_{OUT}. Select the R_2 value less than 180kΩ to compromise noise sensitivity and light load losses.

$$V_{OUT} = V_{FB} \times \left(1+\frac{R_1}{R_2}\right) = 0.6V \times \left(1+\frac{R_1}{R_2}\right) \quad (3)$$

APPLICATION INFORMATION (continued)

Output Capacitor Selection (C_{OUT})

This device is capable to operate with low ESR ceramic capacitors to get low voltage ripple and fast response. 10μF ~ 22μF × 2 capacitors with X7R or X5R dielectric type are recommended. Minimum capacitance of output ripple criteria can be calculated from Equation 2.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (2)$$

For output capacitor selection, transient response and loop stability should also be considered.To simplify customer's design process, the inductor and output capacitor combinations are recommended in Table 4.

Output Filter Design

Table 4 can be used to select the proper LC filter components for most design requirements. The inductor initial tolerance can be as high as -30% to +20% of the nominal value and proper current derating is usually required. Bias voltage may cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value.

L_1 = 2.2μH, C_{OUT} = 22μF are the recommended values for the typical application.

Table 4. Proper Output Capacitor and Inductor Combination

V_{OUT}	L_1	C_{OUT}
0.9V	1μH	22μF
	—	22μF × 2
	2.2μH	22μF
	—	22μF × 2
1.8V	1μH	10μF
	—	22μF
	—	22μF × 2
	2.2μH	10μF
	—	22μF
	—	22μF × 2
3.3V	2.2μH	10μF
	—	22μF
	—	22μF × 2

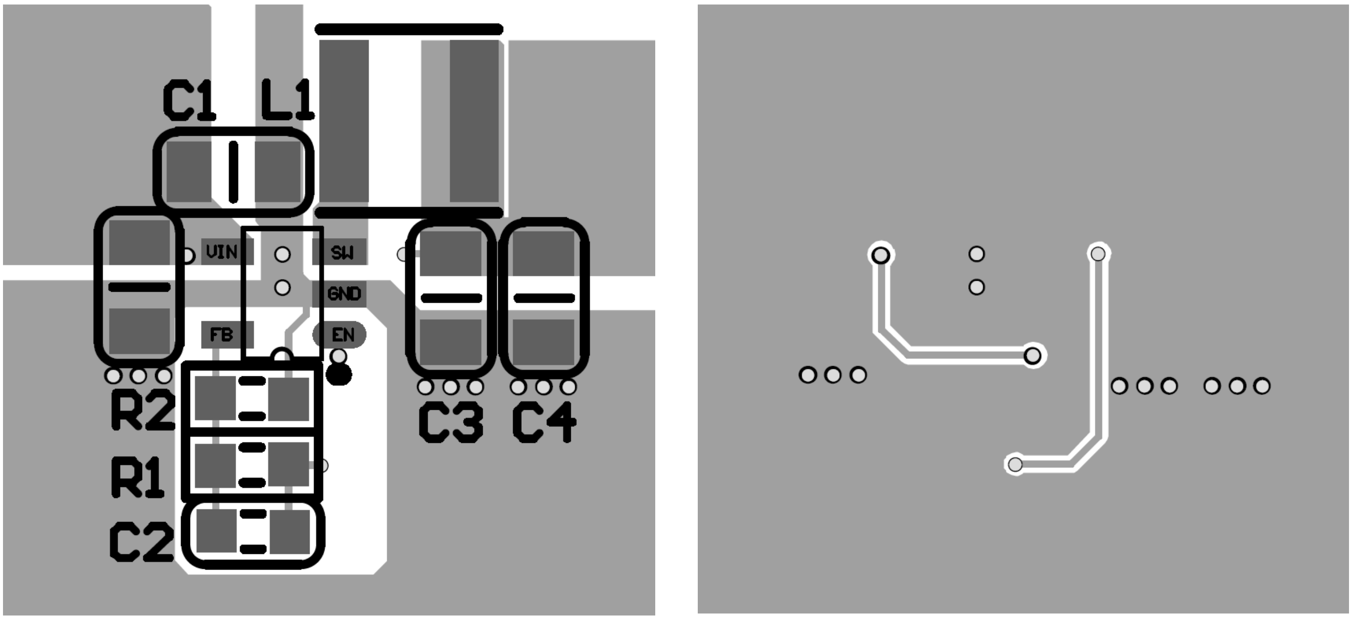
Layout Guidelines

A good printed-circuit-board (PCB) layout is a critical element of any high performance design. Follow the guidelines below for designing a good layout for the SGM61020.

- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device GND pin to minimize the AC current loops. Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep the signal traces like the FB sense line away from SW or other noisy sources.
- Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.

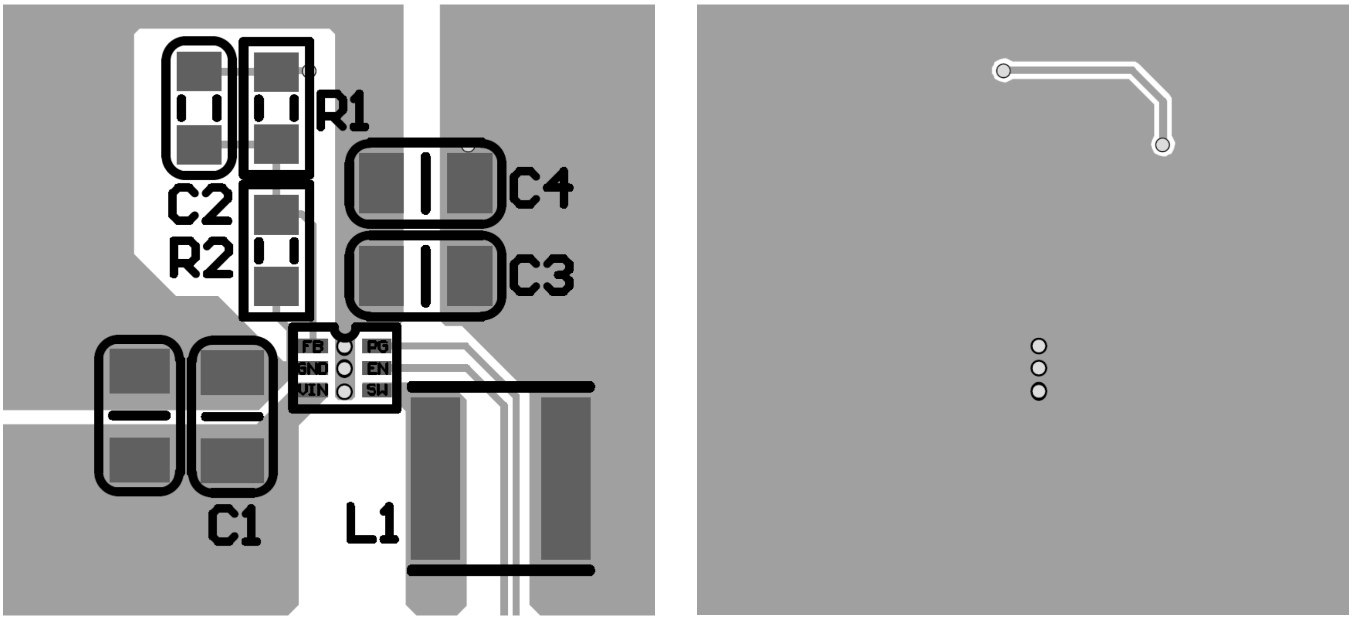
Refer to Figure 4 and Figure 5 for a recommended PCB layout.

APPLICATION INFORMATION (continued)



Top Layer **Bottom Layer**

Figure 4. SOT-23-5 PCB layout

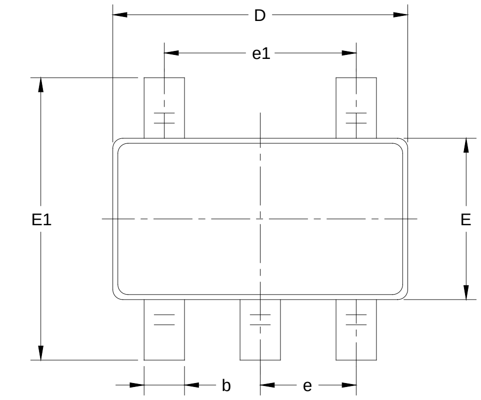


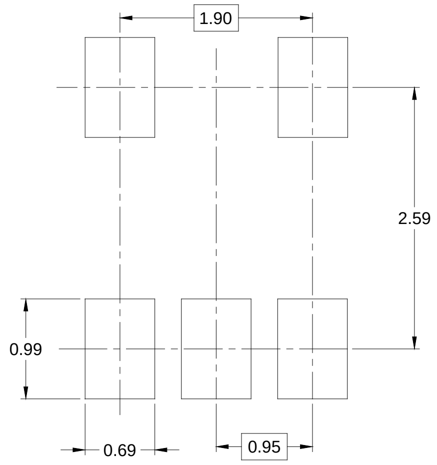
Top Layer **Bottom Layer**

Figure 5. SOT-563-6 PCB layout

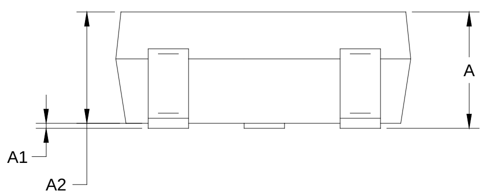
PACKAGE OUTLINE DIMENSIONS

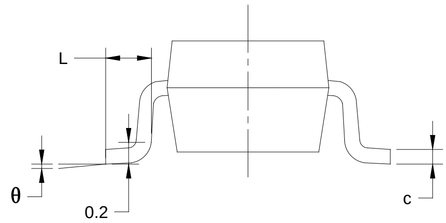
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



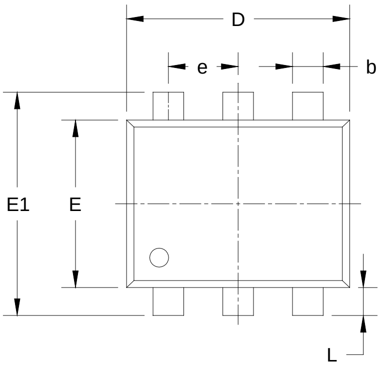


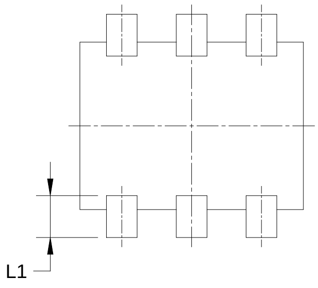
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

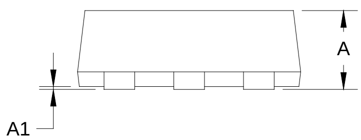
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

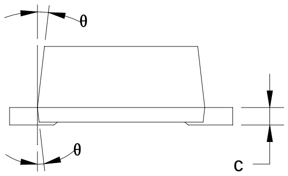
PACKAGE OUTLINE DIMENSIONS

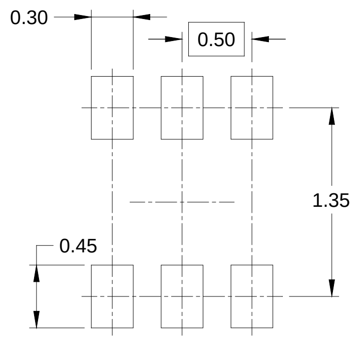
SOT-563-6











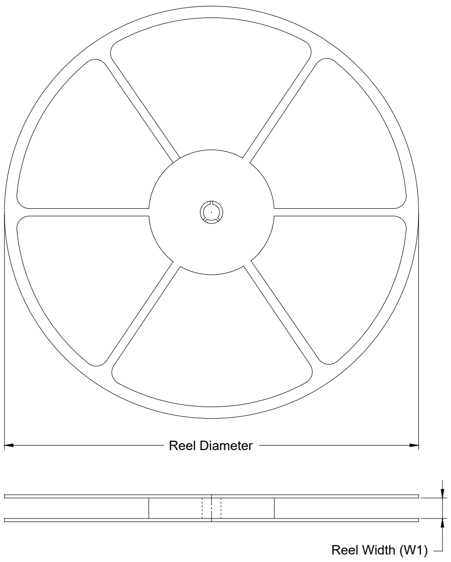
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	**MAX**	**MIN**	**MAX**
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.180	0.004	0.007
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
e	0.450	0.550	0.018	0.022
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016
θ	9° REF		9° REF	

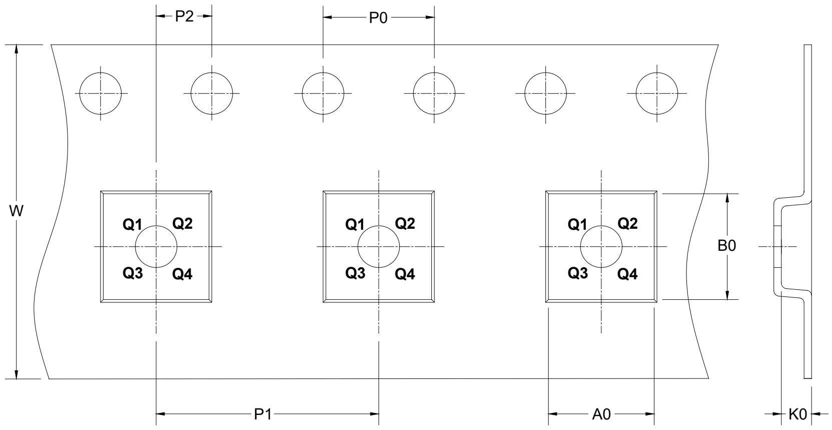
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

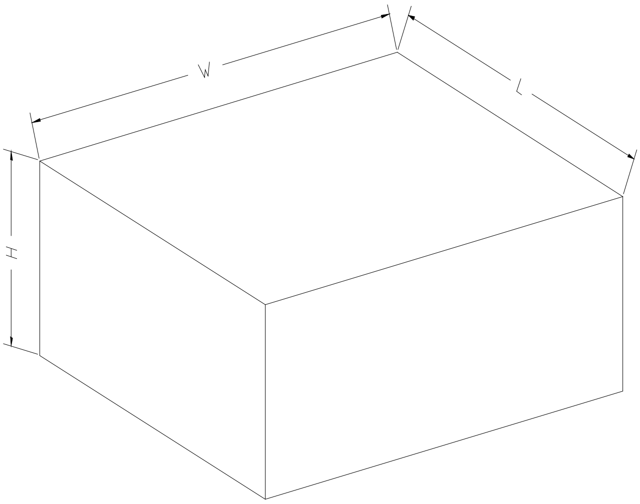
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOT-563-6	7″	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002