HD3SS6126 USB 3.0 和 USB 2.0 差分开关 2:1/1:2 多路复用/解复用器

1 特性

- 非常适合 USB 应用
  - 适用于 USB 3.0（超高速 USB 和 USB 2.0 HS/FS/LS）的信号开关
- 三个双向差分对通道多路复用/解复用开关还适用于 DisplayPort、PCIe Gen1/2/3、SATA 1.5/3/6G、AS 1.5/3/6G 和 XAUI 应用
- 高带宽路径 (SS) 最高支持 10Gbps 的数据速率
- V_{CC} 的工作范围为 3.3V ± 10%
- 高带宽路径 (SS) 上的 -3dB 差分带宽频率最高超过 10GHz
- 使用独特的适配方法在所支持的共模电压范围内保持恒定通道阻抗
- 出色的高带宽路径动态特性（2.5GHz 时）
  - 串扰 = -35dB
  - 隔音 = -23dB
  - 插入损耗 = −1.1dB
  - 回波损耗 = −11dB
- 3.5mm × 9mm、42 引脚小型晶圆级四方扁平无引线 (WQFN) 封装 (RUA)
- 激活模式功耗 = 8mW

2 应用

- 台式电脑
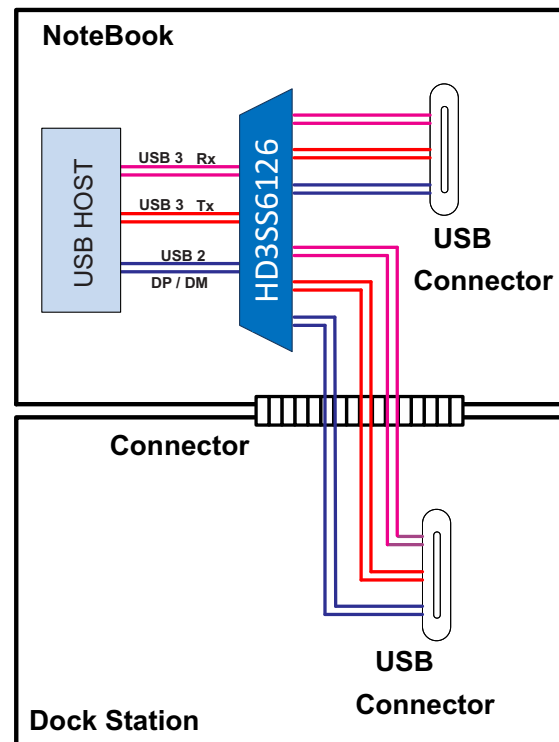- 笔记本电脑
- 平板电脑
- 扩展坞
- 电信
- 电视

3 说明

HD3SS6126 器件是一款针对 USB 应用而设计的高速无源开关，用于 将 SuperSpeed USB RX 和 TX 以及 USB 2.0 DP 和 DM 信号从源位置路由到目标位置，反之亦然。该器件还可用于 DisplayPort、PCI Express、™SATA、SAS 和 XAUI 应用。
HD3SS6126 器件可用于灌电流应用或拉电流 应用。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
HD3SS6126	WQFN (42)	9.00mm x 3.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图

English Data Sheet: SLAS975
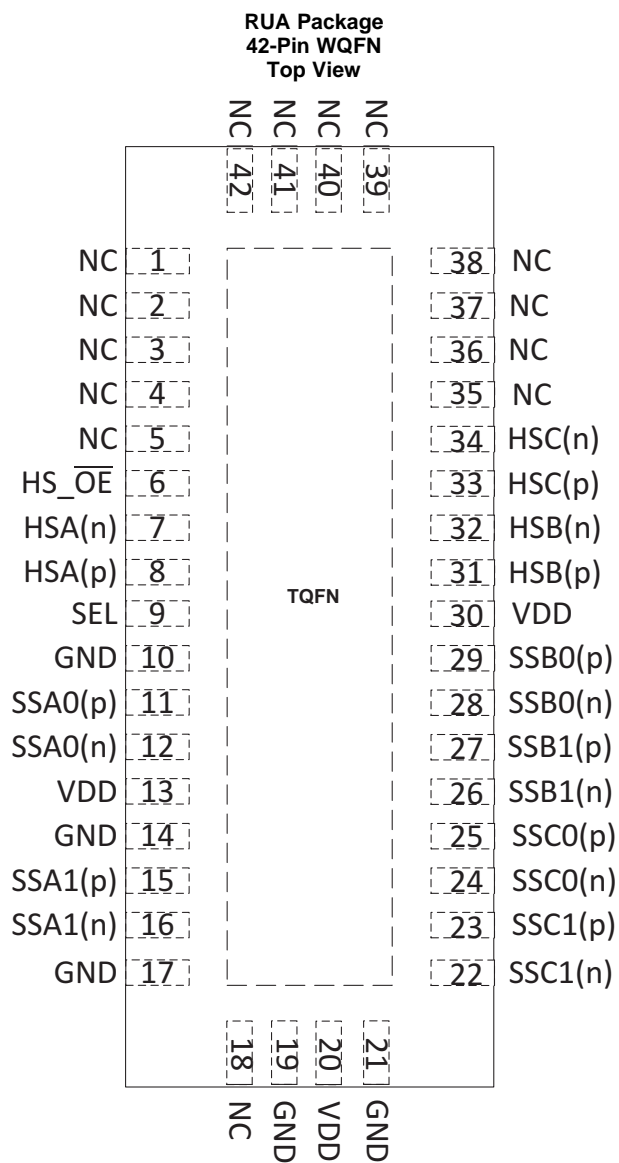
目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (November 2013) to Revision A **Page**

- 已添加 引脚配置和功能部分，*ESD* 额定值表，典型特性部分，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分 1

5 Pin Configuration and Functions

RUA Package
42-Pin WQFN
Top View

Pin	Name		Name	Pin
	NC	(42) (41) (40) (39) NC NC NC NC		
1	NC		NC	38
2	NC		NC	37
3	NC		NC	36
4	NC		NC	35
5	NC		HSC(n)	34
6	HS_$\overline{OE}$		HSC(p)	33
7	HSA(n)		HSB(n)	32
8	HSA(p)	TQFN	HSB(p)	31
9	SEL		VDD	30
10	GND		SSB0(p)	29
11	SSA0(p)		SSB0(n)	28
12	SSA0(n)		SSB1(p)	27
13	VDD		SSB1(n)	26
14	GND		SSC0(p)	25
15	SSA1(p)		SSC0(n)	24
16	SSA1(n)		SSC1(p)	23
17	GND		SSC1(n)	22
	NC GND VDD GND (18) (19) (20) (21)			

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	10, 14, 17, 19, 21	Supply	Ground
HSA(p)	8	I/O	Port A USB 2.0 positive signal
HSA(n)	7		Port A USB 2.0 negative signal
HSB(p)	31	I/O	Port B USB 2.0 positive signal
HSB(n)	32		Port B USB 2.0 negative signal
HSC(p)	33	I/O	Port C USB 2.0 positive signal
HSC(n)	34		Port C USB 2.0 negative signal
HS_$\overline{\text{OE}}$	6	I (Control)	Output Enable H = Power Down L = Normal Operation
NC	1, 2, 3, 4, 5, 18, 35, 36, 37, 38, 39, 40, 41, 42	—	Electrically No Connection
SEL	9	I (Control)	USB 3.0/2.0 Port Selection Control Pins
SSA0(p)	11	I/O	Port A, Channel 0, USB 3.0 Positive Signal
SSA0(n)	12		Port A, Channel 0, USB 3.0 Negative Signal
SSA1(p)	15	I/O	Port A, Channel 1, USB 3.0 Positive Signal
SSA1(n)	16		Port A, Channel 1, USB 3.0 Negative Signal
SSB0(p)	29	I/O	Port B, Channel 0, USB 3.0 Positive Signal
SSB0(n)	28		Port B, Channel 0, USB 3.0 Negative Signal
SSB1(p)	27	I/O	Port B, Channel 1, USB 3.0 Positive Signal
SSB1(n)	26		Port B, Channel 1, USB 3.0 Negative Signal
SSC0(p)	25	I/O	Port C, Channel 0, USB 3.0 Positive Signal
SSC0(n)	24		Port C, Channel 0, USB 3.0 Negative Signal
SSC1(p)	23	I/O	Port C, Channel 1, USB 3.0 Positive Signal
SSC1(n)	22		Port C, Channel 1, USB 3.0 Negative Signal
VDD	13, 20, 30	Supply	3.3-V power supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply Voltage, V_{DD}[2]		−0.3	4	V
Voltage	Differential I/O, High-bandwidth signal path: SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n)	−0.5	4	V
	Differential I/O, Low-bandwidth signal path: HSAp/n), HSB(p/n), HSC(p/n)	-0.5	7	
	Control pin and single ended I/O	−0.3	V_{DD} + 0.3	
Continuous power dissipation		See *Thermal Information*		
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C; all temperature limits are specified by design

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage	Control Pins	2.0		V_{DD}	V
V_{IL}	Input low voltage	Control Pins	−0.1		0.8	V
V_{I/O_Diff}	Differential voltage	Switch I/O differential voltage for High-bandwidth signal path only: SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n)	0		1.8	V_{p-p}
V_{I/O_CM}	Common voltage	Switch I/O common mode voltage for High-bandwidth signal path only: SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n)	0		2.0	V
T_A	Operating free-air temperature		0		70	°C

6.4 Thermal Information

THERMAL METRIC		HD3SS6126 RUA (WQFN) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter [1]	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter [1]	27.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report, SPRA953. Test conditions for Ψ_{JB} and Ψ_{JT} are clarified in the application report..

6.5 Electrical Characteristics – Device Parameters

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	V_{DD} = 3.6 V, SEL = V_{DD} /GND; $\overline{OE}$ = GND; Outputs Floating		2.4	3	mA
SEL						
I_{IH}	Input high current	V_{DD} = 3.6 V, V_{IN} = V_{DD}			95	µA
I_{IL}	Input high current	V_{DD} = 3.6 V, V_{IN} = GND			1	µA
HS_$\overline{OE}$						
I_{IH}	Input high current	V_{DD} = 3.6 V, V_{IN} = V_{DD}			1	µA
I_{IL}	Input high current	V_{DD} = 3.6 V, V_{IN} = GND			1	µA
SSA0/1, SSB0/1, SSC0/1						
I_{LK}	High-impedance leakage current	V_{DD} = 3.6 V, V_{IN} = 2 V, V_{OUT}= 2 V, (I_{LK} on open outputs Port B and C)			130	µA
		V_{DD} = 3.6 V, V_{IN} = 2 V, V_{OUT}= 2 V, (I_{LK} on open outputs Port A)			4	µA
HSA, HSB, HSC						
I_{LK}	High-impedance leakage current	V_{DD} = 3.6 V, V_{IN} = 0 V, V_{OUT}= 0 V to 4 V, HS_$\overline{OE}$_IN = GND			1	µA

6.6 Electrical Characteristics – Signal Switch Parameters

under recommended operating conditions; R_L, R_{SC} = 50 Ω, C_L = 10 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n) Signal Path						
C_{ON}	Outputs ON capacitance	V_{IN} = 0 V, outputs open, switch ON		1.5		pF
C_{OFF}	Outputs OFF capacitance	V_{IN} = 0 V, outputs open, switch OFF		1		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3 V, V_{CM} = 0 V – 2 V, I_O = –8 mA		5	8	Ω
ΔR_{ON}	ON resistance match between pairs of the same channel	V_{DD} = 3.3 V; 0 V ≤ V_{IN} ≤ 2 V; I_O = –8 mA			0.7	Ω
R_{FLAT_ON}	ON resistance flatness ($R_{ON(MAX)}$– $R_{ON(MIN)}$)	V_{DD} = 3.3 V; –0 V ≤ V_{IN} ≤ 2 V			1.15	Ω
R_L	Differential return loss (V_{CM} = 0 V)	f = 0.3 MHz		−25		dB
		f = 2.5 GHz		−11		
		f = 4 GHz		−11		
X_{TALK}	Differential crosstalk (V_{CM} = 0 V)	f = 0.3 MHz		-85		dB
		f = 2.5 GHz		−35		
		f = 4 GHz		−33		
O_{IRR}	Differential off-isolation (V_{CM} = 0 V)	f = 0.3 MHz		-85		dB
		f = 2.5 GHz		-23		
		f = 4 GHz		−21		
I_L	Differential insertion loss (V_{CM} = 0 V)	f = 0.3 MHz		−0.43		dB
		f = 2.5 GHz		−1.1		
		f = 4 GHz		−1.3		
BW	Bandwidth	At −3 dB		10		GHz
HSA(p/n), HSB(p/n), HSC(p/n) SIGNAL PATH						
C_{ON}	Outputs ON capacitance	V_{IN} = 0 V, Outputs Open, Switch ON		6	7.5	pF
C_{OFF}	Outputs OFF capacitance	V_{IN} = 0 V, Outputs Open, Switch OFF		3.5	6	pF
R_{ON}	Output ON resistance	V_{DD} = 3 V, V_{IN} = 0 V, I_O = 30 mA		3	6	Ω
		V_{DD} = 3 V, V_{IN} = 2.4 V, I_O = 30 mA		3.4	6	
ΔR_{ON}	ON resistance match between pairs of the same channel	V_{DD} = 3 V; V_{IN} = 0 V; I_O = 30 mA		0.2		Ω
		V_{DD} = 3 V; V_{IN} = 1.7 V; I_O = -15 mA		0.2		
R_{FLAT_ON}	ON resistance flatness ($R_{ON(MAX)}$– $R_{ON(MIN)}$)	V_{DD} = 3 V; V_{IN} = 0 V; I_O = 30 mA		1		Ω
		V_{DD} = 3 V; V_{IN} = 1.7 V; I_O = −15 mA		1		
X_{TALK}	Differential crosstalk (V_{CM} = 0 V)	R_L = 50 Ω, f = 250 MHz		−40		dB
O_{IRR}	Differential off-isolation (V_{CM} = 0 V)	R_L = 50 Ω, f = 250 MHz		−41		dB
BW	Bandwidth	R_L = 50 Ω		0.9		GHz

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

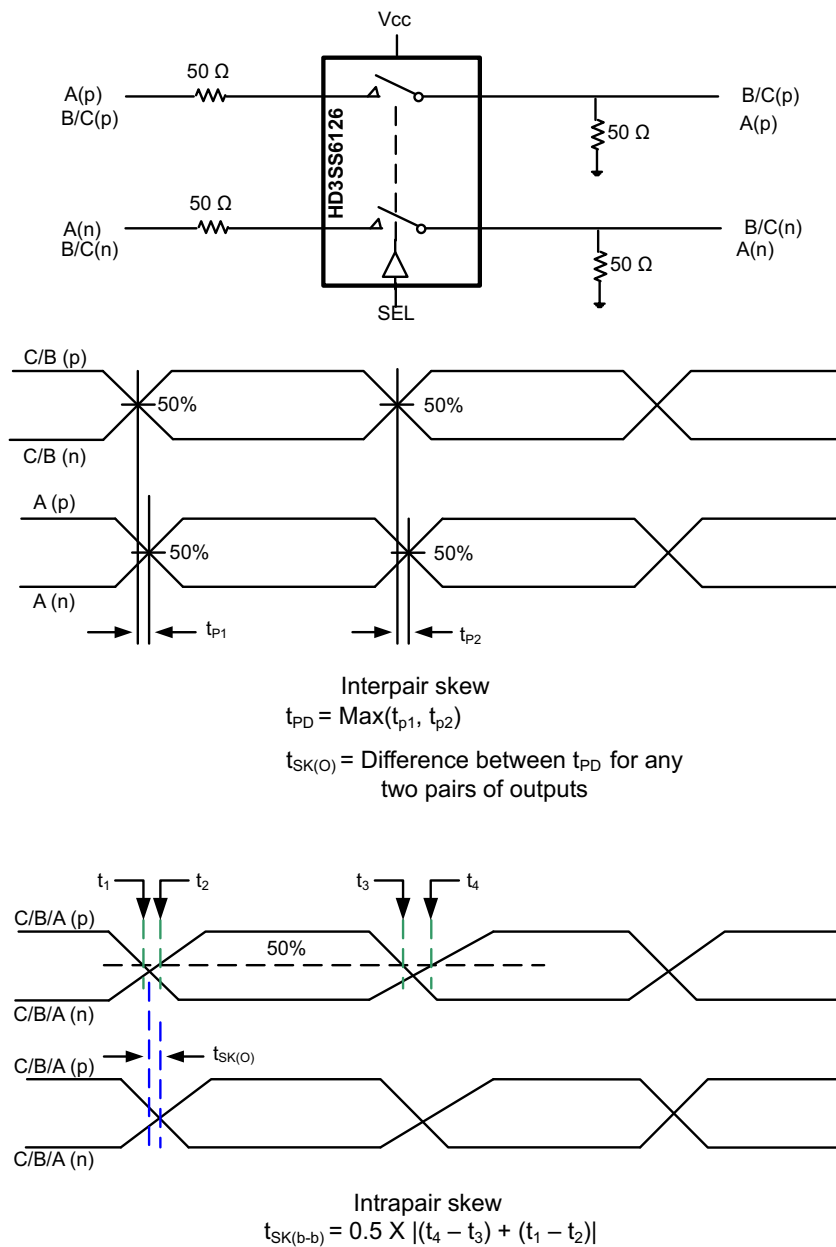| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n) Signal Path						
t_{on}	SEL-to-Switch t_{on}	R_{SC} and R_L = 50 Ω, See Figure 1		70	250	ns
t_{off}	SEL-to-Switch t_{off}	R_{SC} and R_L = 50 Ω, See Figure 1		70	250	ns
t_{PD}	Switch propagation delay	R_{SC} and R_L = 50 Ω, See Figure 3			85	ps
$t_{SK(O)}$	Interpair output skew (CH-CH)	R_{SC} and R_L = 50 Ω, See Figure 3			20	ps
$t_{SK(b-b)}$	Intrapair Output Skew (bit-bit)	R_{SC} and R_L = 50 Ω, See Figure 3			8	ps
HSA(p/n), HSB(p/n), HSC(p/n) SIGNAL PATH						
t_{ON}	SEL to Switch t_{ON}	See Figure 2			30	ns
	HS_$\overline{OE}$ to Switch t_{ON}	See Figure 2			17	
t_{OFF}	SEL to Switch t_{OFF}	See Figure 2			12	ns
	HS_$\overline{OE}$ to Switch t_{OFF}	See Figure 2			10	
t_{PD}[(1)]	Switch propagation delay	See Figure 3		250		ps
$t_{SK(O)}$[(1)]	Interpair output skew (CH-CH)			100	200	ps
$t_{SK(P)}$[(1)]	Intrapair Output Skew (bit-bit)			100	200	ps

(1) Specified by design
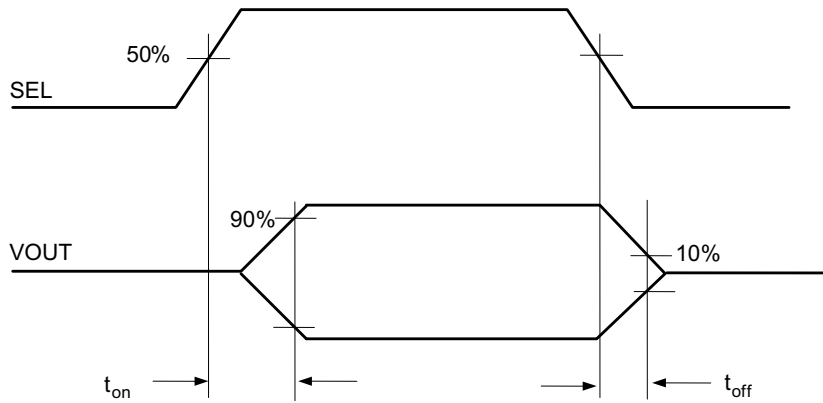
Figure 1. Select to Switch t_{ON} and t_{OFF}
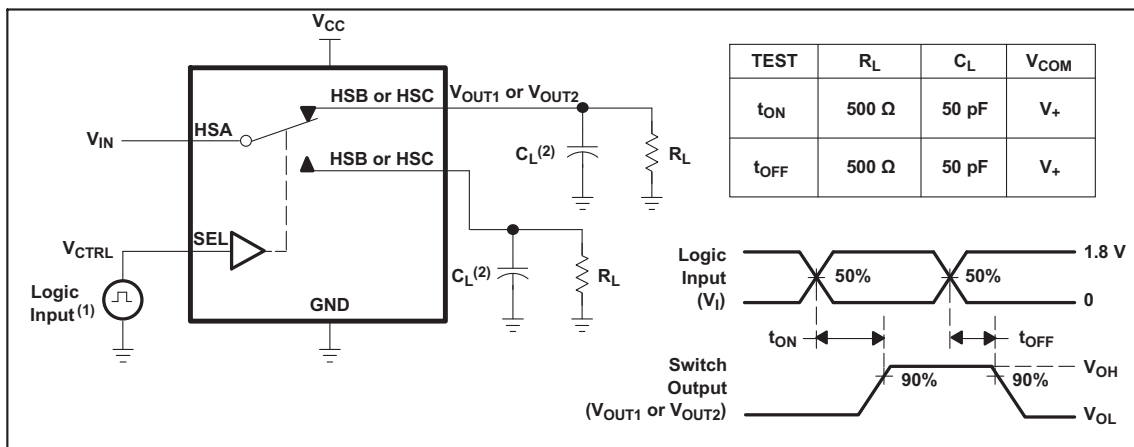
(1) All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHZ, Z_O = 50 Ω, t_r< 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 2. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

Interpair skew

$t_{PD} = Max(t_{p1}, t_{p2})$

$t_{SK(O)}$ = Difference between t_{PD} for any
two pairs of outputs

Intrapair skew

$t_{SK(b-b)} = 0.5 \times |(t_4 - t_3) + (t_1 - t_2)|$

NOTES:
1. Measurements based on an ideal input with zero intrapair skew on the input, i.e. the input at A to B/C or the input at B/C to A
2. Interpair skew is measured from lane to lane on the same channel, e.g. C0 to C1
3. Intrapair skew is defined as the relative difference from the p and n signals of a single lane

Figure 3. Propagation Delay and Skew

6.8 Typical Characteristics

Figure 4. Intrapair Skew SSA to SSB Port

**Figure 5. Intrapair Skew SSA to SSC Port**
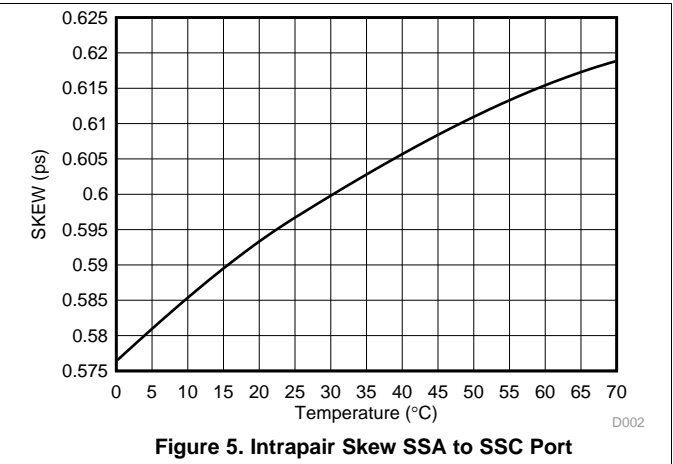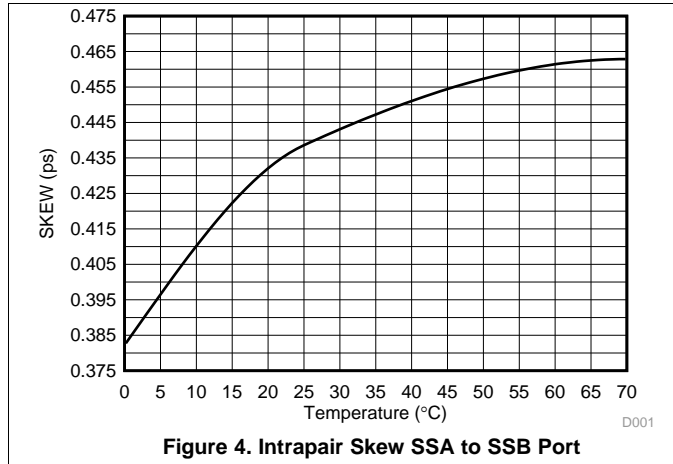
7   Detailed Description

7.1 Overview

The HD3SS6126 is a USB 3.0 and USB 2.0 differential switch, it is designed to support data rates up to 10 Gbps on high-bandwidth paths (SS), it is also suitable for DisplayPort, PCIe Gen1/2/3, SATA 1.5/3/6G, SAS 1.5/3/6G and XAUI applications. The device uses a unique adaptation method to maintain a constant channel impedance over the supported common-mode voltage range, resulting in an excellent high-bandwidth path dynamic characteristics (at 2.5 GHz; Crosstalk = –35 dB, Isolation = –23 dB, Insertion Loss = –1.1 dB, Return Loss = –11 dB).

7.2 Functional Block Diagram
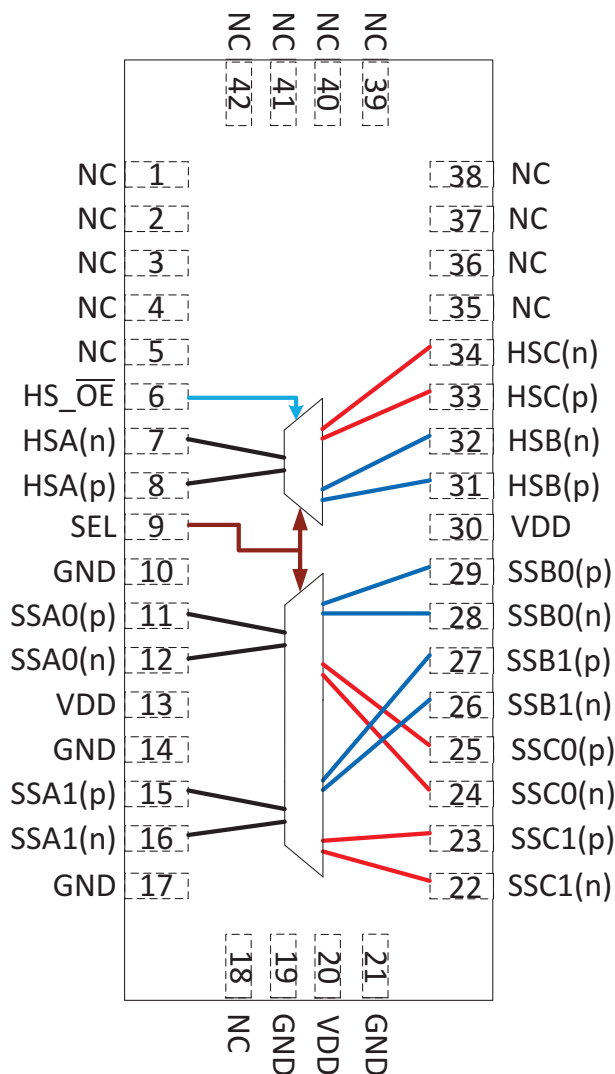
7.3 Feature Description

The HD3SS6126 can be powered by VBUS from the USB Host, and is capable of selecting USB2 independently from USB3. Although the main application of the HD3SS6126 is USB3.0/2.0, the device also supports common interfaces such as PCIe Gen1 and Gen2, DP and SATA/SAS applications. The device is able to support these additional interfaces because of its support of data rates up to 5.4 Gbps and common-mode voltages from 0 V to 2 V with a maximum signal swing of 1.8 V. All of these applications use an 8b or 10b coding technique to achieve DC balance and facilitate terminal equipment.

NOTE
The device may need AC capacitors and additional bias voltage to support the PCIe Gen1 and Gen2 interfaces.

7.4 Device Functional Modes

Table 1. Truth Table USB 3.0 SuperSpeed USB

SEL	USB 3.0 PORT SELECTION		
	SSA0/1	**SSB0/1**	**SSC0/1**
0	To/From SSB0/1	To/From SSA0/1	Off
1	To/From SSC0/1	Off	To/From SSA0/1

Table 2. Truth Table USB 2.0 High-Speed, Full-Speed, Low-Speed Path

HS_$\overline{OE}$	SEL	USB 2.0 Port Selection		
		HSA	**HSB**	**HSC**
0	0	To/From HSB	To/From HSA	Off
0	1	To/From HSC	Off	To/From HSA
1	X	Off	Off	Off

8 Application and Implementation

> **NOTE**
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A typical application for the HD3SS6126 is a USB 3.0 KVM switch, where one of two USB hosts system can be selected for an USB device. These guidelines are also suitable for PCIe(Gen1,Gen2), SATA, XAUI and DP, since the HD3SS6126 device is fully compatible with these protocols.
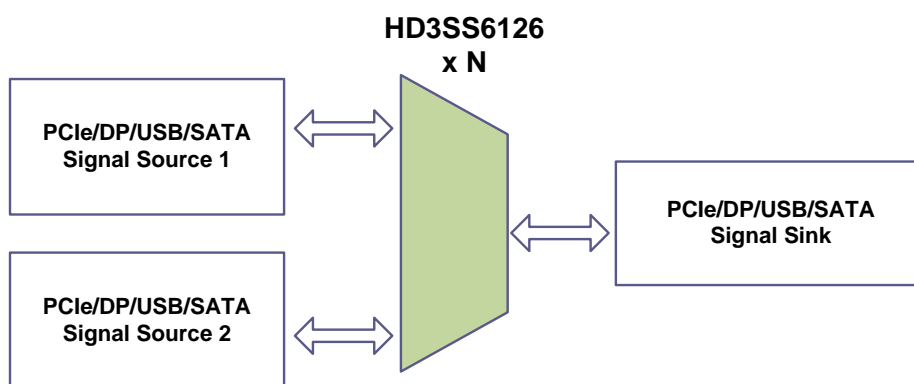
8.2 Typical Application

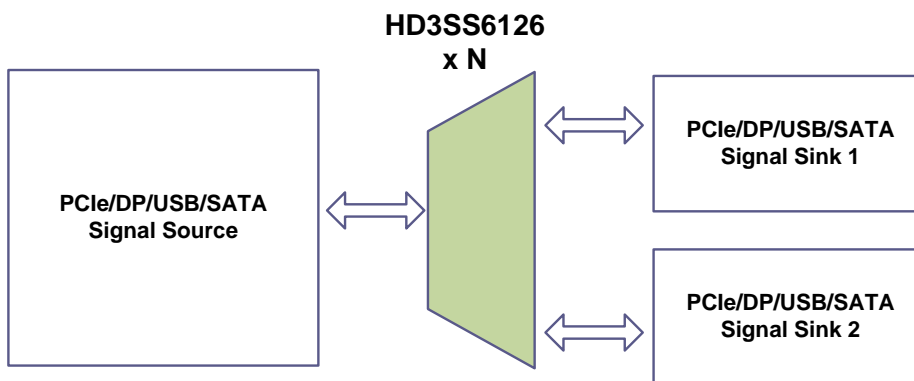**Figure 6. Two Signal Sources to One Destination**

Figure 7. One Signal Sources to Two Destination

Typical Application (continued)

8.2.1   Design Requirements

Power supply requirements:

- V_{DD} from 3 V to 3.6 V

Control pins requirements

- V_{IH} from 2 V to V_{DD}
- V_{IL} from –0.1 V to 0.8 V

Differential pairs requirements:

- V_{I/O_Diff} from 0 V to 1.8 Vp-p
- V_{I/O_CM} from 0 V to 2 V

T_A Operating free-air temperature from 0°C to 70°C

8.2.2   Detailed Design Procedure

8.2.2.1   Power Supply

The first step is to design the power supply and determine the V_{CC} stability and minimum current required (see *Power Supply Recommendations*).
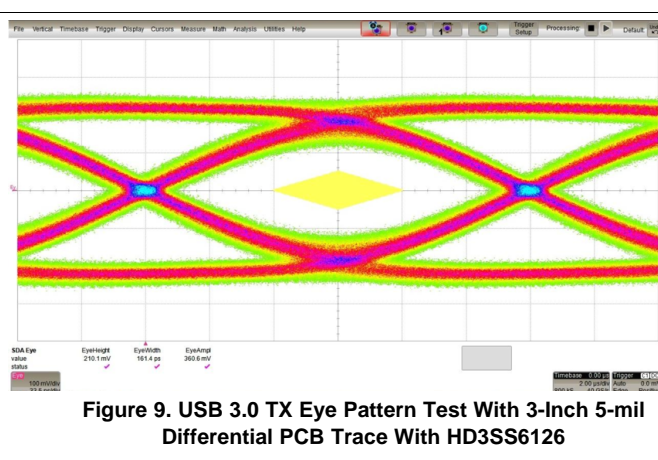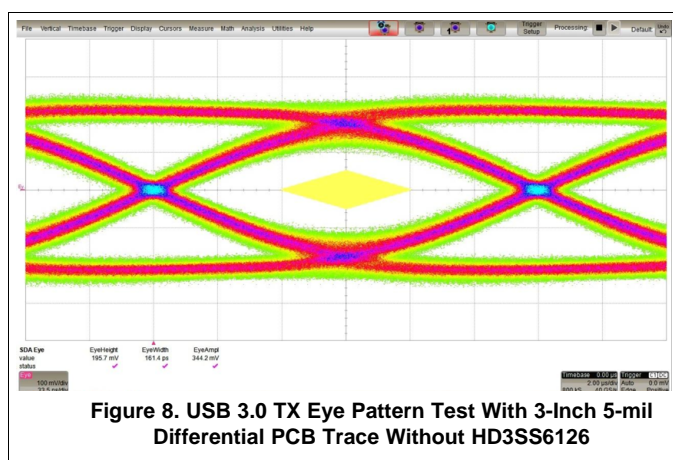
8.2.2.2   Differential Pairs

All of the interfaces the HD3SS6126 device supports require AC coupling between the transmitter and receiver. TI recommends using 0402-sized capacitors to provide AC coupling, but 0603-sized capacitors are also acceptable. Both 0805-sized capacitors and C-packs should be avoided. Best practice is to place AC-coupling capacitors symmetrically. A capacitor value of 0.1uF is best and the value should be matched for the +/-signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board.

All differential pairs must have a matched impedance according to the implemented protocol: 100-Ω differential (±10%) for PCIe and 90-Ω differential (±15%) for USB 2.0 and USB 3.0.

The control logic can be implemented by use of an external control processor or by using a simple selector switch. TI recommends using 5-kΩ pullup and pulldown resistors on the control signals, if they are included. The control logic must not violate the input voltage parameters outlined in the *Recommended Operating Conditions* table.

8.2.3   Application Curves

Figure 8. USB 3.0 TX Eye Pattern Test With 3-Inch 5-mil Differential PCB Trace Without HD3SS6126

Figure 9. USB 3.0 TX Eye Pattern Test With 3-Inch 5-mil Differential PCB Trace With HD3SS6126

9 Power Supply Recommendations

The power supply must provide a constant voltage with a 10% maximum variation of the nominal value, and has to be able to provide at least 3 mA for the HD3SS6126 only (based on the maximum power consumption). It is also possible to provide the power supply from VBUS from the Host, just by including a voltage regulator powered through VBUS. Each V_{CC} pin must have a 0.1-µF bypass capacitor placed as closely as possible. TI recommends including two extra capacitors in parallel, which should be also placed as closely as possible to the V_{CC} pin. The suggested values for these extra capacitors are 1 µF and 0.01 µF.

10 Layout

10.1 Layout Guidelines

Generally, impedance match becomes critical in such high-speed signal applications to avoid reflection. Each differential-signal pair must have a differential impedance of about 90 Ω ±15% (for PCIe or DP, 100 Ω ±10%) with single-end signal impedance about 50 Ω to ground. Usually, Microstrip is used to accomplish impedance match. Four layers are recommended for a low-EMI PCB design. shows physical geometries of differential traces to form Microstrip. In order to better maintain signal integrity, reference the following:

1. Route high-speed differential signals on the top layer with a solid ground layer under them to accomplish controlled impedance, while avoiding vias and stubs which may cause impedance discontinuities. If vias must be used, make sure the space of the vias is as minimal as possible.
2. Be sure both the length of differential traces and the length of differential signal pairs are matched in order to reduce intrapair skew and interpair skew separately which also does good to low EMI. TI recommends keeping the space of the traces of the differential signal the same across the entire length of the trace to keep impedance match and reduce EMI.
3. Route low-speed, but fast-edged control signals on the bottom layer to minimize the crosstalk of the high-speed signal.
4. For other adjacent signal traces on the same layer, make distance L ≥ 3 S to facilitate impedance match.
5. TI reccommends using 45° bends instead of 90° bends in order to maintain signal integrity and low EMI.
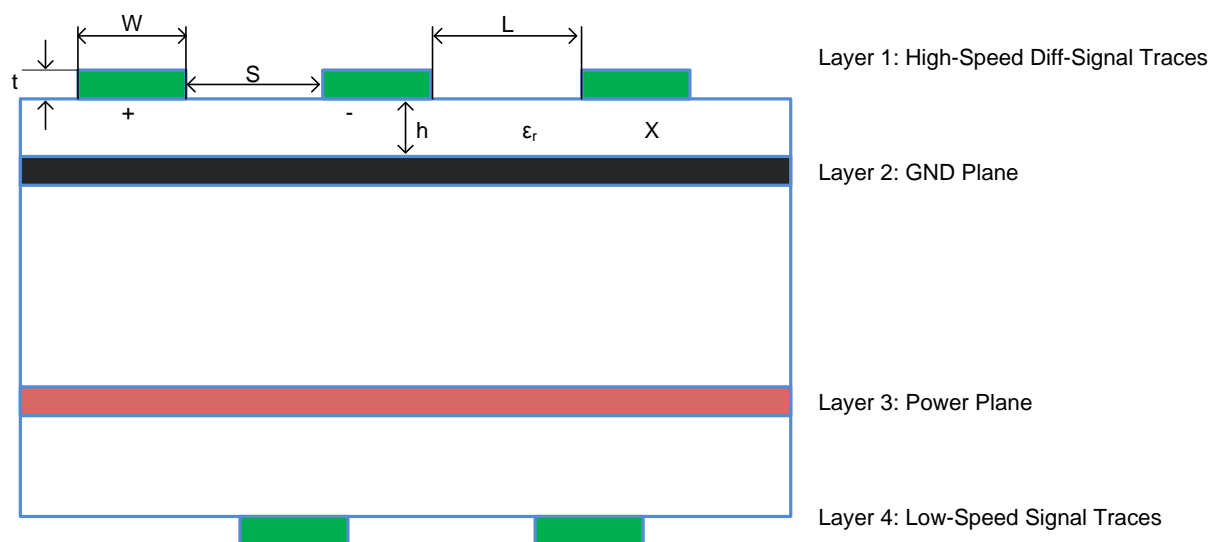
10.2 Layout Examples

Figure 10. PCB Layers Example

Layout Examples (continued)

45° bends and no 90° bends
to maintain signal integrity
and low EMI

Trace lenght = 659.5 mils,
with a +/- 0.04% of
variation

USB_A
U20

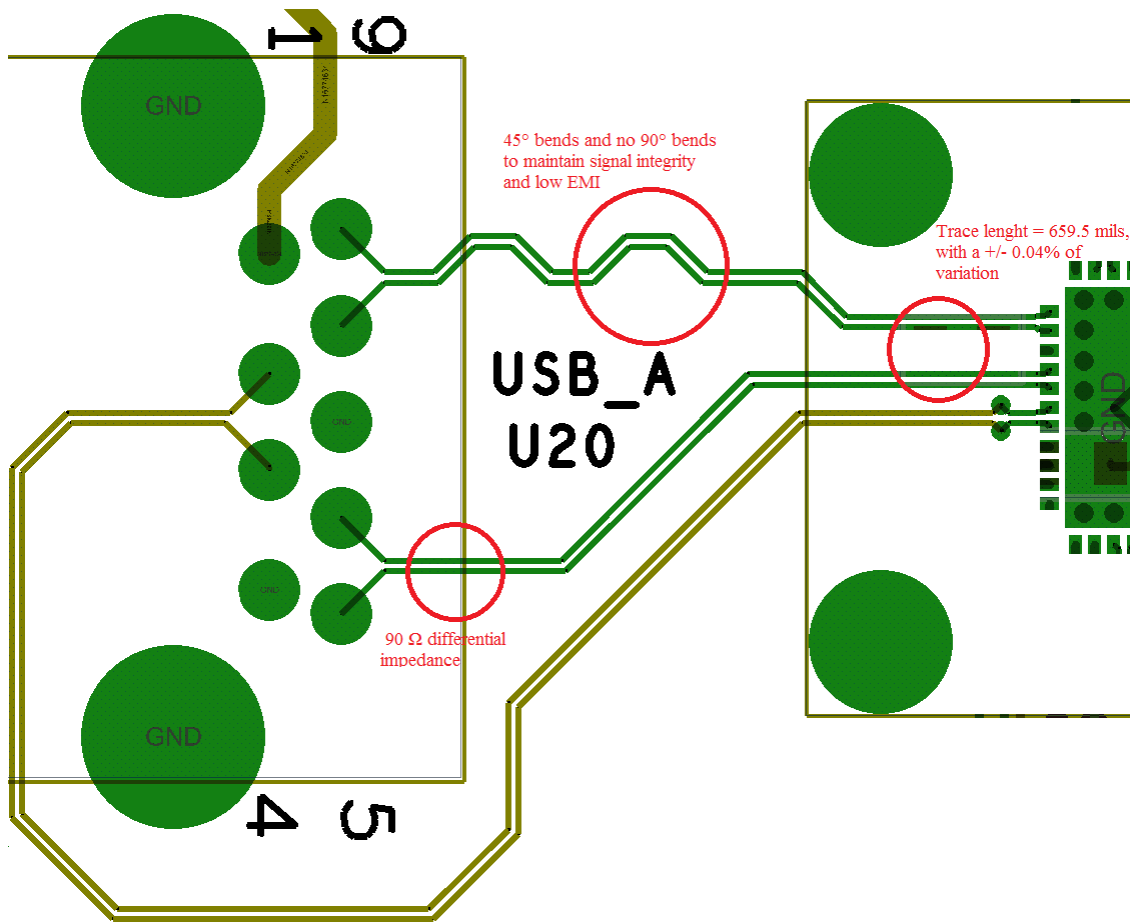90 Ω differential
impedance

GND

GND

Figure 11. USB Signals Routing Example

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
PCI Express、 is a trademark of PCI-SIG.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

产品	应用
数字音频	通信与电信
放大器和线性器件	计算机及周边
数据转换器	消费电子
DLP® 产品	能源
DSP - 数字信号处理器	工业应用
时钟和计时器	医疗电子
接口	安防应用
逻辑	汽车电子
电源管理	视频和影像
微控制器 (MCU)	
RFID 系统	
OMAP应用处理器	
无线连通性	德州仪器在线技术支持社区

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS6126RUAR	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	HD3SS6126	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
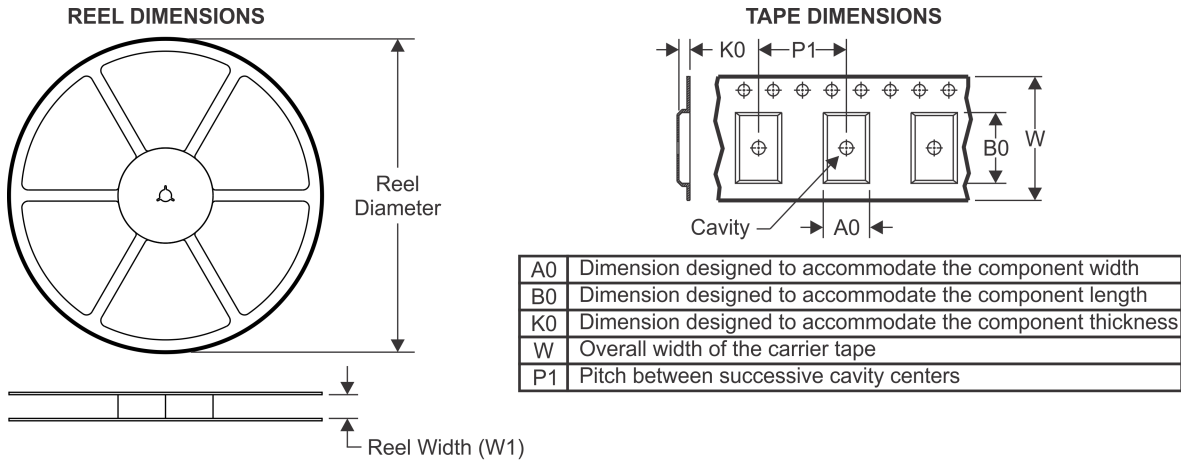
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
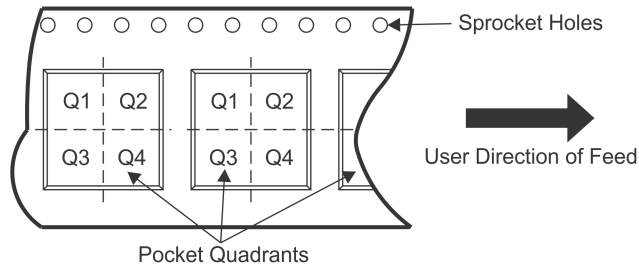
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS6126RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
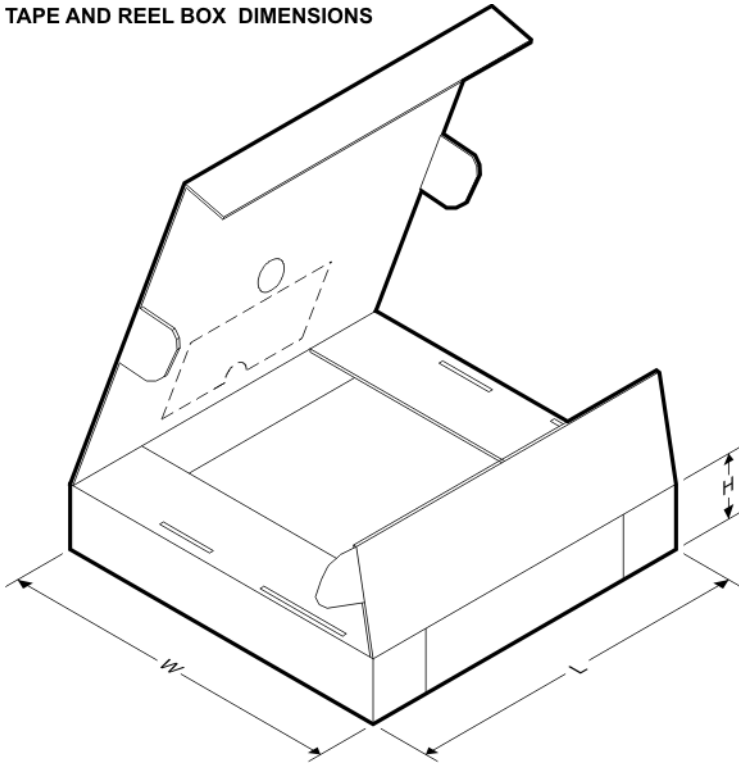
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS6126RUAR	WQFN	RUA	42	3000	367.0	367.0	38.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS INSTRUMENTS

4226504/A

B | 3.6 / 3.4 | A

PIN 1 INDEX AREA

9.1
8.9

0.8
0.6

C

SEATING PLANE

0.05
0.00

⌒ | 0.08 | C

2.05 ± 0.1

2X | 1.5

SYMM ₵

EXPOSED THERMAL PAD

18   21
17   22

2X | 8

SYMM ₵

43

7.55 ± 0.1

(0.1) TYP

1
42   39
38

38X | 0.5

PIN 1 ID

42X | 0.5 / 0.3

42X | 0.3 / 0.2

⊕ | 0.1 Ⓜ | C A B
0.05 Ⓜ

4219139/A   03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

(2.05)

42X (0.6)

42X (0.25)

38X (0.5)

SYMM

SEE SOLDER MASK DETAIL

42   39

38

1

(R0.05) TYP

($\varnothing$ 0.2) TYP VIA

SYMM

43

(3.525) TYP

1.17 TYP

(7.55)   (8.8)

17

22

18   21

(0.775) TYP

(3.3)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

0.05 MAX ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK OPENING

NON SOLDER MASK DEFINED (PREFERRED)

0.05 MIN ALL AROUND

METAL UNDER SOLDER MASK

EXPOSED METAL

SOLDER MASK OPENING

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219139/A   03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RUA0042A

PLASTIC QUAD FLATPACK - NO LEAD

42X (0.6)

42X (0.25)

38X (0.5)

(R0.05) TYP

SYMM

(0.56) TYP

42   39

1

38

43

(0.585) TYP

(8.8)

12X (0.97)

17   22

18   21

SYMM

12X (0.92)

(3.3)
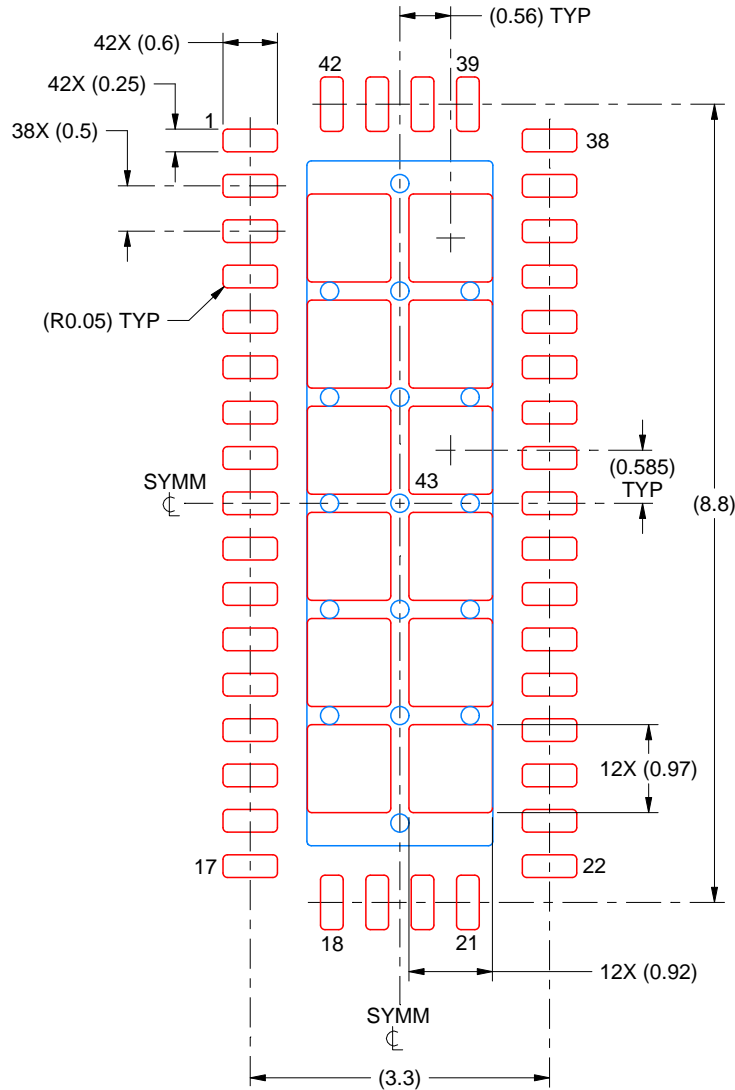
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A   03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。