High Efficiency, 1.2A Continuous, 1.8A Peak, 85V Input Synchronous Step Down Regulator

General Description

The SY8502 develops high efficiency synchronous step-down DC-DC converter capable of delivering 1.2A continuous, 1.8A peak current. The SY8502 operates over a wide input voltage range from 7V to 85V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The device adopts the instant PWM architecture to achieve fast transient responses for high step down applications.

Ordering Information

SY8502 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8502FCC	SO8E	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 500mΩ/240mΩ
- 7-85V Input Voltage Range
- 1.2A Continuous, 1.8A Peak Output Current Capability
- Adjustable Switching Frequency
- Instant PWM Architecture to Achieve Fast Transient Responses
- Programmable Switching Frequency Range: 200~500 kHz
- 2ms Internal Soft-start Limits the Inrush Current
- Precise ±2% 1.2V Reference
- RoHS Compliant and Halogen Free
- Compact Package: SO8E

Applications

- Non-Isolated Telecommunication Buck Regulator
- Secondary High Voltage Post Regulator
- Automotive Systems

Typical Applications

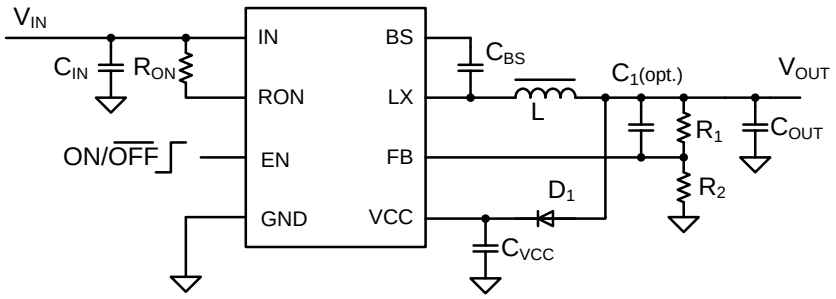


Figure 1. Schematic Diagram

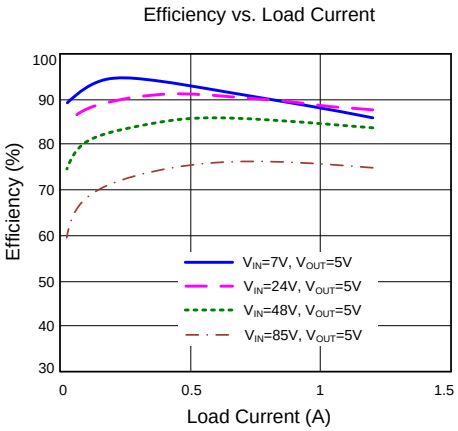
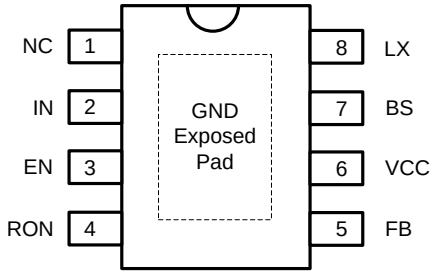


Figure 2. Efficiency

Pinout (top view)

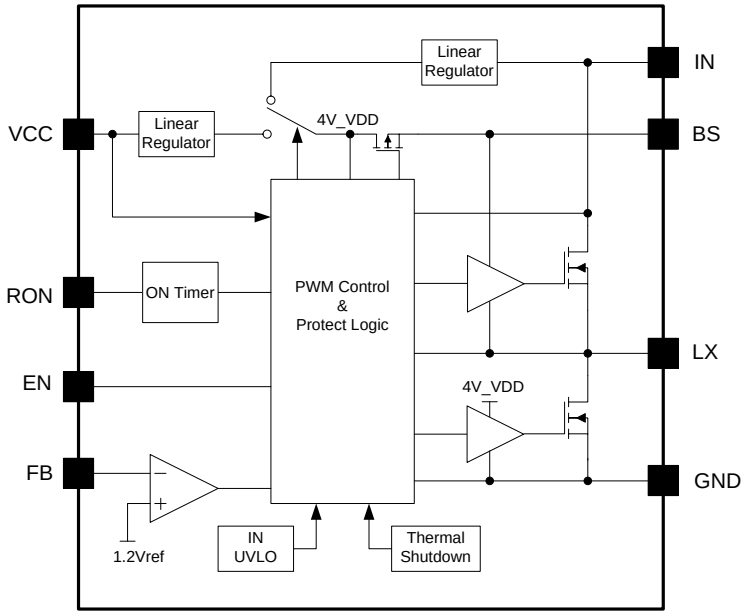


(SO8E)

Top Mark: BDX*xyz* for SY8502FCC (Device code: BDX, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
NC	1	Not connected.
IN	2	Input pin. Decouple this pin to GND with a low ESR ceramic capacitor.
EN	3	Enable control. The device has an accurate 1.21V rising threshold. This pin can also be used for programming the VIN turn on voltage with resistor divider.
RON	4	Connect a resistor from this pin to IN to set the top switch ON time. The switching frequency can be calculated using the following equation: $F_S(kHz)=\frac{11\times V_O(V)+500}{R_{ON}(M\Omega)}$
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=1.2\times(1+R_1/R_2)$
VCC	6	Supply input of the internal LDO.
BS	7	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor.
LX	8	Inductor pin. Connect this pin to the switching node of the inductor.
GND	Exposed Pad	Ground pin.

Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 90V
EN, LX, RON Voltage ---------- VIN + 0.3V
BS Voltage ---------- LX + 6V
FB Voltage ---------- 6V
VCC ---------- 30V
Power Dissipation, P_D @ T_A = 25°C, SO8E ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30°C/W
θ_{JC} ---------- 10°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 7V to 85V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}=48V, V_{OUT}=5V, L=33uH, C_{OUT}=10uF, T_A=25°C, I_{OUT}=1.2A unless otherwise specified)

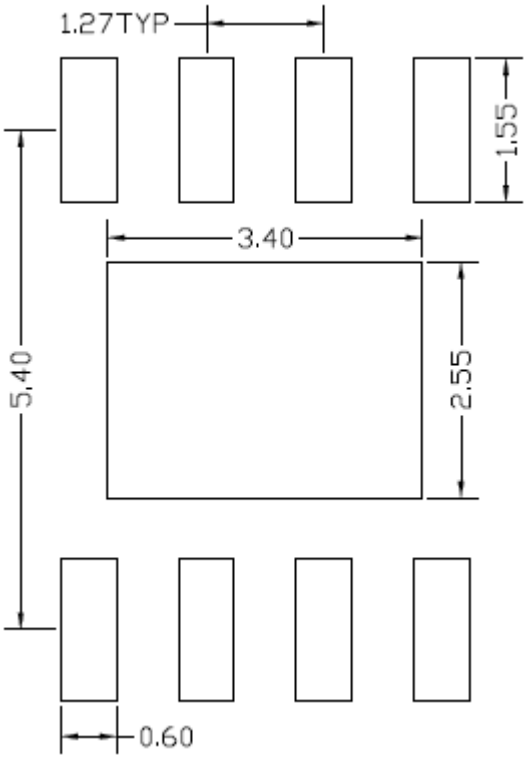
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%			400	μA
Shutdown Current	I_{SHDN}	EN=0		8	11	μA
Feedback Reference Voltage	V_{REF}		1.176	1.2	1.224	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			500		mΩ
Bottom FET RON	$R_{DS(ON)2}$			240		mΩ
Top FET peak Current Limit	$I_{LIM,TOP}$			3.2		A
Bottom FET Valley Current Limit	$I_{LIM,BOTTOM}$		1.6			A
EN Rising Threshold	V_{ENH}		1.11	1.21	1.31	V
EN Falling Threshold	V_{ENL}		1.08	1.18	1.28	V
Input UVLO Rising Threshold	V_{UVLO}		5.8	6.3	6.8	V
Input UVLO Hysteresis	V_{HYS}			0.25		V
Switching Frequency	F_{OSC}	V_{IN}=48V, R_{ON}=1.6MΩ		340		kHz
Min ON Time	t_{ON}			80		ns
Min OFF Time	t_{OFF}			200		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

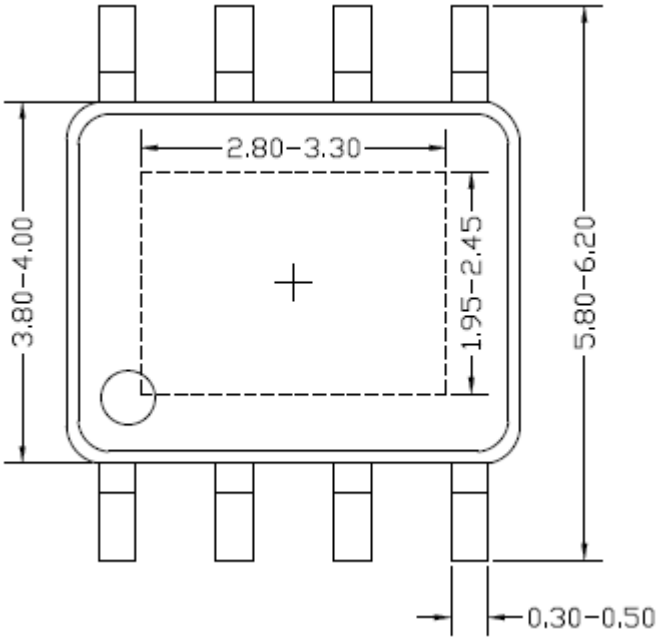
Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SO8E packages is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

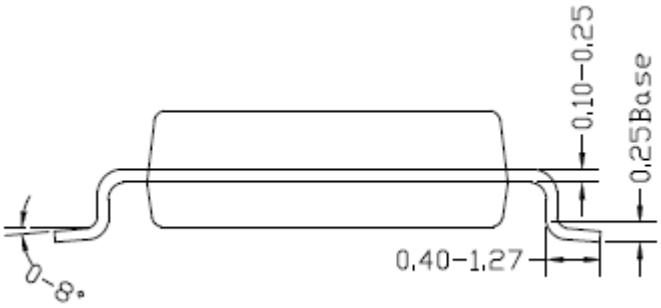
SO8E Package Outline & PCB layout



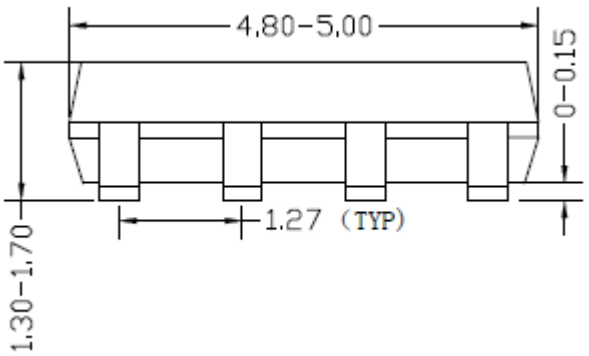
Recommended PCB Layout (Reference Only)



Top view



Side view



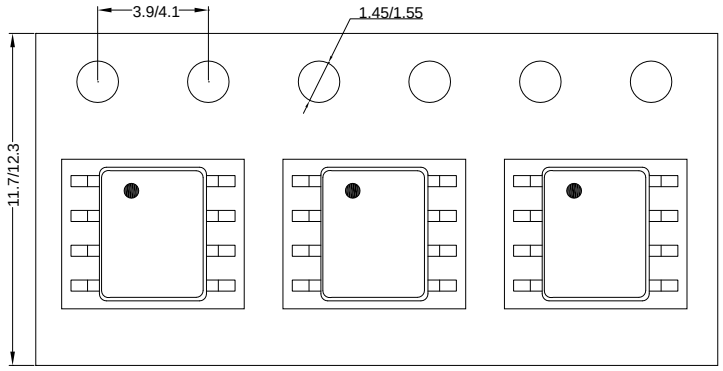
Front view

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

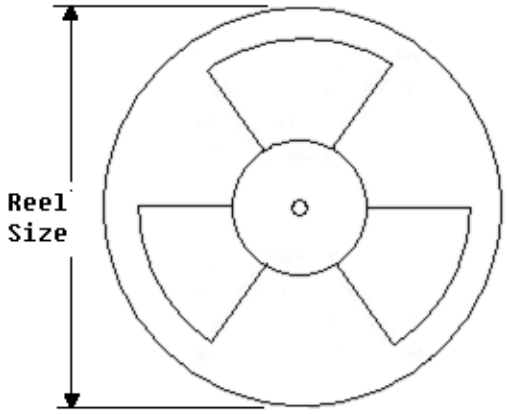
1. Taping orientation

SO8E



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8E	12	8	13"	400	400	2500

3. Others: NA