5-Pin Microprocessor Supervisory Circuit with Watchdog Timer and Manual Reset

GENERAL DESCRIPTION

The SGM823 microprocessor (μP) supervisory circuit combines reset output, watchdog, and manual reset input functions in SOT-23-5 package. It significantly improves system reliability and accuracy compared to separate ICs or discrete components. The SGM823 is specifically designed to ignore fast transients on V_{CC} .

Four preprogrammed reset threshold voltages are available. This device has an active-low reset output, which is guaranteed to be in the correct state for $V_{\rm CC}$ down to 1V. The SGM823 also offers a watchdog input and manual reset input.

The SGM823 is available in a Green SOT-23-5 package. It operates over an ambient temperature range of -40°C to +125°C.

FEATURES

- Ultra-Low Supply Current: < 1μA (TYP)
- Precision Supply-Voltage Monitor
 - + 4.63V for SGM823-L
 - + 3.08V for SGM823-T
 - + 2.93V for SGM823-S
 - + 2.63V for SGM823-R
- Push-Pull nRESET Output
- Guaranteed nRESET Valid at V_{CC} = 1V
- Fully Specified over Temperature
- 200ms Reset Pulse Width
- Power-Supply Transient Immunity
- Watchdog Timer with 1.6s Timeout
- Debounced TTL/CMOS-Compatible
- Manual Reset Input
- No External Components
- -40°C to +125°C Operating Temperature Range
- Available in a Green SOT-23-5 Package

APPLICATIONS

Computers

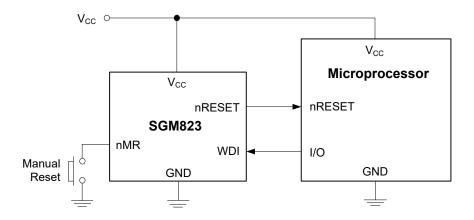
Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

TYPICAL APPLICATION



PACKAGE/ORDERING INFORMATION

| MODEL | RESET THRESHOLD (V) | PACKAGE DESCRIPTION | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---------|------------------------|------------------------|--------------------|--------------------|---------------------|
| | 4.63 | SOT-23-5 | SGM823-LXN5G/TR | MNFXX | Tape and Reel, 3000 |
| 0014000 | 3.08 | SOT-23-5 | SGM823-TXN5G/TR | MG6XX | Tape and Reel, 3000 |
| SGM823 | 2.93 | SOT-23-5 | SGM823-SXN5G/TR | MG7XX | Tape and Reel, 3000 |
| | 2.63 | SOT-23-5 | SGM823-RXN5G/TR | MG8XX | Tape and Reel, 3000 |

MARKING INFORMATION

NOTE: XX = Date Code.

YYY X X

Date Code - Week

Date Code - Year

Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

| Terminal Voltage (With respect to GND) | |
|--|---|
| V _{CC} 0.3V to 6.0V | |
| All Other Inputs0.3V to (V _{CC} + 0.3V) | |
| Input Current | |
| V _{CC} | |
| GND20mA | |
| Output Current | |
| All Outputs | |
| Package Thermal Resistance | |
| SOT-23-5, θ _{JA} | ! |
| Junction Temperature+150°C | |
| Storage Temperature Range65°C to +150°C | |
| Lead Temperature (Soldering, 10s)+260°C | |
| ESD Susceptibility | |
| HBM4000V | , |
| MM400V | , |
| CDM 1000V | , |

RECOMMENDED OPERATING CONDITIONS

Ambient Temperature Range-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

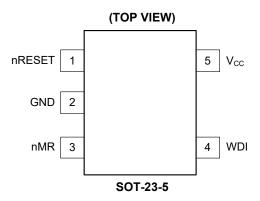
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

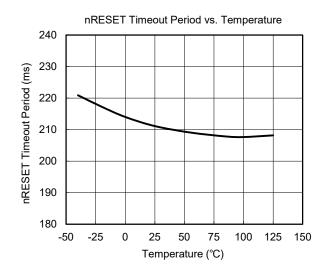
| NAME | FUNCTION |
|--------|---|
| nRESET | Active-Low Reset Output. Pulses low for 200ms when triggered, and remains low whenever V_{CC} is below the reset threshold or when nMR is logic low. It remains low for 200ms after one of the following occurs: V_{CC} rises above the reset threshold, the watchdog triggers a reset, or nMR goes from low to high. |
| GND | Ground. 0V ground reference for all signals. |
| nMR | Manual Reset Input Pin. A logic low on nMR asserts reset. Reset remains asserted as long as nMR is held low and for 200ms after nMR returns high. The active-low input has an internal $59k\Omega$ pull-up resistor. It can be driven from a CMOS logic line or shorted to ground with a switch. Leave open or connect to V_{CC} if unused. |
| WDI | Watchdog Input Pin. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a reset is triggered. The internal watchdog timer clears whenever reset is asserted, or whenever WDI sees a rising or falling edge. If WDI is left unconnected or is connected to a three-stated buffer output, the watchdog feature is disabled. |
| Vcc | Supply Voltage. |

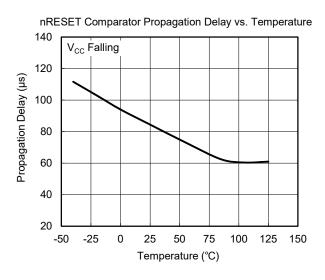
ELECTRICAL CHARACTERISTICS

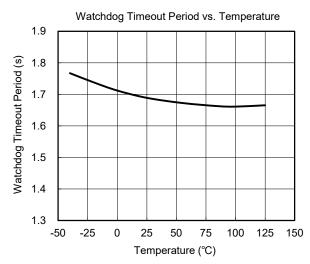
 $(T_A = +25^{\circ}\text{C}, V_{CC} = 4.73\text{V to } 5.5\text{V for SGM823-L}, V_{CC} = 3.14\text{V to } 5.5\text{V for SGM823-T}, V_{CC} = 2.99\text{V to } 5.5\text{V for SGM823-S}, V_{CC} = 2.68\text{V to } 5.5\text{V for SGM823-R}, \text{Full} = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}, \text{ unless otherwise noted.})$

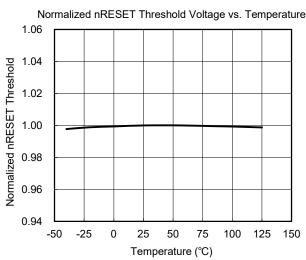
| PARAMETER | | CONDITIONS | TEMP | MIN | TYP | MAX | UNITS | |
|--|-----------------|---|-------|-----------------------|----------|------|------------------|--|
| Operating Voltage Range (V _{CC}) | | | Full | 1 | | 5.5 | V | |
| Cumply Current // | | V _{CC} = 3.6V | Full | | 0.5 | 1.2 | | |
| Supply Current (I _{SUPPLY}) | | V _{CC} = 5.5V | Full | | 0.7 | 1.4 | μΑ | |
| | | 20110001 | +25°C | 4.55 | 4.63 | 4.70 | V | |
| | | SGM823-L | Full | 4.54 | 4.63 | 4.73 | | |
| | | 2011000 7 | +25°C | 3.03 | 3.08 | 3.13 | | |
| | | SGM823-T | Full | 3.02 | 3.08 | 3.14 | | |
| nRESET Threshold (V _{nRST}) | | 0.011000.0 | +25°C | 2.88 | 2.93 | 2.98 | | |
| | | SGM823-S | Full | 2.87 | 2.93 | 2.99 | | |
| | | 2011000 5 | +25°C | 2.59 | 2.63 | 2.67 | | |
| | | SGM823-R | Full | 2.58 | 2.63 | 2.68 | | |
| | | SGM823-L | +25°C | | 20 | | | |
| | , | SGM823-T | +25°C | | 14 | | ., | |
| nRESET Threshold Hysteresis (V _{HY} | s) | SGM823-S | +25°C | | 13 | | mV | |
| | | SGM823-R | +25°C | | 12 | | | |
| nRESET Threshold Temperature Co | oefficient | | Full | | 20 | | ppm/°C | |
| nRESET Pulse Width (t _{RP}) | | | Full | 140 | 200 | 290 | ms | |
| | | SGM823-L, V _{CC} = V _{nRST(MAX)} , | Full | V _{CC} - 1.5 | | | | |
| | V _{OH} | I _{SOURCE} = 120µA SGM823-T/S/R, V _{CC} = V _{nRST(MAX)} , I _{SOURCE} = 30µA | Full | 0.8 × V _{CC} | | | - - - V | |
| nRESET Output Voltage | | $I_{SOURCE} = 30\mu A$ SGM823-L, $V_{CC} = V_{nRST(MIN)}$, | Full | | | 0.4 | | |
| | V _{OL} | | Full | | | 0.3 | | |
| | | $V_{CC} = 1V$, V_{CC} falling, $I_{SINK} = 50\mu A$ | Full | | | 0.3 | | |
| <u> </u> | | SGM823-L, nRESET = 0V, | Full | | | 460 | | |
| nRESET Output Short-Circuit Curre (I _{SOURCE}) | nt | $V_{CC} = 5.5V$ SGM823-T/S/R, nRESET = 0V, $V_{CC} = 3.6V$ | Full | | | 430 | μΑ | |
| V _{CC} to Reset Delay (t _{RD}) | | $V_{\text{nRST}} - V_{\text{CC}} = 100 \text{mV}$ | +25°C | | 84 | | μs | |
| Watchdog Timeout Period (t _{WD}) | | | Full | 1.1 | 1.6 | 2.4 | sec | |
| WDI Pulse Width (t _{WP}) | | V _{IL} = 0V, V _{IH} = V _{CC} | Full | 90 | | | ns | |
| | Low | V _{CC} = 5V | Full | | | 0.8 | | |
| | High | V _{CC} = 5V | Full | 3.5 | | | | |
| WDI Input Threshold | Low | V _{nRST(MAX)} < V _{CC} < 3.6V | Full | | | 0.8 | V | |
| | High | V _{nRST(MAX)} < V _{CC} < 3.6V | Full | 0.7 × V _{CC} | | | | |
| WDI Input Current | | WDI = V _{CC} , time average | Full | | 0.02 0.5 | | _ | |
| | | WDI = 0V, time average | Full | -0.5 | -0.01 | | μA | |
| | V _{IL} | Full | | | | 0.8 | | |
| nMR Input Voltage | V _{IH} | | Full | 2 | | | V | |
| nMR Pulse Width (t _{MR}) | | | Full | 300 | | | ns | |
| nMR Noise Immunity (Pulse width with no reset) | | | +25℃ | | 130 | | ns | |
| nMR to nRESET Out Delay (t _{MD}) | | | Full | | | 470 | ns | |
| nMR Pull-Up Resistance (Internal) | | | Full | 44 | 59 | 78 | kΩ | |

TYPICAL PERFORMANCE CHARACTERISTICS

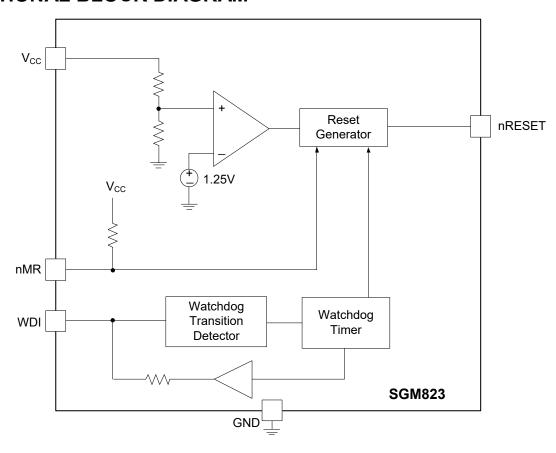








FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

nRESET Output

A microprocessor's (μ P's) reset input starts the μ P in a known state. The SGM823 μ P supervisory circuit asserts a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. nRESET is guaranteed to be a logic low for V_{CC} down to 1V. During power-up, when V_{CC} exceeds the rising threshold voltage (V_{nRST} + V_{HYS}), an internal timer keeps nRESET low for the specified reset timeout period (t_{RP}); after this interval, nRESET returns high (Figure 1).

If V_{CC} drops below the falling threshold voltage (V_{nRST}) (a brownout condition occurs), nRESET goes low. Each time nRESET is asserted, it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold, the internal timer restarts. nRESET both sources and sinks current.

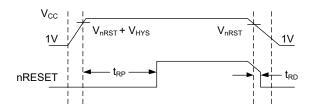


Figure 1. nRESET Timing Diagram

Manual Reset Input

Many $\mu P\text{-}based$ products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the SGM823, a logic low on nMR asserts reset. Reset remains asserted while nMR is low, and for t_{RP} (200ms nominal) after it returns high. nMR has an internal $59k\Omega$ pull-up resistor, so it can be left open if not used. This input can be driven with CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from nMR to GND to create a manual reset function; external debounce circuitry is not required. If nMR is driven from long cables or the device is used in a noisy environment, connect a $0.1\mu F$ capacitor from nMR to GND to provide additional noise immunity.

Watchdog Input

On the SGM823, the watchdog circuit monitors the μP 's activity. If the μP does not toggle the watchdog input (WDI) within t_{WD} (1.6s), reset asserts. The internal 1.6s timer is cleared by either a reset pulse or by toggling WDI, which detects pulses as short as 90ns. While reset is asserted, the timer remains cleared and does not count. As soon as reset is released, the timer starts counting (Figure 2).

Disable the watchdog function by leaving WDI unconnected or by three-stating the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period and high for the last 1/8 of the watchdog timeout period. When WDI is left unconnected, this internal driver clears the 1.6s timer every 1.4s. When WDI is three-stated or unconnected, the maximum allowable leakage current is $10\mu A$ and the maximum allowable load capacitance is 200pF.

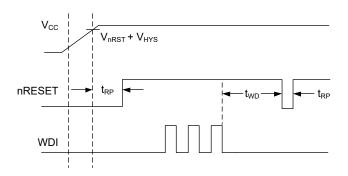


Figure 2. Watchdog Timing Relationship

APPLICATION INFORMATION

Interfacing to µPs with Bidirectional Reset Pins

The nRESET output maximum pull-up current is $460\mu A$ for L version ($430\mu A$ for T/S/R versions). This allows μPs with bidirectional resets, such as the 68HC11, to force nRESET low when the SGM823 is pulling nRESET high (Figure 3).

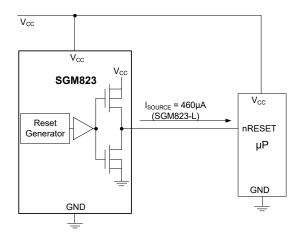


Figure 3. Interfacing to µP with Bidirectional Resets

Negative-Going Vcc Transients

This supervisor is relatively immune to short duration, negative-going V_{CC} transients (glitches), which usually do not require the entire system to shut down. Resets are issued to the μP during power-up, power-down and brownout conditions.

An optional 0.1 μF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

Watchdog Input Current

The SGM823 WDI is internally driven through a buffer and series resistor from the watchdog counter. When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within the first 7/8 of the watchdog timeout period to reset the watchdog timer.

Watchdog Software Considerations

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

Figure 4 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. As described in the Watchdog Input Current section, this scheme results in higher time average WDI input current than leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

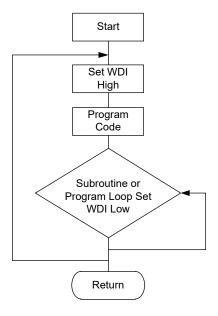


Figure 4. Watchdog Flow Diagram

5-Pin Microprocessor Supervisory Circuit with Watchdog Timer and Manual Reset

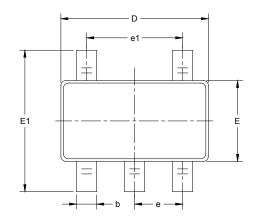
SGM823

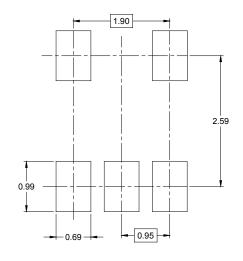
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

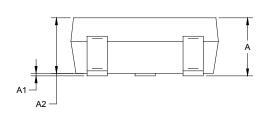
| JULY 2020 – REV.A.1 to REV.A.2 | Page |
|---|------|
| Updated Features section | 1 |
| Changed Detailed Description section | 7 |
| JANUARY 2020 – REV.A to REV.A.1 | Page |
| Changed Electrical Characteristics section | 4 |
| Changed Typical Performance Characteristics section | 5 |
| Changed Figure 1 | |
| Changes from Original (DECEMBER 2018) to REV.A | Page |
| Changed from product preview to production data | All |

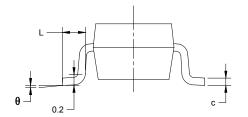
PACKAGE OUTLINE DIMENSIONS SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)

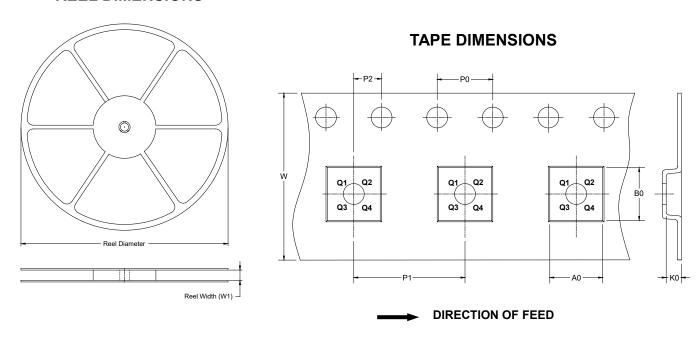




| Symbol | | nsions meters | Dimensions In Inches | | |
|--------|-----------|------------------|-------------------------|-------|--|
| | MIN | MAX | MIN | MAX | |
| Α | 1.050 | 1.250 | 0.041 | 0.049 | |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 | |
| A2 | 1.050 | 1.150 | 0.041 | 0.045 | |
| b | 0.300 | 0.500 | 0.012 | 0.020 | |
| С | 0.100 | 0.200 | 0.004 | 0.008 | |
| D | 2.820 | 3.020 | 0.111 | 0.119 | |
| E | 1.500 | 1.700 | 0.059 | 0.067 | |
| E1 | 2.650 | 2.950 | 0.104 | 0.116 | |
| е | 0.950 | BSC | 0.037 BSC | | |
| e1 | 1.900 BSC | | 0.075 | BSC | |
| L | 0.300 | 0.600 | 0.012 | 0.024 | |
| θ | 0° | 8° | 0° | 8° | |

TAPE AND REEL INFORMATION

REEL DIMENSIONS



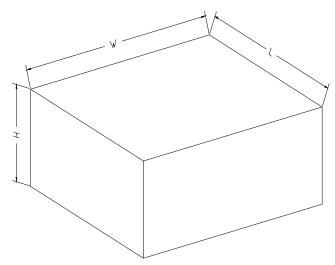
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|--------------|------------------|--------------------------|------------|------------|------------|------------|------------|------------|-----------|------------------|
| SOT-23-5 | 7" | 9.5 | 3.20 | 3.20 | 1.40 | 4.0 | 4.0 | 2.0 | 8.0 | Q3 |

TX10000.000

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton | |
|-------------|----------------|---------------|----------------|--------------|--|
| 7" (Option) | 368 | 227 | 224 | 8 | |
| 7" | 442 | 410 | 224 | 18 | |