# Up to 24V Supply, 4-A Dual Channel High Speed Low Side Driver

## FEATURES

- Wide Supply Voltage Range: 4.5V - 24V
- 4A Peak Source Current and 4A Peak Sink Current
- Negative Input Voltage Capability: Down to -5V
- TTL Compatible Input Logic Threshold
- Propagation Delay: 13ns
- Typical Rising and Falling Times: 8ns
- Low Quiescent Current: 55uA
- Output Low When Input Floating
- Independent Enable Logic for Each Channel
- Thermal Shutdown Protection: 170°C
- Available in SOP-8 Package

## APPLICATIONS

- IGBT/MOSFET Gate Driver
- Variable Frequency-Drive (VFD)
- Switching Power Supply
- Motor Control
- Solar Power Inverter

## DESCRIPTION

The SCT52241 is a wide supply, dual channel, high speed, low side gate drivers for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with rail-to-rail output capability. The 24V power supply rail enhances the driver output ringing endurance during the power device transition.

The minimum 13ns input to output propagation delay enables the SCT52241 suitable for high frequency power converter application.

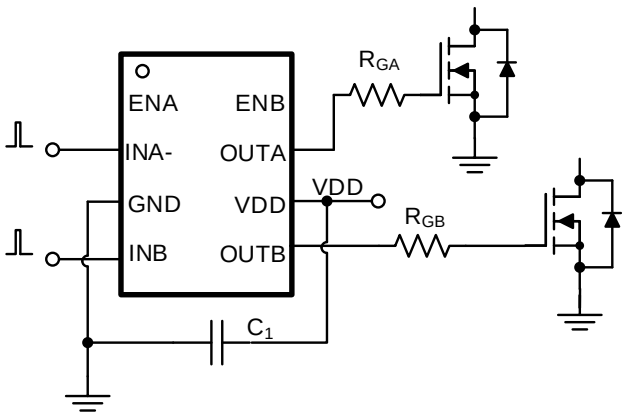
The SCT52241 features wide input hysteresis that is compatible for TTL low voltage logic. The SCT52241 has the capability to handle negative input down to -5V, which increases the input noise immunity.

The SCT52241 has very low quiescent current that reduces the stand-by loss in the power converter. The SCT52241 each channel driver adopts non-overlap driver design to avoid the shoot-through of output stage.

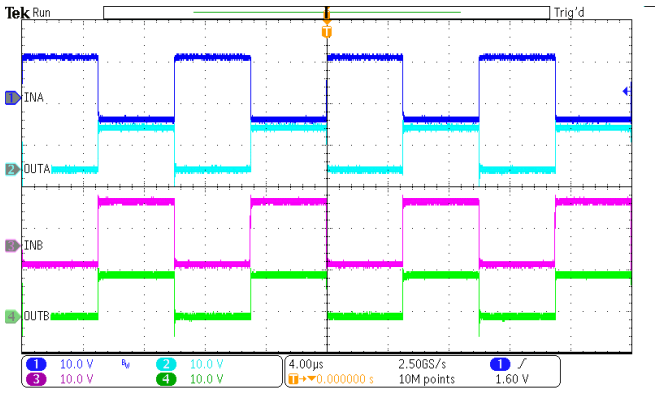
The SCT52241 features 170°C thermal shut down. The SCT52241 is available in SOP-8 package

## TYPICAL APPLICATION

SCT52241 Typical Application




Application Waveform



## REVISION HISTORY

*NOTE: Page numbers for previous revisions may differ from page numbers in the current version.*

Revision 1.0: Production.

Revision 1.1: Format adjustment, update ABS max, add EC table max limit

Revision 1.2: Correct package information in Page 16

## DEVICE ORDER INFORMATION

| PART NUMBER | PACKAGE MARKING | PACKAGE DISCRIPTION |
|---|---|---|
| SCT52241STD | 2241 | SOP-8 |

1）For Tape & Reel, Add Suffix R (e.g. SCT52241STDR).

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

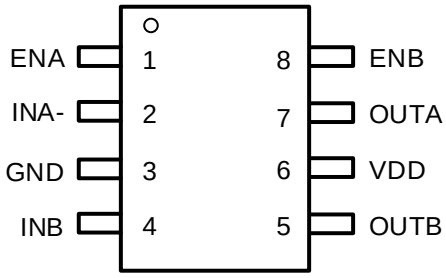
| DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|
| ENA, ENB | -0.3 | 26 | V |
| INA-, INB | -5 | 26 | V |
| OUTA, OUTB | -0.3 | VDD+0.3 | V |
| VDD | -0.3 | 26 | V |
| Operating junction temperature TJ (2) | -40 | 150 | °C |
| Storage temperature $T_{STG}$ | -65 | 150 | °C |

(1) Stresses beyond those listed under Absolut Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

## PIN CONFIGURATION

Top View: SOP-8pin Plastic




## PIN FUNCTIONS

| NAME | NO. | PIN FUNCTION |
|---|---|---|
| ENA | 1 | Channel A enable logic input, TTL compatible. Floating logic high. |
| INA- | 2 | Channel A logic input, TTL compatible. Floating logic low. |
| GND | 3 | Power ground. Must be soldered directly to ground plane for thermal performance improvement and electrical contact. |
| INB | 4 | Channel B logic input, TTL compatible. Floating logic low. |
| OUTB | 5 | Channel B gate driver output |
| VDD | 6 | Power Supply, must be locally bypassed by the ceramic cap. |
| OUTA | 7 | Channel A gate driver output |
| ENB | 8 | Channel B enable logic input, TTL compatible. Floating logic high. |

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage range | 4.5 | 24 | V |
| $V_{INA-,INB}$ | Input voltage range | -5 | 24 | |
| $T_J$ | Operating junction temperature | -40 | 150 | °C |

## ESD RATINGS

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1) | -2 | +2 | kV |
| | Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1) | -0.5 | +0.5 | kV |

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

## THERMAL INFORMATION

| PARAMETER | THERMAL METRIC | SOP-8L | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction to ambient thermal resistance (1) | 130 | °C/W |
| $R_{\theta JC}$ | Junction to case thermal resistance (1) | 80 | |

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT52241 is mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT52241. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

## ELECTRICAL CHARACTERISTICS

$V_{DD}$=12V, $T_J$=-40°C~150°C, typical values are tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply and Output** | | | | | | |
| $V_{DD}$ | Operating supply voltage | | 4.5 | | 24 | V |
| $V_{DD_UVLO}$ | Input UVLO<br>Hysteresis | $V_{DD}$ rising | | 4.2<br>300 | 4.5 | V<br>mV |
| $I_Q$ | Supply current | EN=$V_{DD}$=3.5V, INA- =INB=3.5V | | 55 | | uA |
| | | EN=$V_{DD}$=12V,<br>INA- =INB= $V_{DD}$=12V | | 120 | | uA |
| **INPUTS** | | | | | | |
| $V_{INA-,INB_H}$ | Input logic high threshold<br>Output low for inverting input<br>Output high for non-inverting input | | | 2.1 | 2.4 | V |
| $V_{INA-,INB_L}$ | Input logic low threshold<br>Output high for inverting input<br>Output low for non-inverting input | | 0.8 | 1 | | V |
| $V_{IN_Hys}$ | Hysteresis | | | 1.1 | | V |
| $V_{ENA,ENB_H}$ | Enable logic high threshold | | | 2.1 | 2.4 | V |
| $V_{ENA,ENB_L}$ | Enable logic low threshold | | 0.8 | 1 | | V |
| $V_{EN_Hys}$ | Hysteresis | | | 1.1 | | V |
| **OUTPUTS** | | | | | | |
| $V_{DD_VOH}$ | Output – output high voltage | $I_{OUT}$= - 10mA | | | 150 | mV |
| $V_{OL}$ | Output low voltage | $I_{OUT}$= 10mA | | | 10 | mV |
| $I_{SINK/SRC}$ | Output sink/source peak current | $C_{Load}$=10nF, $F_{SW}$=1kHz | | 4 | | A |
| $R_{OH}$ | Output pull high resistance (only PMOS ON) | $I_{OUT}$= - 10mA | 5 | 9 | 18 | Ω |
| $R_{OL}$ | Output pull low resistance | $I_{OUT}$= 10mA | 0.3 | 0.6 | 1.2 | Ω |
| **Timing** | | | | | | |
| $T_R$ | Output rising time | $C_{Load}$=1nF | | 8 | 20 | ns |
| $T_F$ | Output falling time | $C_{Load}$=1nF | | 8 | 20 | ns |
| $T_{D_IN}$ | Input to output propagation delay, Rising edge | | 7 | 13 | 25 | ns |
| | Input to output propagation delay, Falling edge | | 7 | 13 | 25 | ns |
| $T_{M_IN}$ | Input to output delay matching | | | 1 | 4 | ns |
| $T_{MIN_ON}$ | Minimum input pulse width | $C_{Load}$=1nF | | 20 | 30 | ns |
| **Protection** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold | $T_J$ rising | | 170 | | °C |
| | Hysteresis | | | 25 | | °C |

## TYPICAL CHARACTERISTICS

$V_{IN}$=12V, $T_A$= 25°C.

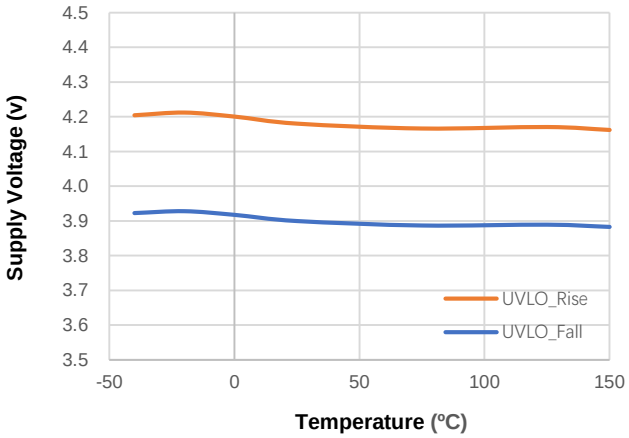



Figure 1. UVLO vs Temperature

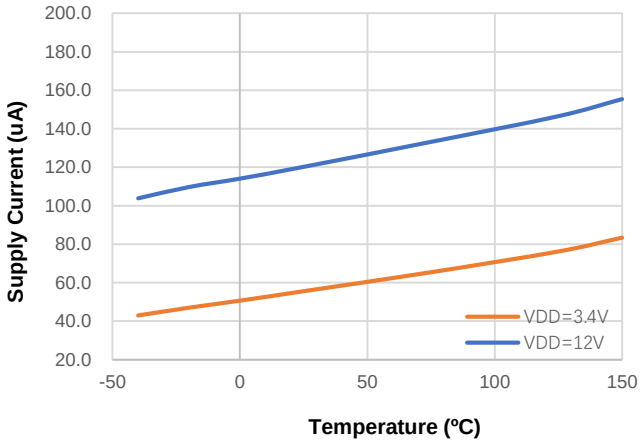



Figure 2. Supply current vs Temperature

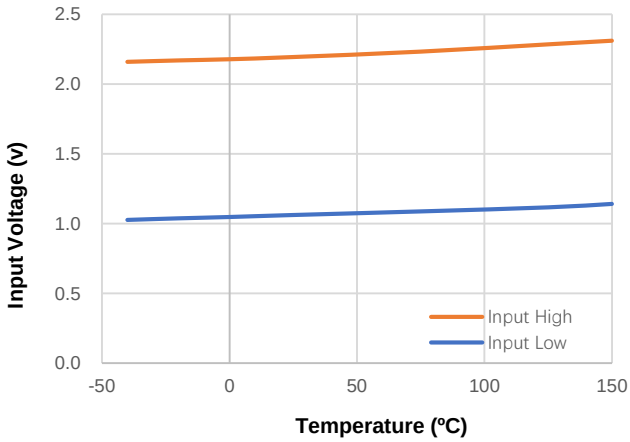



Figure 3. Input Threshold vs Temperature

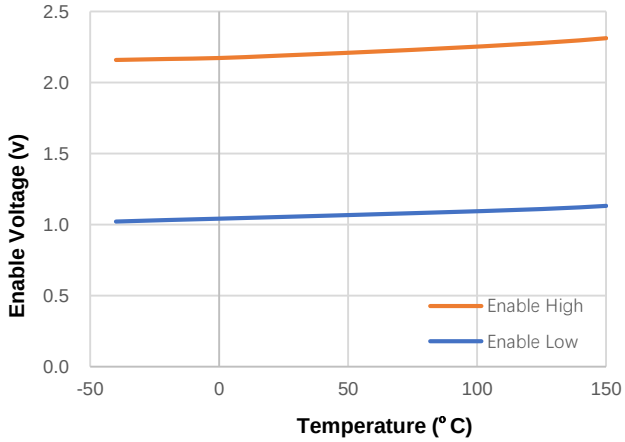



Figure 4. Enable Threshold vs Temperature

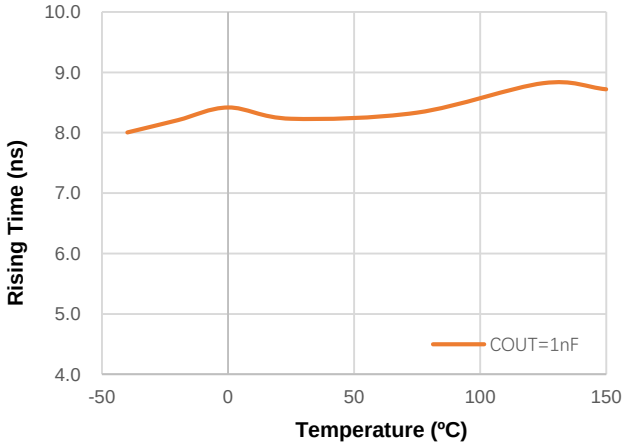



Figure 5 Output Rising Time vs Temperature

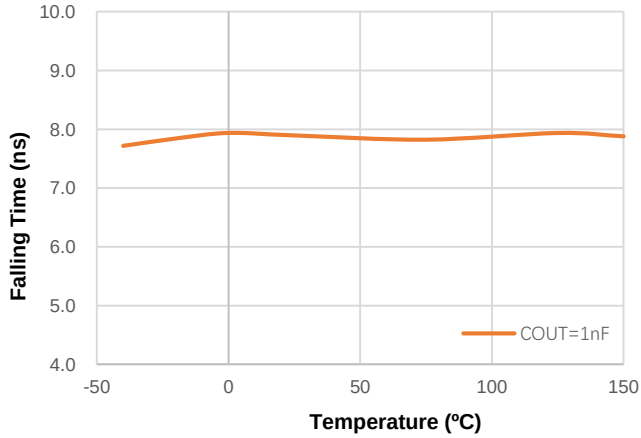



Figure 6. Output Falling Time vs Temperature

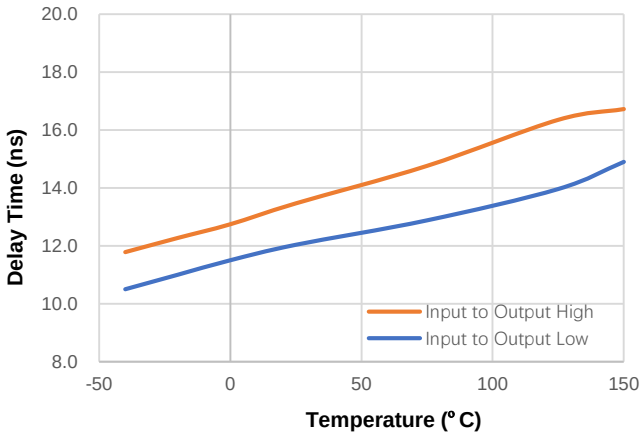



Figure 7. Input to Output Propagation Delay vs Temperature

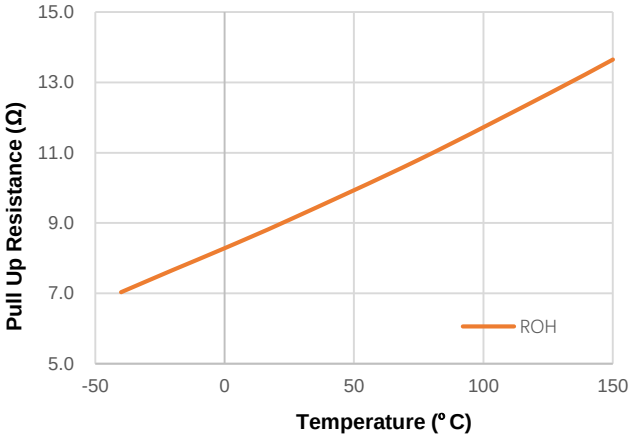



Figure 8. ROH vs Temperature

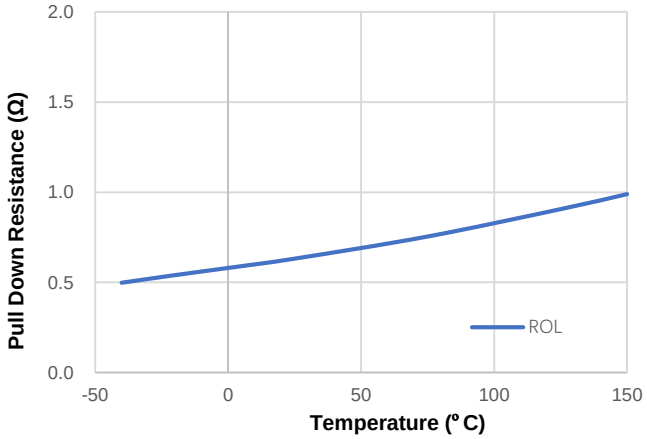



Figure 9. ROL vs Temperature

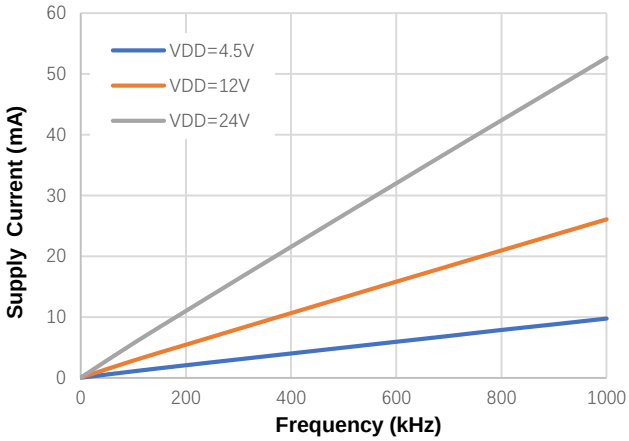
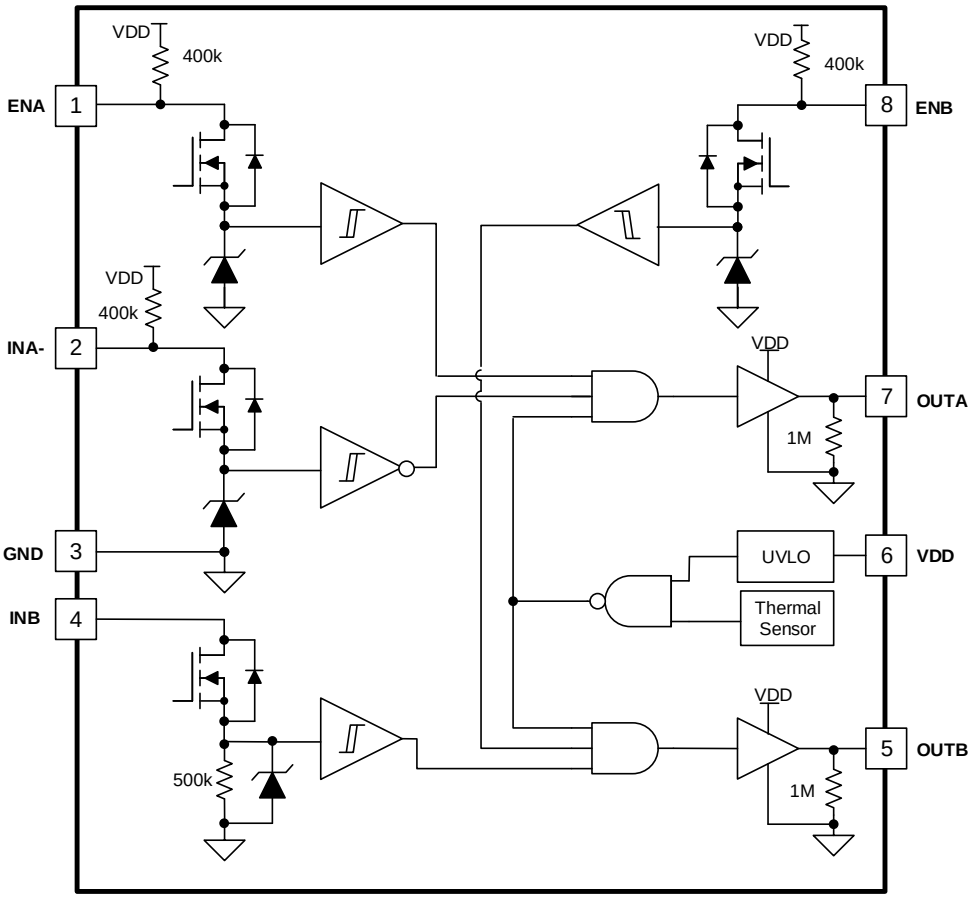



Figure 10. Operation Supply Current vs Frequency, $C_{OUT}$=1nF

## FUNCTIONAL BLOCK DIAGRAM



## OPERATION

### Overview

The SCT52241 is a dual-channel high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output improves the SCT52241 output stage robustness during switching load fast transition. The SCT52241 has flexible input and enable pin configuration, table 1 shows the device output logic truth table.

. Table 1: the SCT52241 Device Logic.

| ENA | ENB | INA- | INB | OUTA | OUTB |
|---|---|---|---|---|---|
| H | H | L | L | H | L |
| H | H | L | H | H | H |
| H | H | H | L | L | L |
| H | H | H | H | L | H |
| L | L | Any | Any | L | L |
| Any | Any | Floating | Floating | L | L |
| Floating | Floating | L | L | H | L |
| Floating | Floating | L | H | H | H |
| Floating | Floating | H | L | L | L |
| Floating | Floating | H | H | L | H |

### VDD Power Supply

The SCT52241 operates under a supply voltage range between 4.5V to 24V. For the best high-speed circuit performance, two VDD bypass capacitors in parallel are recommended to prevent noise problems on supply VDD. A 0.1-μF surface mount ceramic capacitor must be located as close as possible to the VDD to GND pins of the SCT52241. In addition, a larger capacitor (such as 1-μF or 10uF) with relatively low ESR must be connected in parallel, in order to help avoid the unexpected VDD supply glitch. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

### Under Voltage Lockout (UVLO)

SCT52241 device Under Voltage Lock Out (UVLO) rising threshold is typically 4.2 V with 300-mV typical hysteresis. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low regardless of the status of the inputs. The hysteresis prevents output bouncing when low VDD supply voltages have noise from the power supply. The capability to operate at low voltage below 5 V, is especially suited for driving new emerging wide band gap power device like GaN. For example, at power up, the driver output remains low until the VDD voltage reaches the UVLO threshold if enable pin is active or floating. The magnitude of the OUT signal rises with VDD until steady state VDD reached.

The non-inverting operation in Figure 11 shows that the output remains low until the UVLO threshold reached, and then the output is in-phase with the input.

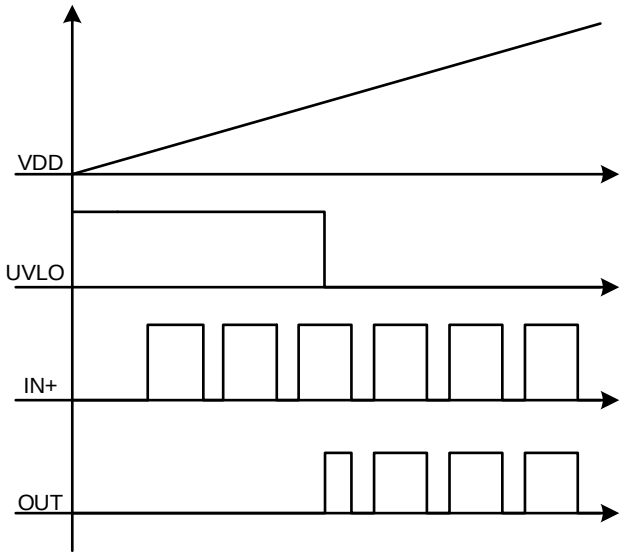



Figure 11. SCT52241 Non-inverting Output Vs VDD

**Enable Function**

SCT52241 provides independent enable pins ENA and ENB for external control of each channel operation. The enable pins are based on a TTL compatible input-threshold logic that is independent of the supply voltage and is effectively controlled with logic signals from 3.3-V and 5-V microcontrollers. When applying a voltage higher than the high threshold (typical 2.1V) the pin, the SCT52241 enables all functions and starts gate driver operation. Driver operation is disabled when ENx voltage falls below its lower threshold (typical 1V). The ENx pins are internally pulled up to VDD with 400k pullup resistors. Hence, the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not required.

**Input Stage**

The input of SCT52241 is compatible on TTL input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5V. SCT52241 also features tight control of the input pin threshold voltage that ensures stable operation across temperature. The very low input parasitic capacitance on the input pins increases switching speed and reduces the propagation delay.

**Output Stage**

The SCT52241 output stage features the pull up structure with P-type MOSFET PM1 and N-type MOSFET NM1 in parallel, as shown in Figure 12. PM1 provides the pull up capability when OUT approaches VDD and the NM1 holds off state, which guarantees the driver output is up to VDD rail. The measurable on-resistance $R_{OH}$ in steady state is the conduction resistance of PM1. NM1 provides a narrow instant peak sourcing current up to 4A to eliminate the turn on time and delay. During the output turn on transition, the equivalent hybrid pull on transient resistance is $1.5R_{OL}$, which is much lower than the DC measured $R_{OH}$.

The N-type MOSFET NM2 composes the output stage pull down structure; the $R_{OL}$ is the DC measurement and represents the pull down impedance. The output stage of SCT52241 provides rail-to-rail operation, and is able to supply 4A sourcing and 4A sinking peak current. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. The outputs of the dual channel drivers are designed to withstand 500-mA reverse current without either damaging the device or logic malfunction.

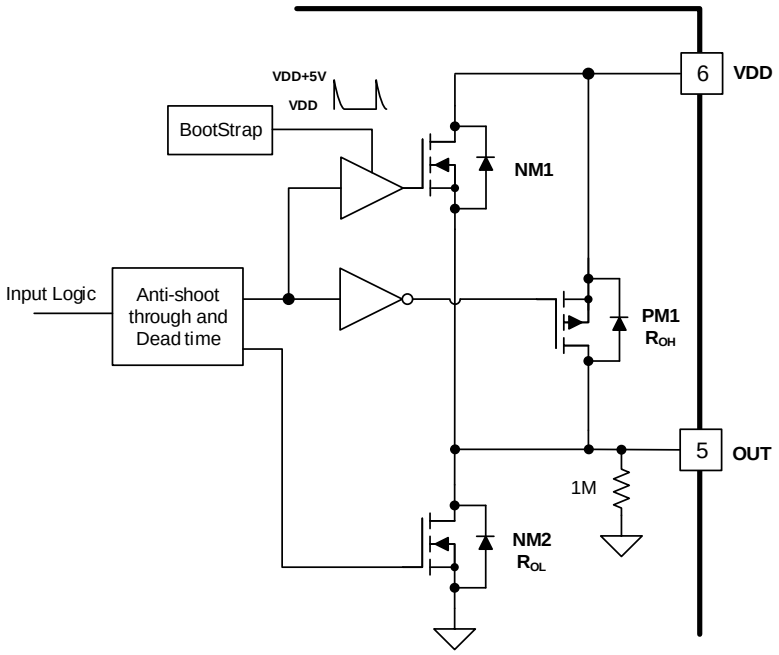



Figure 12. SCT52241 Output Stage

**Thermal Shutdown**

Once the junction temperature in the SCT52241 exceeds 170° C, the thermal sensing circuit stops switching until the junction temperature falling below 145° C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

## APPLICATION INFORMATION

### Typical Application

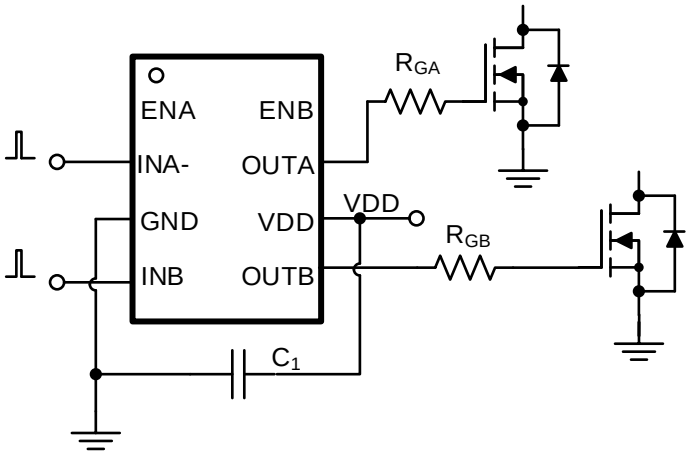



Figure 16. Dual Channel Driver Typical Application

### Driver Power Dissipation

Generally, the power dissipated in the SCT52241 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52241 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52241 is:

$$P_G = C_{Load} * V_{DD}^2 * f_{SW} \quad (1)$$

Where

- $V_{DD}$ is supply voltage
- $C_{Load}$ is the output capacitance
- $F_{SW}$ is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52241 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

$$P_G = Q_g * V_{DD} * f_{SW} \quad (2)$$

Where

- $Q_g$ is the gate charge of the power device
- $f_{SW}$ is the switching frequency
- $V_{DD}$ is the supply voltage

If $R_G$ applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

$$P_G = \frac{1}{2} * Q_g * V_{DD} * f_{SW} * \left(\frac{R_{OL}}{R_{OL} + R_G} + \frac{R_{OH}}{R_{OH} + R_G}\right) \quad (3)$$

Where

- $R_{OH}$ is the equivalent pull up resistance of SCT52241
- $R_{OL}$ is the  pull down resistance of SCT52241
- $R_G$ is the gate resistance between driver output and gate of power device.

## Application Waveforms

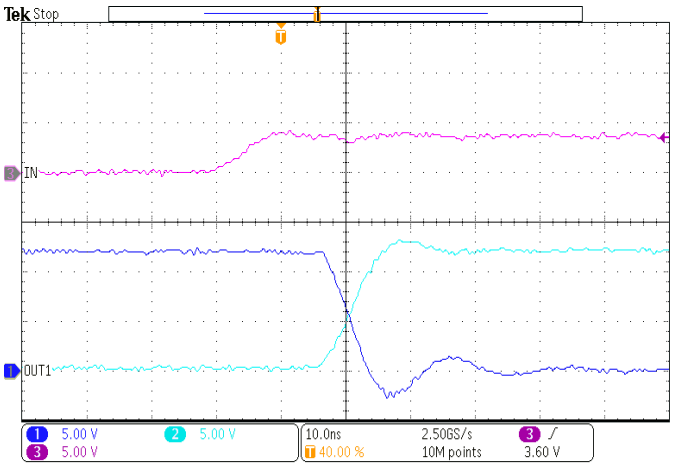



Figure 17. Driver Switching ON

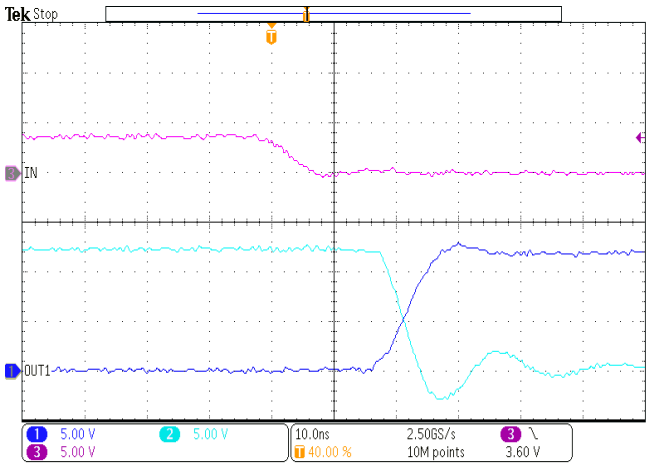



Figure 18. Driver Switching OFF

**Layout Guideline**

The SCT52241 provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. Below are the layout recommendations with using SCT52241 and Figure 19 is the layout example.

Put the SCT52241 as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GND pin to reduce the supply ripple.

Star-point grounding is recommend to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit nodes such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be as short as possible to reduce parasitic inductance. A ground plane is to provide noise shielding and thermal dissipation as well.

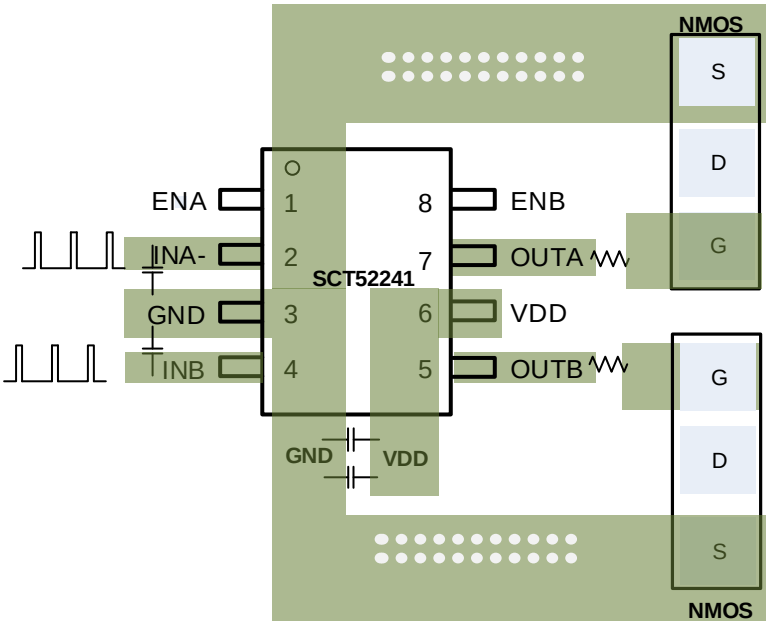



Figure 19. SCT52241 PCB Layout Example

**Thermal Considerations**

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$ , and keep the actual power dissipation less than or equal to $P_{D(max)}$ . The maximum-power-dissipation limit is determined using Equation (4).

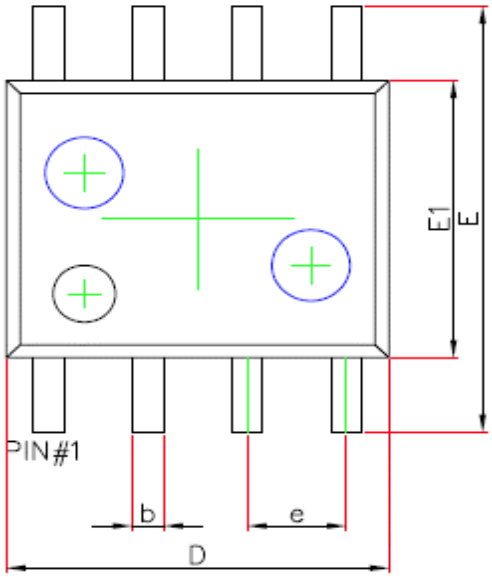
$$P_{D(MAX)} = \frac{150 - T_A}{R_{\theta JA}} \quad (4)$$

where

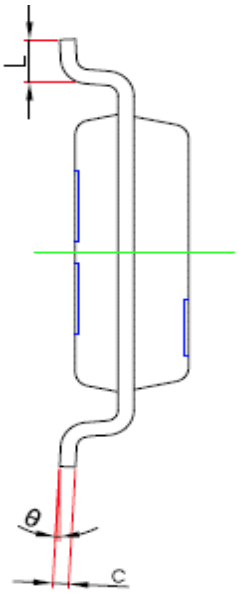
- $T_A$ is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

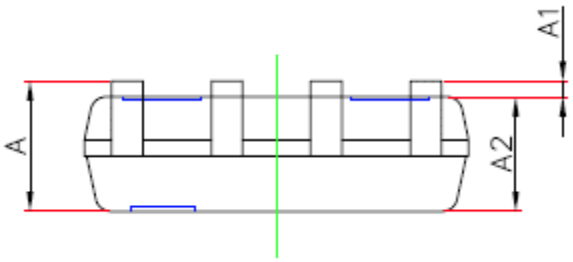
## PACKAGE INFORMATION (SOP-8)




TOP VIEW




BOTTOM VIEW



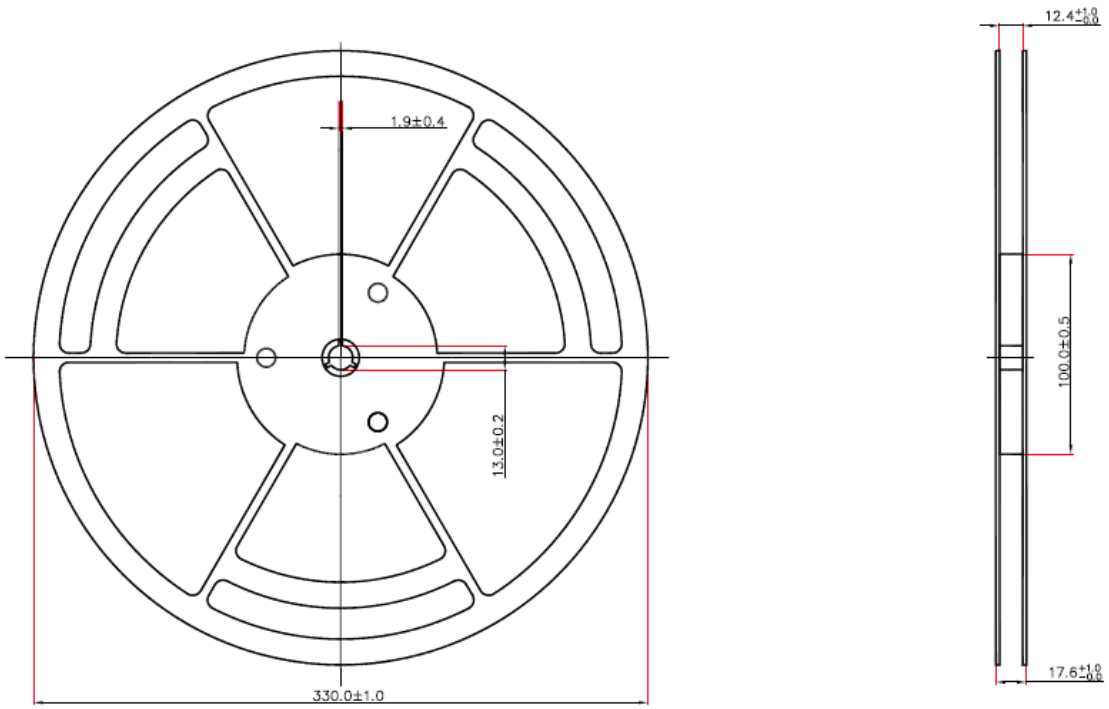

SIDE VIEW

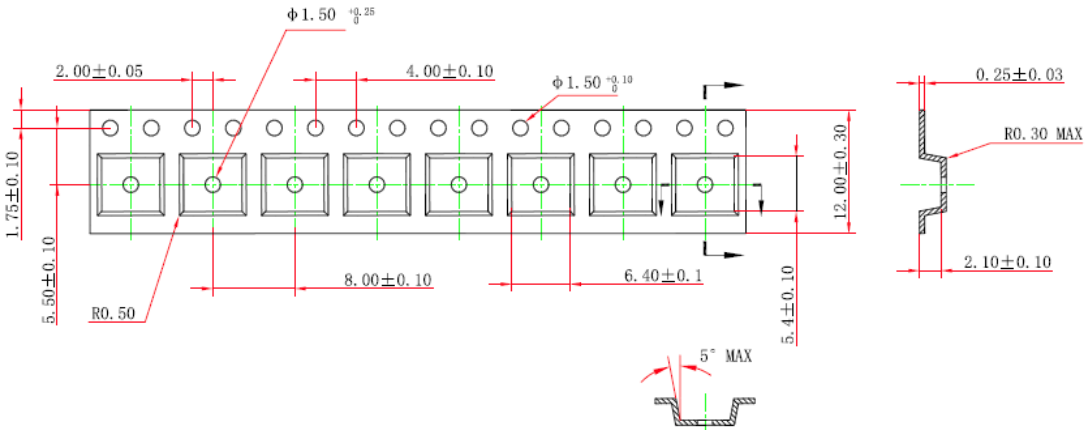
| SYMBOL | Unit: Millimeter | | |
|---|---|---|---|
| | MIN | TYP | MAX |
| A | 1.45 | --- | 1.75 |
| A1 | 0.1 | --- | 0.25 |
| A2 | 1.35 | --- | 1.55 |
| b | 0.33 | --- | 0.51 |
| c | 0.17 | --- | 0.25 |
| D | 4.7 | | 5.1 |
| E | 5.8 | | 6.2 |
| E1 | 3.8 | | 4.0 |
| e | 1.27BSC | | |
| L | 0.4 | | 1.27 |
| θ | 0° | | 8° |

**NOTE:**

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

## TAPE AND REEL INFORMATION

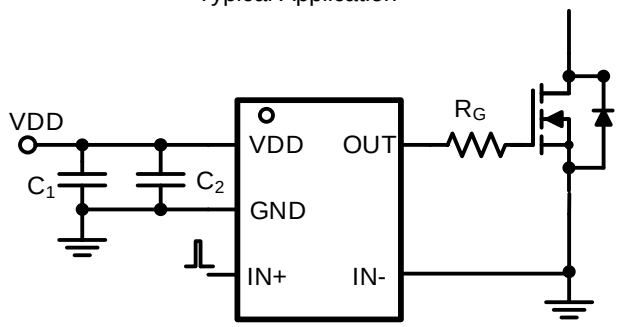


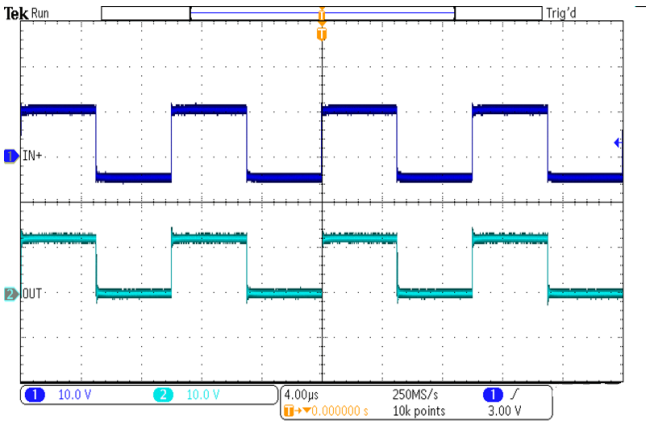

**Feeding Direction**

## TYPICAL APPLICATION

Single Channel, Non-Inverting MOSFET Gate Drive Typical Application




Typical Application Waveform




## RELATED PARTS

| PART NUMBERS | DESCRIPTION | COMMENTS |
|---|---|---|
| **SCT51240** | Up to 24V Supply, 4-A Single Channel High Speed Low Side Driver | • Compatible for both Inverting and Non-inverting application<br>• Supporting down to -5V input |

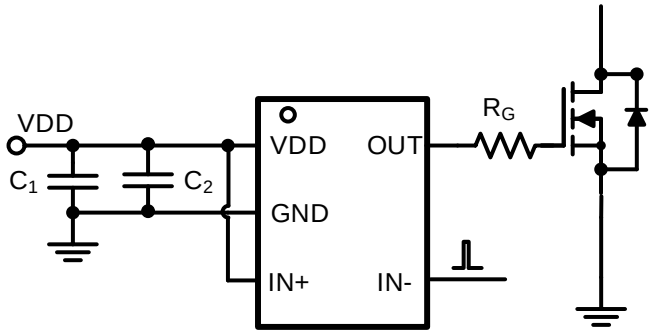



Figure 20. SCT51240 Inverting MOSFET Gate Drive Typical Application

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