SGM823
5-Pin Microprocessor Supervisory Circuit with Watchdog Timer and Manual Reset

GENERAL DESCRIPTION

The SGM823 microprocessor (μP) supervisory circuit combines reset output, watchdog, and manual reset input functions in SOT-23-5 package. It significantly improves system reliability and accuracy compared to separate ICs or discrete components. The SGM823 is specifically designed to ignore fast transients on V_{CC}.

Four preprogrammed reset threshold voltages are available. This device has an active-low reset output, which is guaranteed to be in the correct state for V_{CC} down to 1V. The SGM823 also offers a watchdog input and manual reset input.

The SGM823 is available in a Green SOT-23-5 package. It operates over an ambient temperature range of -40℃ to +125℃.

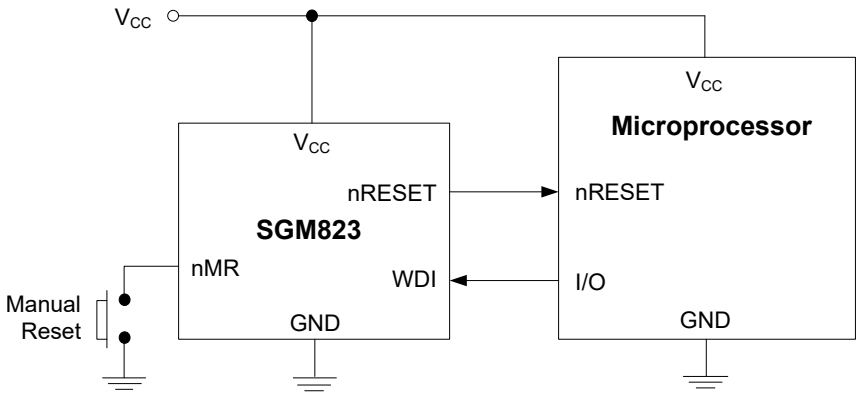
FEATURES

- **Ultra-Low Supply Current: < 1μA (TYP)**
- **Precision Supply-Voltage Monitor**
  - **4.63V for SGM823-L**
  - **3.08V for SGM823-T**
  - **2.93V for SGM823-S**
  - **2.63V for SGM823-R**
- **Guaranteed nRESET Valid at V_{CC} = 1V**
- **Fully Specified over Temperature**
- **200ms Reset Pulse Width**
- **Power-Supply Transient Immunity**
- **Watchdog Timer with 1.6s Timeout**
- **Debounced TTL/CMOS-Compatible**
- **Manual Reset Input**
- **No External Components**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOT-23-5 Package**

APPLICATIONS

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μP Power Monitoring

TYPICAL APPLICATION

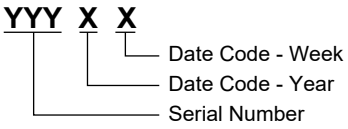


PACKAGE/ORDERING INFORMATION

MODEL	RESET THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM823	4.63	SOT-23-5	SGM823-LXN5G/TR	MNFXX	Tape and Reel, 3000
	3.08	SOT-23-5	SGM823-TXN5G/TR	MG6XX	Tape and Reel, 3000
	2.93	SOT-23-5	SGM823-SXN5G/TR	MG7XX	Tape and Reel, 3000
	2.63	SOT-23-5	SGM823-RXN5G/TR	MG8XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (With respect to GND)

V_{CC} ..... -0.3V to 6.0V

All Other Inputs ..... -0.3V to (V_{CC} + 0.3V)

Input Current

V_{CC} 20mA

GND 20mA

Output Current

All Outputs 20mA

Package Thermal Resistance

SOT-23-5, θ_{JA} ..... 234℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 4000V

MM 400V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

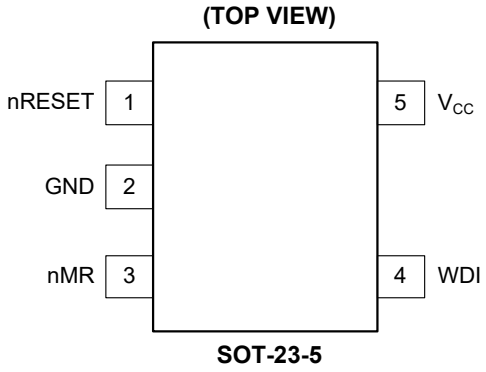
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

NAME	FUNCTION
nRESET	Active-Low Reset Output. Pulses low for 200ms when triggered, and remains low whenever V_{CC} is below the reset threshold or when nMR is logic low. It remains low for 200ms after one of the following occurs: V_{CC} rises above the reset threshold, the watchdog triggers a reset, or nMR goes from low to high.
GND	Ground. 0V ground reference for all signals.
nMR	Manual Reset Input Pin. A logic low on nMR asserts reset. Reset remains asserted as long as nMR is held low and for 200ms after nMR returns high. The active-low input has an internal 59kΩ pull-up resistor. It can be driven from a CMOS logic line or shorted to ground with a switch. Leave open or connect to V_{CC} if unused.
WDI	Watchdog Input Pin. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a reset is triggered. The internal watchdog timer clears whenever reset is asserted, or whenever WDI sees a rising or falling edge. If WDI is left unconnected or is connected to a three-stated buffer output, the watchdog feature is disabled.
V_{CC}	Supply Voltage.

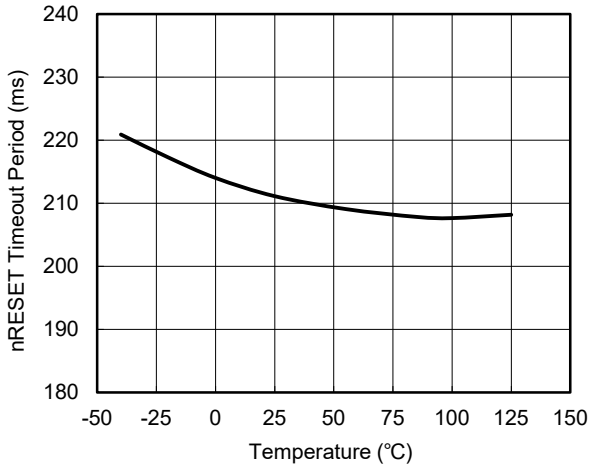
ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{CC} = 4.73V to 5.5V for SGM823-L, V_{CC} = 3.14V to 5.5V for SGM823-T, V_{CC} = 2.99V to 5.5V for SGM823-S, V_{CC} = 2.68V to 5.5V for SGM823-R, Full = -40℃ to +125℃, unless otherwise noted.)

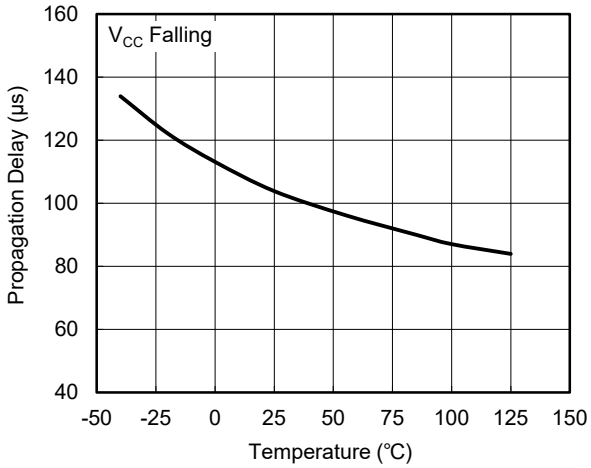
PARAMETER		CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Operating Voltage Range (V_{CC})			Full	1		5.5	V
Supply Current (I_{SUPPLY})		V_{CC} = 3.6V	Full		0.5	1.2	μA
		V_{CC} = 5.5V	Full		0.7	1.4	
nRESET Threshold (V_{nRST})		SGM823-L	+25℃	4.55	4.63	4.70	V
			Full	4.54	4.63	4.73	
		SGM823-T	+25℃	3.03	3.08	3.13	
			Full	3.02	3.08	3.14	
		SGM823-S	+25℃	2.88	2.93	2.98	
			Full	2.87	2.93	2.99	
		SGM823-R	+25℃	2.59	2.63	2.67	
			Full	2.58	2.63	2.68	
nRESET Threshold Hysteresis		SGM823-L	+25℃		20		mV
		SGM823-T	+25℃		14		
		SGM823-S	+25℃		13		
		SGM823-R	+25℃		12		
nRESET Threshold Temperature Coefficient			Full		20		ppm/℃
nRESET Pulse Width (t_{RP})			Full	140	200	290	ms
nRESET Output Voltage	V_{OH}	SGM823-L, V_{CC} = $V_{nRST(MAX)}$, I_{SOURCE} = 120μA	Full	V_{CC} - 1.5			V
		SGM823-T/S/R, V_{CC} = $V_{nRST(MAX)}$, I_{SOURCE} = 30μA	Full	0.8 × V_{CC}			
	V_{OL}	SGM823-L, V_{CC} = $V_{nRST(MIN)}$, I_{SINK} = 3.2mA	Full			0.4	
		SGM823-T/S/R, V_{CC} = $V_{nRST(MIN)}$, I_{SINK} = 1.2mA	Full			0.3	
		V_{CC} = 1V, V_{CC} falling, I_{SINK} = 50μA	Full			0.3	
nRESET Output Short-Circuit Current (I_{SOURCE})		SGM823-L, nRESET = 0V, V_{CC} = 5.5V	Full			460	μA
		SGM823-T/S/R, nRESET = 0V, V_{CC} = 3.6V	Full			430	
V_{CC} to Reset Delay (t_{RD})		V_{nRST} - V_{CC} = 100mV	+25℃		110		μs
Watchdog Timeout Period (t_{WD})			Full	1.1	1.6	2.4	sec
WDI Pulse Width (t_{WP})		V_{IL} = 0V, V_{IH} = V_{CC}	Full	90			ns
WDI Input Threshold	Low	V_{CC} = 5V	Full			0.8	V
	High	V_{CC} = 5V	Full	3.5			
	Low	$V_{nRST(MAX)}$ < V_{CC} < 3.6V	Full			0.8	
	High	$V_{nRST(MAX)}$ < V_{CC} < 3.6V	Full	0.7 × V_{CC}			
WDI Input Current		WDI = V_{CC}, time average	Full		0.02	0.5	μA
		WDI = 0V, time average	Full	-0.5	-0.01		
nMR Input Voltage	V_{IL}		Full			0.8	V
	V_{IH}		Full	2			
nMR Pulse Width (t_{MR})			Full	300			ns
nMR Noise Immunity (Pulse width with no reset)			+25℃		130		ns
nMR to nRESET Out Delay (t_{MD})			Full			470	ns
nMR Pull-Up Resistance (Internal)			Full	44	59	78	kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

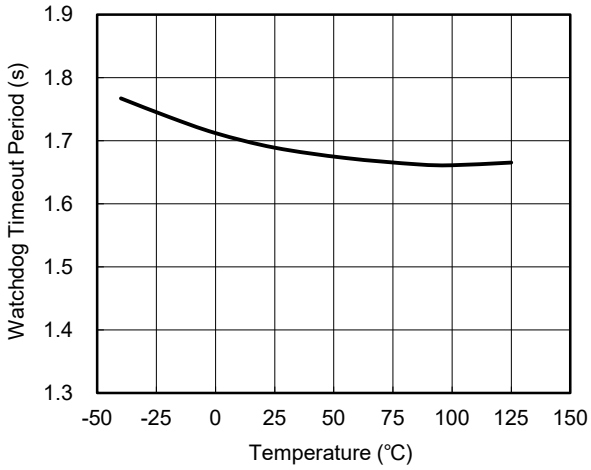
nRESET Timeout Period vs. Temperature



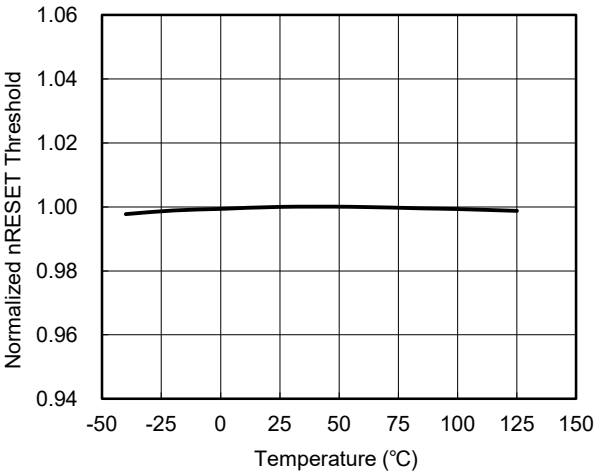
nRESET Comparator Propagation Delay vs. Temperature



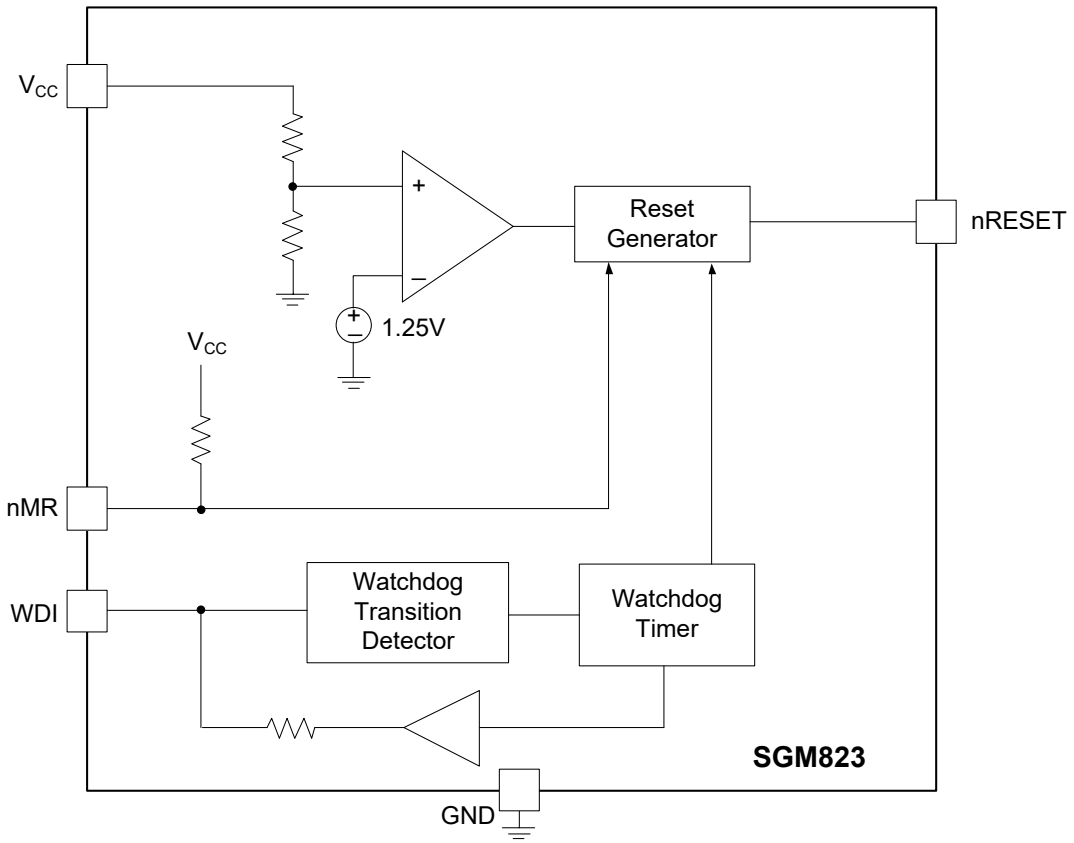
Watchdog Timeout Period vs. Temperature



Normalized nRESET Threshold Voltage vs. Temperature



FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

nRESET Output

A microprocessor's (μP's) reset input starts the μP in a known state. The SGM823 μP supervisory circuit asserts a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. nRESET is guaranteed to be a logic low for V_{CC} down to 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps nRESET low for the specified reset timeout period (t_{RP}); after this interval, nRESET returns high (Figure 1).

If a brownout condition occurs (V_{CC} dips below the reset threshold), nRESET goes low. Each time nRESET is asserted, it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold, the internal timer restarts. nRESET both sources and sinks current.

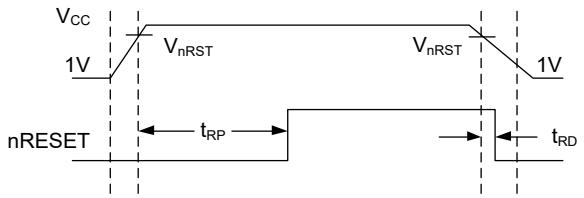


Figure 1. nRESET Timing Diagram

Manual Reset Input

Many μP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the SGM823, a logic low on nMR asserts reset. Reset remains asserted while nMR is low, and for t_{RP} (200ms nominal) after it returns high. nMR has an internal 59kΩ pull-up resistor, so it can be left open if not used. This input can be driven with CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from nMR to GND to create a manual reset function; external debounce circuitry is not required. If nMR is driven from long cables or the device is used in a noisy environment, connect a 0.1μF capacitor from nMR to GND to provide additional noise immunity.

Watchdog Input

On the SGM823, the watchdog circuit monitors the μP's activity. If the μP does not toggle the watchdog input (WDI) within t_{WD} (1.6s), reset asserts. The internal 1.6s timer is cleared by either a reset pulse or by toggling WDI, which detects pulses as short as 90ns. While reset is asserted, the timer remains cleared and does not count. As soon as reset is released, the timer starts counting (Figure 2).

Disable the watchdog function by leaving WDI unconnected or by three-stating the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period and high for the last 1/8 of the watchdog timeout period. When WDI is left unconnected, this internal driver clears the 1.6s timer every 1.4s. When WDI is three-stated or unconnected, the maximum allowable leakage current is 10μA and the maximum allowable load capacitance is 200pF.

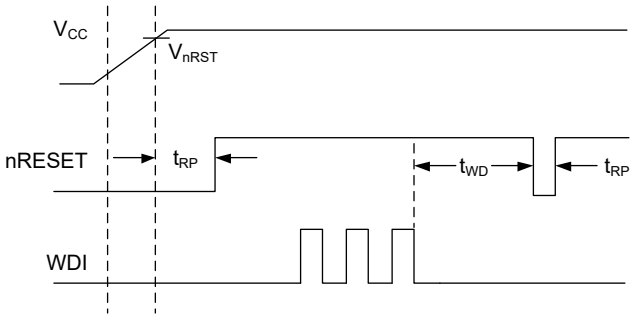


Figure 2. Watchdog Timing Relationship

APPLICATION INFORMATION

Interfacing to µPs with Bidirectional Reset Pins

The nRESET output maximum pull-up current is 460µA for L version (430µA for T/S/R versions). This allows µPs with bidirectional resets, such as the 68HC11, to force nRESET low when the SGM823 is pulling nRESET high (Figure 3).

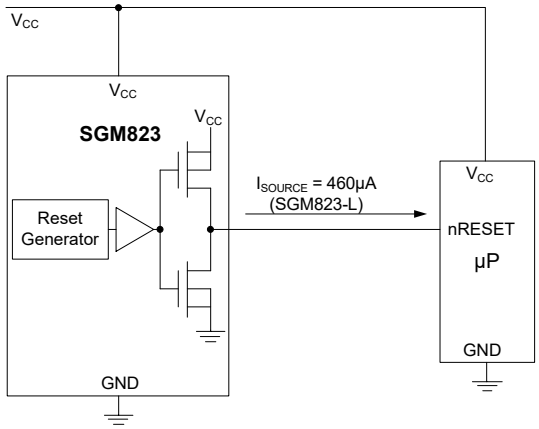


Figure 3. Interfacing to µP with Bidirectional Resets

Negative-Going V_{CC} Transients

This supervisor is relatively immune to short duration, negative-going V_{CC} transients (glitches), which usually do not require the entire system to shut down. Resets are issued to the µP during power-up, power down and brownout conditions.

An optional 0.1µF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

Watchdog Input Current

The SGM823 WDI is internally driven through a buffer and series resistor from the watchdog counter. When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within the first 7/8 of the watchdog timeout period to reset the watchdog timer.

Watchdog Software Considerations

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

Figure 4 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. As described in the Watchdog Input Current section, this scheme results in higher time average WDI input current than leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

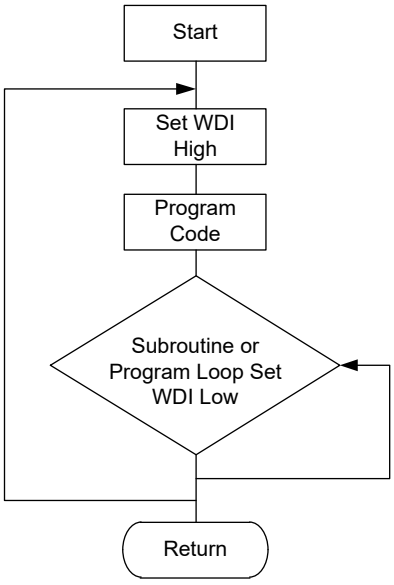


Figure 4. Watchdog Flow Diagram

REVISION HISTORY

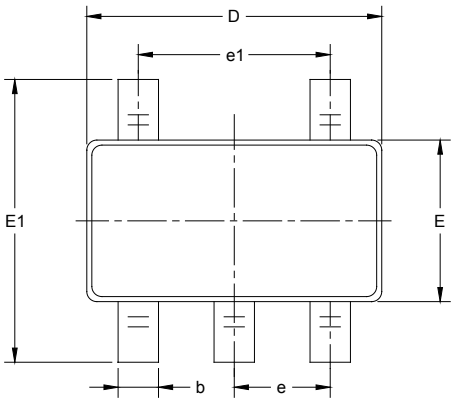
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

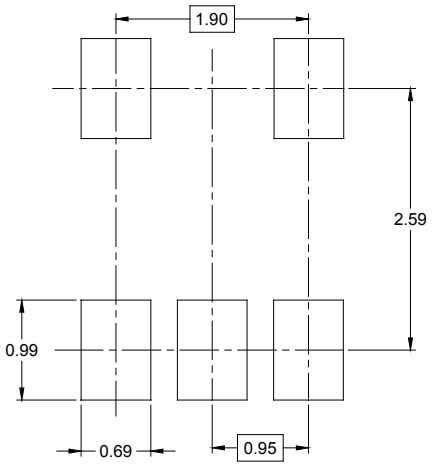
Changes from Original (DECEMBER 2018) to REV.A

Changed from product preview to production data ..... All

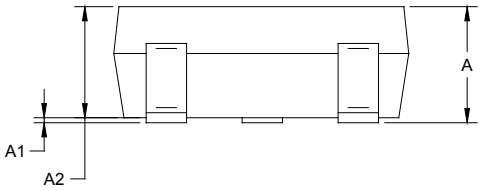
PACKAGE OUTLINE DIMENSIONS

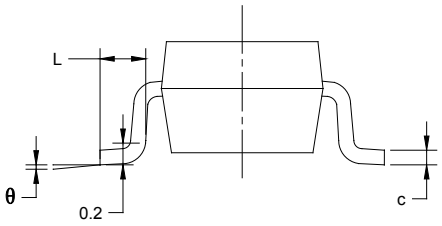
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)

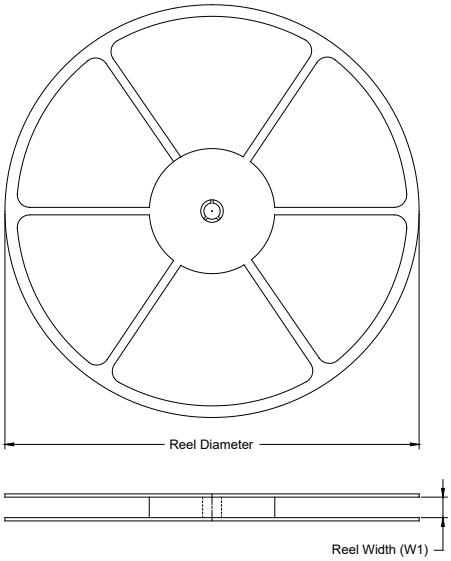




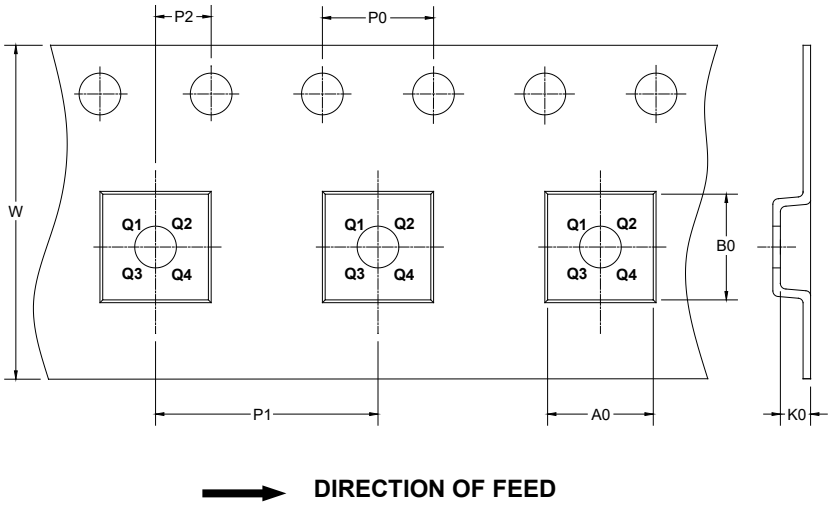
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

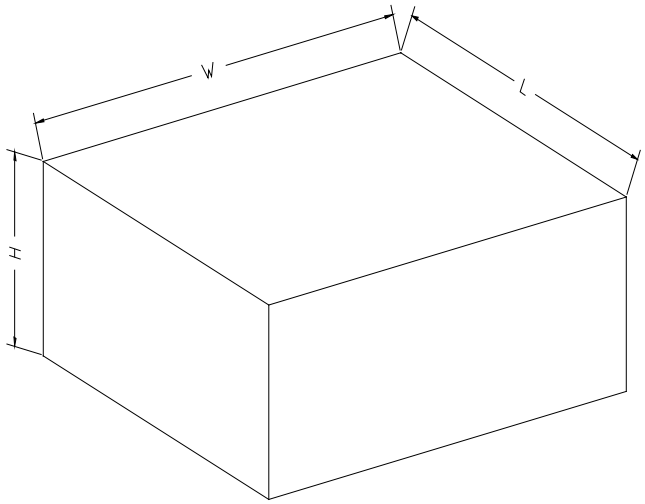
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002