SGM61020
2A High Efficiency Synchronous Step-Down Converter

GENERAL DESCRIPTION

The SGM61020 is a high efficiency synchronous step-down DC/DC converter with 2A output current capability and adjustable output voltage. The input supply voltage is in the range of 2.5V to 5.5V. Using adaptive off-time peak current control, the efficiency of this device is higher than 80% for loads over 1mA and reaches 95% in the moderate load ranges (5V to 3.3V).

This device operates with a quasi-fixed 1.5MHz pulse width modulation (PWM) mode for moderate or heavy loads. But at light loads, pulse skip modulation is used for power-save mode (PSM). The PSM operating quiescent current is very low, typically 42μA, which is well suitable for battery powered applications to prolong battery life. Despite such low quiescent current, the transient response to large load variations is excellent. The device shutdown current is typically 0.02μA.

The SGM61020 provides an adjustable output voltage by an external resistor divider. The device is capable for low dropout operation with 100% duty cycle. Some other features include internal soft-start for limiting startup inrush current, over-current and thermal shutdown protections, enable input and power good output (for P version only).

The SGM61020 is available in Green SOT-23-5 and SOT-563-6 packages and can operate in the -40℃ to +125℃ ambient temperature range.

FEATURES

- **2.5V to 5.5V Input Voltage Range**
- **Adjustable Output Voltage from 0.6V to V_{IN}**
- **Up to 95% Efficiency**
- **Low R_{DSON} Switches (102mΩ/57mΩ)**
- **Power-Save Mode for Light Load Efficiency**
- **42μA (TYP) Operating Quiescent Current**
- **100% Duty Cycle for Low Dropout Operation**
- **1.5MHz PWM Switching Frequency**
- **Power Good Output (SGM61020P Only)**
- **Over-Current Protection**
- **Thermal Shutdown Protection**
- **Input Under-Voltage Lockout (UVLO) Protection**
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM61020: Available in Green SOT-23-5 and SOT-563-6 Packages
  SGM61020P: Available in a Green SOT-563-6 Package

APPLICATIONS

General Purpose POL Supply
Set-Top Box
Network Video Camera
Wireless Router
Hard Disk Driver

TYPICAL APPLICATION

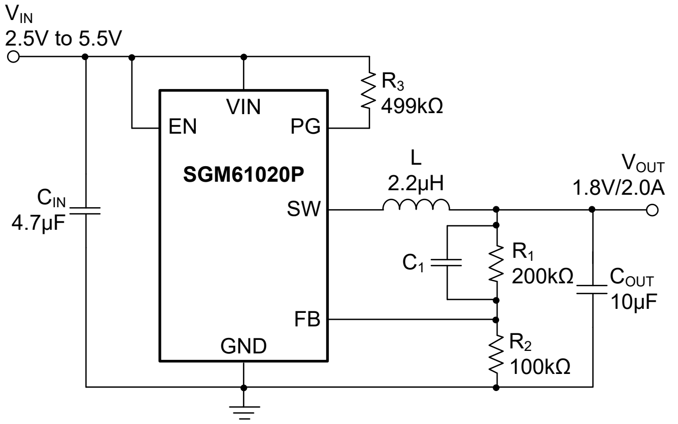


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61020	SOT-23-5	-40℃ to +125℃	SGM61020XN5G/TR	RAAXX	Tape and Reel, 3000
	SOT-563-6	-40℃ to +125℃	SGM61020XKB6G/TR	ZMXX	Tape and Reel, 5000
SGM61020P	SOT-563-6	-40℃ to +125℃	SGM61020PXKB6G/TR	ZNXX	Tape and Reel, 5000

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

MARKING INFORMATION

SOT-23-5

(1) XX = Date Code.

YYY X X
- X: Date Code - Week
- X: Date Code - Year
- YYY: Serial Number

SOT-563-6

(2) XX = Date Code.

YY X X
- X: Date Code - Week
- X: Date Code - Year
- YY: Serial Number

ABSOLUTE MAXIMUM RATINGS

Voltage Range [1]

VIN, EN, PG.. -0.3V to 6V

SW (DC) ....-0.3V to V_{IN} + 0.3V

SW (AC, less than 10ns) [2]..................................... -2V to 9V

FB .... -0.3V to 5.5V

Package Thermal Resistance

SOT-23-5, θ_{JA} .... 193℃/W

SOT-563-6, θ_{JA} .... 170℃/W

Junction Temperature ....+150℃

Storage Temperature Range........................-65℃ to +150℃

Lead Temperature (Soldering, 10s) ....+260℃

NOTES:
1. All voltage values are with respect to the ground terminal.
2. While switching.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN}....................................2.5V to 5.5V

Output Voltage Range, V_{OUT} .... 0.6V to V_{IN}

Output Current Range, I_{OUT} ....0 to 2A

Sink Current at PG Pin, I_{SINK_PG} 1mA

Operating Ambient Temperature Range......-40℃ to +125℃

Operating Junction Temperature Range......-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

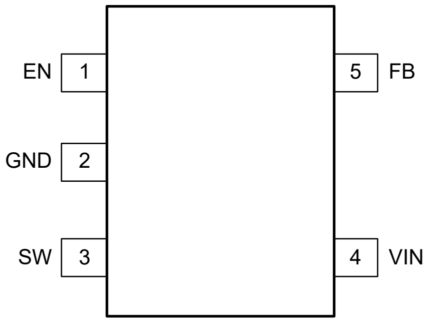
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

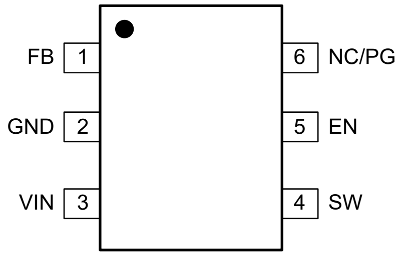
PIN CONFIGURATIONS

SGM61020 (TOP VIEW)



SOT-23-5

SGM61020/SGM61020P (TOP VIEW)



SOT-563-6

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
SOT-23-5	SOT-563-6			
1	5	EN	I	Active High Enable Input. Apply a logic low to shut down the device or pull EN up to VIN to enable it. Do not leave EN floating.
2	2	GND	G	Ground Pin.
3	4	SW	O	Switching Node Output Pin. Connect to the filter inductor.
4	3	VIN	P	Power Supply Input. Decouple VIN with at least 4.7μF ceramic capacitor to GND, close to the device. (If the input voltage oscillates, the input capacitance can be increased.)
5	1	FB	I	Feedback Input. Use a resistor divider to feedback the output voltage to this pin and set the voltage.
—	6	NC	—	No Connection. This pin can be left open or connected to GND.
		PG	O	Open-Drain Power Good Output (SGM61020P Only). Pull it up with a resistor to a positive voltage no more than 5.5V. It can be left open if unused.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

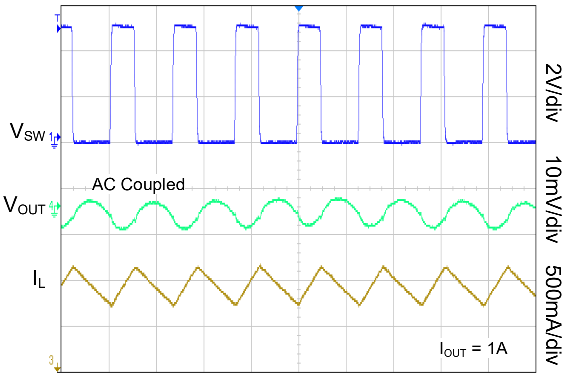
(V_{IN} = 5.0V, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Quiescent Current into VIN Pin	I_Q	Not switching		42		μA
Shutdown Current into VIN Pin	I_{SD}	EN = 0V		0.02		μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling		2.3		V
Under-Voltage Lockout Hysteresis	V_{HYS}			100		mV
Thermal Shutdown	T_{JSD}	Junction temperature rising		150		℃
		Junction temperature falling		130		
Logic Interface						
High-Level Threshold at EN Pin	V_{IH}	2.5V ≤ V_{IN} ≤ 5.5V		0.98		V
Low-Level Threshold at EN Pin	V_{IL}	2.5V ≤ V_{IN} ≤ 5.5V		0.85		V
Soft Startup Time	t_{SS}	SGM61020 SOT-23-5 package		800		μs
		SGM61020/P SOT-563-6 package		800		
Output						
Feedback Regulation Voltage	V_{FB}			0.6		V
High-side FET On-Resistance	R_{DSON}			102		mΩ
Low-side FET On-Resistance				57		
High-side FET Current Limit	I_{LIM}	SGM61020 SOT-23-5 package		3.2		A
		SGM61020/P SOT-563-6 package		3.2		
Switching Frequency	f_{SW}	V_{OUT} = 2.5V		1.5		MHz
SGM61020P Only						
Power Good Threshold	V_{PG}	V_{FB} rising, referenced to V_{FB} nominal		95% × V_{REF}		V
		V_{FB} falling, referenced to V_{FB} nominal		90% × V_{REF}		
Power Good Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA		0.1		V
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V		0.01		μA
Power Good Delay Time	t_{PG_DLY}	V_{FB} falling		43		μs

TYPICAL PERFORMANCE CHARACTERISTICS

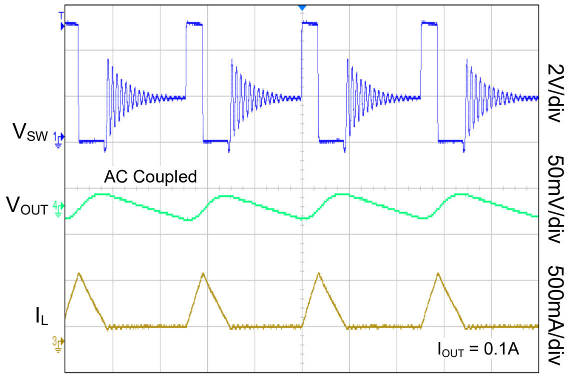
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, unless otherwise noted.

PWM Operation



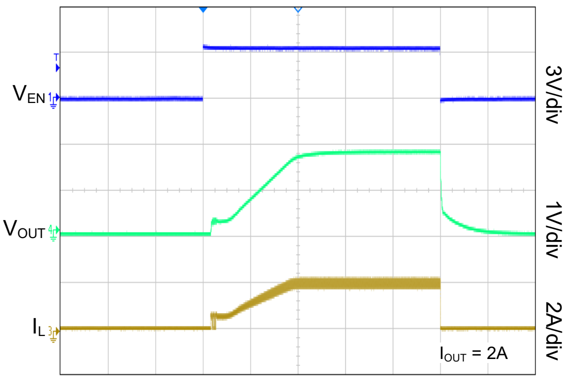
Time (500ns/div)

Power-Save Mode Operation



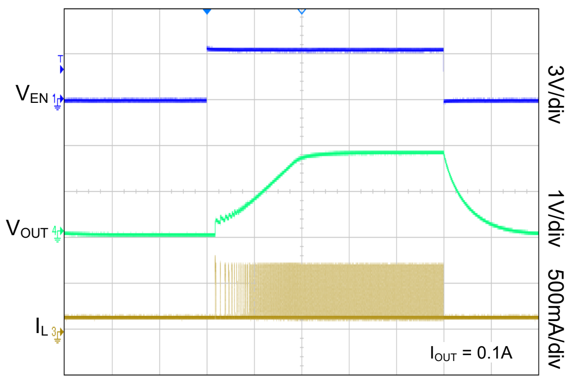
Time (1μs/div)

Startup and Shutdown with Load



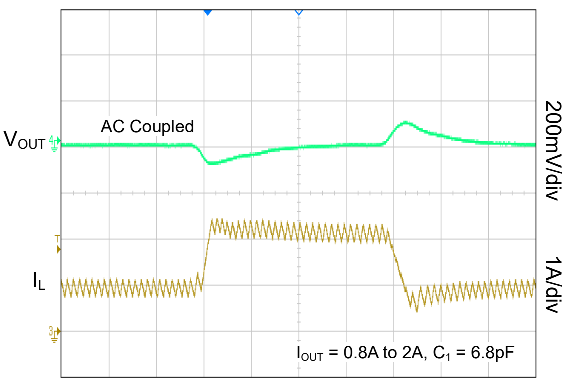
Time (500μs/div)

Startup and Shutdown with Load



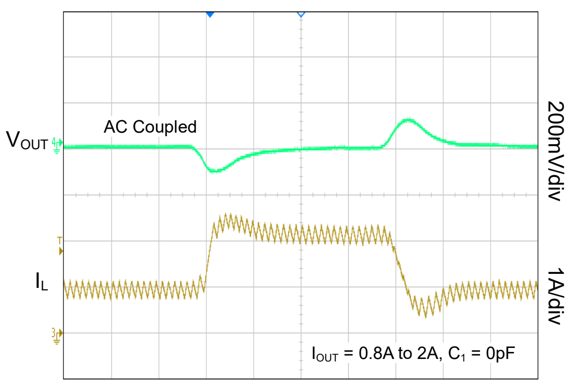
Time (500μs/div)

Load Transient



Time (5μs/div)

Load Transient

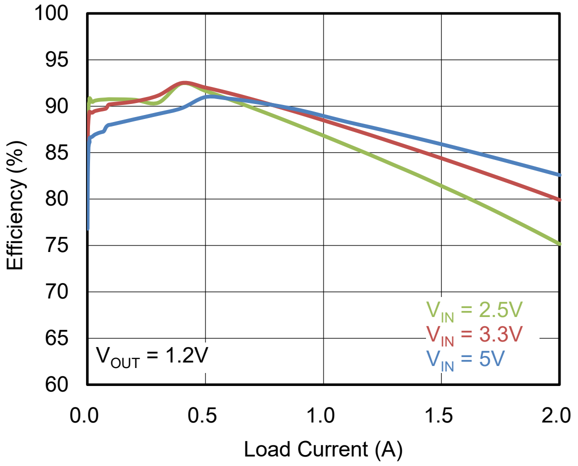


Time (5μs/div)

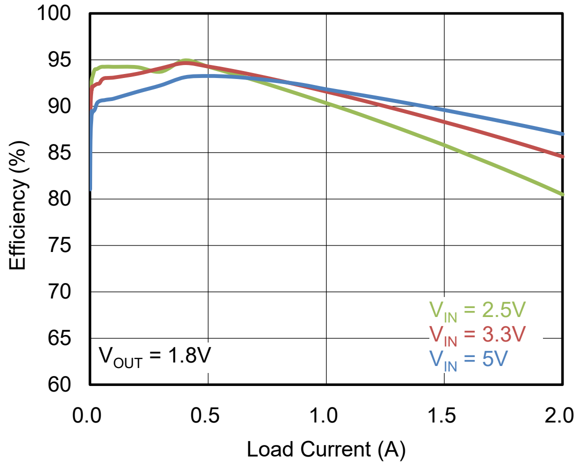
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, unless otherwise noted.

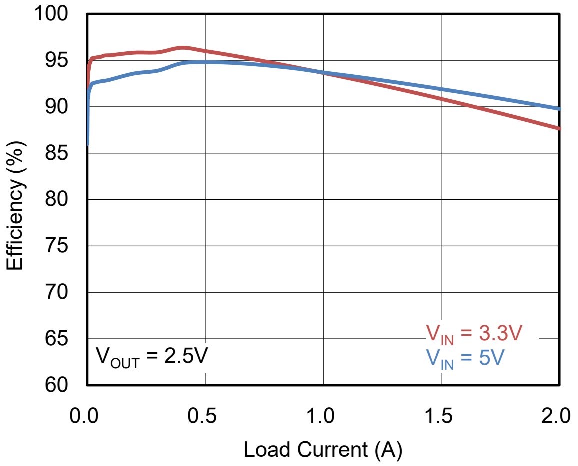
Efficiency vs. Load Current



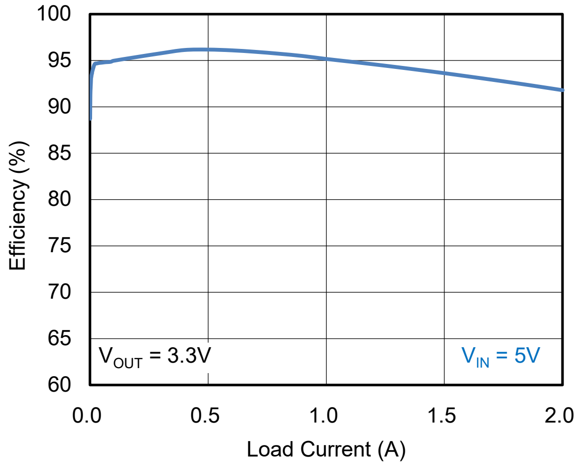
Efficiency vs. Load Current



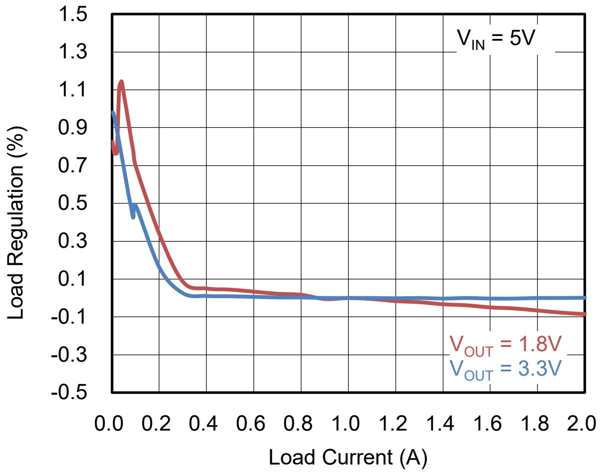
Efficiency vs. Load Current



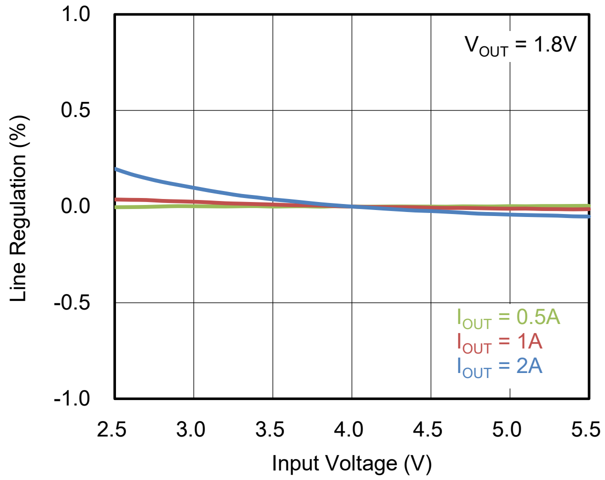
Efficiency vs. Load Current



Load Regulation

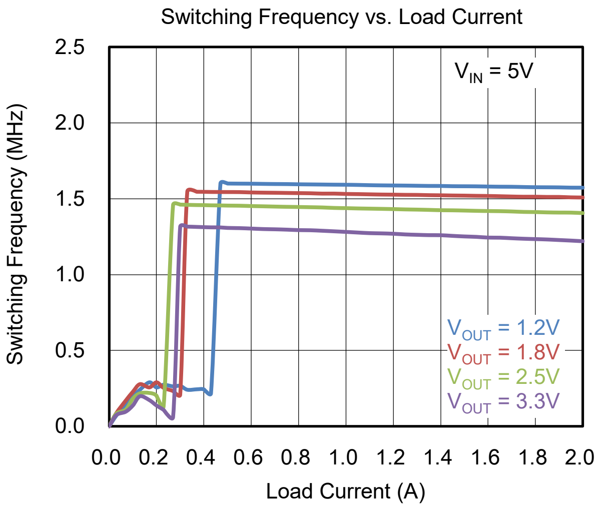


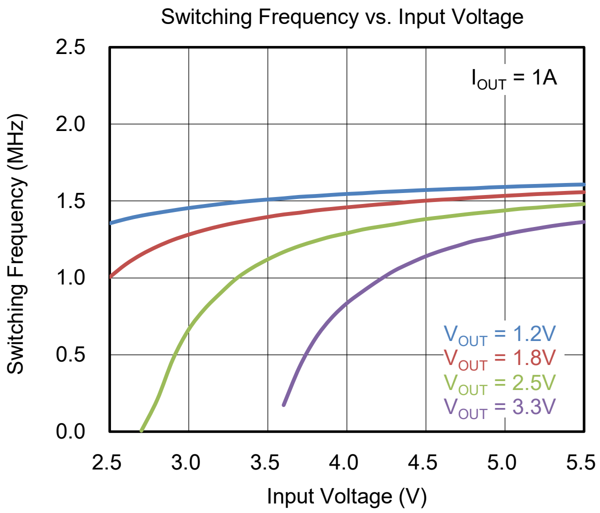
Line Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, unless otherwise noted.





FUNCTIONAL BLOCK DIAGRAM

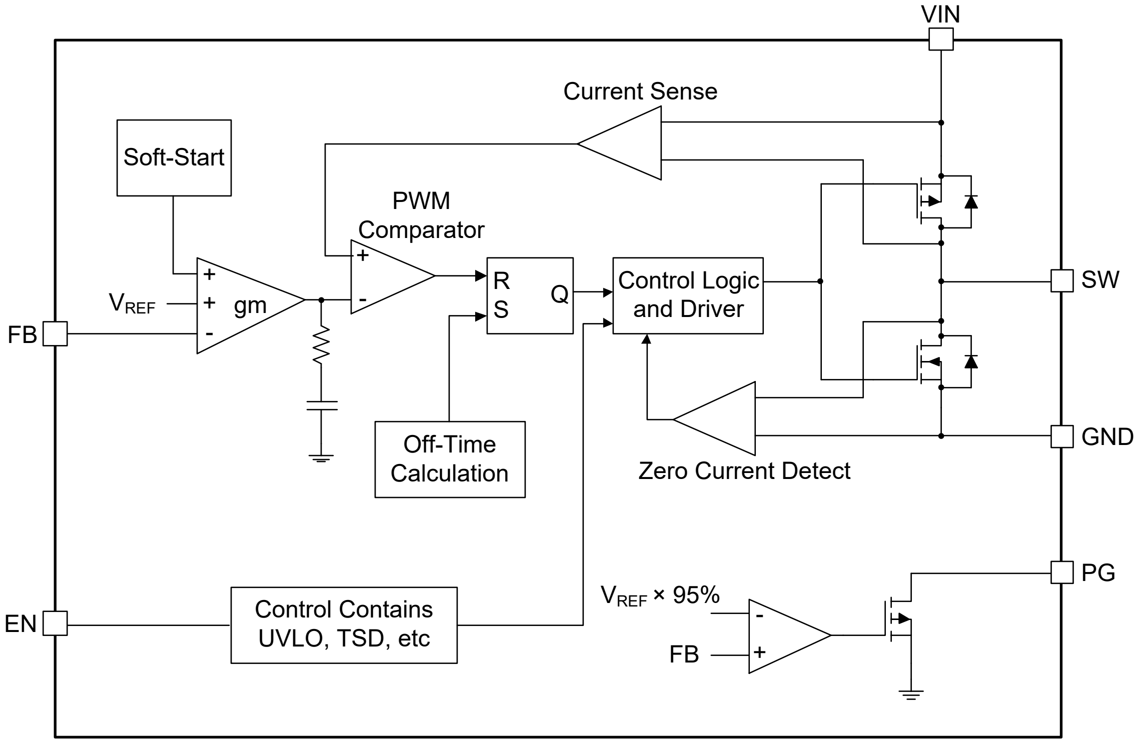


Figure 2. SGM61020/SGM61020P Block Diagram

DETAILED DESCRIPTION

The SGM61020 is a high efficiency step-down switching regulator optimized for handheld battery-powered applications. It operates at a quasi-fixed frequency of 1.5MHz and uses adaptive off-time PWM control for the moderate to heavy load range. This allows using a small inductor and small capacitors for compact designs. At light load condition, this device operates in power-save mode (PSM) to reduce the switching frequency and losses for longer battery life. The PSM quiescent current is typically 42μA while the shutdown current is only 0.02μA (TYP).

Power-Save Mode (PSM)

At light load condition, the SGM61020 shifts to the PSM mode and operates with pulse skip modulation to reduce the switching frequency and minimize the losses. It also shuts down most of the internal circuits in PSM. In this mode, one or more PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal again and the switches will turn off. In power-save mode, the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Low Dropout Operation (100% Duty Cycle)

When the input voltage reduces, the on-time increases. When the input voltage is lower than the regulation output voltage, the output voltage drops, and the SGM61020 goes into 100% duty cycle mode. The high-side switch is always on, and the output voltage is determined by the load current times the R_{DSON} composed by the high-side switch and inductor.

DETAILED DESCRIPTION (continued)

Soft Startup

An 800μs internal soft-start circuit is included to prevent input inrush current and voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage (V_{REF} = 0.6V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61020 is also capable of starting with a pre-biased output capacitor when it is powering up or enabled. When the device is turning on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device may not be able to startup properly. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value.

Current Limit Protection

The SGM61020 uses the peak current mode control by sensing the current of the high-side switch. At the beginning of each cycle, the high-side switch is turned on. If the converter is overloaded or a short occurs on the output, the inductor current sensed by the high-side switch exceeds the maximum current limit threshold. Under this condition, the high-side switch is turned off and the on-time is ended to avoid damage. The shortened on-time will result in reduced output voltage.

Note that the measured peak current limit in the closed-loop and open-loop (I_{LIM_OL}) test conditions is slightly different, mainly due to the current comparator propagation delay.

Under-Voltage Lockout Protection

When the input voltage is below the UVLO threshold (2.3V, TYP), the device is shut down. If the input voltage rises above the UVLO threshold plus hysteresis, the IC will restart.

Thermal Shutdown Protection

A thermal shutdown function is implemented to prevent damage caused by excessive heat and power dissipation. Once the junction temperature exceeds +150°C, the device is shut down. The device is released from shutdown automatically when the junction temperature decreases by 20℃.

Enable Input

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn it off. Connect the EN pin directly to a voltage source that can't be higher than the VIN pin. The EN input should not be left floating.

Power Good Output (SGM61020P Only)

The PG pin is an open-drain output. PG requires a pull-up resistor (e.g. 499kΩ). PG pin is pulled to GND before the output voltage is above 95% of the nominal voltage. After FB voltage reaches 95% of V_{REF}, the PG pin is pulled high immediately. When the FB voltage drops below 90% of V_{REF}, the PG pin will be pulled low after a 43μs delay. Leave the PG pin unconnected when not used.

Table 1. PG Output Logic

Device Conditions		Logic Status	
		High Z	Low
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_A > T_{JSD}$		√
UVLO	$0.53V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 0.53V$	√	

APPLICATION INFORMATION

An application circuit schematic of the SGM61020P with adjustable output is provided in Figure 3.

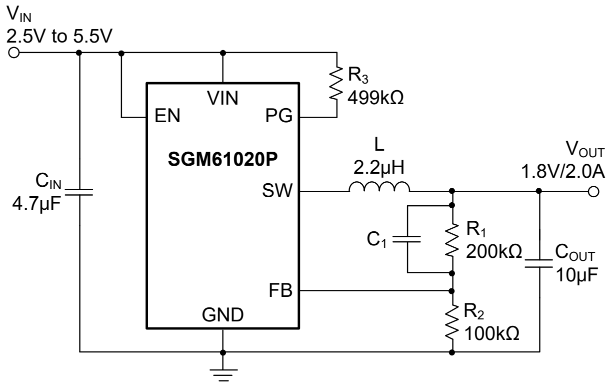


Figure 3. SGM61020P Application Example with 1.8V/2.0A Output

Output Voltage Setting

A resistor divider network (R_1 and R_2 in Figure 3) can be used to set the SGM61020 output voltage based on the Equation 1. Use a 100kΩ resistor for R_2 to compromise between the quiescent current and the bias error/noise immunity of the FB pin.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

When V_{IN} decreases to near V_{OUT} value, the switching frequency is decreased and the duty cycle is increased until it reaches 100%.

A feedforward capacitor can be placed in parallel with R_1 to improve the bandwidth and achieve faster transient response and reduce the V_{OUT} ripple in PSM.

Output Capacitor Design

For the SGM61020, the output capacitance is generally designed to limit the output voltage ripple below the required level. C_{OUT} also reduces the voltage transients when fast load changes occur. The inductor ripple current that is absorbed by C_{OUT} is determined by L, V_{OUT} and V_{IN}. The output voltage ripple is determined by the interaction of inductor current ripple with the capacitor impedance including its capacitance (C_{OUT}), ESR and ESL values.

During a load transient, the output capacitor provides or absorbs the extra load current alone that results in a droop or quick rise in its voltage, until the loop can respond, and the inductor average current reaches the new load level. The C_{OUT} capacitance determines the transient magnitude.

Note that high ripple current in the capacitor ESR can cause high temperature due to power dissipation in the capacitor. High operating temperature shortens the capacitor lifetime. Therefore, the maximum allowed ripple current in the capacitor that depends on the ambient temperature must not be exceeded.

Low ESL capacitors can be chosen if ringing in the low megahertz region is seen. Limiting the trace lengths on the PCB or replacing large capacitors with several smaller parallel ones can also help.

To have small output ripple and stable regulation loop, use low-ESR X5R or X7R ceramic capacitors with high ripple current ratings.

The output ripple caused by limited C_{OUT} capacitance and its parasitic ESR can be calculated from Equation 2:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (2)$$

Inductor Design and Selection

In most cases, a 1μH to 2.2μH inductor works well for the SGM61020. Typically, a lower value inductor has a smaller physical size but may result in higher loss due to higher switching frequency required (the lower DCR may compensate for that at heavy loads). For a required ripple (ΔI_L), the inductor can be chosen based on Equation 3:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (3)$$

Typically, the ΔI_L is chosen around 30% of the maximum load current that is ΔI_L = 600mA for 2A rated load. For higher output voltage settings (above 2.0V), the minimum recommended inductor is 2.2μH for good light-load efficiency.

APPLICATION INFORMATION (continued)

Inductor manufacturers usually provide thermal current rating (RMS) and saturation current rating (DC or peak). Choose the DC current rating above the ($I_{LOAD,MAX}$ + $\Delta I_L/2$) × 1.2 to avoid saturation.

The inductor DCR is also an important factor for efficiency and loss consideration. For better efficiency, we suggest to choose the DCR of the inductor as small as possible.

Input Capacitor Design

The input capacitor provides the converter pulsating and high frequency input currents, and decouples them from the input line. The C_{IN} impedance at the switching frequency should be very low and less than the source impedance to filter the switching currents and prevent them from flowing in the input source. The input voltage ripple must be small for proper regulation and stability. The following Equation 4 can be used to calculate C_{IN} based on the required peak-to-peak input ripple (V_{PP}).

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_{LOAD}} - ESR\right) \times f_{SW}} \quad (4)$$

The worst-case, ripple occurs when the duty cycle is near to 50% (V_{OUT}/V_{IN} ≈ 0.5). Use Equation 5 to calculate C_{IN}:

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_{LOAD}} - ESR\right) \times 4 \times f_{SW}} \quad (5)$$

Use at least a 4.7μF low-ESR X5R or X7R ceramic capacitor for C_{IN}. A 22μF capacitor works well for most applications but for better filtering, a larger capacitor can be used. Consider the capacitor rated RMS current for the design. The C_{IN} RMS current is given by Equation 6:

$$I_{RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

In worst case, I_{RMS} is equal to 1/2 of the load DC current:

$$I_{RMS(MAX)} = \frac{1}{2} \times I_{LOAD} \quad (7)$$

Note that using long test leads for powering the converter on a lab bench can cause stability issues such as excessive ringing in the output during load transients. It is due to the large inductance of such wires that along with the low-ESR ceramic input capacitors create a high-Q network. Moreover, it can cause errors in loop phase and gain measurements. It is not the case in normal applications with short PCB traces feeding the input. However, if in an application the input inductance cannot be reduced, a high-ESR tantalum or aluminum electrolytic capacitor must be used in parallel with the low-ESR ceramic capacitors to stabilize the system by added the damping to the high-Q network.

Thermal Considerations

The SGM61020 internal losses consist of switching losses, conduction losses, and quiescent current losses. Conduction losses are caused by the R_{DSON} of the switches. The external conduction losses caused by the inductor DCR and voltage drops on the power connectors may also increase the heat dissipation. Switching losses are mainly due to the switches gate charges. A simplified device loss equation at full load assuming continuous conduction mode (CCM) operation is given by Equation 8:

$$P_{TOTAL} = \frac{I_{LOAD}^2 \times [R_{DSON\_HS} \times V_{OUT} + R_{DSON\_LS} \times (V_{IN} - V_{OUT})]}{V_{IN}} + (t_{SW} \times f_{SW} \times I_{LOAD} + I_Q) \times V_{IN} \quad (8)$$

where I_Q is the quiescent current and the t_{SW} (the rising or falling edge of the SW node) parameter is used to estimate the full load converter switching losses.

When the device is operating at 100% duty cycle, the total device loss reduces to:

$$P_{TOTAL} = I_{LOAD}^2 \times R_{DSON\_HS} + I_Q \times V_{IN} \quad (9)$$

Since R_{DSON}, I_Q and switching losses vary with input voltage, the total losses should be investigated over the complete input voltage range.

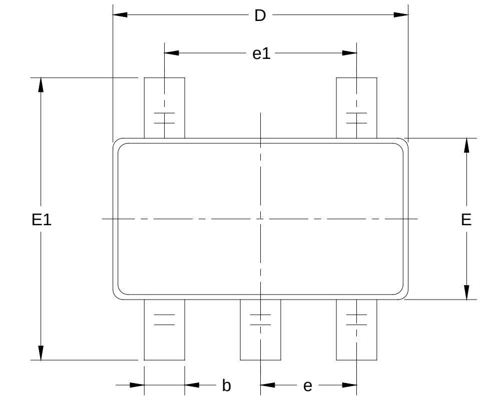
Layout Considerations

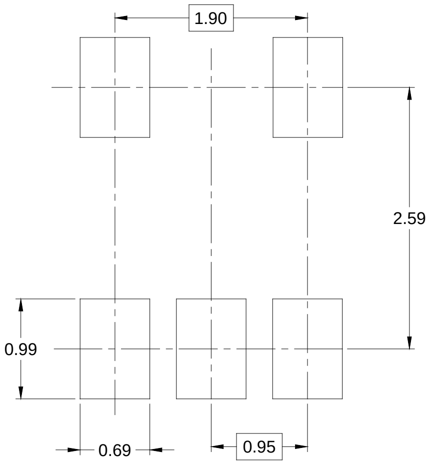
Some important PCB layout design considerations for the SGM61020 are listed below:

- Place the low-ESR input/output capacitors and the inductor as close as possible to the device with short, wide and direct traces on the same layer.
- Connect the GND terminal of the input and output capacitors together and to the device GND pin and the GND power plane in one point.
- Keep the FB feedback traces away from noisy elements or traces such as the SW node.
- Use GND layers under the device, switching traces and inductor for better shielding.

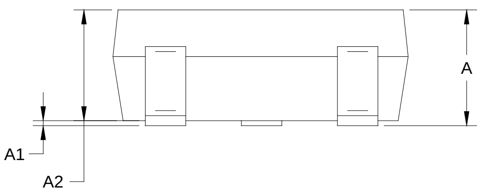
PACKAGE OUTLINE DIMENSIONS

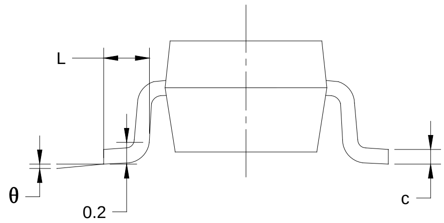
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



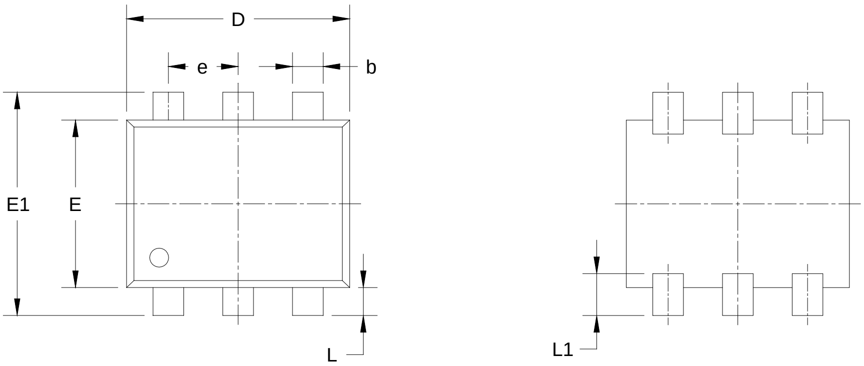


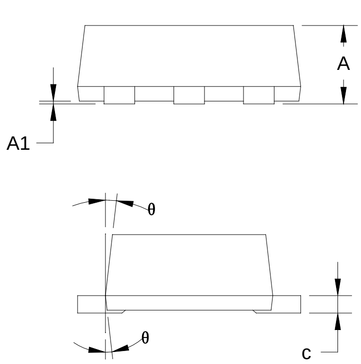
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

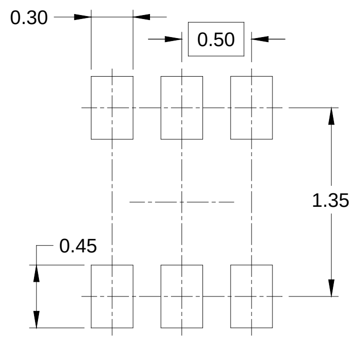
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

SOT-563-6







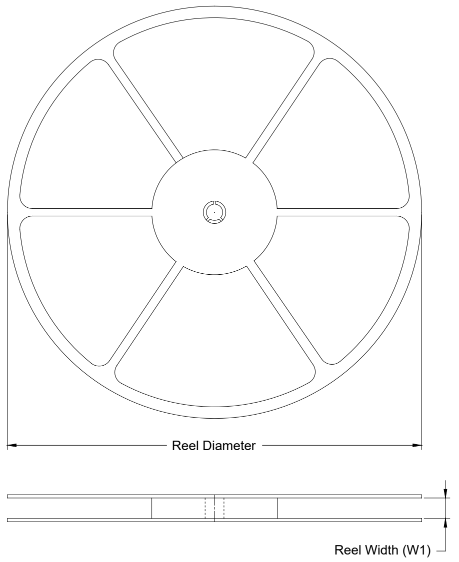
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	**MAX**	**MIN**	**MAX**
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.180	0.004	0.007
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
e	0.450	0.550	0.018	0.022
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016
θ	9° REF		9° REF	

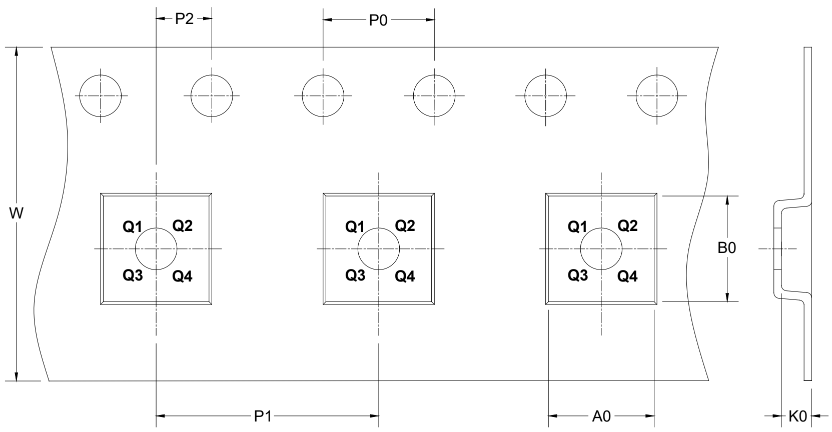
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

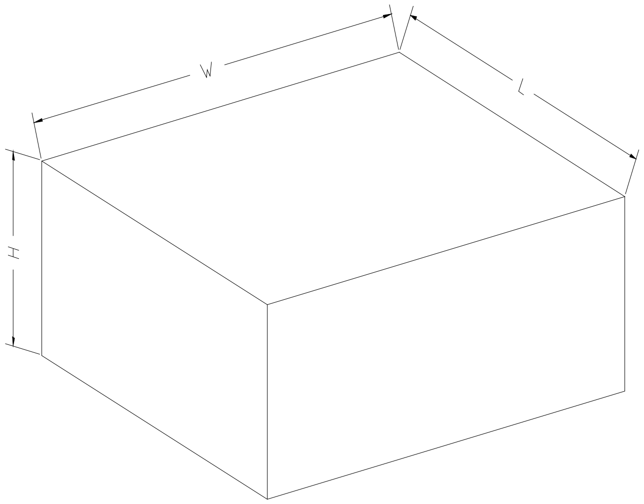
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOT-563-6	7″	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002