White LED Driver With Digital and PWM Brightness Control

■ General Description

With a 40-V rated integrated switch FET, the OCP8178 is a boost converter that drives LEDs in series. The boost converter runs at 600kHz fixed switching frequency to reduce output ripple, improve conversion efficiency, and allows for the use of small external components.

The default white LED current is set with the external sensor resistor Rset, and the feedback voltage is regulated to 200mV, as shown in the typical application. During the operation, the LED current can be controlled using the 1-wire digital interface through the CTRL pin. Alternatively, a pulse width modulation (PWM) signal can be applied to the CTRL pin through which the duty cycle determines the feedback reference voltage. In either digital or PWM mode, the OCP8178 does not burst the LED current; therefore, it does not generate audible noises on the output capacitor. For maximum protection, the device features integrated open LED protection that disables the OCP8178 to prevent the output voltage from exceeding the IC's absolute maximum voltage ratings during open LED conditions.

The OCP8178 is available in a space-saving, 2mm × 2mm DFN package with thermal pad.

● Features

- 2.7V to 5.5V Input Voltage Range
- 38V Open LED Protection
- 200mV Reference Voltage
- Flexible Digital and PWM Brightness Control
- Built-in Soft Start
- Up to 90% Efficiency
- 2mm × 2mm × 0.8mm DNF2X2-6L(6-pinDFN) Package With Thermal Pad

● Applications

- Cellular Phones
- Portable Media Players
- Ultra Mobile Devices
- GPS Receivers
- White LED Backlighting for Media Form Factor Display

■ Pin Configuration

DFN2X2-6L

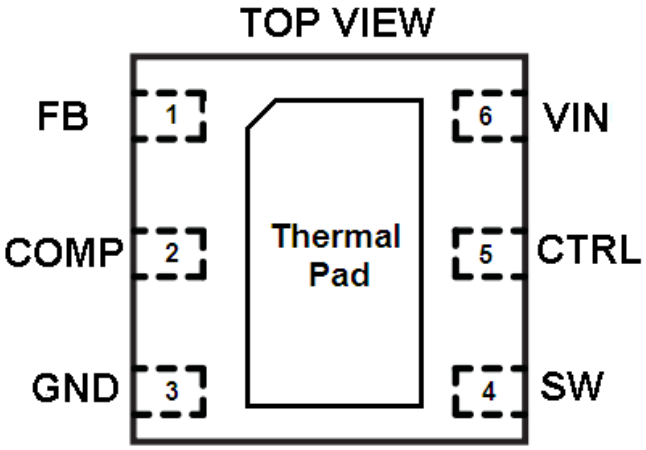


Figure 1, Pin Assignments of OCP8178

Pin Name	Pin No. DFN-6pins	I/O	Pin Function
VIN	6	I	The input supply pin for the IC. Connect VIN to a supply voltage between 2.7V and 5.5V.
SW	4	O	This is the switching node of the IC. Connect the inductor between the VIN and SW pin. This pin is also used to sense the output voltage for open LED protection
GND	3	I	Ground
FB	1	I	Feedback pin for current. Connect the sense resistor from FB to GND.
COMP	2	O	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the converter.
CTRL	5	I	Control pin of the boost converter. It is a multi-functional pin which can be used for enable control, PWM and digital dimming.
Thermal Pad			The thermal pad should be soldered to the analog ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation.

■ Typical Application Circuit

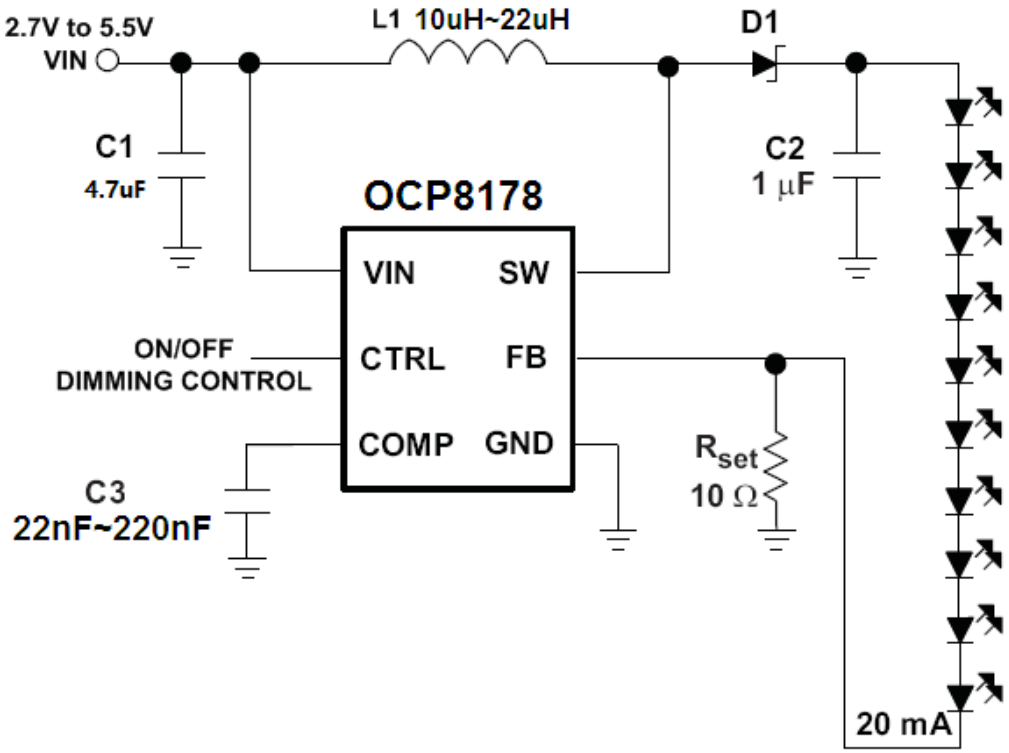


Figure 2, Typical Application Circuit of OCP8178

■ Block Diagram

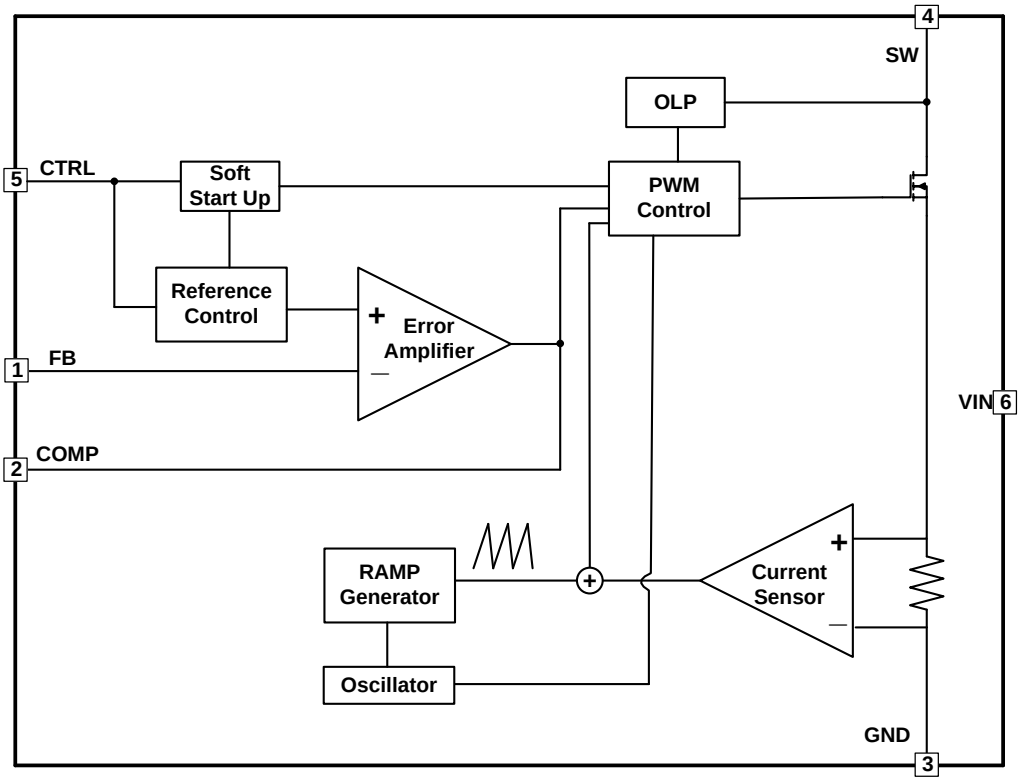


Figure 3, Block Diagram of OCP8178

■ Absolute Maximum Ratings (T_A=25°C, unless otherwise noted)

Parameter	Symbol	Rating	Unit
Supply Voltages on VIN	V_I	-0.3 to 6	V
V_{SW} Pin to GND	V_{SW}	-0.3 to 40	V
All Other Pins to GND		-0.3 to 6	V
Operating Junction Temperature Range	T_J	–40 to 150	℃
Storage Temperature Range	T_{STG}	–65 to 150	℃
Maximum Soldering Temperature (at leads, 10 sec)	T_{LEAD}	300	℃

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Input voltage range	V_{IN}	2.7 to 5.5	V
Output voltage range	V_{SW}	V_{IN} to 38	V
Inductor	L1	10 to 22	uH
PWM dimming frequency	f_{dim}	5 to 100	kHZ
Output capacitor	C2	0.47 to 10	uF
Operating ambient temperature	T_A	-40 to 85	℃
Operating junction temperature	T_J	-40 to 125	℃

■ Electrical Characteristics

Typical limits tested at T_A= 25°C. Minimum and maximum limits apply over the full operating ambient temperature range(−40°C ≤T_A≤85°C). Unless otherwise specified, VIN= 3.6V, CTRL=V_{IN}.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SUPPLY CURRENT						
V_I	Input voltage range, VIN		2.7	-	5.5	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load	-	-	1.8	mA
I_{SD}	Shutdown current	CRTL=GND, VIN = 4.2 V	-	-	1	uA
UVLO	Undervoltage lockout threshold	VIN falling	-	2.2	2.5	V
V_{hys}	Undervoltage lockout hysteresis		-	70	-	mV
ENABLE AND REFERENCE CONTROL						
V(CTRLh)	CTRL logic high voltage	VIN = 2.7 V to 5.5 V	1.2	-	-	V
V(CTRLl)	CTRL logic low voltage	VIN = 2.7 V to 5.5 V	-	-	0.4	V
R(CTRL)	CTRL pull down resistor		400	800	1200	kΩ
t_{off}	CTRL pulse width to shutdown	CTRL high to low	2.5	-	-	mS
t_{1w_det}	1-Wire interface detection time(1)	CTRL pin low	260	-	-	uS
t_{1w_delay}	1-Wire interface detection delay		100	-		uS
t_{1w_win}	1-Wire interface detection window time	Measured from CTRL high	1	-	-	mS
Sd	Stable dimming range		0.3	1	100	%
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		193	200	207	mV
$V_{(REF\_PWM)}$	Voltage feedback regulation voltage under brightness control	V_{FB}=50mV	44	50	56	mV
		V_{FB}=20mV	14	20	26	
I_{FB}	Voltage feedback input bias current	V_{FB}=200mV	-	-	2	uA
f_S	Oscillator frequency		500	600	700	kHz
D_{max}	Maximum duty cycle	V_{FB}= 100 mV, measured on the drive signal of the switching FET	93%	95%	-	

■ Electrical Characteristics(continued)

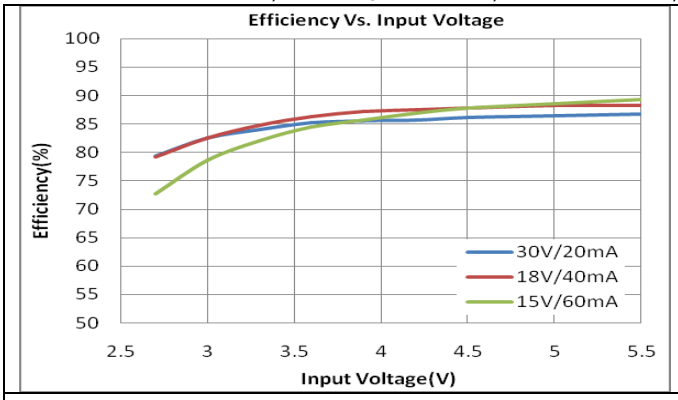
Typical limits tested at T_A= 25°C. Minimum and maximum limits apply over the full operating ambient temperature range(−40°C ≤T_A≤85°C). Unless otherwise specified, VIN= 3.6V, CTRL=V_{IN}.

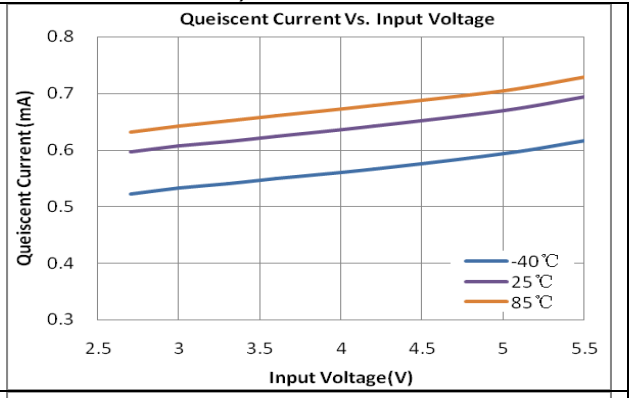
t_{min_on}	Minimum on pulse width		-	40	-	ns
I_{sink}	Comp pin sink current		-	100	-	uA
I_{source}	Comp pin source current		-	100	-	uA
G_{ea}	Error amplifier transconductance		-	320	-	uS
R_{ea}	Error amplifier output resistance		-	6	-	MΩ
POWER SWITCH						
$R_{DS(on)}$	N-channel MOSFET on-resistance	VIN=3.6	-	0.4	-	Ω
		VIN=3.0	-	-	0.7	
I_{LN_NFET}	N-channel leakage current	V_{SW}= 35 V, T_A= 25°C	-	-	1	uA
OC and OLP						
I_{LIM}	N-Channel MOSFET current limit	D=D_{max}	-	1.1	-	A
I_{LIM_Start}	Start up current limit	D=D_{max}	-	0.55	-	A
t_{Half_LIM}	Time step for half current limit		-	5	-	mS
V_{ovp}	Open LED protection threshold	Measured on the SW pin	-	38	-	V
$V_{(FB\_OVP)}$	Open LED protection threshold on FB	Measured on the FB pin, percentage of Vref, Vref=200mV and 20mV	-	50%	-	
t_{REF}	VREF filter time constant		-	180	-	us
t_{step}	VREF ramp up time		-	213	-	us
1-Wire interface TIMING						
t_{start}	Start time of program stream		2	-	-	us
t_{EOS}	End time of program stream		2		360	us
t_{H_LB}	High time low bit	Logic 0	2	-	180	us
t_{L_LB}	Low time low bit	Logic 0	2×t_{H_LB}	-	360	us
t_{H_HB}	High time high bit	Logic 1	2×t_{L_HB}	-	360	us
t_{L_HB}	Low time high bit	Logic 1	2	-	360	us
V_{ACKNL}	Acknowledge output voltage low	Open drain, R_{pullup}=15kΩ to VIN	-	-	0.4	V
$t_{valACKN}$	Acknowledge valid time	See(1)	-	-	2	us
t_{ACKN}	Duration of acknowledge condition	See(1)	-	-	512	us
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold		-	160	-	℃
$T_{hysteresis}$	Thermal shutdown threshold hysteresis		-	15	-	℃

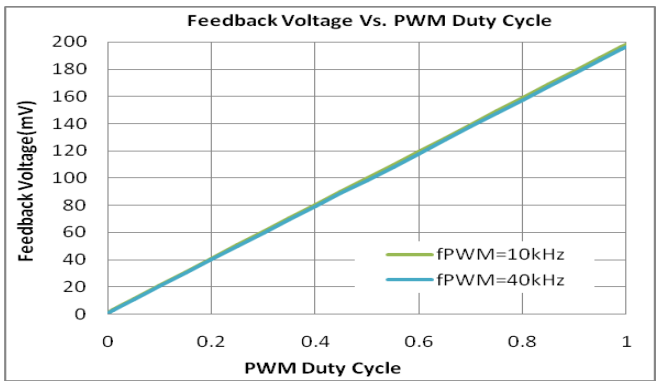
(1) Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open drain output, line needs to be pulled high by the host with resistor load.

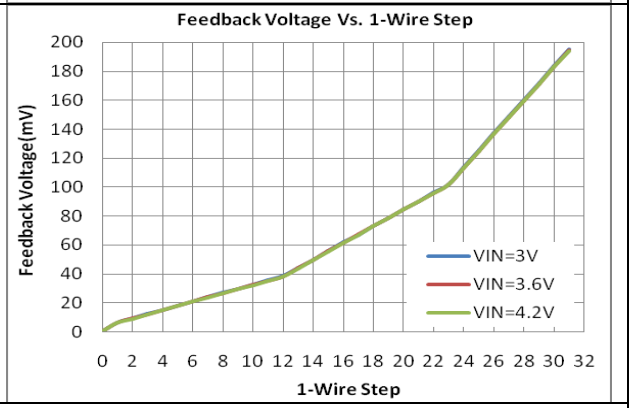
■ Typical Characteristics

(Unless otherwise noted, V_{IN} = V_{CTRL} = 3.6V, C1=C2=1.0uF, L=22uH, I_{LOAD}=20mA)



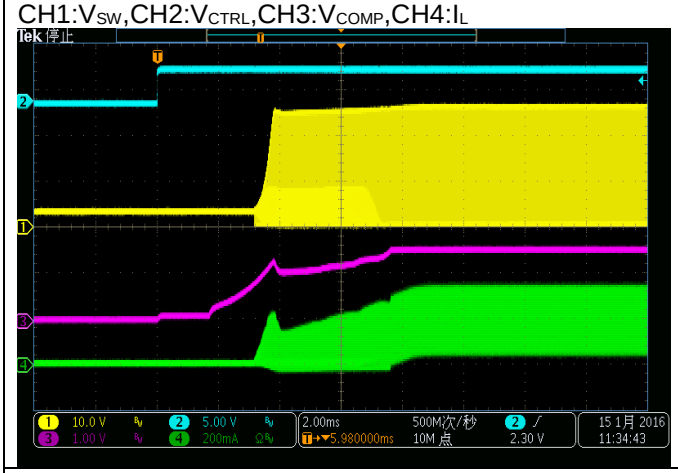






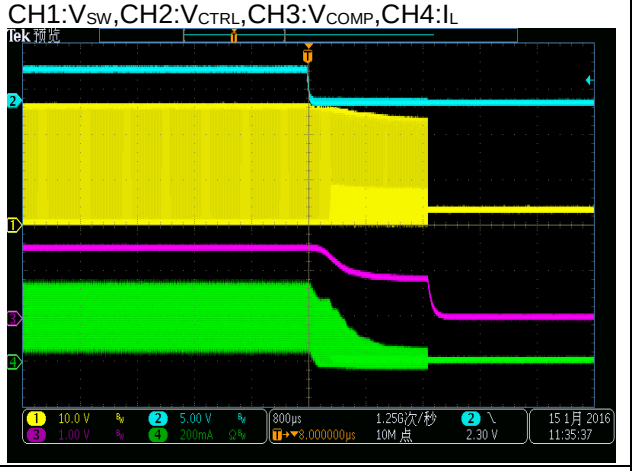
START-UP

CH1:V_{SW},CH2:V_{CTRL},CH3:V_{COMP},CH4:I_L



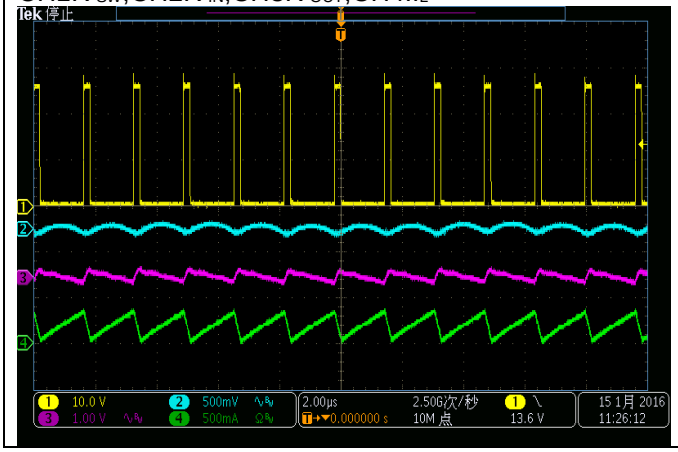
SHUTDOWN

CH1:V_{SW},CH2:V_{CTRL},CH3:V_{COMP},CH4:I_L



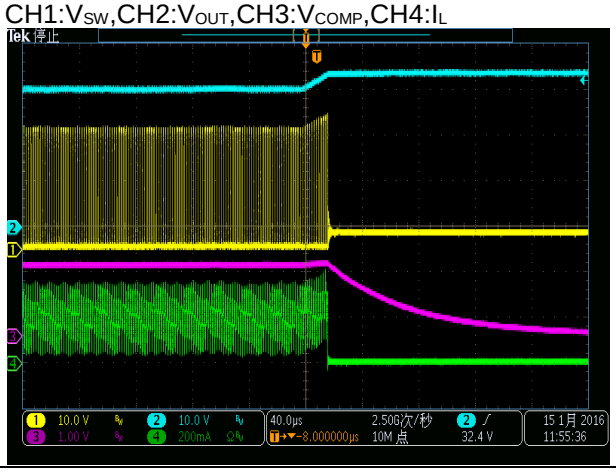
SWITCHING WAVEFORM

CH1:V_{SW},CH2:V_{IN},CH3:V_{OUT},CH4:I_L



OPEN LED PROTECTION

CH1:V_{SW},CH2:V_{OUT},CH3:V_{COMP},CH4:I_L



■ Functional Description

OPERATION

The OCP8178 is a high efficiency, high output voltage boost converter in a small package size. The device is ideal for driving white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40V/0.7A switch FET and operates in pulse width modulation (PWM) with 600kHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current mode control; therefore, a slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%. The feedback loop regulates the FB pin to a low reference voltage (200mV typical), reducing the power dissipation in the current sense resistor.

SOFT START-UP

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps with each step taking 213μs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, for the first 5ms after the COMP voltage ramps, the current limit of the switch is set to half of the normal current limit spec. During this period, the input current is kept below 400mA (typical).

OPEN LED PROTECTION

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The OCP8178 monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the IC when both of the following conditions: (1) the SW voltage exceeds the V_{OVP} threshold and (2) the FB voltage is less than half of regulation voltage. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin logic. The threshold is set at 38V. Make sure that the product of the number of external LEDs and each LED's maximum forward voltage plus the 200mV reference voltage does not exceed the minimum OVP threshold or $(N_{LEDS} \times V_{LED(MAX)})+200mV \leqslant V_{OVP(MIN)}$.

SHUTDOWN

The OCP8178 enters shutdown mode when the CTRL voltage is logic low for more than 2.5ms. During shutdown, the input supply current for the device is less than 1μA (max). Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. However, in the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the Schottky and keep leakage current low.

CURRENT PROGRAM

The FB voltage is regulated by a low 0.2V reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the R_{SET} is calculated using Equation 1:

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \quad (1)$$

Where

I_{LED}=output current of LEDs

V_{FB}=regulated voltage of FB

R_{SET}=current sense resistor

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy

LED BRIGHTNESS DIMMING MODE SELECTION

The CTRL pin is used for the control input for both dimming modes, PWM dimming and 1-Wire dimming. The dimming mode for the OCP8178 is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter the 1-Wire mode, the following digital pattern on the CTRL pin must be recognized by the IC every time the IC starts from the shutdown mode.

1. Pull CTRL pin high to enable the OCP8178, and to start the 1-Wire detection window.

2. After the 1-Wire interface detection delay (t_{1w_delay}, 100μs) expires, drive CTRL low for more than the 1-Wire interface detection time (t_{1w_detect}, 260μs).

3. The CTRL pin has to be low for more than 1-Wire interface detection time before the 1-Wire interface detection window (t_{1w_win}, 1ms) expires. 1-Wire interface detection window starts from the first CTRL pin low to high transition.

The IC enters the 1-Wire mode once the above 3 conditions are met. the 1-Wire interface communication can start before the detection window expires. Once the dimming mode is programmed, it can not be changed without another start up. This means the IC needs to be shut down by pulling the CTRL low for 2.5ms and restarts.

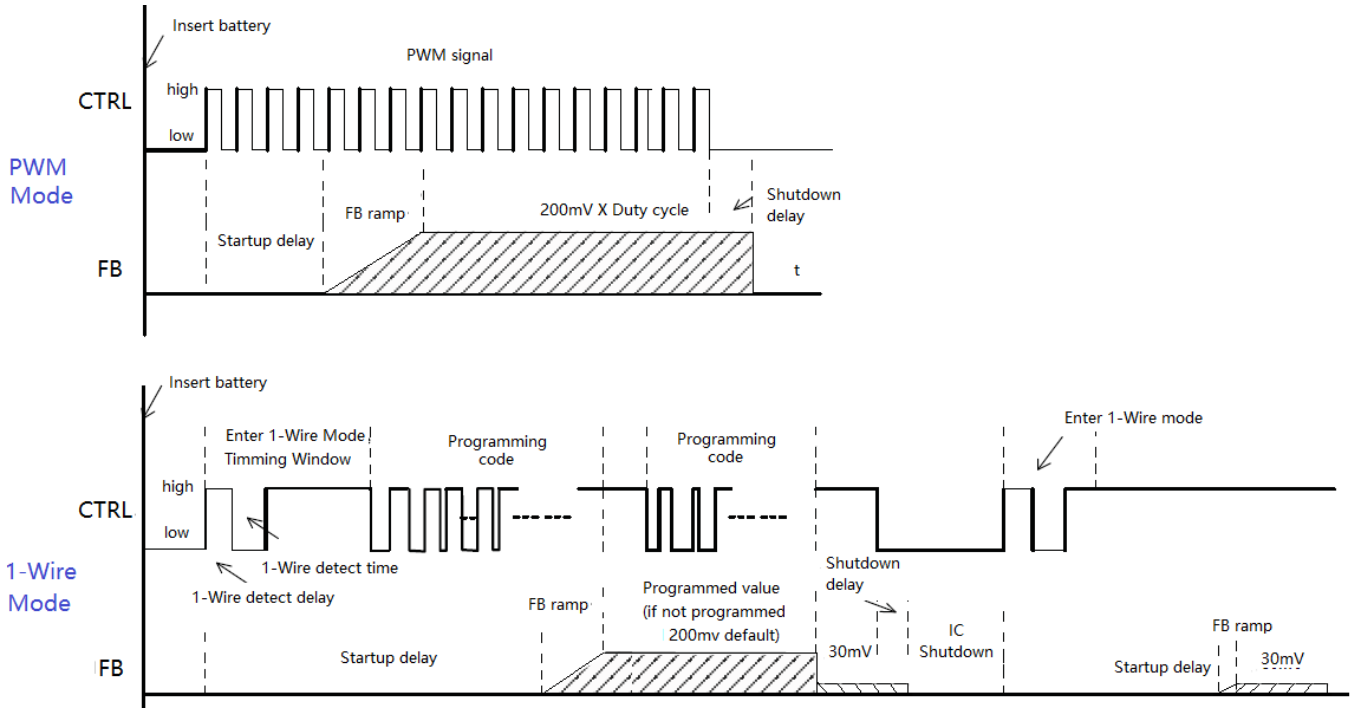


Figure 4, Dimming Mode Detection and Soft Start PWM Brightness Dimming

PWM BRIGHTNESS DIMMING

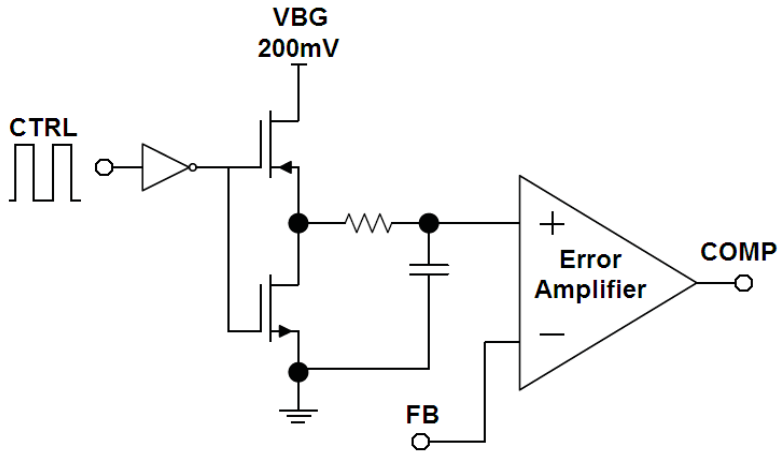


Figure 5, Block Diagram of Programmable FB Voltage Using PWM Signal

As shown in figure 5, the IC chops up the internal 200mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, OCP8178 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5kHz to 100kHz. The requirement of minimum dimming frequency comes from the 1-Wire interface detection delay and detection time specification in the dimming mode selection. Since the CTRL pin is logic only pin, adding an external RC filter applied to the pin does not work.

DIGITAL 1-Wire BRIGHTNESS DIMMING

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The OCP8178 adopts the 1-Wire interface protocol for the digital dimming, which can program the FB voltage to

any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See the Table 1 for the FB pin voltage steps. The default step is full scale when the device is first enabled (VFB=200 mV). The programmed reference voltage is stored in an internal register. A power reset clears the register value and reset it to default.

1-Wire INTERFACE DIGITAL DIMMING

1-Wire interface is a simple but flexible one pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. Figure 6 and Table 2 give an overview of the protocol.

The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72 hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the Request for Acknowledge condition. The Acknowledge condition is only applied if the protocol was received correctly. The advantage of 1-Wire interface compared with other on pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7kBit/sec and up to 160kBit/sec.

Table 1, Selectable FB Voltage

	FB voltage(mV)	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	5	0	0	0	0	1
2	8	0	0	0	1	0
3	11	0	0	0	1	1
4	14	0	0	1	0	0
5	17	0	0	1	0	1
6	20	0	0	1	1	0
7	23	0	0	1	1	1
8	26	0	1	0	0	0
9	29	0	1	0	0	1
10	32	0	1	0	1	0
11	35	0	1	0	1	1
12	38	0	1	1	0	0
13	44	0	1	1	0	1
14	50	0	1	1	1	0
15	56	0	1	1	1	1
16	62	1	0	0	0	0
17	68	1	0	0	0	1
18	74	1	0	0	1	0
19	80	1	0	0	1	1
20	86	1	0	1	0	0
21	92	1	0	1	0	1
22	98	1	0	1	1	0
23	104	1	0	1	1	1
24	116	1	1	0	0	0
25	128	1	1	0	0	1
26	140	1	1	0	1	0
27	152	1	1	0	1	1
28	164	1	1	1	0	0
29	176	1	1	1	0	1
30	188	1	1	1	1	0
31	200	1	1	1	1	1

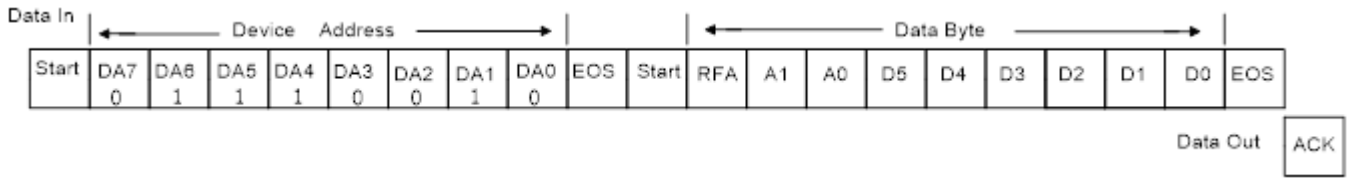


Figure 6, 1-Wire interface Protocol Overview

Table 2. 1-Wire interface Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte 72 Hex	7	DA7	IN	0 MSB device address
	6	DA6		1
	5	DA5		1
	4	DA4		1
	3	DA3		0
	2	DA2		0
	1	DA1		1
	0	DA0		0 LSB device address
Data byte	7(MSB)	RFA	IN	Request for acknowledge. If high, acknowledge is applied by device
	6	A1		0 Address bit 1
	5	A0		0 Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0(LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open drain output, Line needs to be pulled high by the host with a pull up resistor. This feature can only be used if the master has an open drain output stage. In case of a push pull output stage Acknowledge condition may not be requested!

All bits are transmitted MSB first and LSB last. Figure7 shows the protocol without acknowledge request (Bit RFA=0), Figure7 with acknowledge (Bit RFA=1) request. Prior to both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least t_{start} (2μs) before the bit transmission starts with the falling edge. If the CTRL pin is already at high level, no start condition is needed prior to the device address byte. The transmission of each byte is closed with an End of Stream condition for at least t_{EOS}(2μs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH}. It can be simplified to:

High Bit: $t_{HIGH} > t_{LOW}$, but with t_{HIGH} at least 2 x t_{LOW}, see Figure8.

Low Bit: $t_{HIGH} < t_{LOW}$, but with t_{LOW} at least 2 x t_{HIGH}, see Figure8.

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

(1) Acknowledge is requested by a set RFA bit.

(2) The transmitted device address matches with the device address of the device.

(3) 16 bits is received correctly.

If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time t_{ACKN}, which is 512μs maximum then the Acknowledge condition is valid after an internal delay time t_{valACK}. This means that the internal ACKN-MOSFET is turned on after t_{valACK}, when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after t_{valACK} and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

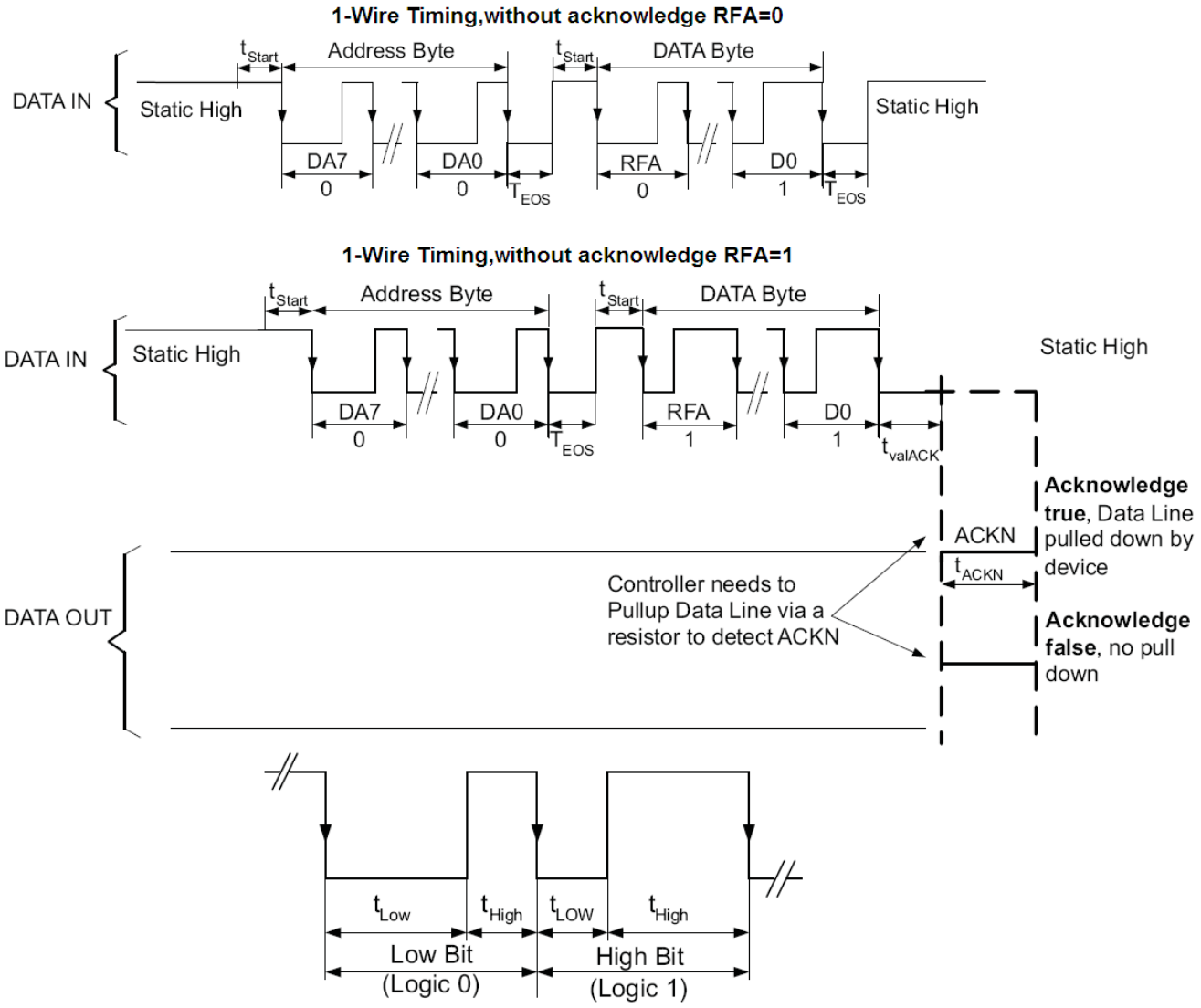


Figure 7, 1-Wire Interface Bit Coding

Note that the acknowledge condition may only be requested in case the master device has an open drain output. For a push-pull output stage, the use a series resistor in the CRTL line to limit the current to 500μA is recommended to for such cases as: (1) an accidentally requested acknowledge, or (2) to protect the internal ACKN-MOSFET.

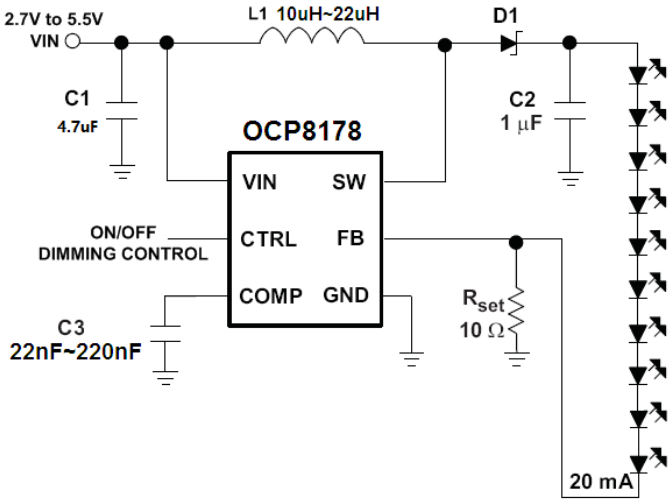
UNDERVOLTAGE LOCKOUT

An undervoltage lockout prevents operation of the device at input voltages below typical 2.2V. When the input voltage is below the undervoltage threshold, the device is shutdown and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

■ Application Information



Design Parameter	Example Value
PWM Dimming Control Frequency	5KHZ To 100KHZ
Inductor (L1)	10uH To 22uH
C3	22 To 220nF
VOUT(max)	38V

Figure 9, OCP8178 Typical Application

Input Capacitor (C1) Selection

The input capacitor can reduce peak current and noise at power source. Choosing the correct size and type of input capacitor helps minimize the input voltage ripple caused by the switching of the OCP8178's boost converter, and reduces noise on the boost converters input terminal that can feed through and disrupt internal analog signals. The capacitor in the range of 1uF to 10uF is recommended for input side. It is important to place the input capacitor as close as possible to the OCP8178's input (VIN) terminals. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents.

Output Capacitor (C2) Selection

To estimate the output voltage ripple considering the ripple due to capacitor discharge (ΔVQ) and the ripple due to the capacitors ESR (ΔVESR) use the following equations.

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{V_{OUT} \times V_{RIPPLE} \times F_S} \quad (3)$$

Where, V_{RIPPLE}=peak-to-peak output ripple. The additional output ripple component caused by ESR is calculated using:

$$V_{RIPPLE\_ESR} = [(\frac{I_{OUT} \times V_{OUT}}{V_{IN}}) + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times F_S \times L \times V_{OUT}}] \times R_{ESR} \quad (4)$$

Due to its low ESR, V_{RIPPLE_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Inductor (L1) Selection

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The OCP8178 is designed to use a 10μH to 22μH inductor. When the device is boosting (VOUT>VIN) the inductor is typically the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the OCP8178. This prevents excess efficiency loss that can occur with inductors that operate in saturation. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the OCP8178 are greater than I_{PEAK} in the following calculation:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + DI_L \quad (5)$$

Where

$$\begin{cases} DI_L = \dfrac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \\ f_{SW} = 600\,kHz \end{cases} \quad (6)$$

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by Equation 3, pause the inductor DC current given by:

$$I_{in\_DC} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} \quad (7)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10μH to 22μH inductor value range is recommended. A 22μH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple.

OCP8178 has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 10μH, the slope compensation may not be adequate, and the loop can be unstable.

Maximum Output Current

The over current limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$Ip = \frac{1}{L \times F_S \times \left(\dfrac{1}{V_{OUT} + V_f - V_{in}} + \dfrac{1}{V_{in}} \right)} \quad (8)$$

Where:

Ip= inductor peak to peak ripple;

L = inductor value;

V_f= Schottky diode forward voltage;

Fs = switching frequency;

Vout = output voltage of the boost converter. It is equal to the sum of VFB and the voltage drop across LEDs.

$$I_{out\_max} = \frac{V_{in} \times (I_{lim} - I_p/2) \times \eta}{V_{out}} \quad (9)$$

Where:

I_{out_max}= maximum output current of the boost converter;

I_{lim}= over current limit;

η= efficiency.

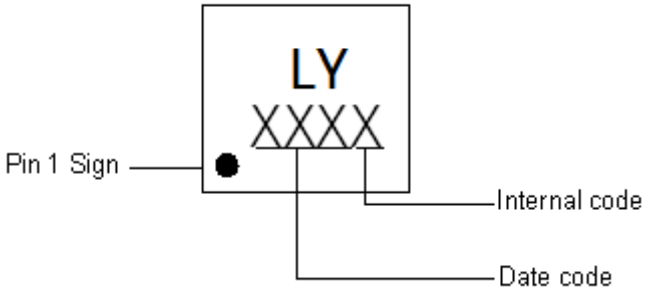
For instance, when VIN is 5V, 10 LEDs output equivalent to VOUT of 32V, the inductor is 22μH, the Schottky forward voltage is 0.2V; and then the maximum output current is 85mA in typical condition.

■ Ordering Information

Part Number	Maximum VOUT	VFB	Package Type	Package Qty	Temperature	Eco Plan	Lead/Ball Finish
OCP8178VAD	38V	200mV	DFN2X2-6L	7-in reel 3000pcs/reel	-40～85℃	Green	NIPDAU

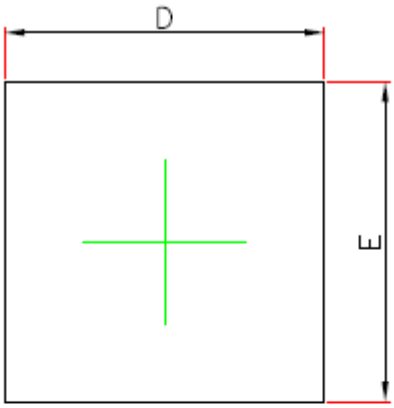
■ Marking Information

DFN2X2-6L：

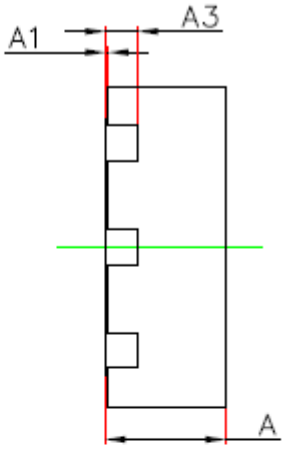


■ Package Information

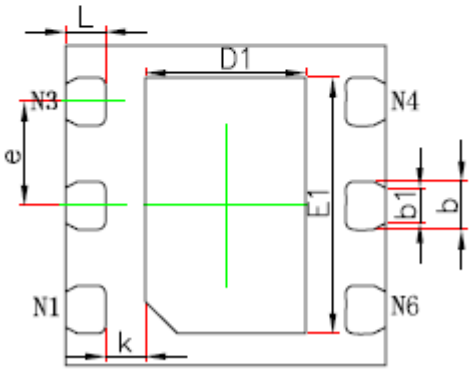
DFN2X2-6L:



TOP VIEW



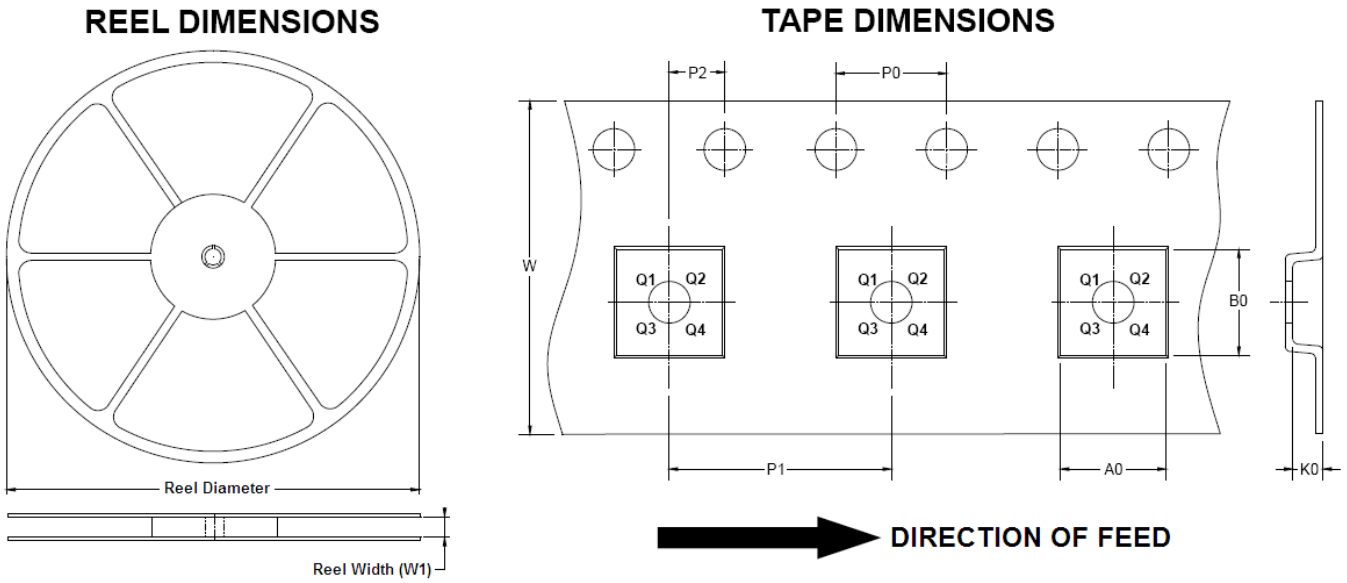
SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E1	1.500	1.700	0.059	0.067
k	0.250 REF		0.010 REF	
b	0.250	0.350	0.010	0.014
b1	0.220 REF		0.009 REF	
e	0.650 BSC		0.026 BSC	
L	0.174	0.326	0.007	0.013

■ Packing Information



Note: The picture is only for reference. Please make the object as the standard.

Key parameter list of tape and reel

Package Type	Reel Diameter	SPQ (PCS)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
DFN2X2-6L	7″	3000	9	2.3	2.3	1.1	4	4	2	8	Q1