# SGM8263-1/SGM8263-2
# Ultra Low Offset Voltage, High Linearity, Low Noise Operational Amplifiers

## GENERAL DESCRIPTION

The SGM8263-1 (single) and SGM8263-2 (dual) bipolar-input operational amplifiers achieve very low noise density with a low distortion of 0.0001% at 1kHz. The SGM8263-1/2 offer rail-to-rail output swing to within 190mV of supply rails with a 2kΩ load, which increases headroom and maximizes dynamic range. The devices also have a high output drive capability of ±55mA.

SGM8263-1/2 have ultra low offset voltage and ultra low offset voltage drift over temperature. The maximum offset voltage is 8.5μV. SGM8263-1/2 are very suitable for amplifying low noise and low amplitude signal.

The devices operate over a wide supply range of 4V to 36V or ±2V to ±18V, on only 2.5mA of supply current per amplifier. The SGM8263-1/2 operational amplifiers are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

The SGM8263-1 is available in Green SOT-23-5 and SOIC-8 packages. The SGM8263-2 is available in a Green SOIC-8 package. They are specified from -40℃ to +85℃ temperature range.

## FEATURES

- **Ultra Low Offset Voltage: 8.5μV (MAX)**
- **Ultra Low Input Offset Voltage Drift: 10nV/℃**
- **Low Noise: 4.5nV/$\sqrt{Hz}$ at 1kHz**
- **Low Distortion: 0.0001% at 1kHz**
- **High Slew Rate: 10V/μs**
- **Gain-Bandwidth Product: 10MHz (G = +1)**
- **High Open-Loop Gain: 145dB**
- **Unity-Gain Stable**
- **Low Quiescent Current: 2.5mA/Amplifier**
- **Rail-to-Rail Output**
- **Support Single or Dual Power Supplies:**
  **4V to 36V or ±2V to ±18V**
- **-40℃ to +85℃ Operating Temperature Range**
- **Small Packaging:**
  **SGM8263-1 Available in Green SOT-23-5 and SOIC-8 Packages**
  **SGM8263-2 Available in a Green SOIC-8 Package**

## APPLICATIONS

Temperature Measurements
Pressure Sensors
Precision Current Sensing
Electronic Scales
Strain Gauge Amplifiers
Medical Instrumentation
Thermocouple Amplifiers
Handheld Test Equipment

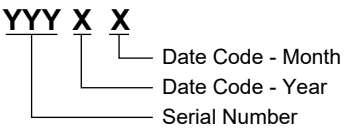
# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM8263-1 | SOT-23-5 | -40℃ to +85℃ | SGM8263-1YN5G/TR | GJ8XX | Tape and Reel, 3000 |
| | SOIC-8 | -40℃ to +85℃ | SGM8263-1YS8G/TR | SGM<br>82631YS8<br>XXXXX | Tape and Reel, 4000 |
| SGM8263-2 | SOIC-8 | -40℃ to +85℃ | SGM8263-2YS8G/TR | SGM<br>82632YS8<br>XXXXX | Tape and Reel, 4000 |

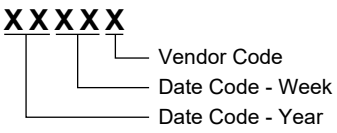
## MARKING INFORMATION

NOTE: XX = Date Code. XXXXX = Date Code and Vendor Code.

**SOT-23-5**




**SOIC-8**




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ ..... 40V
Input Voltage Range ..... $(-V_S)$ - 0.3V to $(+V_S)$ + 0.3V
Input Current (All pins except power supply pins)..... ±10mA
Output Short-Circuit Current ..... ±80mA
Junction Temperature ..... +150℃
Storage Temperature Range..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM (SGM8263-1) ..... 3000V
HBM (SGM8263-2) ..... 5000V
MM (SGM8263-1) ..... 200V
MM (SGM8263-2) ..... 300V
CDM ..... 1000V

## RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

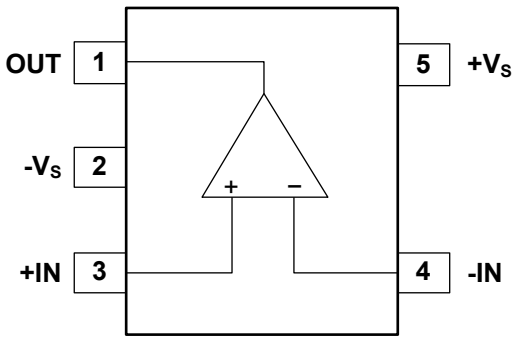
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

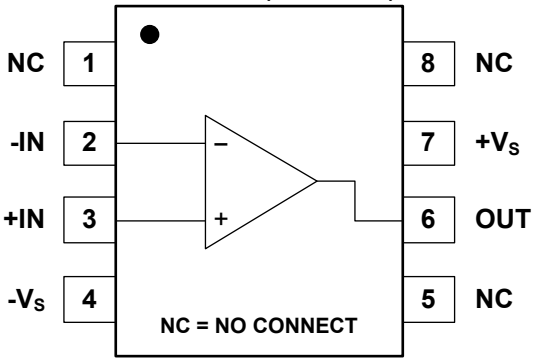
## PIN CONFIGURATIONS

SGM8263-1 (TOP VIEW)



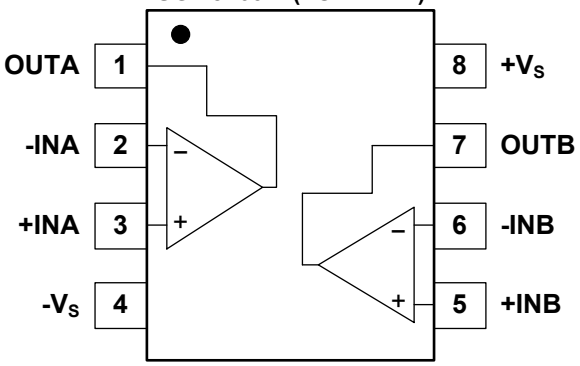

SOT-23-5

SGM8263-1 (TOP VIEW)




SOIC-8

SGM8263-2 (TOP VIEW)




SOIC-8

## ELECTRICAL CHARACTERISTICS

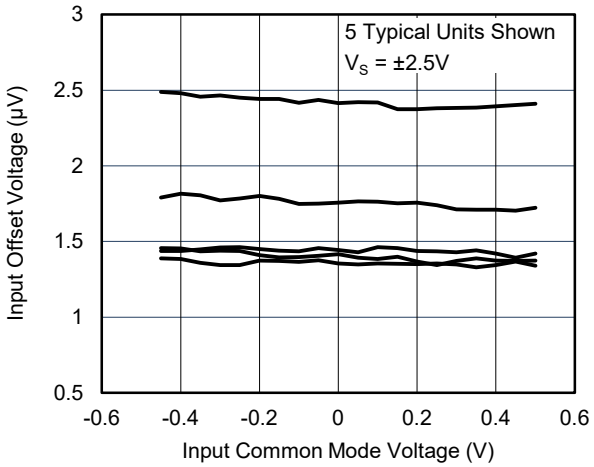
(At $T_A$ = +25℃, $V_S$ = 4.5V to 36V or $V_S$ = ±2.25V to ±18V, $R_L$ = 2kΩ, $V_{CM}$ = $V_{OUT}$ = $V_S$/2, Full = -40℃ to +85℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | TEMP | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Input Characteristics** | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_S$ = ±15V | +25℃ | | 1.5 | 8.5 | μV |
| | | | Full | | | 10 | |
| Input Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | Full | | 10 | | nV/℃ |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0V | +25℃ | | ±60 | ±300 | nA |
| | | | Full | | | ±350 | |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 0V | +25℃ | | ±20 | ±190 | nA |
| | | | Full | | | ±210 | |
| Input Common Mode Voltage Range | $V_{CM}$ | | Full | $(-V_S)$ + 2 | | $(+V_S)$ - 2 | V |
| Common Mode Rejection Ratio | CMRR | $(-V_S)$ + 2V ≤ $V_{CM}$ ≤ $(+V_S)$ - 2V | +25℃ | 107 | 135 | | dB |
| | | | Full | 102 | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $(-V_S)$ + 0.2V ≤ $V_{OUT}$ ≤ $(+V_S)$ - 0.2V, $R_L$ = 10kΩ | +25℃ | 118 | 145 | | dB |
| | | | Full | 115 | | | |
| | | $(-V_S)$ + 0.6V ≤ $V_{OUT}$ ≤ $(+V_S)$ - 0.6V, $R_L$ = 2kΩ | +25℃ | 115 | 145 | | |
| | | | Full | 112 | | | |
| **Input Impedance** | | | | | | | |
| Differential | | | +25℃ | | 16k \|\| 10 | | Ω \|\| pF |
| Common Mode | | | +25℃ | | $10^9$ \|\| 10 | | Ω \|\| pF |
| **Output Characteristics** | | | | | | | |
| Output Voltage Swing from Rail | | $R_L$ = 10kΩ | +25℃ | | 40 | 75 | mV |
| | | | Full | | | 85 | |
| | | $R_L$ = 2kΩ | +25℃ | | 190 | 320 | |
| | | | Full | | | 360 | |
| Output Short-Circuit Current | $I_{SC}$ | | +25℃ | ±36 | ±55 | | mA |
| | | | Full | ±27 | | | |
| **Dynamic Performance** | | | | | | | |
| Gain-Bandwidth Product | GBP | G = +1 | +25℃ | | 10 | | MHz |
| Phase Margin | $\varphi_O$ | $V_{OUT}$ = 100m$V_{P-P}$, $R_L$ = 2kΩ, $C_L$ = 10pF | +25℃ | | 50 | | ° |
| Slew Rate | SR | G = -1, $V_{OUT}$ = 2$V_{P-P}$ | +25℃ | | 10 | | V/μs |
| Settling Time to 0.1% | $t_S$ | 10V step, G = +1 | +25℃ | | 3 | | μs |
| Overload Recovery Time | | $V_{IN}$ × G > $V_S$ | +25℃ | | 0.2 | | μs |
| Total Harmonic Distortion + Noise | THD+N | G = +1, $V_{OUT}$ = 1$V_{RMS}$, f = 1kHz, BW = 80kHz | +25℃ | | 0.0001 | | % |
| **Noise Performance** | | | | | | | |
| Input Voltage Noise | | f = 0.1Hz to 10Hz | +25℃ | | 100 | | $nV_{P-P}$ |
| Input Voltage Noise Density | $e_n$ | f = 1kHz | +25℃ | | 4.5 | | $nV/\sqrt{Hz}$ |
| Input Current Noise Density | $i_n$ | f = 1kHz | +25℃ | | 5 | | $pA/\sqrt{Hz}$ |
| **Power Supply** | | | | | | | |
| Supply Voltage | $V_S$ | | Full | ±2 | | ±18 | V |
| Quiescent Current/Amplifier | $I_Q$ | $I_{OUT}$ = 0A | +25℃ | | 2.5 | 3.2 | mA |
| | | | Full | | | 3.4 | |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ±2V to ±18V | +25℃ | | 0.02 | 0.4 | μV/V |
| | | | Full | | | 0.6 | |

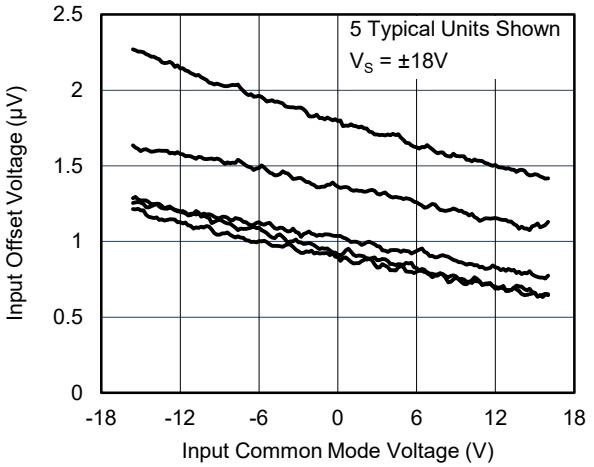
## TYPICAL PERFORMANCE CHARACTERISTICS

At $T_A$ = +25℃, $V_S$ = ±18V and $R_L$ = 10kΩ, unless otherwise noted.

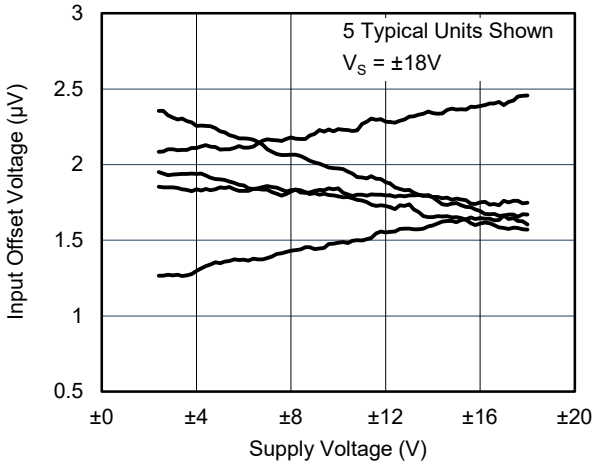
Input Offset Voltage vs. Input Common Mode Voltage



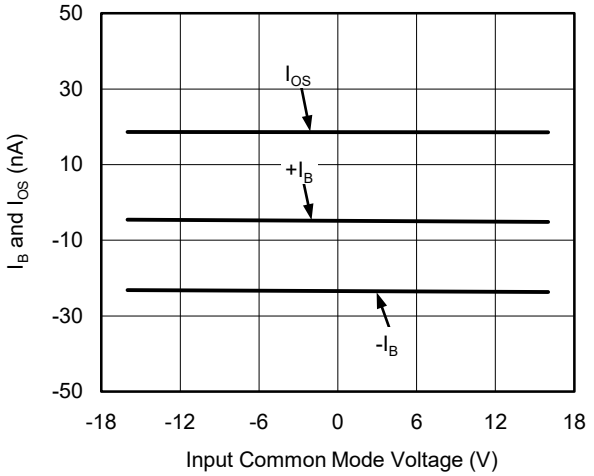

Input Offset Voltage vs. Input Common Mode Voltage



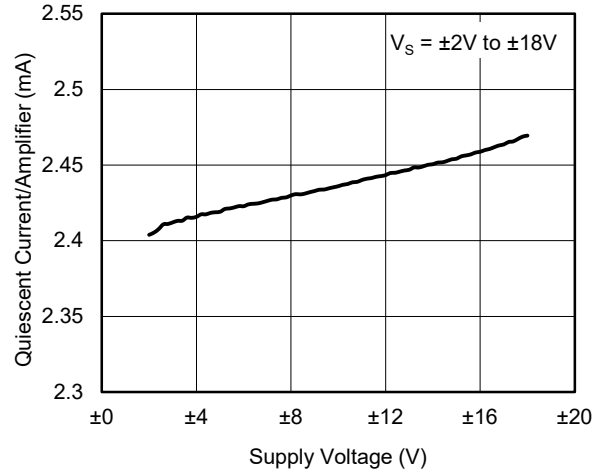

Input Offset Voltage vs. Supply Voltage



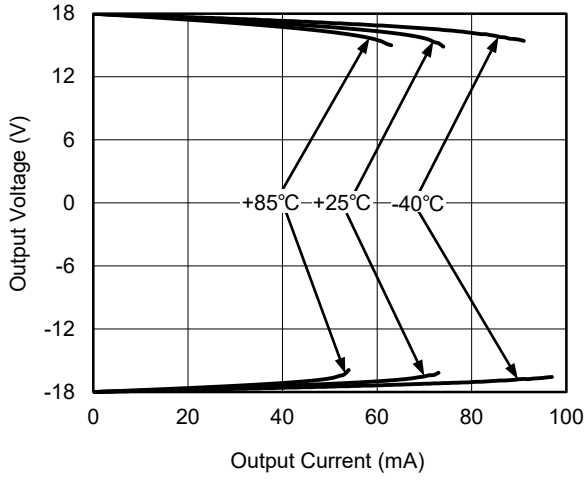

$I_B$ and $I_{OS}$ vs. Input Common Mode Voltage




Quiescent Current vs. Supply Voltage



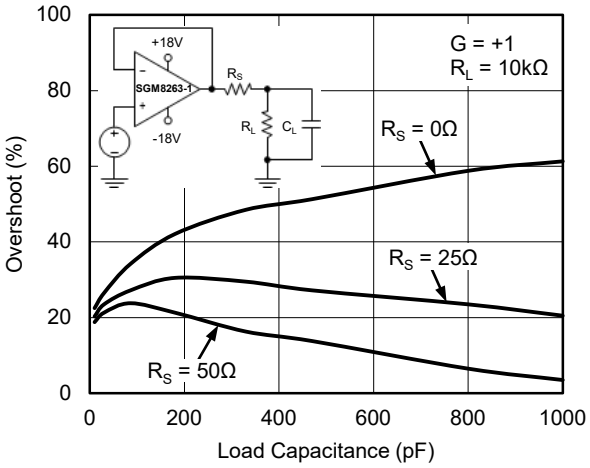

Output Voltage vs. Output Current (Maximum Supply)



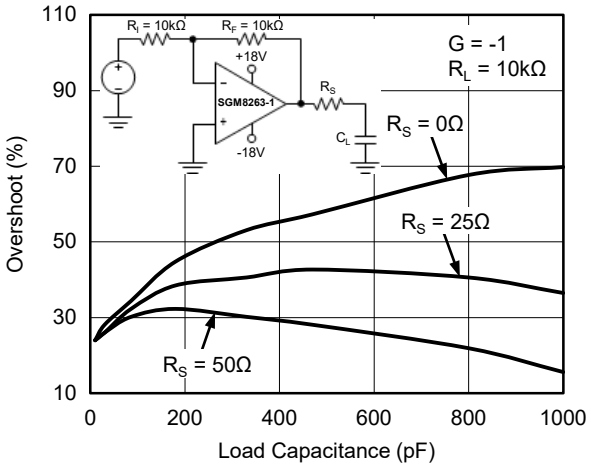
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A$ = +25℃, $V_S$ = ±18V and $R_L$ = 10kΩ, unless otherwise noted.

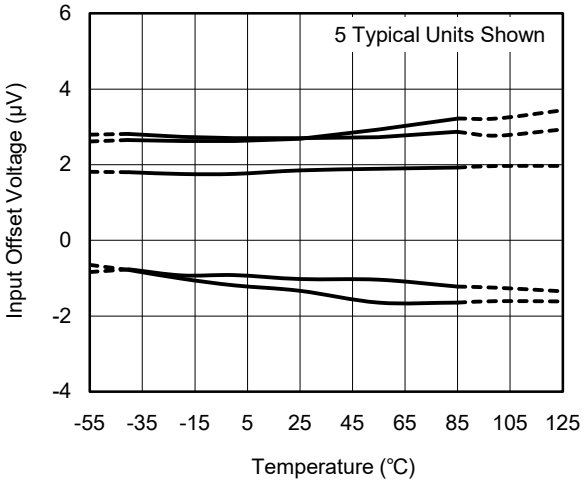
Small-Signal Overshoot vs.
Capacitive Load (100mV Output Step)



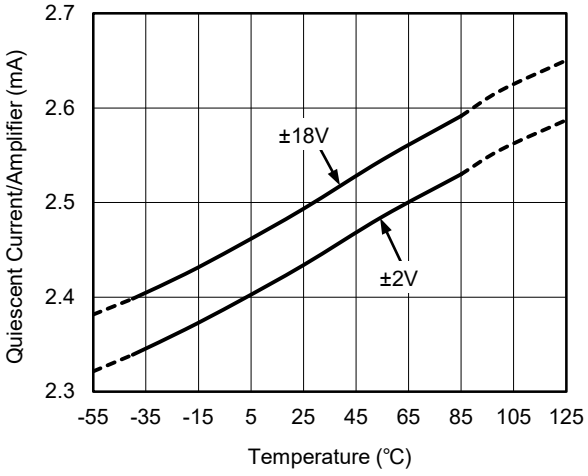

Small-Signal Overshoot vs.
Capacitive Load (100mV Output Step)



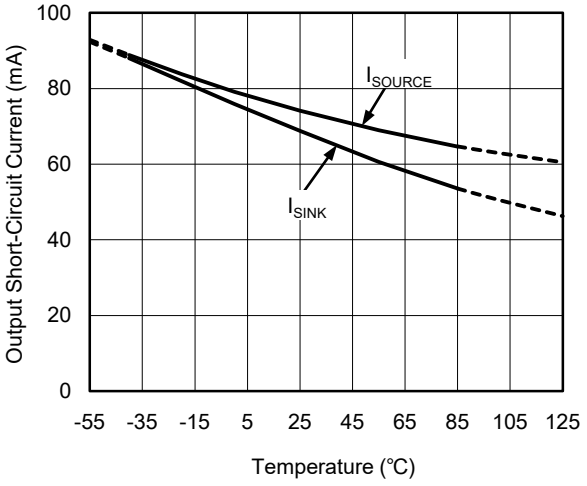

Input Offset Voltage vs. Temperature



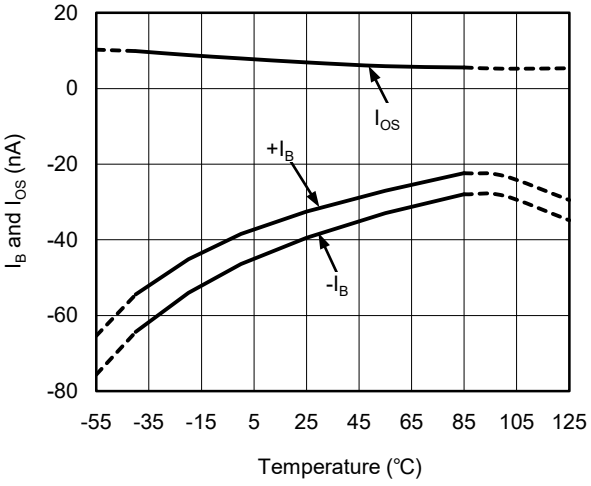

Quiescent Current vs. Temperature




Output Short-Circuit Current vs. Temperature



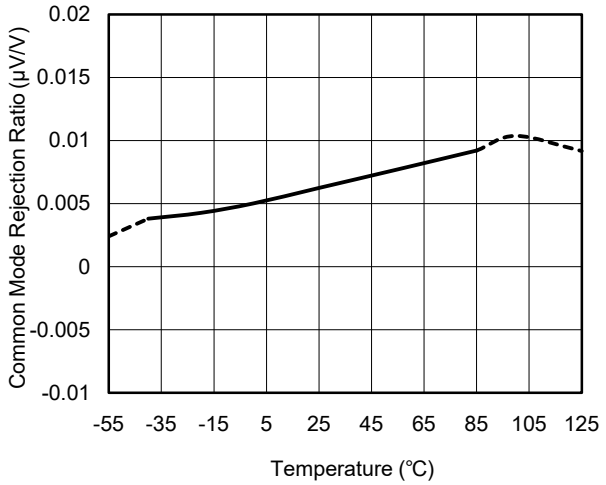

$I_B$ and $I_{OS}$ vs. Temperature



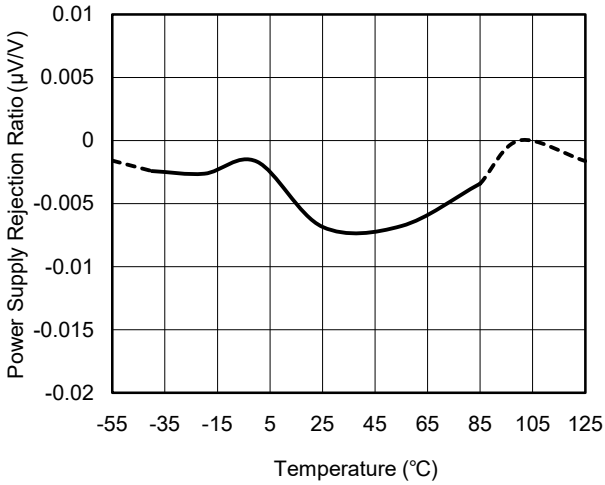
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A$ = +25℃, $V_S$ = ±18V and $R_L$ = 10kΩ, unless otherwise noted.

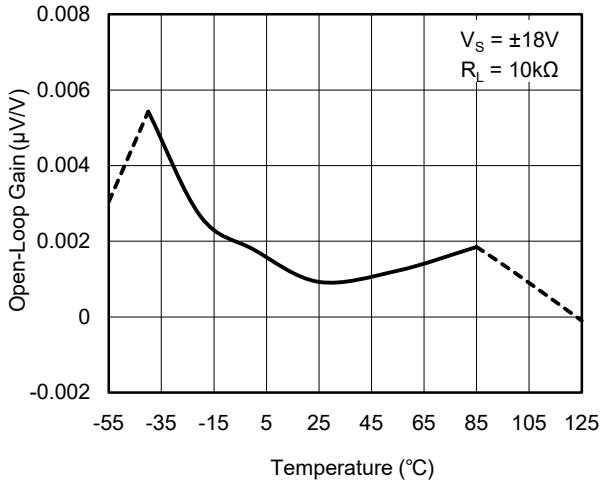
CMRR vs. Temperature



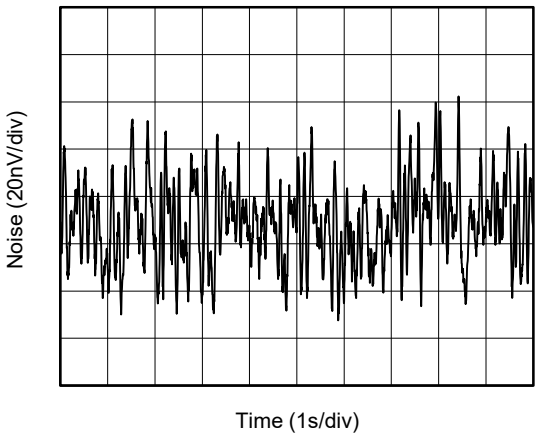

PSRR vs. Temperature



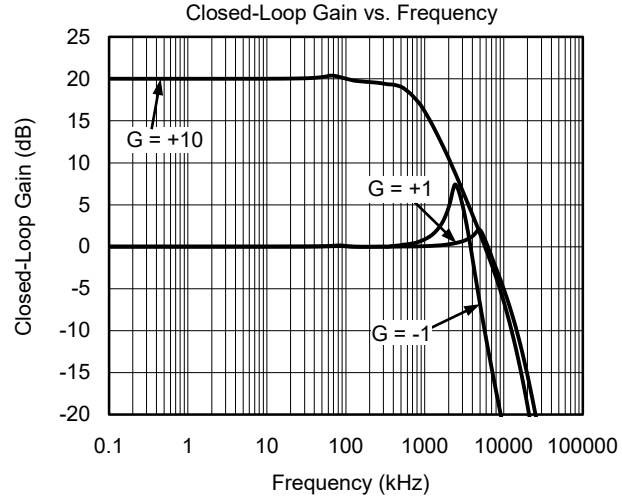

Open-Loop Gain vs. Temperature



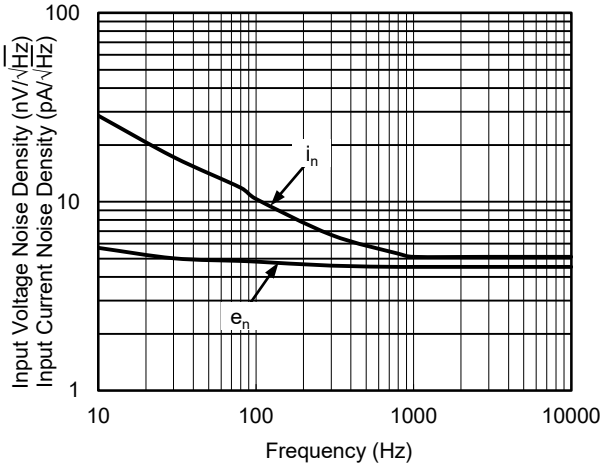

0.1Hz to 10Hz Input Voltage Noise




Closed-Loop Gain vs. Frequency



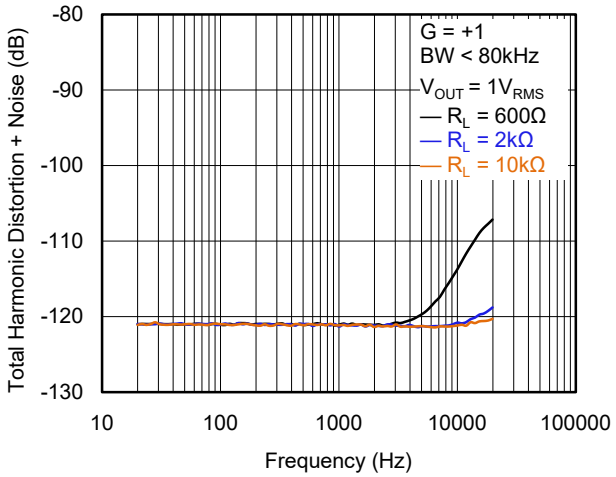

Input Voltage Noise Density ($e_n$) and
Input Current Noise Density ($i_n$) vs. Frequency



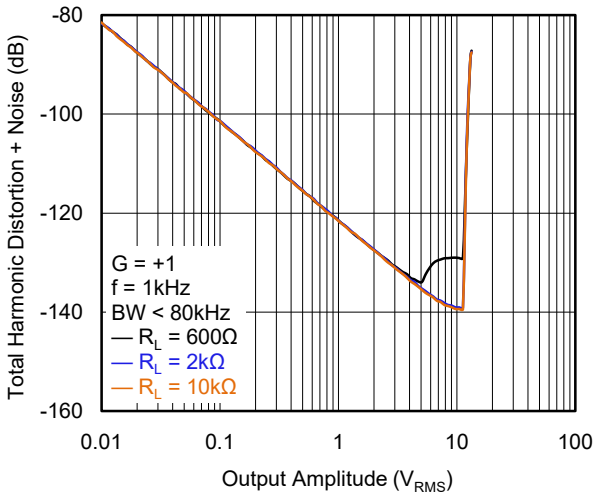
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A$ = +25℃, $V_S$ = ±18V and $R_L$ = 10kΩ, unless otherwise noted.

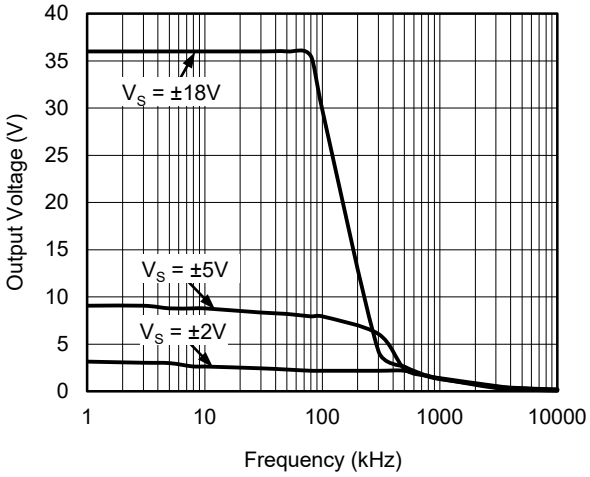
THD+N vs. Frequency



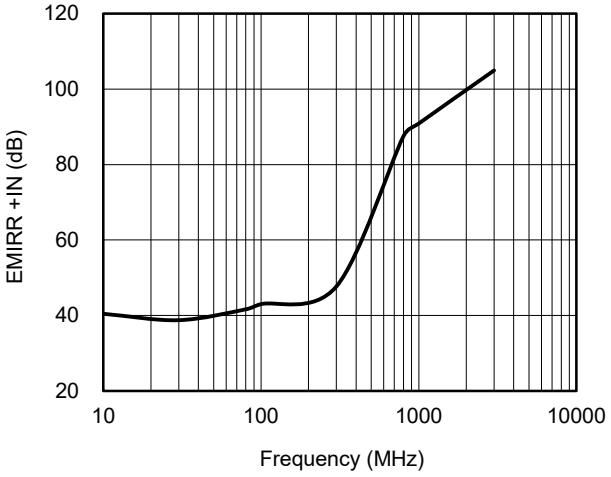

THD+N vs. Output Amplitude



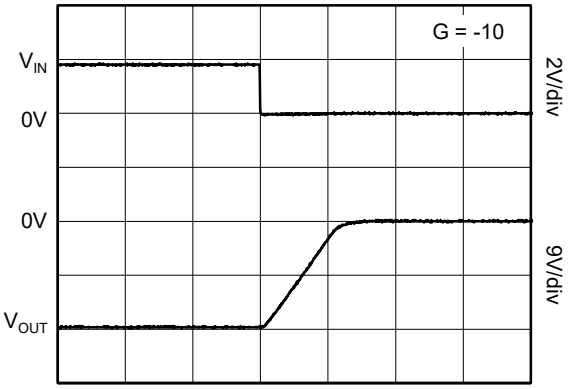

Maximum Output Voltage vs. Frequency



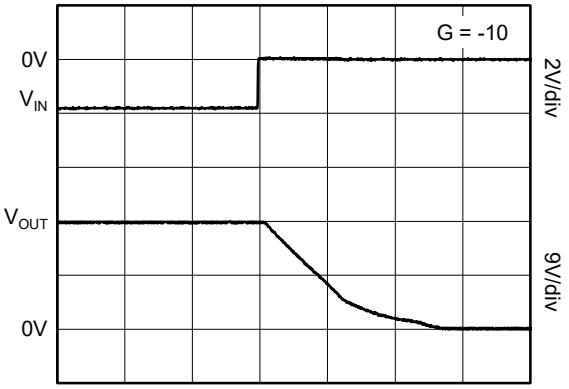

EMIRR IN+ vs. Frequency




Positive Overload Recovery



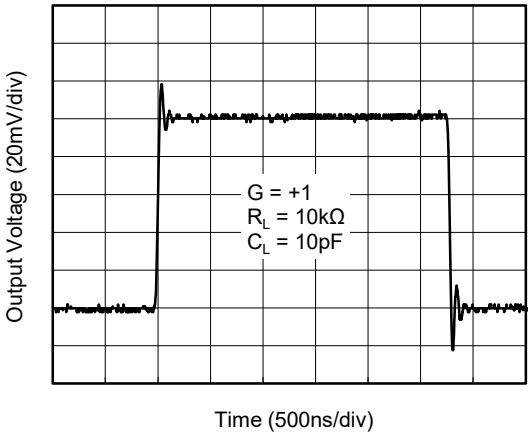

Negative Overload Recovery



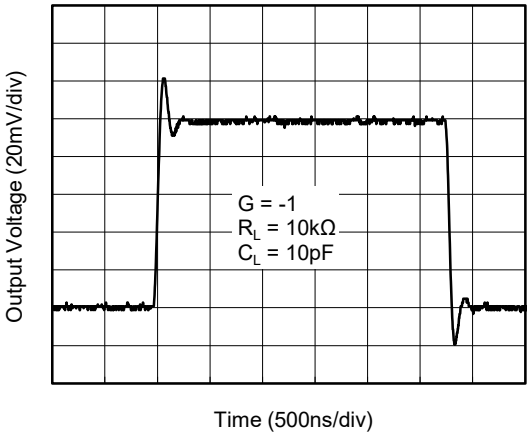
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A$ = +25℃, $V_S$ = ±18V and $R_L$ = 10kΩ, unless otherwise noted.

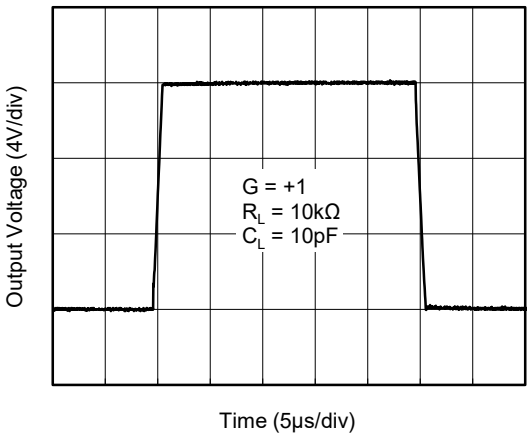
Small-Signal Step Response (100mV)



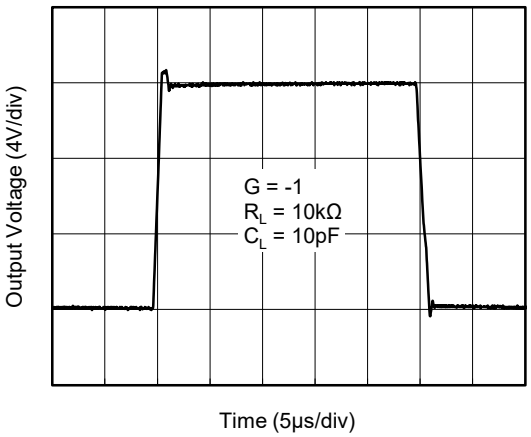

Small-Signal Step Response (100mV)



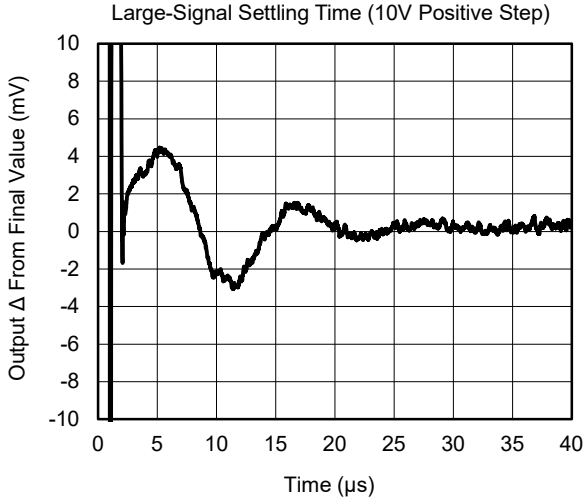

Large-Signal Step Response



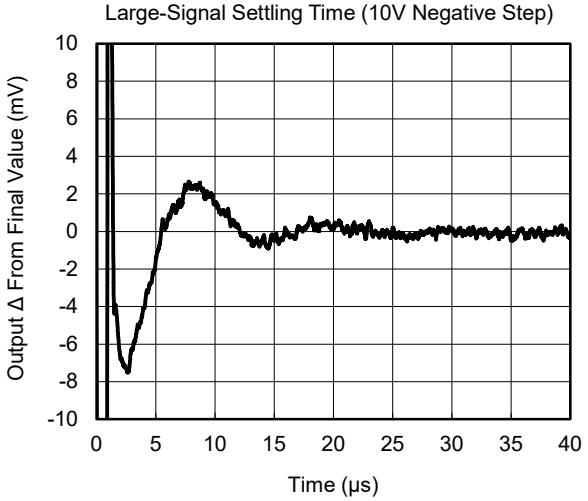

Large-Signal Step Response




Large-Signal Settling Time (10V Positive Step)



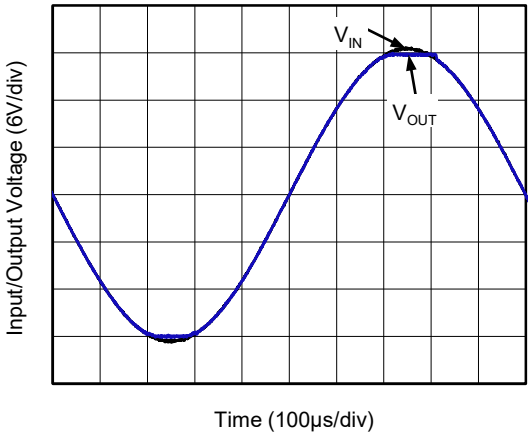

Large-Signal Settling Time (10V Negative Step)



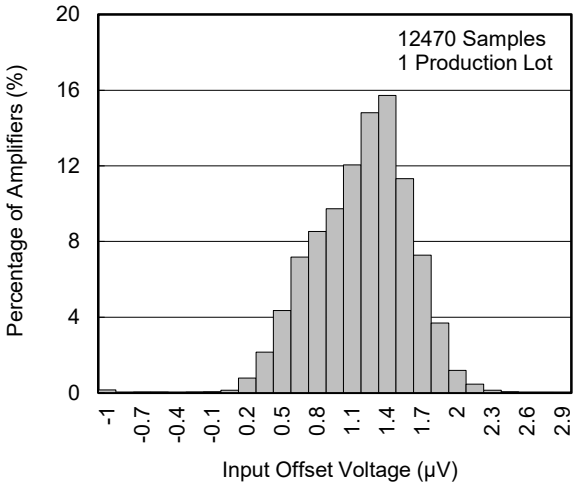
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A$ = +25℃, $V_S$ = ±18V and $R_L$ = 10kΩ, unless otherwise noted.

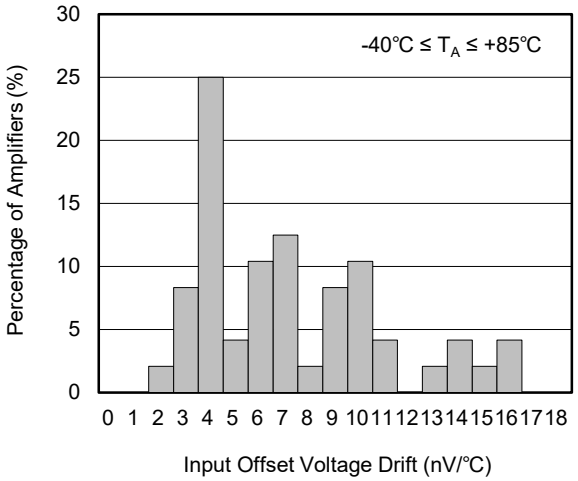
No Phase Reversal




Input Offset Voltage Production Distribution




Input Offset Voltage Drift Distribution



# APPLICATION INFORMATION

The SGM8263-1/2 are unity-gain stable, high precision operational amplifiers with very low noise, very low offset voltage and very low offset voltage drift; the devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power supply pins. In most cases, 0.1μF capacitors are adequate.

## Operating Voltage

The SGM8263-1/2 operational amplifiers operate from 4V to 36V or ±2V to ±18V supplies while maintaining excellent performance. However, some applications do not require equal positive and negative output voltage swing. With the SGM8263-1/2, power supply voltages do not need to be equal. For example, the positive supply could be set to 25V with the negative supply at -5V. In all cases, the input common mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of $T_A$ = -40℃ to +85℃.

## Input Protection

The input terminals of the SGM8263-1/2 are protected from excessive differential voltage with back-to-back diodes, as Figure 1 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor ($R_I$) and/or a feedback resistor ($R_F$) can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the SGM8263-1/2 and is examined in the following Noise Performance section. Figure 1 shows an example configuration when both current-limit input and feedback resistors are used.

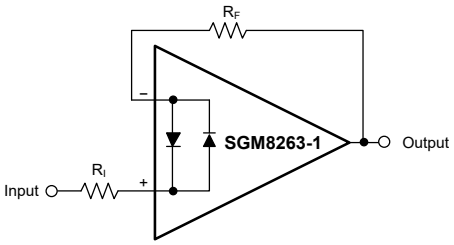



**Figure 1. Input Current Limiting**

## Noise Performance

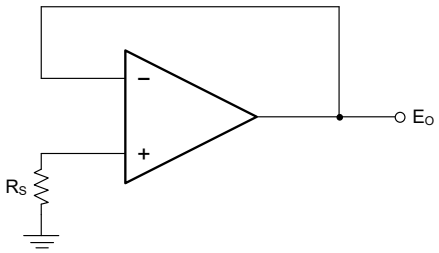
Equation 1 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (Figure 2, no feedback resistor network, and therefore no additional noise contributions).

The SGM8263-1/2 (GBP = 10MHz, G = +1) are shown with total circuit noise calculated. The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the SGM8263-1/2 operational amplifiers makes them good choices for use in applications where the source impedance is less than 1kΩ.

The equation 1 shows the calculation of the total circuit noise, with these parameters:

- $e_n$ = voltage noise
- $i_n$ = current noise
- $R_S$ = source impedance
- k = Boltzmann's constant = $1.38 \times 10^{-23}$J/K
- T = temperature in degrees Kelvin (K)

$$E_O^2 = e_n^2 + (i_n R_S)^2 + 4kTR_S \quad (1)$$



# APPLICATION INFORMATION (continued)

## Basic Noise Calculations

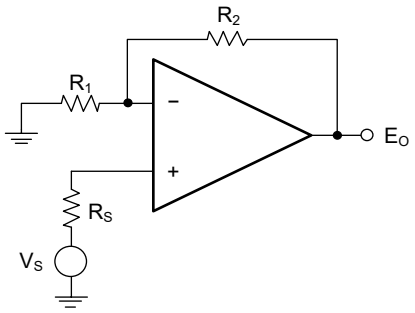
Design of low-noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is usually fixed; consequently, select the operational amplifier and the feedback resistors to minimize the respective contributions to the total noise.

Figure 3 illustrates both inverting and non-inverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise.

The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

**Noise in Non-Inverting Gain Configuration**




Noise at the output:

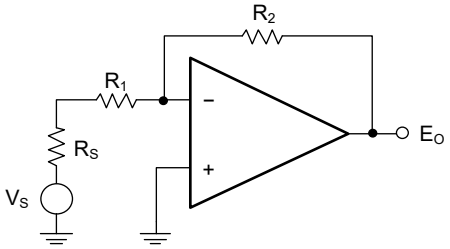
$$E_O^2 = \left[1 + \frac{R_2}{R_1}\right]^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left[1 + \frac{R_2}{R_1}\right]^2$$

Where $e_S = \sqrt{4kTR_S} \times \left[1 + \frac{R_2}{R_1}\right]$ = thermal noise of $R_S$

$e_1 = \sqrt{4kTR_1} \times \left[\frac{R_2}{R_1}\right]$ = thermal noise of $R_1$

$e_2 = \sqrt{4kTR_2}$ = thermal noise of $R_2$

**Noise in Inverting Gain Configuration**




Noise at the output:

$$E_O^2 = \left[1 + \frac{R_2}{R_1 + R_S}\right]^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left[\frac{R_2}{R_1 + R_S}\right]$ = thermal noise of $R_S$

$e_1 = \sqrt{4kTR_1} \times \left[\frac{R_2}{R_1 + R_S}\right]$ = thermal noise of $R_1$

$e_2 = \sqrt{4kTR_2}$ = thermal noise of $R_2$

NOTE: For the SGM8263-1/2 operational amplifiers at 1kHz, $e_n$ = 4.5nV/$\sqrt{Hz}$ and $i_n$ = 5pA/$\sqrt{Hz}$.

**Figure 3. Noise Calculation in Gain Configurations**

## APPLICATION INFORMATION (continued)

### Capacitive Loads

The dynamic characteristics of the SGM8263-1/2 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor ($R_S$ equal to 50Ω, for example) in series with the output.

### Power Dissipation

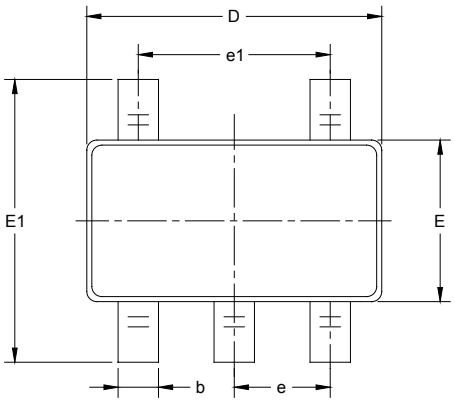
SGM8263-1/2 operational amplifiers are capable of driving 2kΩ loads with a power supply voltage up to ±18V. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the SGM8263-1/2 operational amplifiers improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

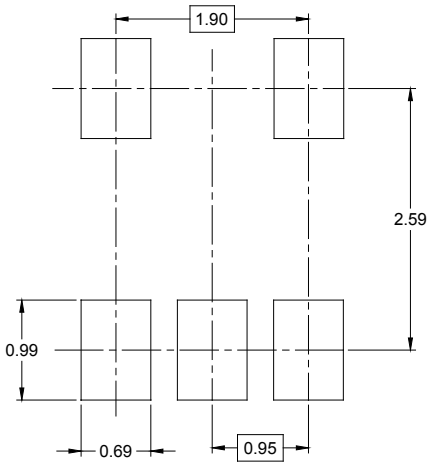
### Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions has electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

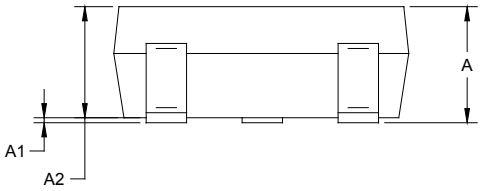
# PACKAGE OUTLINE DIMENSIONS

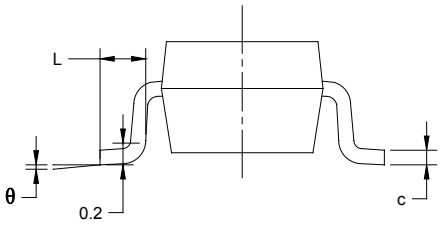
## SOT-23-5




**RECOMMENDED LAND PATTERN** (Unit: mm)

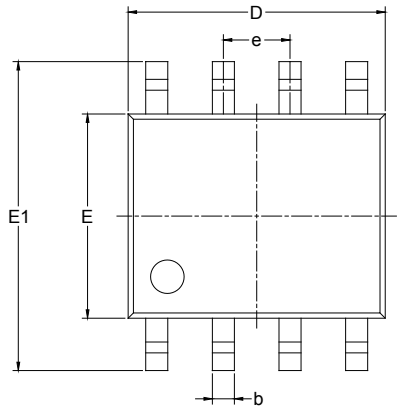


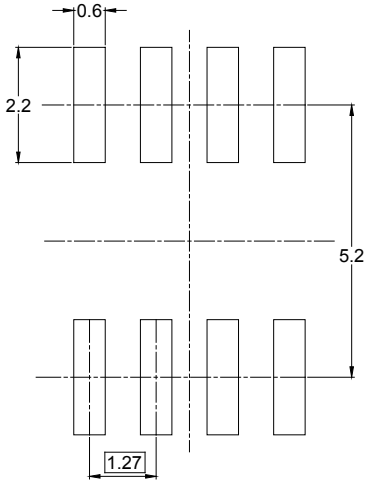




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.050 | 1.250 | 0.041 | 0.049 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 1.050 | 1.150 | 0.041 | 0.045 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.100 | 0.200 | 0.004 | 0.008 |
| D | 2.820 | 3.020 | 0.111 | 0.119 |
| E | 1.500 | 1.700 | 0.059 | 0.067 |
| E1 | 2.650 | 2.950 | 0.104 | 0.116 |
| e | 0.950 BSC | | 0.037 BSC | |
| e1 | 1.900 BSC | | 0.075 BSC | |
| L | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 8° | 0° | 8° |

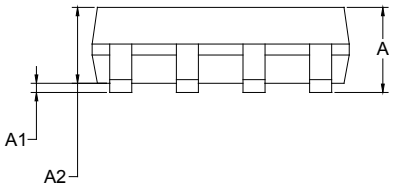
# PACKAGE OUTLINE DIMENSIONS

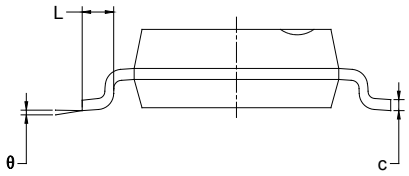
## SOIC-8




**RECOMMENDED LAND PATTERN** (Unit: mm)

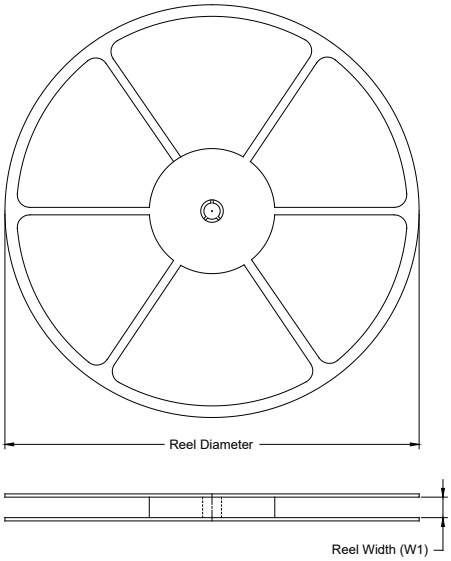


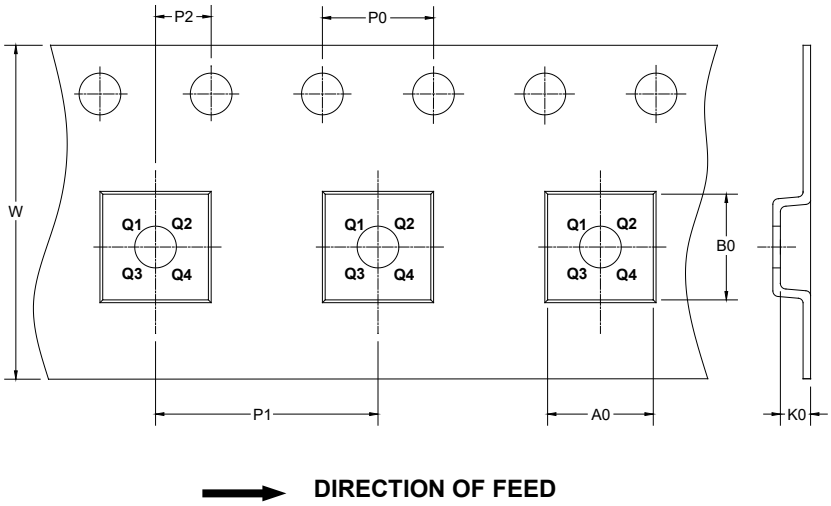

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS




DIRECTION OF FEED

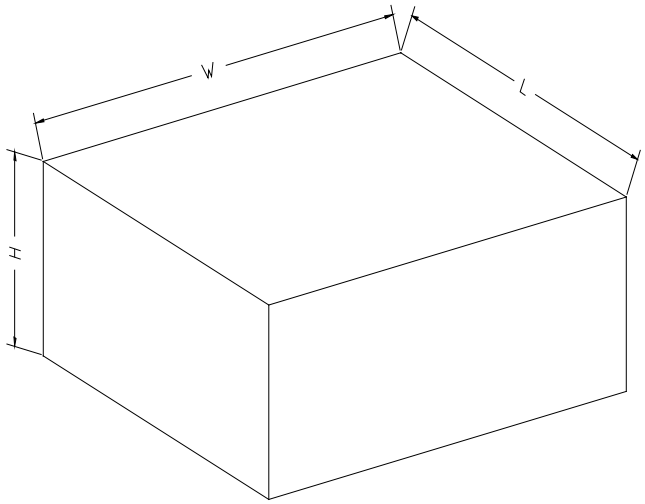
NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| SOT-23-5 | 7″ | 9.5 | 3.20 | 3.20 | 1.40 | 4.0 | 4.0 | 2.0 | 8.0 | Q3 |
| SOIC-8 | 13″ | 12.4 | 6.40 | 5.40 | 2.10 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |
| 13″ | 386 | 280 | 370 | 5 |

DD0002