OPAx197-Q1 36V、精密、轨至轨输入/输出、低失调电压、低输入偏置电流运算放大器 - 采用 e-trim™

1 特性

- 符合汽车应用 标准
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件 HBM ESD 分类等级 3A
  - 器件 CDM ESD 分类等级 C4A
- 低失调电压：±250μV（最大值）
- 低失调电压漂移：±0.2μV/°C
- 低噪声：1kHz 时为 5.5nV/$\sqrt{Hz}$
- 高共模抑制：140dB
- 低偏置电流：±5pA
- 轨到轨输入和输出
- 高带宽：10MHz GBW
- 高压摆率：20V/μs
- 低静态电流：每个放大器 1mA
- 宽电源电压范围：±2.25V 至 ±18V，4.5V 至 36V
- 已过滤电磁干扰 (EMI)/射频干扰 (RFI) 的输入
- 电源轨的差分输入电压范围
- 高容性负载驱动能力：1nF
- 行业标准封装：
  - 单通道，采用极小的 8 引脚 VSSOP 封装
  - 双通道，采用 8 引脚 VSSOP 封装

2 应用

- 汽车电机控制
- 牵引逆变器
- 车载充电器
- 高精度电流检测

3 说明

OPAx197-Q1 系列（OPA197-Q1 和 OPA2197-Q1）是新一代 36V e-trim 运算放大器的一部分。OPAx197-Q1 系列运算放大器使用 e-trim 方法，这是一种在塑模成型工艺之后，在最终制造步骤阶段对失调电压和温漂实施封装级微调的方法。该方法最大限度地减少了固有的输入晶体管不匹配的影响和在封装成型过程中引入的误差。

这些器件具有出色的直流精度和交流性能，包括轨至轨输入/输出、低失调电压（典型值为 ±5μV）、低温漂（典型值为 ±0.2μV/°C）和 10MHz 带宽。

OPAx196 拥有 诸多独一无二的特性（例如电源轨的差分输入电压范围、高输出电流 (±65mA)、高达 1nF 的高电容负载驱动以及高压摆率 (20V/μs)）使 OPAx197-Q1 成为一款稳定可靠的高性能运算放大器，适用于各种高电压工业 应用。

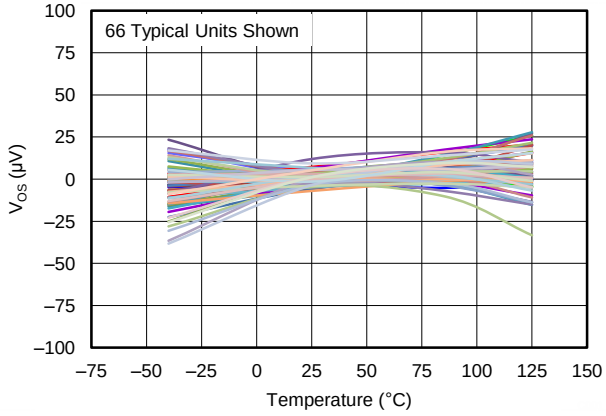
OPAx197-Q1 系列运算放大器采用标准封装，其额定工作温度范围为 -40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA197-Q1	VSSOP (8)	3.00mm × 3.00mm
OPA2197-Q1		

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

OPAx197-Q1 在整个温度范围内保持超低的输入失调电压



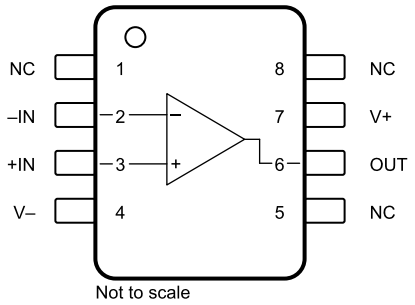
目录

4 修订历史记录

日期	修订版本	说明
2018 年 3 月	*	初始发行版

5 Pin Configuration and Functions

OPA197-Q1 DGK Package
8-Pin VSSOP
Top View

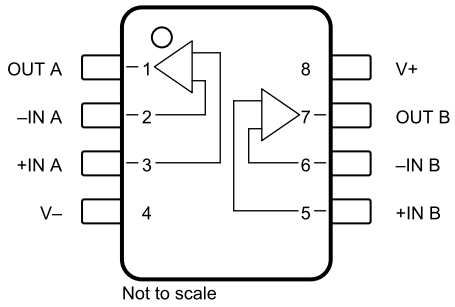


NC – No internal connection.

Pin Functions: OPA197-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	2	I	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	O	Output
V+	7	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

OPA2197-Q1 DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2197-Q1

PIN		I/O	DESCRIPTION
NAME	DGK (VSSOP)		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				±20 (40, single-supply)	V
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit[2]				Continuous	
Latch-up per JESD78D				Class IIA	
Temperature	Operating range		–55	150	°C
	Junction			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
OPA197-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged device model (CDM), per AEC Q100-011	±500	
OPA2197-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		+125	°C

6.4 Thermal Information: OPA197-Q1

THERMAL METRIC(1)		OPA197-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2197-Q1

THERMAL METRIC(1)		OPA2197-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±25	±250	µV
		T_A = 0°C to 85°C			±30	±350	
		T_A = –40°C to 125°C			±50	±400	
		V_{CM} = (V+) – 1.5 V			±10	±250	
			T_A = 0°C to 85°C		±25	±350	
			T_A = –40°C to 125°C		±50	±500	
dV_{OS}/dT	Input offset voltage drift		T_A = 0°C to 85°C		±0.5	±2.5	µV/°C
			T_A = –40°C to 125°C		±0.8	±4.5	
PSRR	Power-supply rejection ratio	T_A = –40°C to 125°C			±0.3	±1.0	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to 125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to 125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.30		$µV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		4		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		$nV/\sqrt{Hz}$
			f = 1 kHz		5.5		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		
			f = 1 kHz		12.5		
NOISE (continued)							
i_n	Input current noise density	f = 1 kHz			1.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		120	140		dB
			T_A = –40°C to 125°C	114	126		
		(V+) – 1.5 V < V_{CM} < (V+)		100	120		
			T_A = –40°C to 125°C	86	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		120	134		dB
			T_A = –40°C to 125°C	114	126		
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		126	140		
			T_A = –40°C to 125°C	120	134		

Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±18 V, G = 1, 10-V step		1.4		µs
			V_S = ±18 V, G = 1, 5-V step		0.9		
		To 0.001%	V_S = ±18 V, G = 1, 10-V step		2.1		
			V_S = ±18 V, G = 1, 5-V step		1.8		
t_{OR}	Overload recovery time	V_{IN} × G = V_S			200		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00008%		
	Crosstalk	OPA2197-Q1 at dc			150		dB
		OPA2197-Q1 at f = 100 kHz			130		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A; see 图 29			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.2	mA
		T_A = –40°C to 125°C, I_O = 0 A				1.5	
TEMPERATURE							
	Thermal protection(1)				140		°C

(1) For a detailed description of thermal protection, see *Thermal Protection* .

6.7 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = (V+) – 3 V			±5	±250	µV
			T_A = 0°C to 85°C		±8	±350	
			T_A = –40°C to 125°C		±10	±400	
		(V+) – 3.5 V < V_{CM} < (V+) – 1.5 V			See *Common-Mode Voltage Range*		
		V_{CM} = (V+) – 1.5 V			±10	±250	µV
			T_A = 0°C to 85°C		±25	±350	
			T_A = –40°C to 125°C		±50	±500	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = (V+) – 3 V	T_A = –40°C to 125°C		±0.5	±2.5	µV/°C
		V_{CM} = (V+) – 1.5 V			±0.8	±4.5	
PSRR	Power-supply rejection ratio	T_A = –40°C to 125°C, V_{CM} = V_S / 2 – 0.75 V			±2		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to 125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to 125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V, f = 0.1 Hz to 10 Hz			1.30		$µV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V, f = 0.1 Hz to 10 Hz			4		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		$nV/\sqrt{Hz}$
			f = 1 kHz		5.5		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		
			f = 1 kHz		12.5		
i_n	Input current noise density		f = 1 kHz		1.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		94	110		dB
			T_A = –40°C to 125°C	90	104		
		(V+) – 1.5 V < V_{CM} < (V+)		100	120		
			T_A = –40°C to 125°C	84	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		110	120		dB
			T_A = –40°C to 125°C	100	114		
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		110	126		
			T_A = –40°C to 125°C	110	120		

Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±3 V, G = 1, 5-V step		1		µs
t_{OR}	Overload recovery time	V_{IN}× G = V_S			200		ns
	Crosstalk	OPA2197-Q1 at dc			150		dB
		OPA2197-Q1 at f = 100 kHz			130		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A; see 图 29			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.2	mA
			T_A = –40°C to 125°C			1.5	
TEMPERATURE							
	Thermal protection(1)				140		°C

(1) For a detailed description of thermal protection, see *Thermal Protection* .

6.8 Typical Characteristics

表 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1 to 图 6
Offset Voltage Drift Distribution	图 7 to 图 8
Offset Voltage vs Temperature	图 9
Offset Voltage vs Common-Mode Voltage	图 10 to 图 12
Offset Voltage vs Power Supply	图 13
Open-Loop Gain and Phase vs Frequency	图 14
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Short-Circuit Current vs Temperature	图 42
Maximum Output Voltage vs Frequency	图 43
Propagation Delay Rising Edge	图 44
Propagation Delay Falling Edge	图 45
Crosstalk vs Frequency	图 46

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

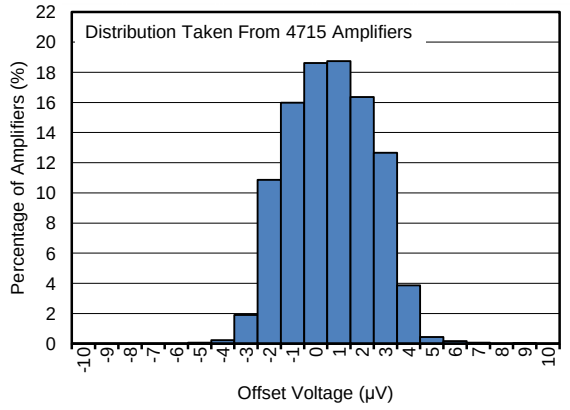
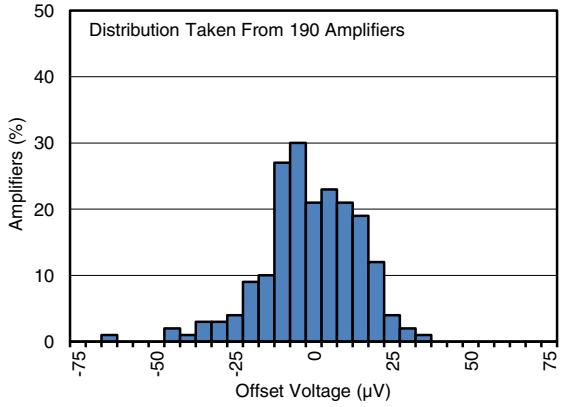
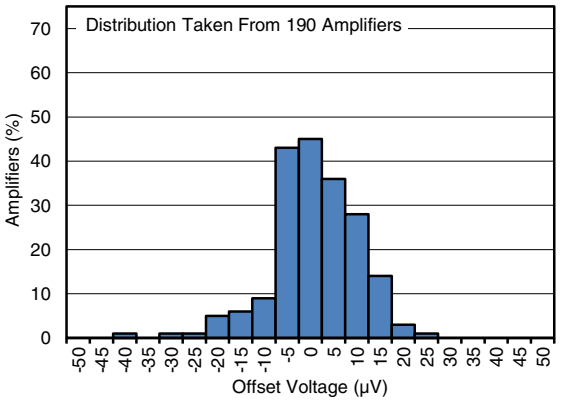


图 1. Offset Voltage Production Distribution at 25°C



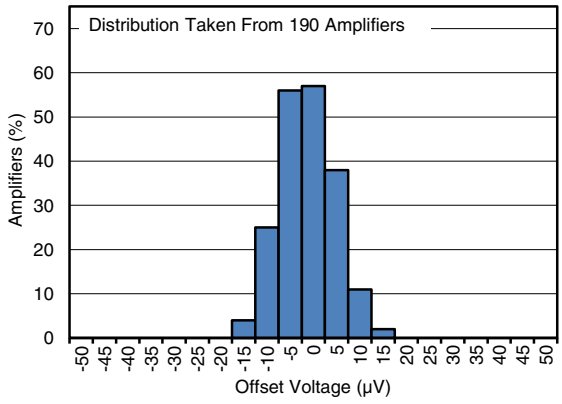
T_A = 125°C

图 2. Offset Voltage Production Distribution at 125°C



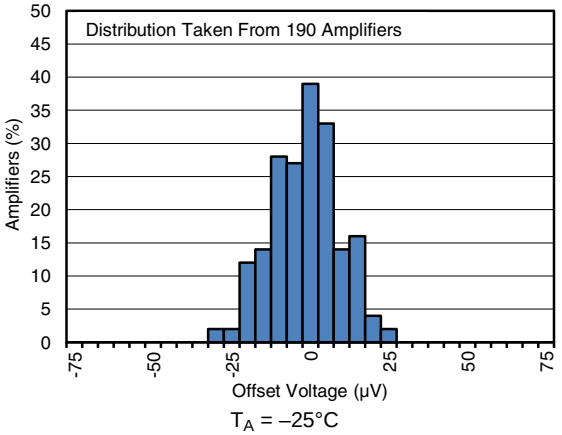
T_A = 85°C

图 3. Offset Voltage Production Distribution at 85°C



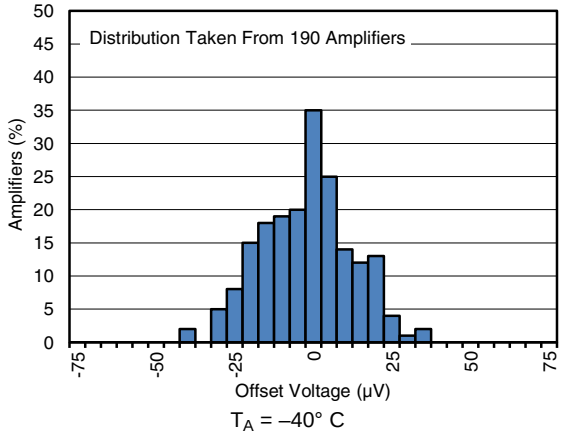
T_A = 0°C

图 4. Offset Voltage Production Distribution at 0°C



T_A = –25°C

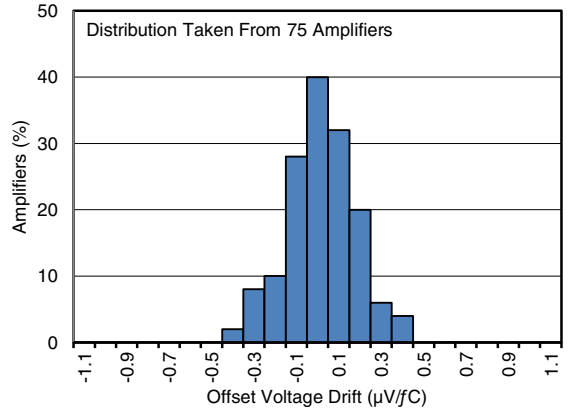
图 5. Offset Voltage Production Distribution at –25°C



T_A = –40° C

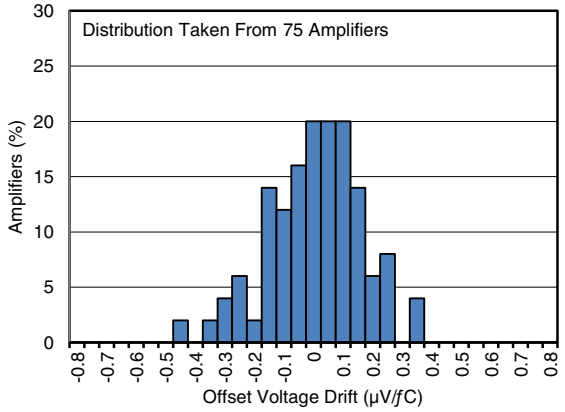
图 6. Offset Voltage Production Distribution at –40°C

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)



T_A = –40°C to +125°C

图 7. Offset Voltage Drift Distribution from –40°C to +125°C



T_A = 0°C to 85°C

图 8. Offset Voltage Drift Distribution from 0°C to 85°C

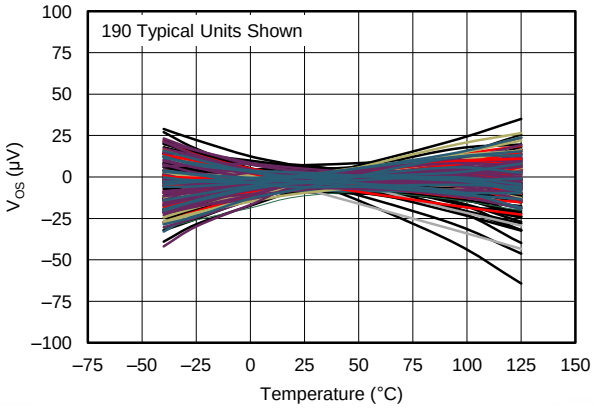


图 9. Offset Voltage vs Temperature

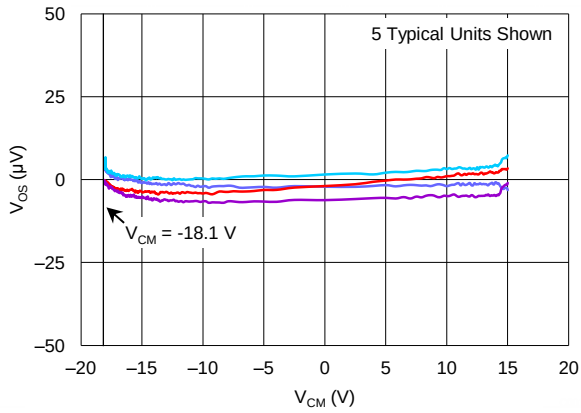


图 10. Offset Voltage vs Common-Mode Voltage

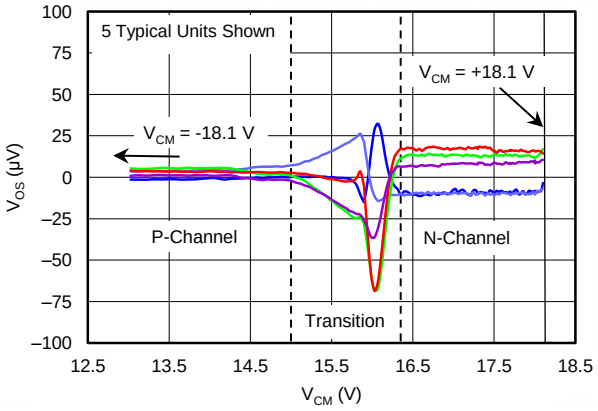
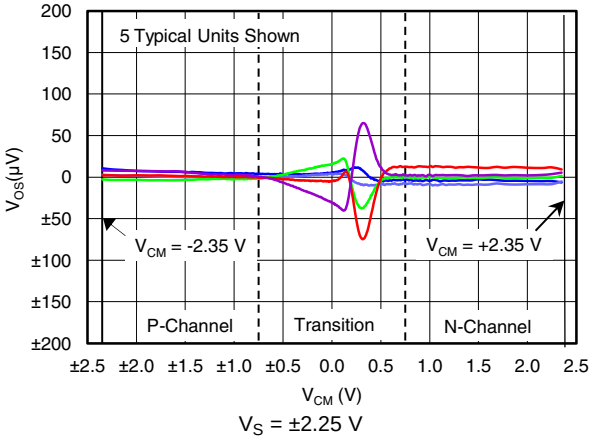


图 11. Offset Voltage vs Common-Mode Voltage



V_S = ±2.25 V

图 12. Offset Voltage vs Common-Mode Voltage

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

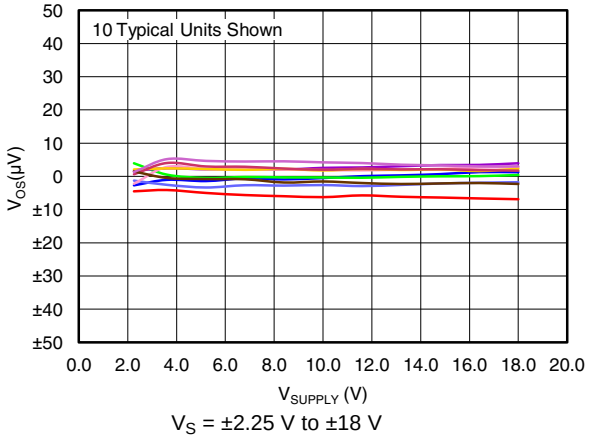


图 13. Offset Voltage vs Power Supply

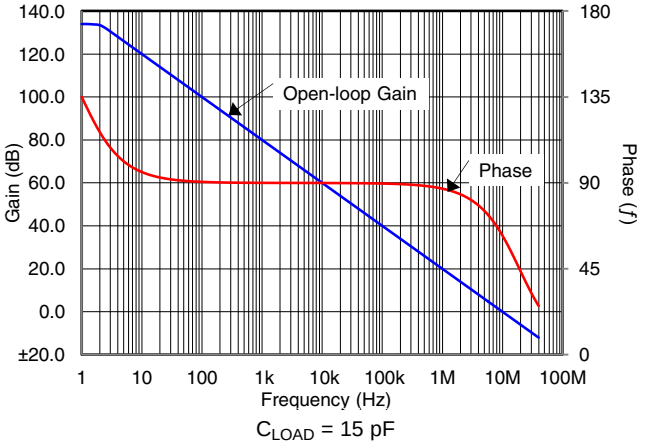


图 14. Open-Loop Gain and Phase vs Frequency

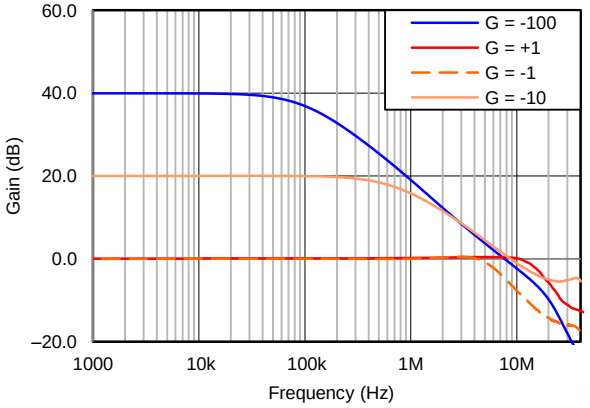


图 15. Closed-Loop Gain and Phase vs Frequency

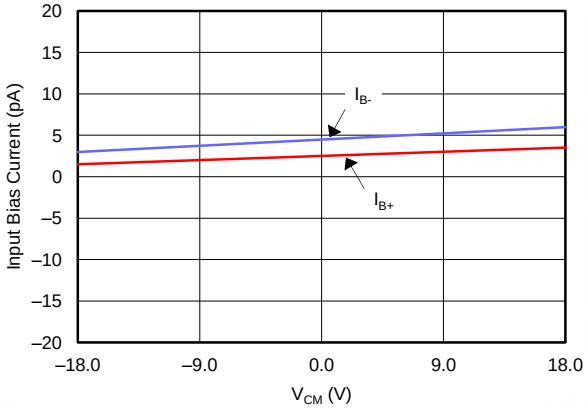


图 16. Input Bias Current vs Common-Mode Voltage

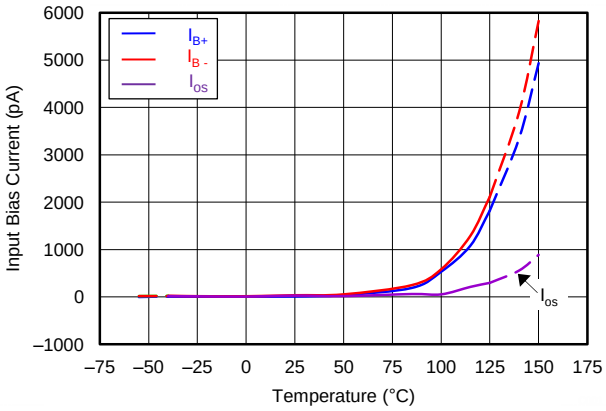


图 17. Input Bias Current vs Temperature

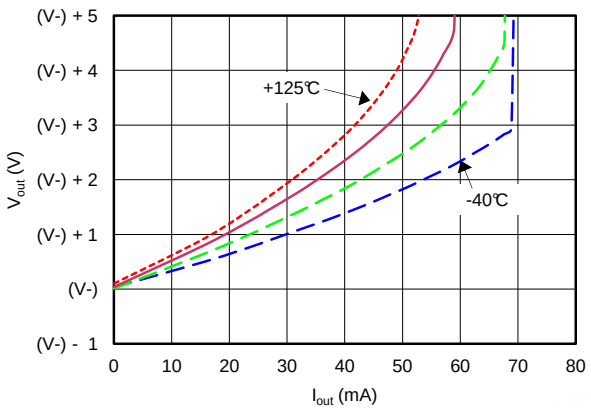


图 18. Output Voltage Swing vs Output Current (Maximum Supply)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

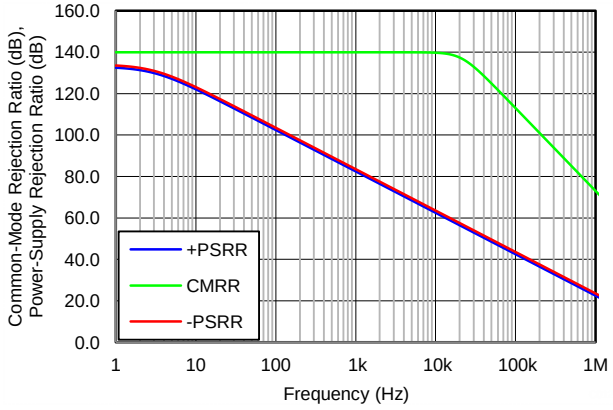


图 19. CMRR and PSRR vs Frequency

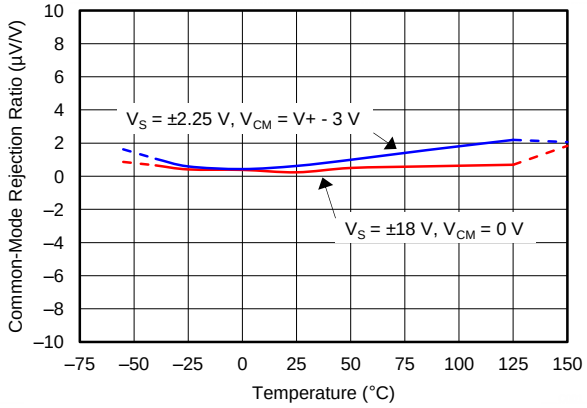


图 20. CMRR vs Temperature

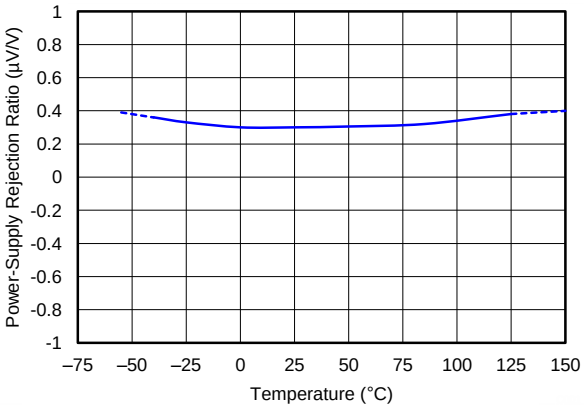


图 21. PSRR vs Temperature

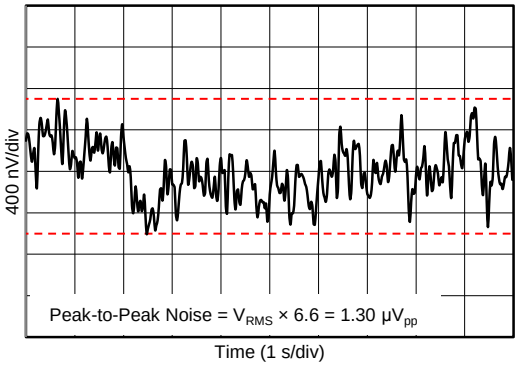


图 22. 0.1-Hz to 10-Hz Noise

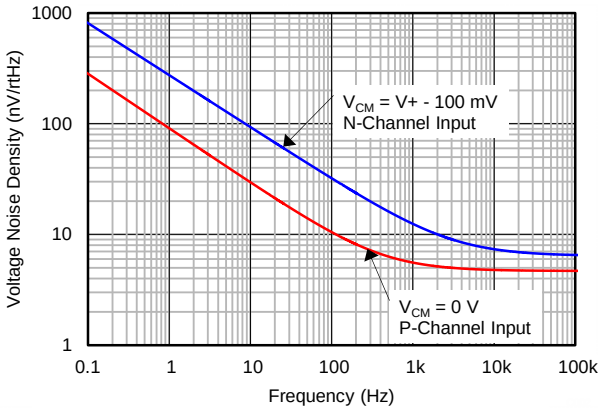


图 23. Input Voltage Noise Spectral Density vs Frequency

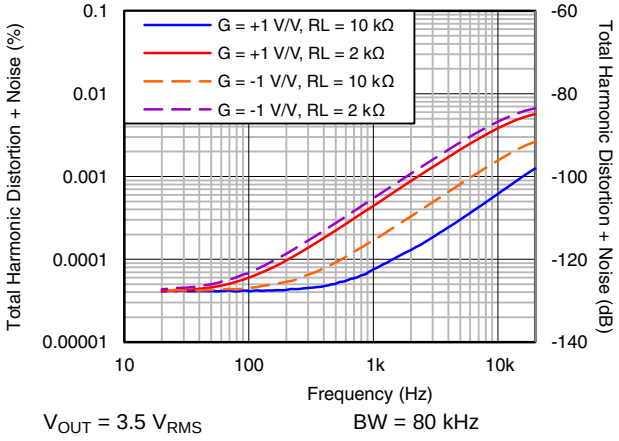


图 24. THD+N Ratio vs Frequency

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

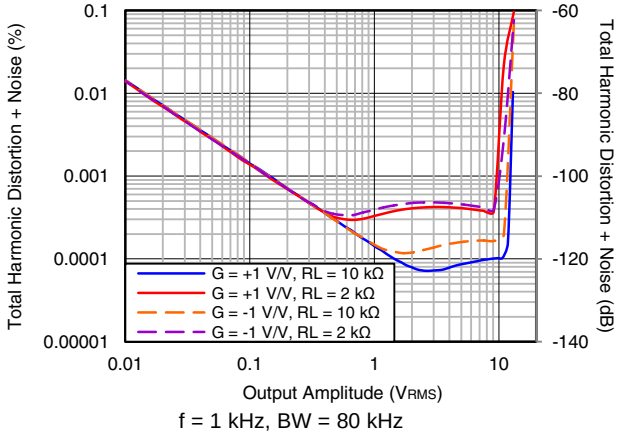


图 25. THD+N vs Output Amplitude

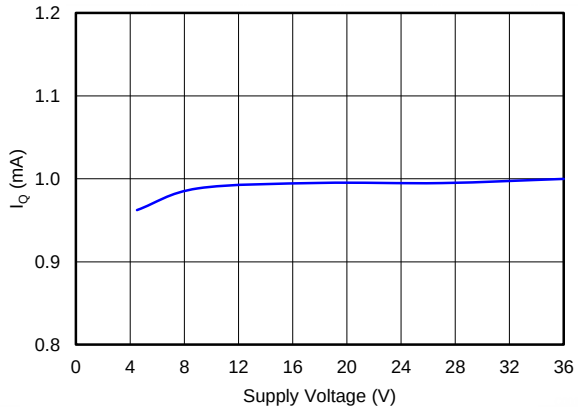


图 26. Quiescent Current vs Supply Voltage

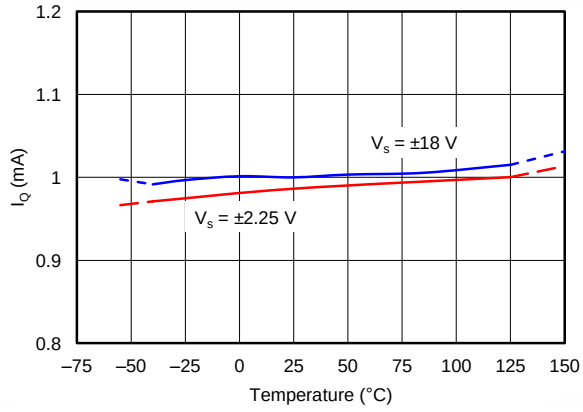


图 27. Quiescent Current vs Temperature

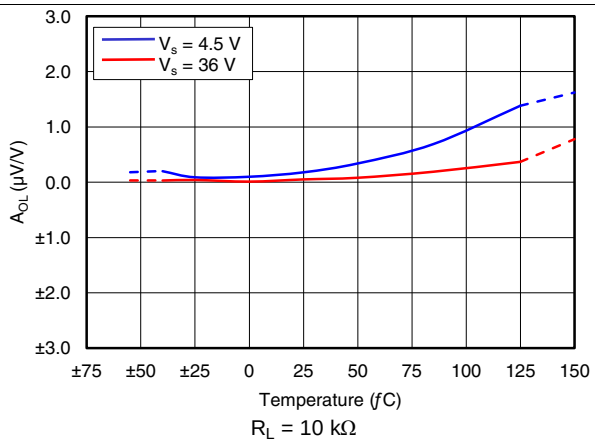


图 28. Open-Loop Gain vs Temperature

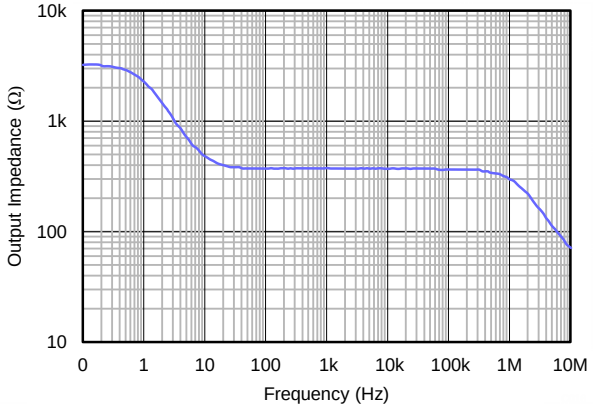


图 29. Open-Loop Output Impedance vs Frequency

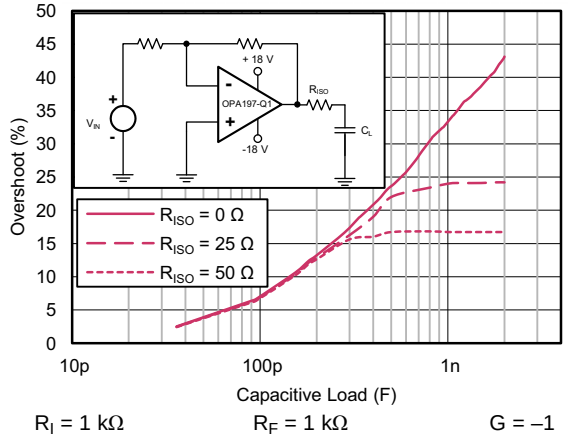


图 30. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

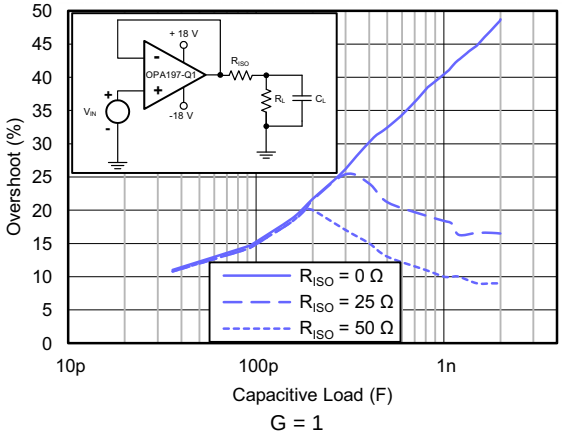


图 31. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

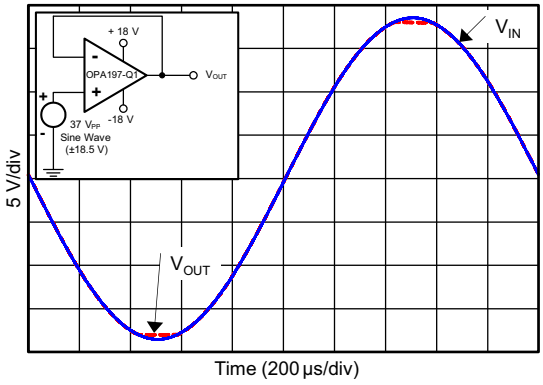
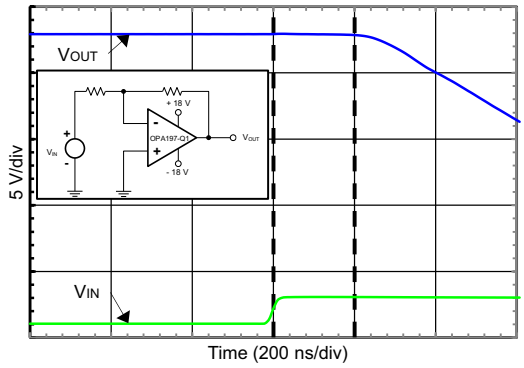
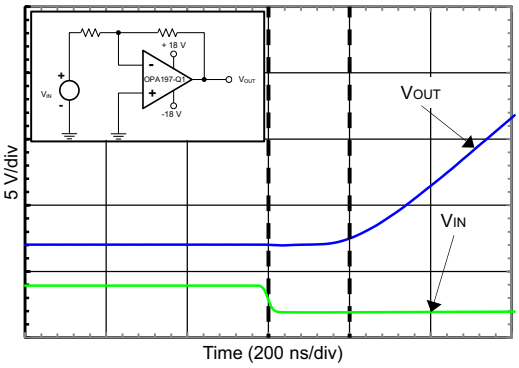


图 32. No Phase Reversal



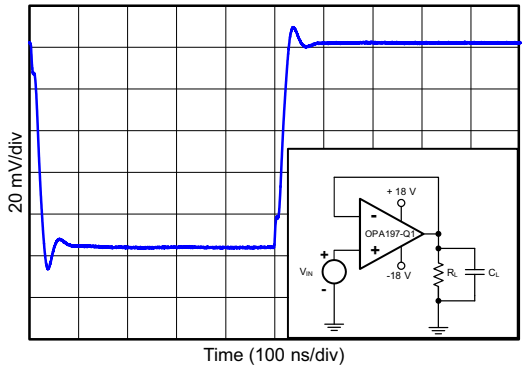
R_I = 1 kΩ R_F = 10 kΩ G = –10

图 33. Positive Overload Recovery



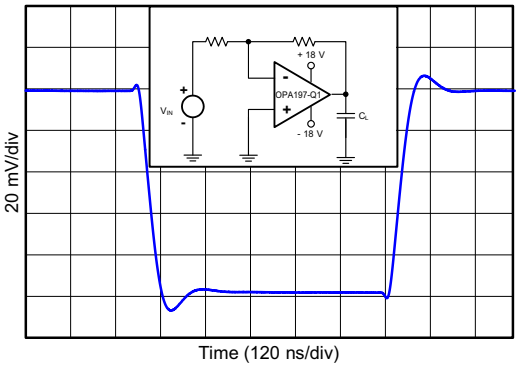
R_I = 1 kΩ G = –10 R_F = 10 kΩ

图 34. Negative Overload Recovery



C_L = 10 pF G = 1

图 35. Small-Signal Step Response (100 mV)



R_L = 1 kΩ C_L = 10 pF G = –1

图 36. Small-Signal Step Response (100 mV)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

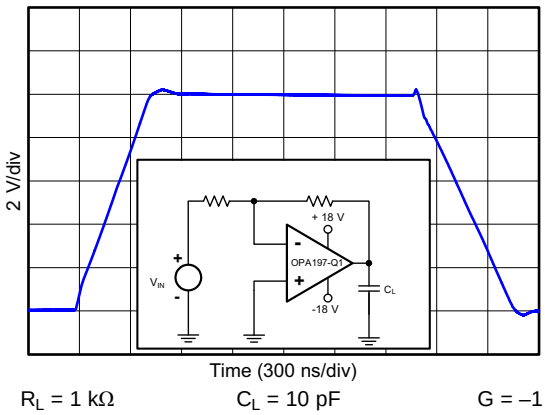


图 37. Large-Signal Step Response

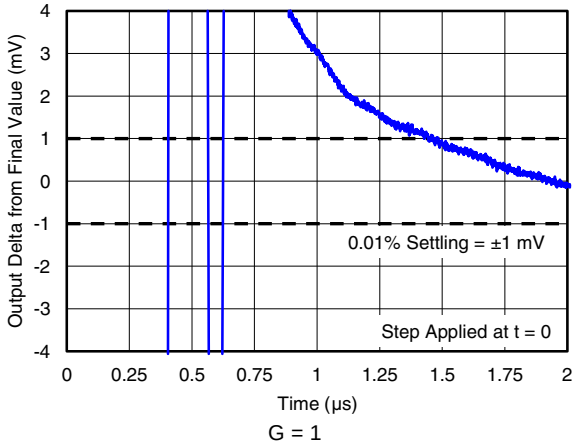


图 38. Settling Time (10-V Positive Step)

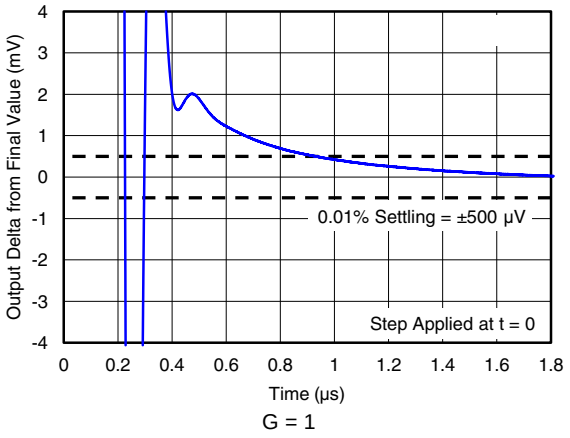


图 39. Settling Time (5-V Positive Step)

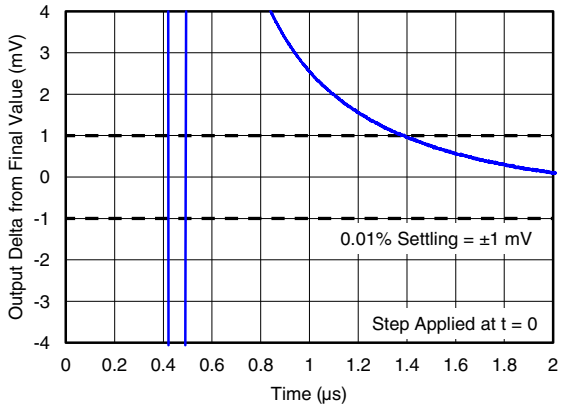


图 40. Settling Time (10-V Negative Step)

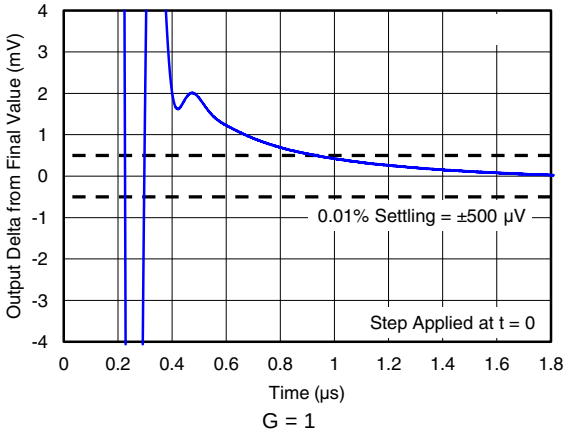


图 41. Settling Time (5-V Negative Step)

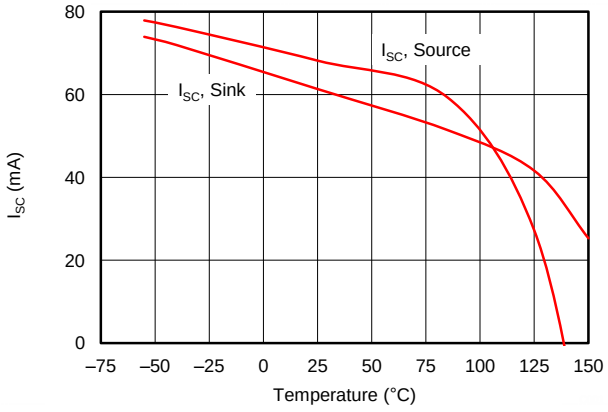


图 42. Short-Circuit Current vs Temperature

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

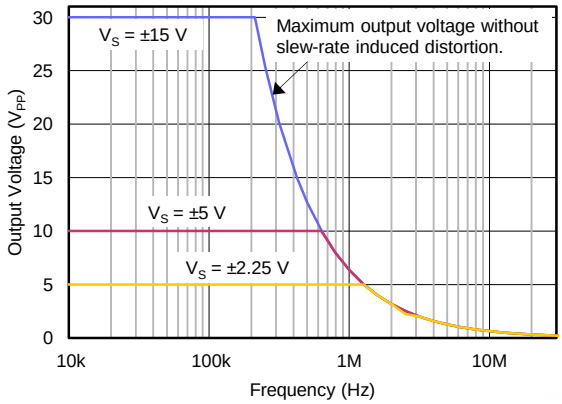


图 43. Maximum Output Voltage vs Frequency

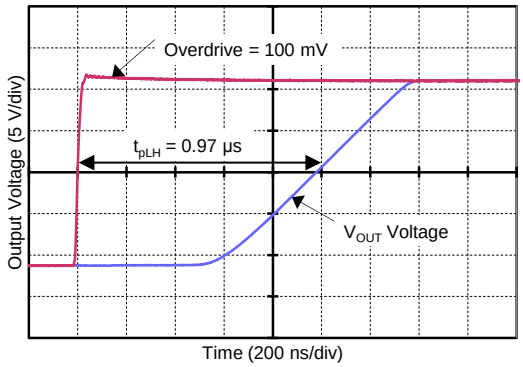


图 44. Propagation Delay Rising Edge

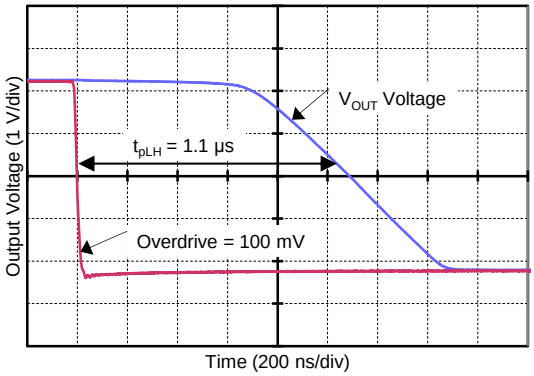


图 45. Propagation Delay Falling Edge

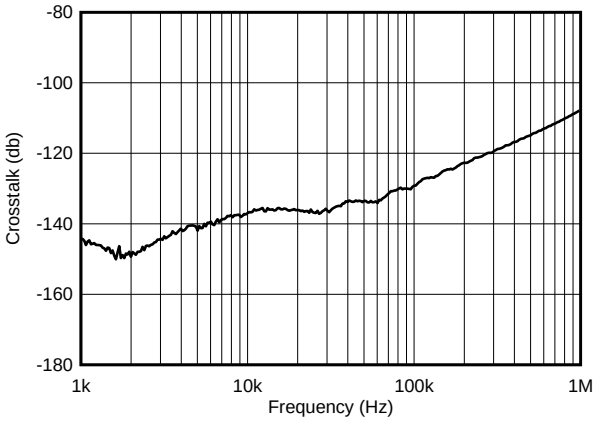


图 46. Crosstalk vs Frequency

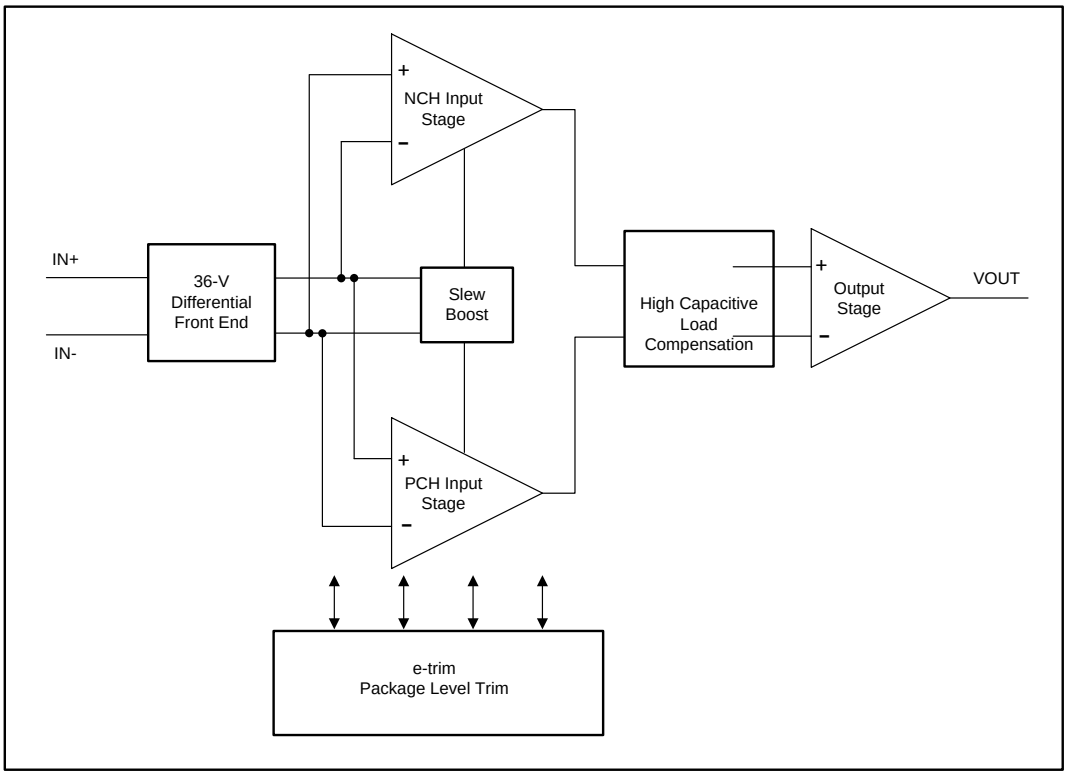
7 Detailed Description

7.1 Overview

The OPAx197-Q1 family of operational amplifiers use *e-trim*, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. The *Functional Block Diagram* shows the simplified diagram of the OPAx197-Q1 with e-trim.

Unlike previous e-trim op amps, the OPAx197-Q1 uses a patented two-temperature trim architecture to achieve a very low offset voltage of 25 µV (maximum) and low voltage offset drift of 0.5 µV/°C (maximum) over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection Circuitry

The OPAx197-Q1 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in 图 47 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in 图 48. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current, and resulting in extended settling time, as shown in 图 49.

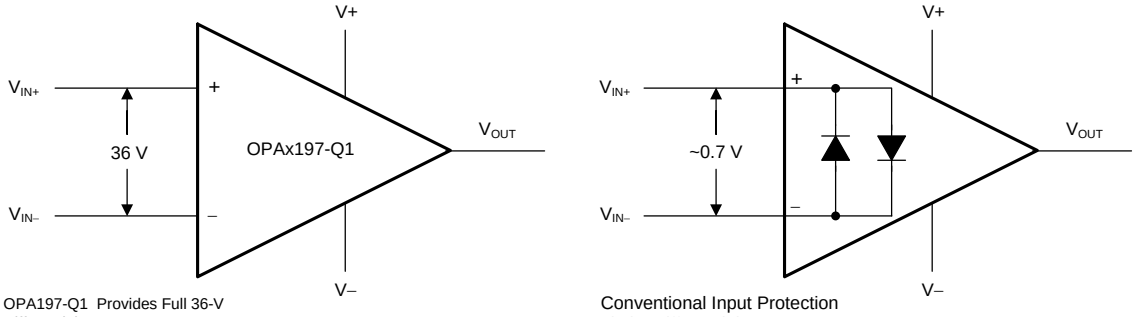


图 47. OPAx197-Q1 Input Protection Does Not Limit Differential Input Capability

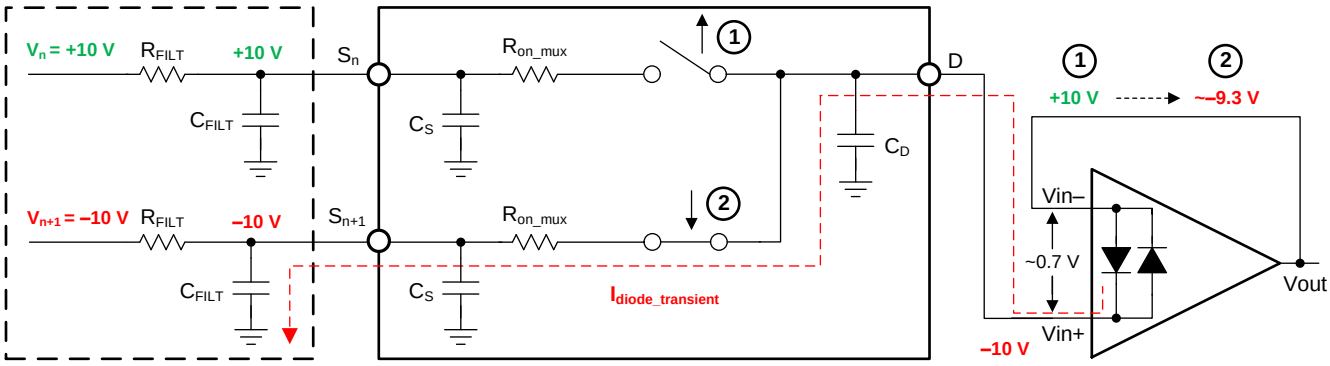


图 48. Back-to-Back Diodes Create Settling Issues

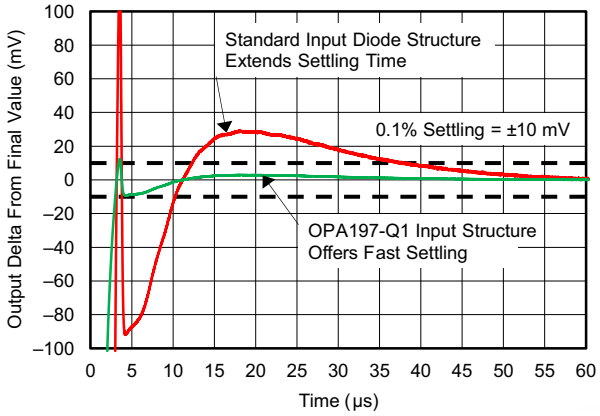


图 49. OPAx197-Q1 Protection Circuit Maintains Fast-Settling Transient Response

Feature Description (接下页)

The OPAx197-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPAx197-Q1 can tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems; see 图 59.

7.3.2 EMI Rejection

The OPAx197-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx197-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 50 shows the results of this testing on the OPAx197-Q1. 表 2 shows the EMIRR IN+ values for the OPAx197-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the TI application report *EMI Rejection Ratio of Operational Amplifiers* available for download from www.ti.com.

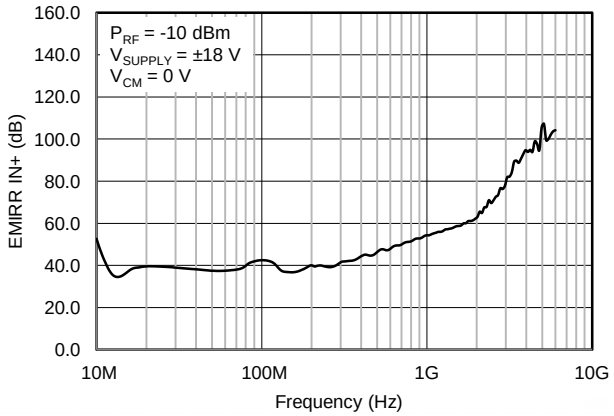


图 50. EMIRR Testing

表 2. OPAx197-Q1 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	44.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	61.0 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.5 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105.5 dB

7.3.3 Phase Reversal Protection

The OPAx197-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx197-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 图 51.

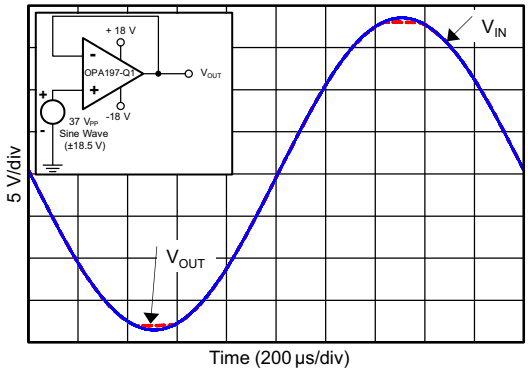


图 51. No Phase Reversal

7.3.4 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx197-Q1 is 150°C. Exceeding this temperature causes damage to the device. The OPAx197-Q1 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. 图 52 shows an application example for the OPAx197-Q1 that has significant self heating (159°C) because of the power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. 图 52 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

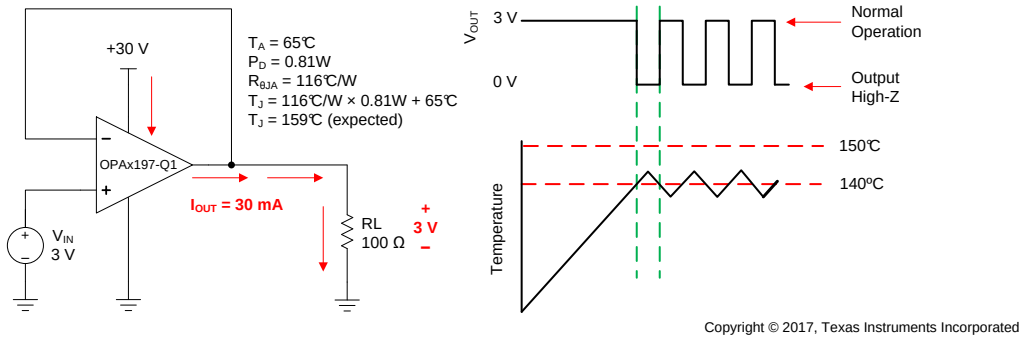


图 52. Thermal Protection

7.3.5 Capacitive Load and Stability

The OPAx197-Q1 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 53 and 图 54. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

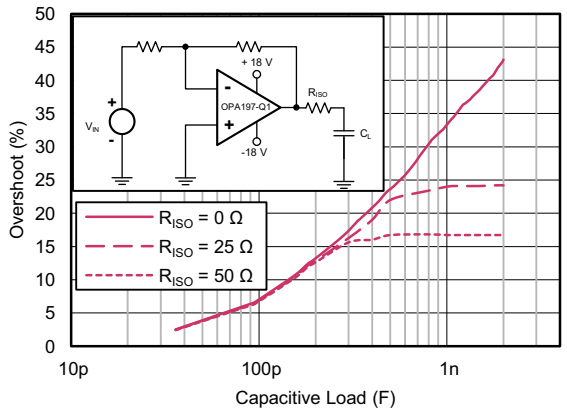


图 53. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

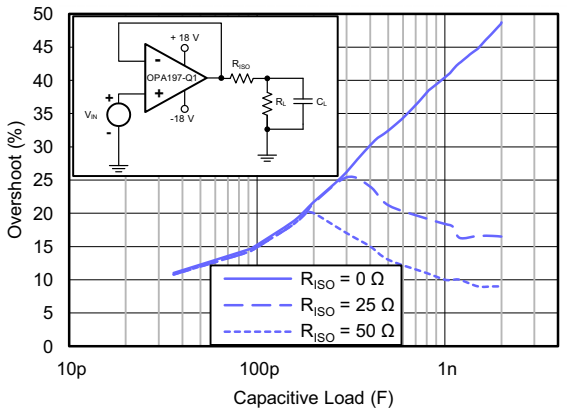


图 54. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10-Ω to 20-Ω) resistor, R_{ISO}, in series with the output, as shown in 图 55. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx197-Q1 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 55 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin, and results using the OPAx197-Q1 are summarized in 表 3. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

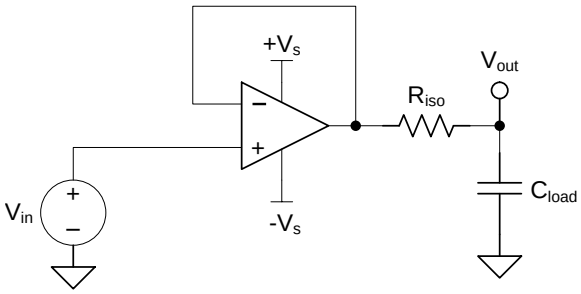


图 55. Extending Capacitive Load Drive with the OPAx197-Q1

表 3. OPAx197-Q1 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results

PARAMETER	VALUE									
Capacitive Load	100 pF		1000 pF		0.01 µF		0.1 µF		1 µF	
Phase Margin	45°	60°	45°	60°	45°	60°	45°	60°	45°	60°
R_{ISO} (Ω)	47	360	24	100	20	51	6.2	15.8	2	4.7
Measured Overshoot (%)	23.2 8.6	10.4	22.5	9	22.1	8.7	23.1	8.6	21	8.6
Calculated PM	45.1°	58.1°	45.8°	59.7°	46.1°	60.1°	45.2°	60.2°	47.2°	60.2°

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design TIDU032, *Capacitive Load Drive Solution using an Isolation Resistor* .

7.3.6 Common-Mode Voltage Range

The OPAx197-Q1 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 图 56. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation outside this region.

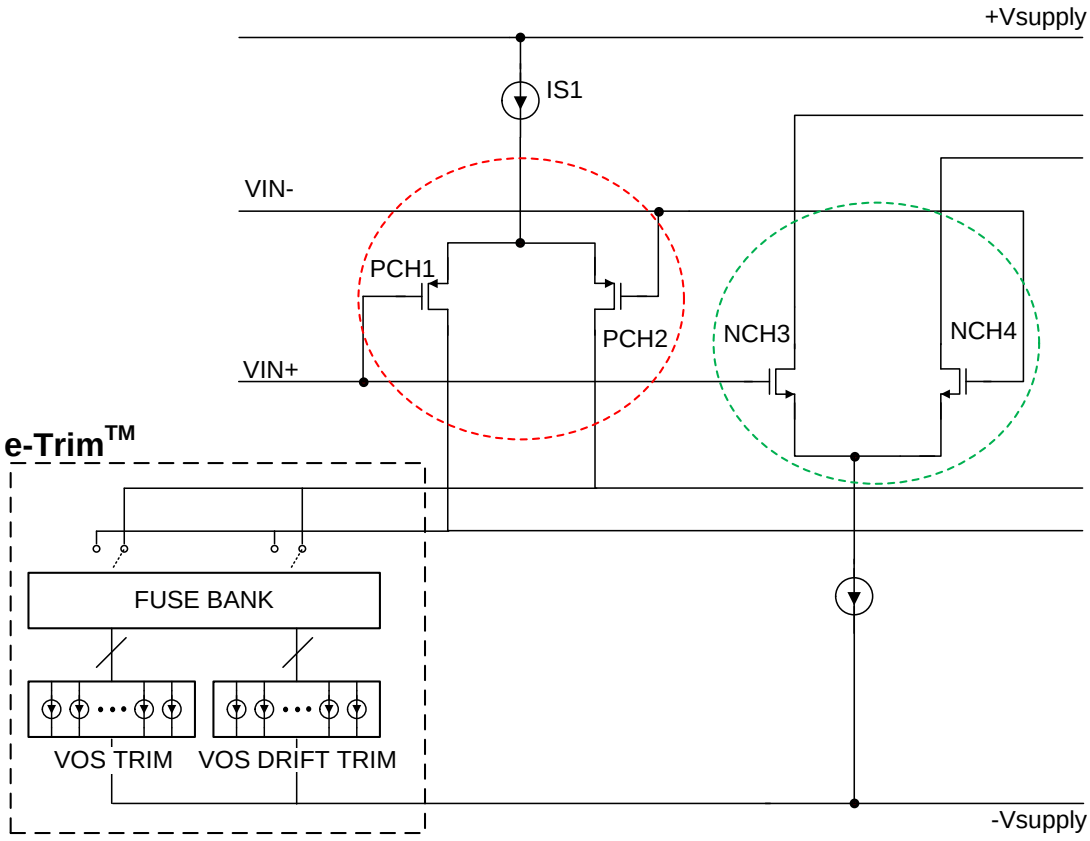


图 56. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx197-Q1 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in 图 57.

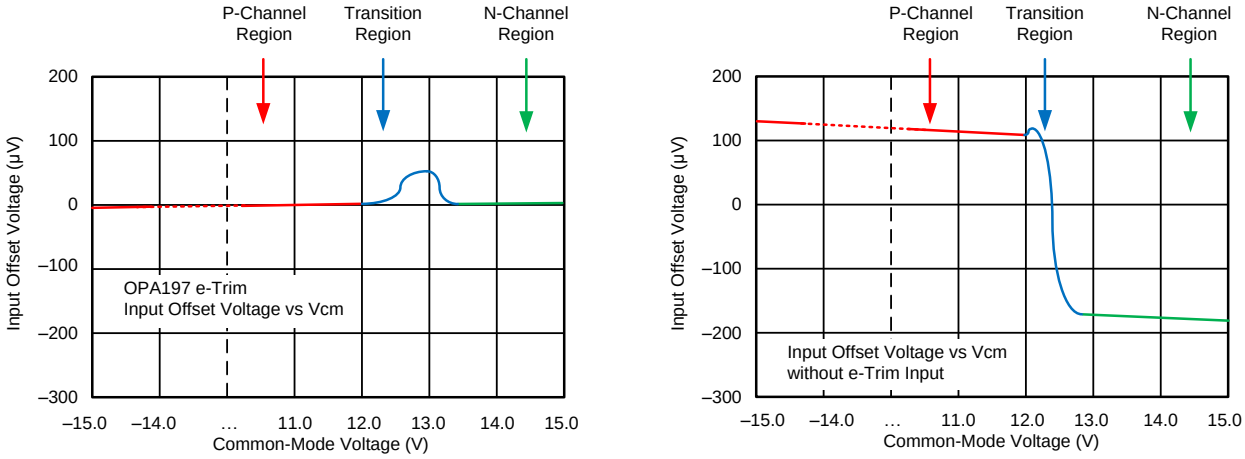


图 57. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 58 shows an illustration of the ESD circuits contained in the OPAx197-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

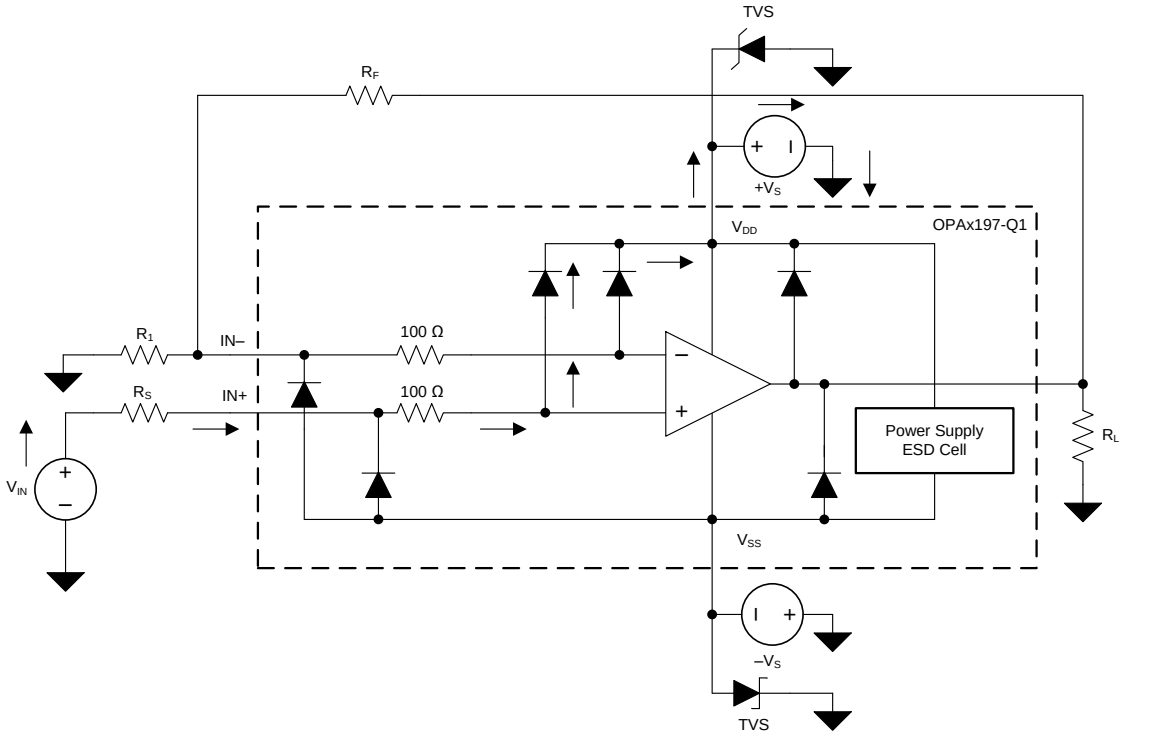


图 58. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx197-Q1 is approximately 200 ns.

7.4 Device Functional Modes

The OPAx197-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx197-Q1 is 36 V (±18 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx197-Q1 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input and output, ultra-low offset voltage and offset voltage drift, as well as 10-MHz bandwidth and high capacitive load drive. These features make the OPAx197-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 16-Bit Precision Multiplexed Data-Acquisition System

图 59 shows a 16-bit, differential, 4-channel, multiplexed data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential multiplexer (mux). This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the OPAx197-Q1 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

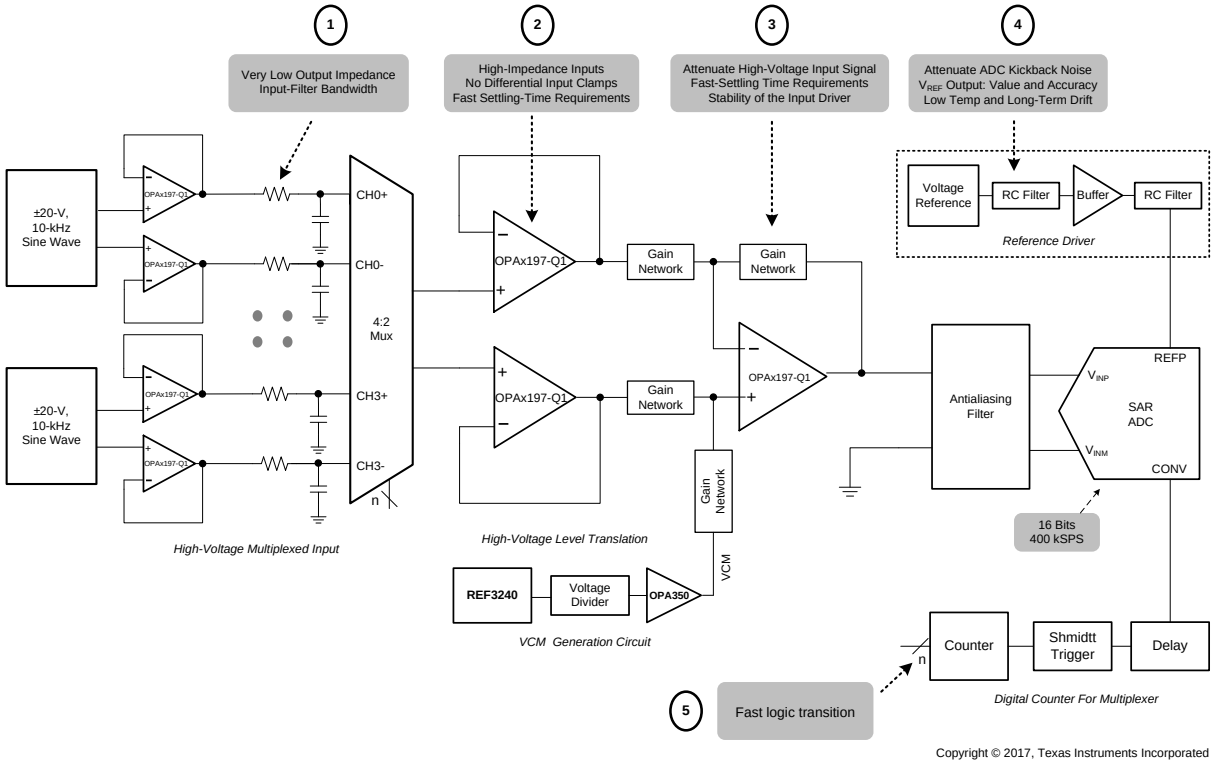


图 59. OPAx197-Q1 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion

Typical Applications (接下页)

8.2.1.1 Design Requirements

The primary objective is to design a ±20 V, differential 4-channel multiplexed data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10 kHz full-scale pure sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

8.2.1.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal high voltage multiplexed data acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in 图 59. The circuit is a multichannel data acquisition signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for mux and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision multiplexed data acquisition system are the mux input analog front-end and the high-voltage level translation SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. 图 59 includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for extremely low impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input when maintaining amplifier stability. The next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

8.2.1.3 Application Curve

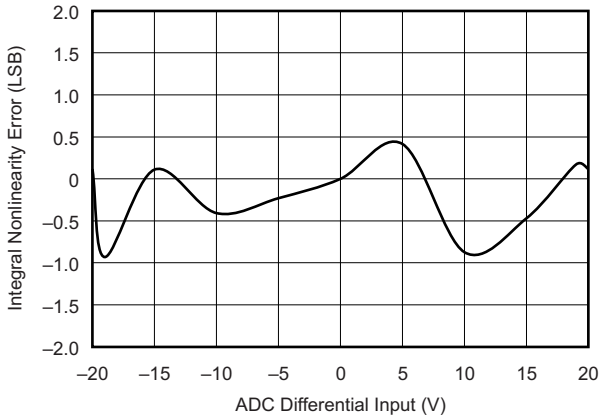


图 60. ADC 16-Bit Linearity Error for the Multiplexed Data Acquisition Block

8.2.2 Slew-Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx197-Q1 make the device an optimal amplifier to achieve slew-rate control for both dual- and single-supply systems.图 61 shows the OPAx197-Q1 in a slew-rate limit design.

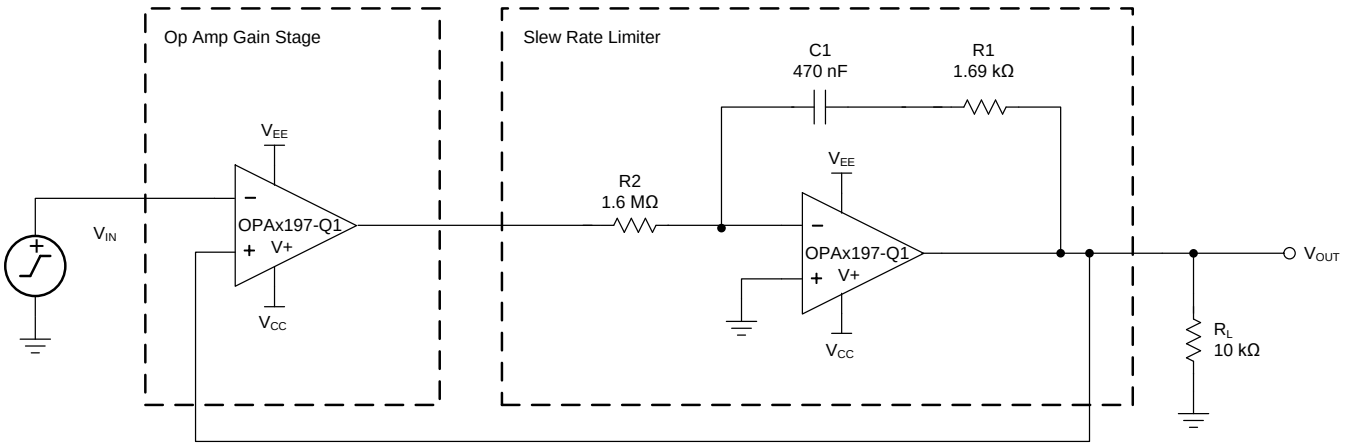


图 61. Slew-Rate Limiter Uses One Op Amp

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see TI Precision Design TIDU026, *Slew Rate Limiter Uses One Op Amp*.

8.2.3 Precision Reference Buffer

The OPAx197-Q1 features high output-current-drive capability and low input offset voltage, making the device an excellent reference buffer to provide an accurate buffered output with ample drive current for transients. For the 10-µF ceramic capacitor shown in 图 62, R_{ISO}, a 37.4-Ω isolation resistor, provides separation of two feedback paths for optimal stability. Feedback path number one is through R_F and is directly at the output (V_{OUT}). Feedback path number two is through R_{Fx} and C_F and is connected at the output of the op amp. The optimized stability components shown for the 10-µF load give a closed-loop signal bandwidth at V_{OUT} of 4 kHz and still provides a loop gain phase margin of 89°. Any other load capacitances require recalculation of the stability components: R_F, R_{Fx} , C_F , and R_{ISO}.

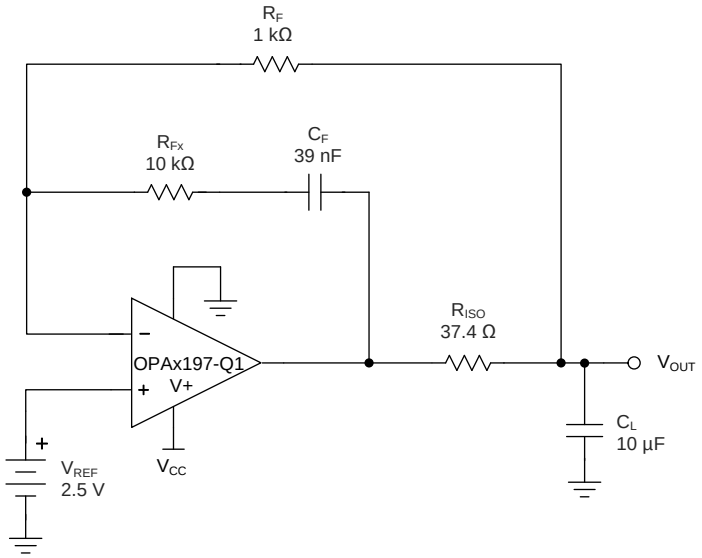


图 62. Precision Reference Buffer

9 Power Supply Recommendations

The OPAx197-Q1 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in 图 64, keep RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Examples

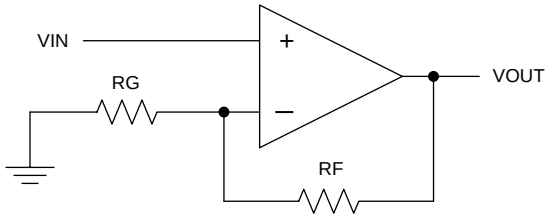


图 63. Schematic Representation

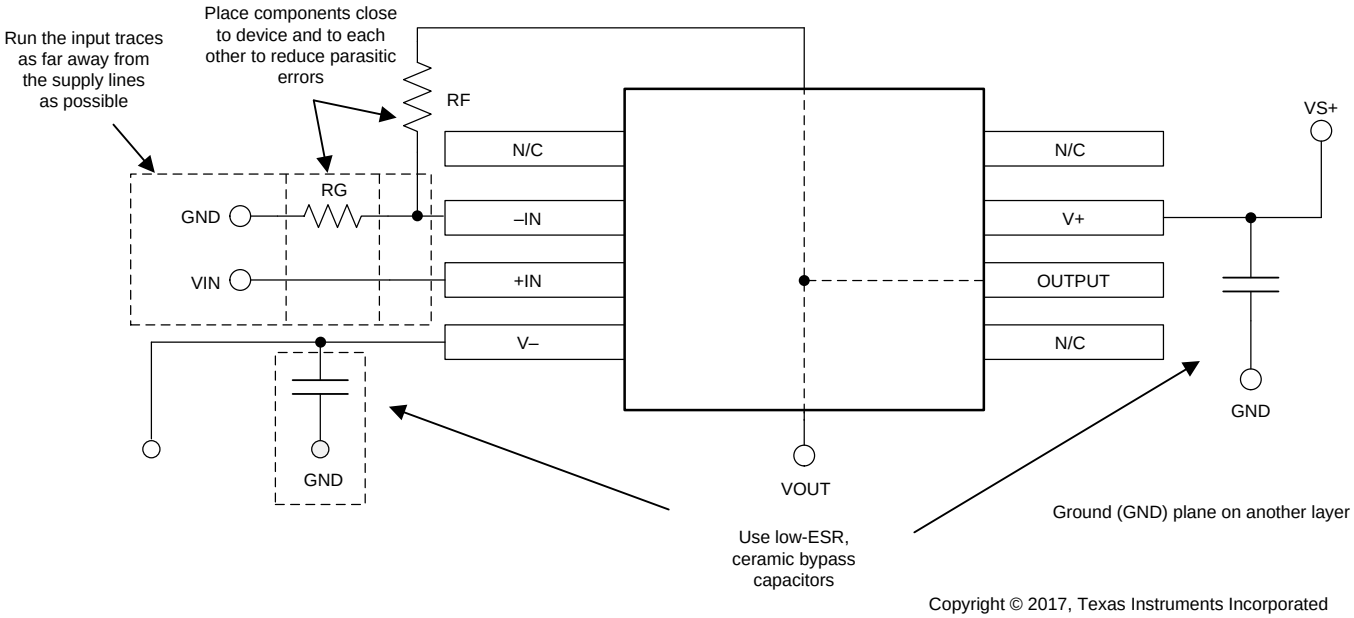


图 64. Operational Amplifier Board Layout for Noninverting Configuration

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 TI 高精度设计

OPA197 采用多种德州仪器 (TI) 精密设计，可通过 http://www.ti.com/ww/en/analog/precision-designs/ 在线获取这些设计。TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

11.2 文档支持

11.2.1 相关文档

如需相关文档，请参阅：

- TI 应用报告 *《运算放大器的 EMI 抑制比》*
- TI 设计 *《采用隔离电阻器的电容式负载驱动器解决方案》*

11.3 相关链接

表 4 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 4. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
OPA197-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2197-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。请单击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.6 商标

e-trim, E2E are trademarks of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA197QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	197	Samples
OPA2197QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2197	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

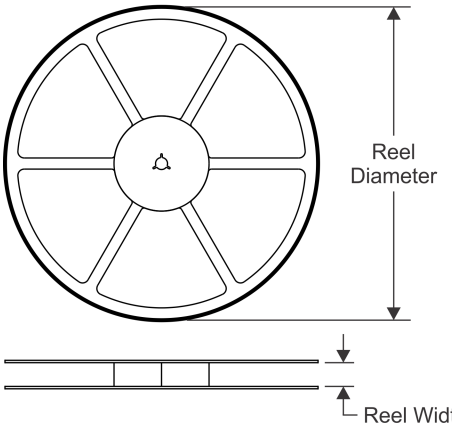
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

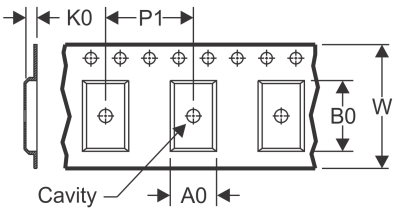
17-Jul-2020

TAPE AND REEL INFORMATION

REEL DIMENSIONS

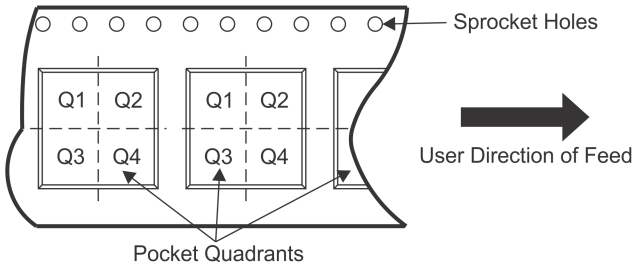


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



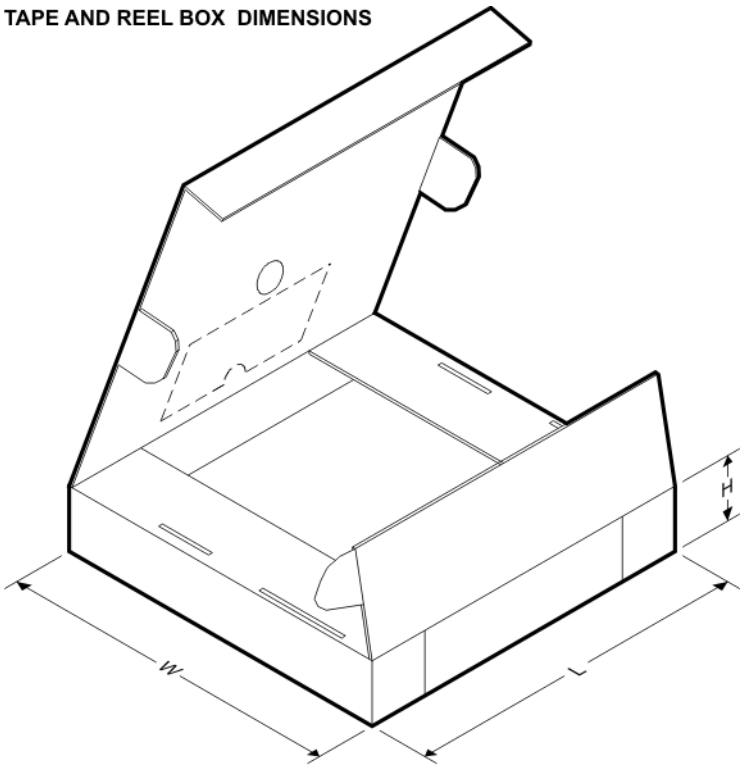
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA197QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2197QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

17-Jul-2020

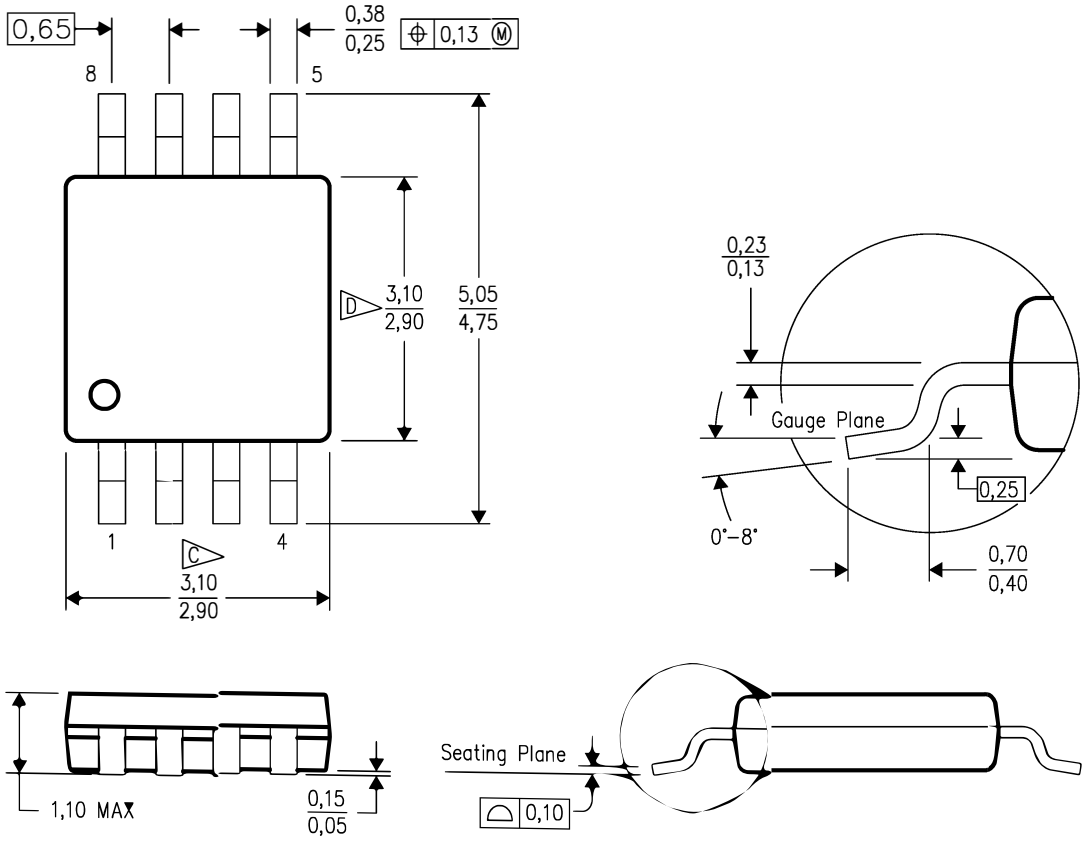
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA197QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2197QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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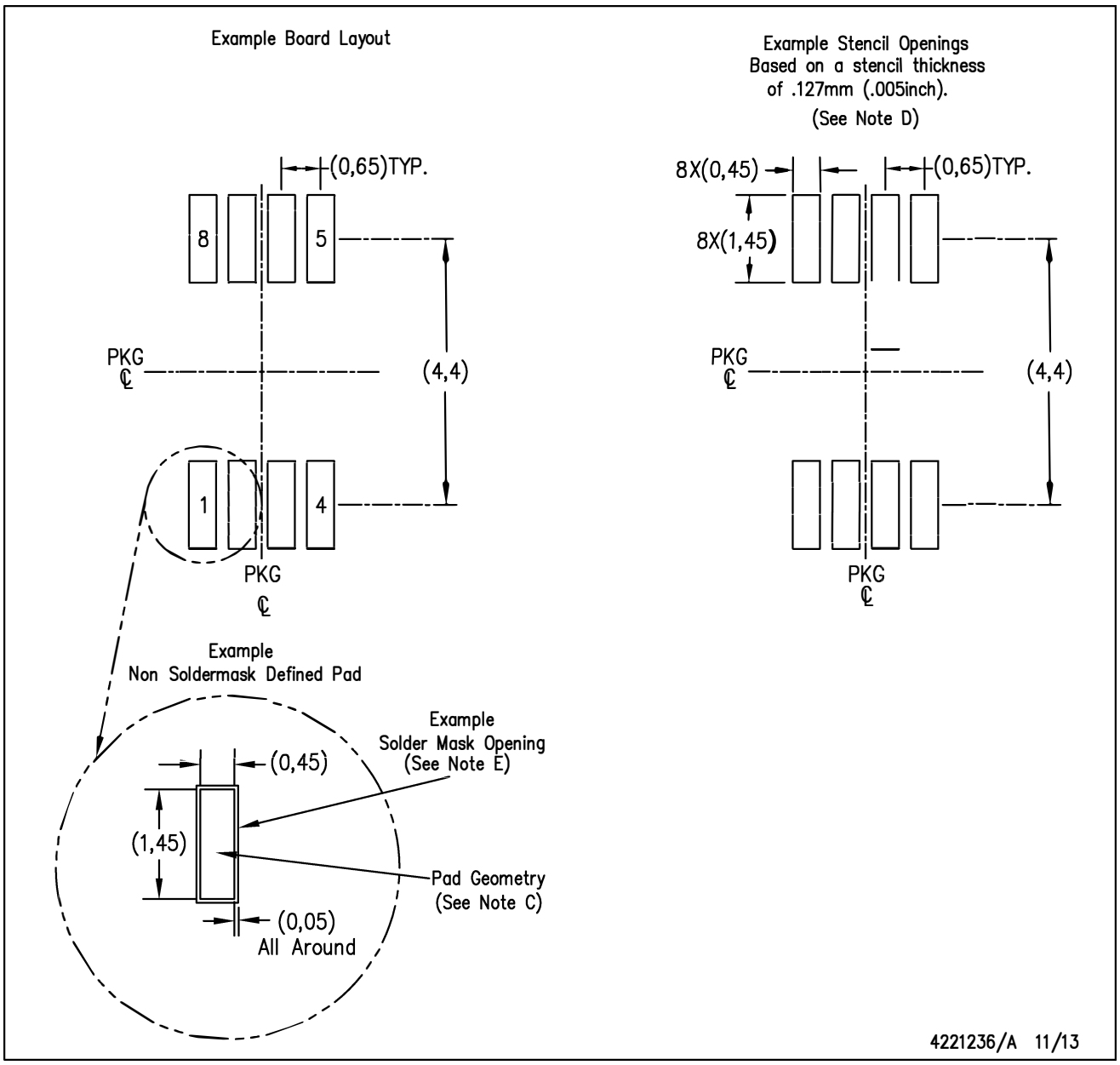
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.