SN74AUP1T08 低功耗、1.8/2.5/3.3V 输入、3.3V CMOS 输出、单路 2 输入{1}正与门

1 特性

- 静电放电 (ESD) 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型{1} (A114-B，II 类)
  - 1000V 充电器件模型 (C101)
- 单电源电压转换器
- 输出电平高达电源 V_{CC}CMOS 电平
  - 1.8V 至 3.3V (V_{CC}=3.3V 时)
  - 2.5V 至 3.3V (V_{CC}=3.3V 时)
  - 1.8V 至 2.5V (V_{CC}=2.5V 时)
  - 3.3V 至 2.5V (V_{CC}=2.5V 时)
- 施密特触发器输入可抑制输入噪声并提供更佳的输出信号完整性
- $I_{关闭}$支持部分断电 (V_{CC}=0)
- 超低静态功耗：
  0.1μA
- 超低动态功耗：
  0.9μA
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- 可提供无铅封装：SC70 (DCK)
  2 x 2.1 x 0.65mm (高 1.1mm)
- 有关更多逻辑门选项，请访问 www.ti.com/littlelogic

2 说明

SN74AUP1T08 执行布尔函数 $Y = A \bullet B$ or $Y = \overline{A + B}$，专门用于逻辑电平转换应用，在此类应用中输出以电源 V_{CC} 为基准。

AUP 技术是行业最低功耗逻辑技术，此技术设计用于扩展运行中的电池寿命。所有接受 1.8V LVCMOS 信号的输入电平，同时由一个单 3.3V 或 2.5V V_{CC} 电源供电运行。该产品还可以保持出色的信号完整性 (请见图 5-1 和图 5-2)。

2.3V 至 3.6V 的宽 V_{CC} 范围有可能实现开关输出电平连接至外部控制器或处理器。

施密特触发器输入 (正负输入转换之间的 ΔV_T=210mV) 改进了开关转换期间的抗扰度，这对于模拟混合模式设计十分有用。施密特触发器输入抑制输入噪声、确保输出信号的完整性并可实现慢输入信号转换。

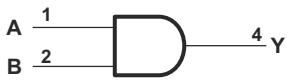
$I_{关闭}$特性可实现省电条件 (V_{CC}=0V)，这在便携式和移动应用中十分重要。当 V_{CC}=0V 时，介于 0V 至 3.6V 范围内的信号可被施加到器件的输入和输出上。在这些条件下，不会对器件造成损坏。

SN74AUP1T08 经设计优化具有 4mA 电流驱动能力，可减少由高驱动输出导致的线路反射、过冲和下冲。

器件信息

器件型号	封装(1)	封装尺寸 (标称值)
SN74AUP1T08	SC70 (5)	2mm x 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图 (与门)

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3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (April 2010) to Revision A (September 2020)	Page
• 添加了*器件信息*表、*器件功能模式*、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1
• 更新了整个文档的表、图和交叉参考的编号格式	1

4 Pin Configuration and Functions

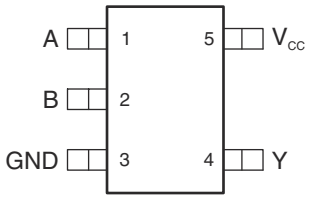


图 4-1. DCK Package 5-Pin SC70 Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage range in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DCK package		259	°C/W
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 Recommended Operating Conditions

See(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–3.1	mA
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		3.1	mA
		V_{CC} = 3 V		4	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.3 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage		2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V
		3 V to 3.6 V	0.75		1.16	0.75	1.19	
V_{T-} Negative-going input threshold voltage		2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V
		3 V to 3.6 V	0.5		0.85	0.5	0.85	
ΔV_T Hysteresis (V_{T+} – V_{T-})		2.3 V to 2.7 V	0.23		0.6	0.1	0.6	V
		3 V to 3.6 V	0.25		0.56	0.15	0.56	
V_{OH}	I_{OH} = –20 μA	2.3 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V

5.3 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
		I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = –3.1 mA		1.9			1.85		
		I_{OH} = –2.7 mA	3 V	2.72			2.67		
		I_{OH} = –4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 μA	2.3 V to 3.6 V			0.1		0.1	V
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	All inputs	V_I = 3.6 V or GND	0 V to 3.6 V			0.1		0.5	μA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.1		0.5	μA
ΔI_{off}		V_I or V_O = 3.6 V	0 V to 0.2 V			0.2		0.5	μA
I_{CC}		V_I = 3.6 V or GND, I_O = 0	2.3 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}		One input at 0.3 V or 1.1 V, Other inputs at 0 or V_{CC}, I_O = 0	2.3 V to 2.7 V					4	μA
		One input at 0.45 V or 1.2 V, Other inputs at 0 or V_{CC}, I_O = 0	3 V to 3.6 V					12	
C_i		V_I = V_{CC} or GND	3.3 V		1.5				pF
C_o		V_O = V_{CC} or GND	3.3 V		3				pF

5.4 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

5.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 2.5 V ± 0.2 V (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 3.3 V ± 0.3 V (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

5.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

5.8 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, V_I = 2.5 V ± 0.2 V (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

5.9 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, V_I = 3.3 V ± 0.3 V (unless otherwise noted) (see 图 6-1)

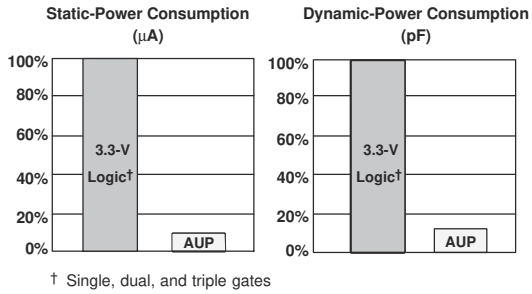
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

5.10 Operating Characteristics

T_A = 25°C

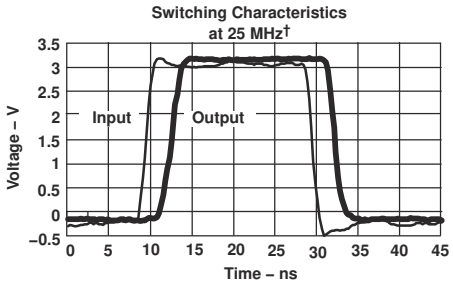
PARAMETER		TEST CONDITIONS	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	4	5	pF

5.11 Typical Characteristics



† Single, dual, and triple gates

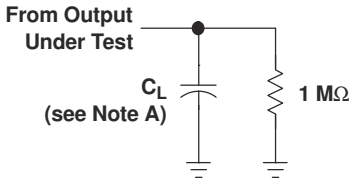
图 5-1. AUP – The Lowest-Power Family



† AUP1G08 data at C_L = 15 pF

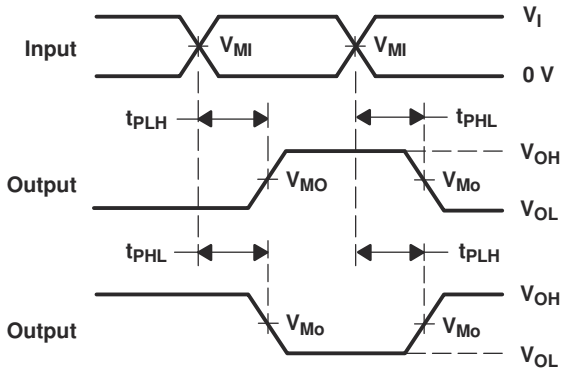
图 5-2. Excellent Signal Integrity

6 Parameter Measurement Information



LOAD CIRCUIT

	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_{MI}	$V_I/2$	$V_I/2$
V_{MO}	$V_{CC}/2$	$V_{CC}/2$



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 6-1. Load Circuit And Voltage Waveforms

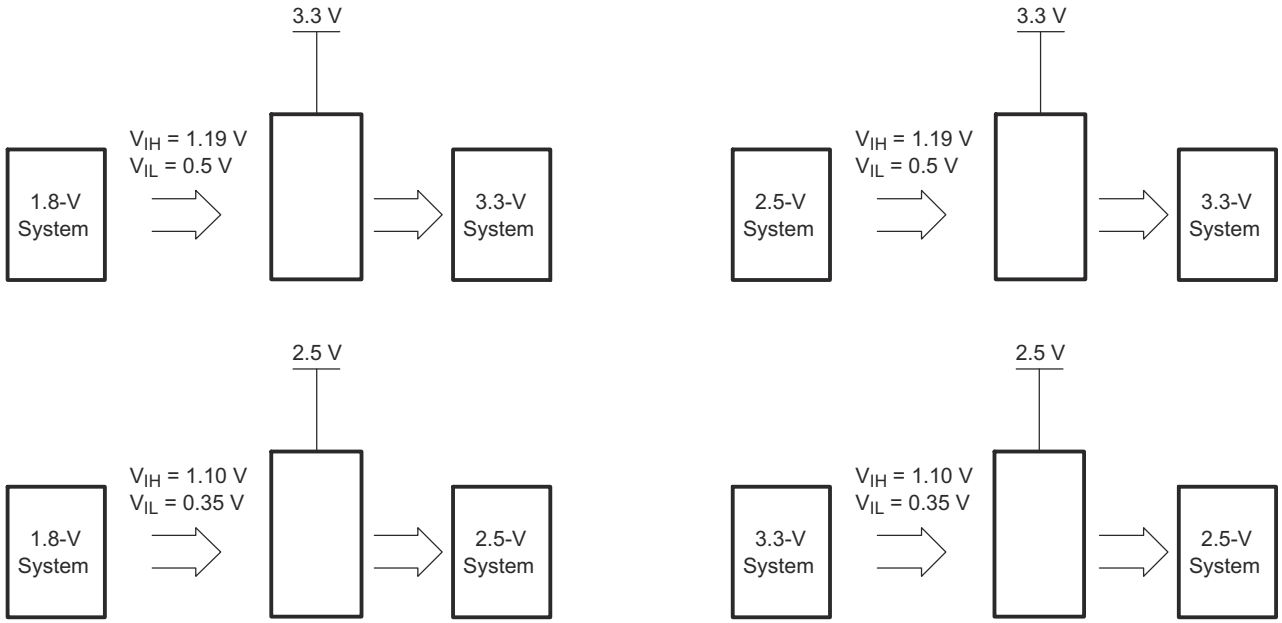


图 6-2. Typical Design Examples

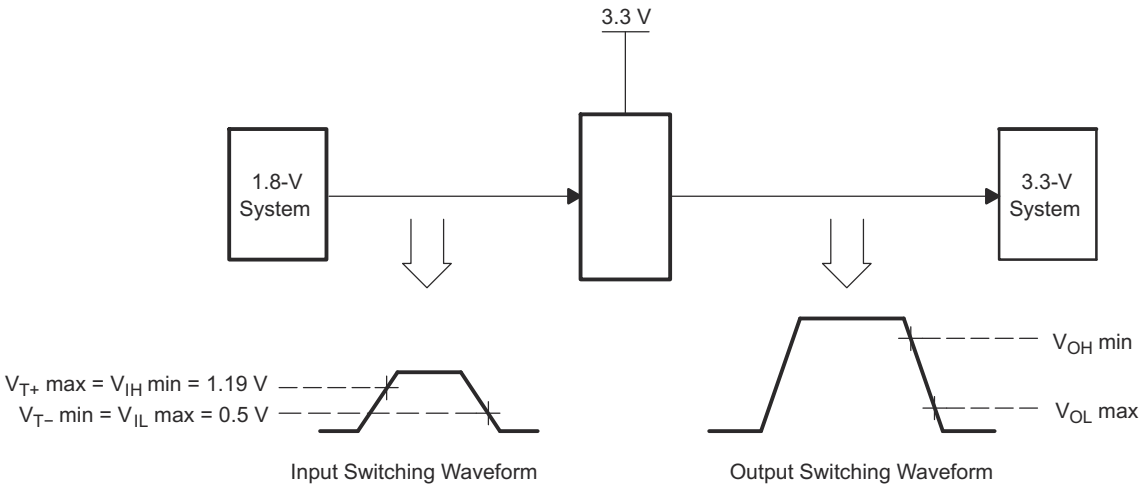


图 6-3. Switching Thresholds For 1.8-V To 3.3-V Translation

7 Detailed Description

7.1 Functional Block Diagram

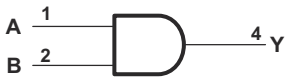


图 7-1. Logic Diagram (AND Gate)

7.2 Device Functional Modes

表 7-1 through 表 7-3 list the functional modes of the SN74AUP1T08 device.

Table 7-1. Function Table

INPUTS (Lower Level Input)		OUTPUT (V_{CC} CMOS)
A	**B**	**Y**
H	H	H
L	X	L
X	L	L

Table 7-2. Supply V_{CC} = 2.3 V To 2.7 V (2.5 V)

INPUTS V_{T+} max = V_{IH} min V_{T-} min = V_{IL} max		OUTPUT CMOS
A	**B**	**Y**
V_{IH} = 1.1 V V_{IL} = 0.35 V		V_{OH} = 1.85 V V_{OL} = 0.45 V

Table 7-3. Supply V_{CC} = 3 V To 3.6 V (3.3 V)

INPUTS V_{T+} max = V_{IH} min V_{T-} min = V_{IL} max		OUTPUT CMOS
A	**B**	**Y**
V_{IH} = 1.19 V V_{IL} = 0.5 V		V_{OH} = 2.55 V V_{OL} = 0.45 V

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T08DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6EF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

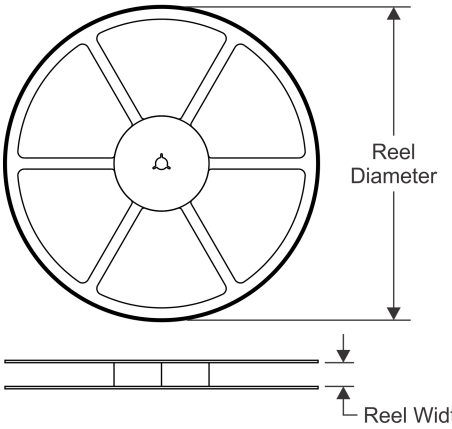
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

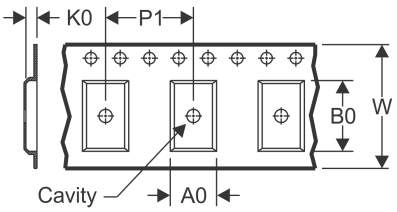
9-Sep-2020

TAPE AND REEL INFORMATION

REEL DIMENSIONS

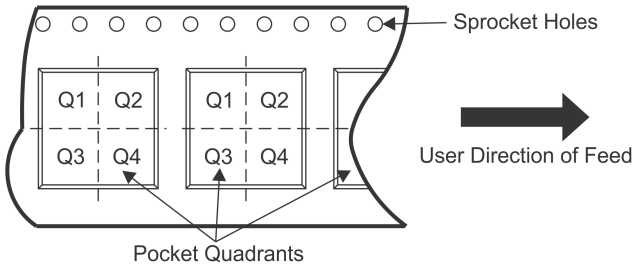


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



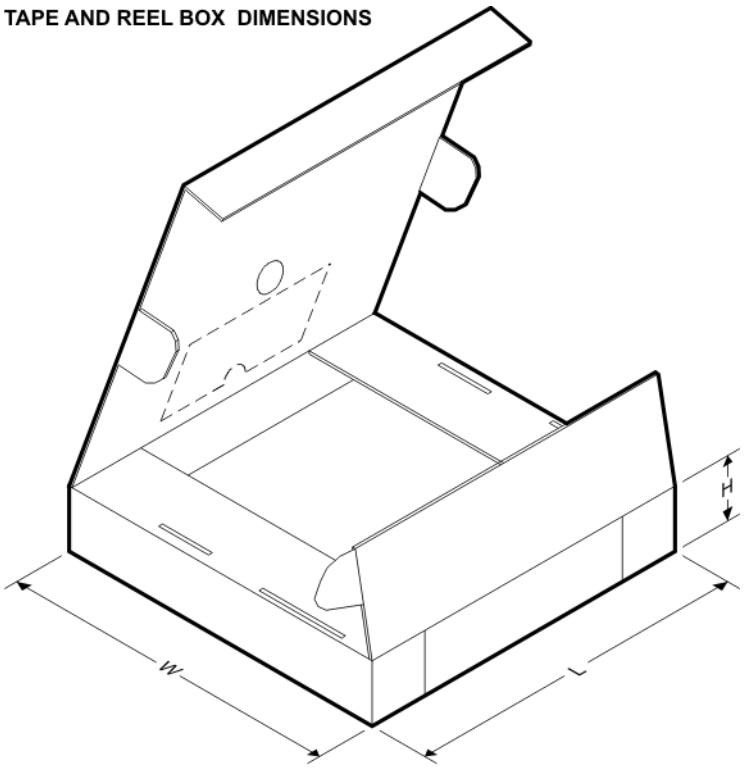
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T08DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

9-Sep-2020

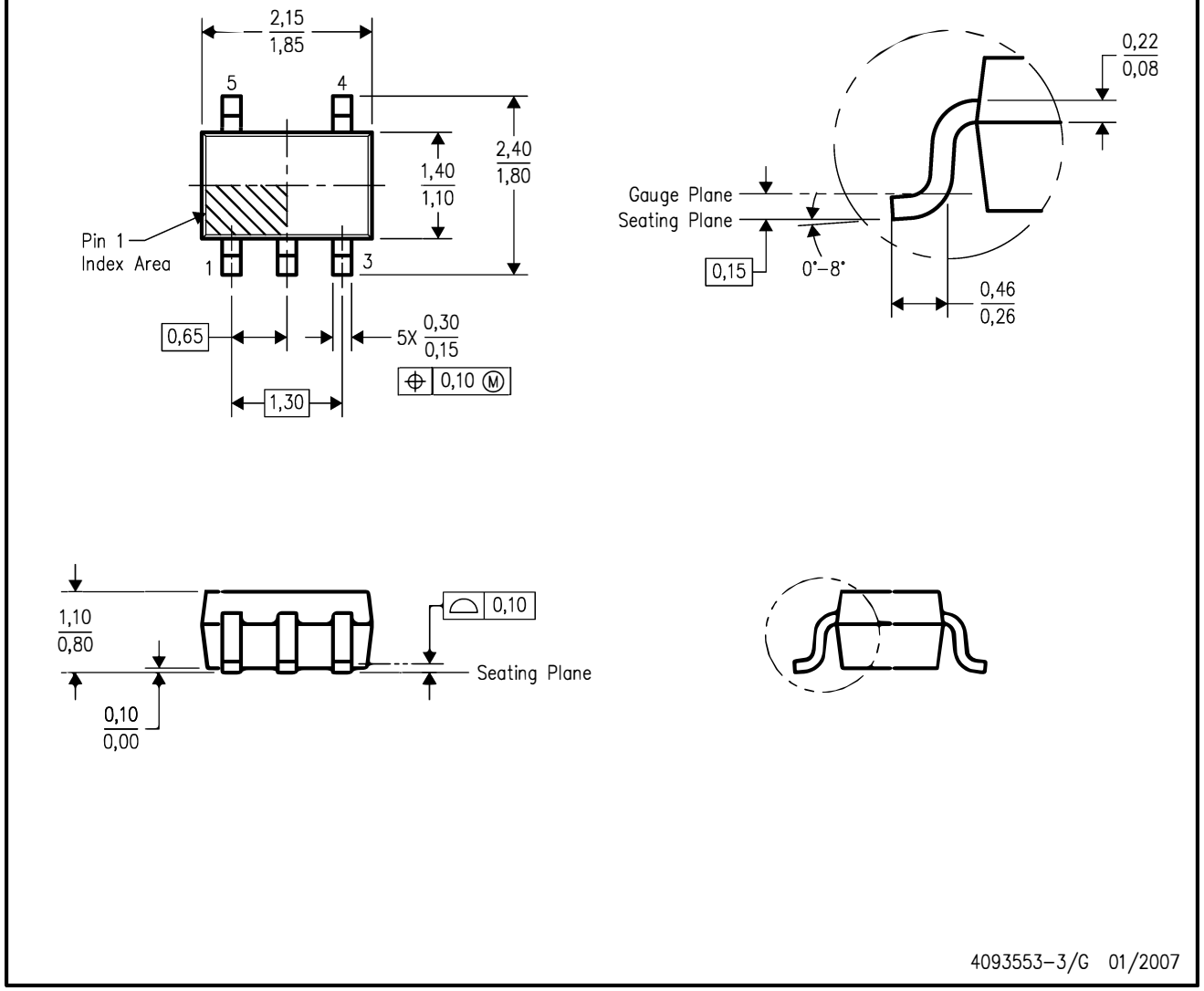
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

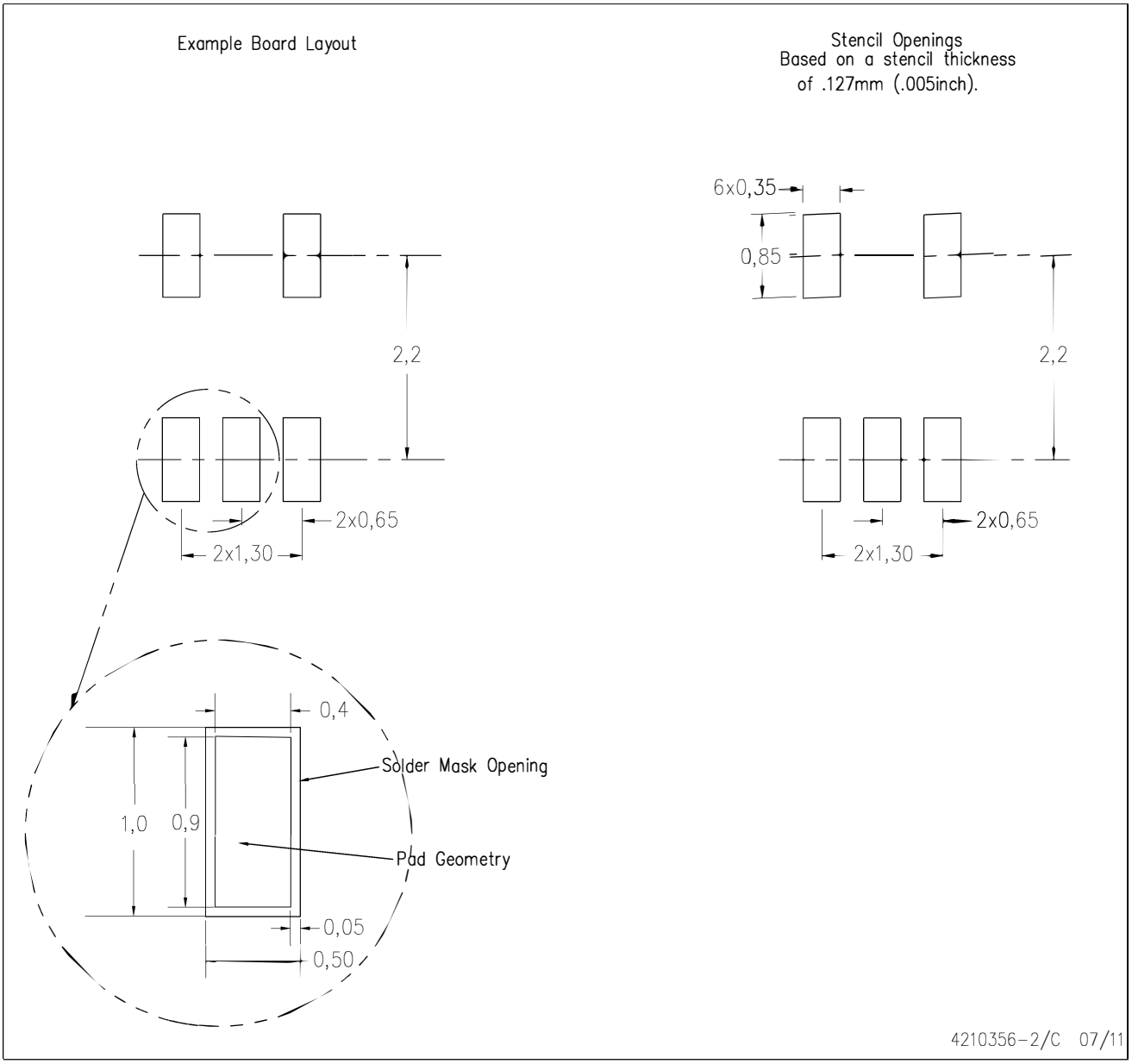
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.