

## SN74AVC4T245 Dual-Bit Bus Transceiver with Configurable Voltage Translation and 3-State Outputs

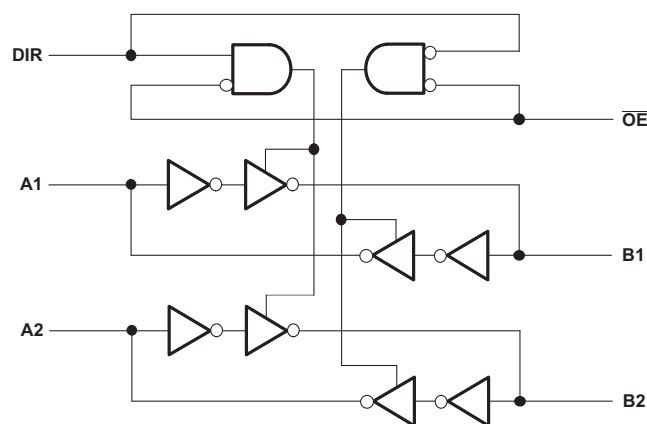
### 1 Features

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- $I_{off}$  Supports Partial Power-Down-Mode Operation
- Maximum Data Rates
  - 380 Mbps (1.8-V to 3.3-V Translation)
  - 200 Mbps (< 1.8-V to 3.3-V Translation)
  - 200 Mbps (Translate to 2.5 V or 1.8 V)
  - 150 Mbps (Translate to 1.5 V)
  - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 150-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

Logic Diagram (Positive Logic)  
for 1/2 of SN74AVC4T245



### 3 Description

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. The SN74AVC4T245 is optimized to operate with  $V_{CCA}/V_{CCB}$  set at 1.4 V to 3.6 V. It is operational with  $V_{CCA}/V_{CCB}$  as low as 1.2 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC4T245 device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

The SN74AVC4T245 device is designed so that the control pins (1DIR, 2DIR, 1OE, and 2OE) are supplied by  $V_{CCA}$ .

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, then both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC4T245	SOIC (16)	9.90 mm x 3.91 mm
	TVSOP (16)	3.60 mm x 4.40 mm
	TSSOP (16)	5.00 mm x 4.40 mm
	VQFN (16)	4.00 mm x 3.50 mm
	UQFN (16)	2.60 mm x 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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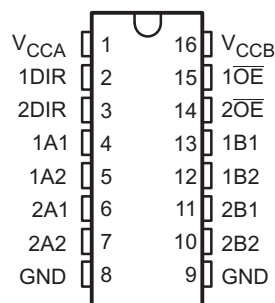
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**4 Revision History**

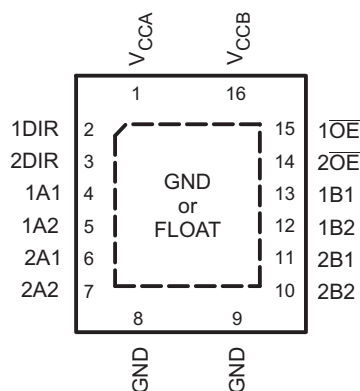
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## 5 Pin Configuration and Functions

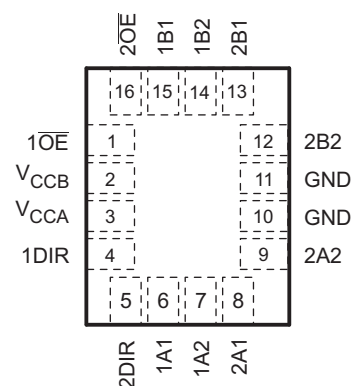
D, DGV, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



RSV PACKAGE  
(TOP VIEW)



### Pin Functions

PIN NAME	NO.		TYPE	DESCRIPTION
	D, DGV, PW, RGY	RSV		
1A1	4	6	I/O	Input/output 1A1. Referenced to $V_{CCA}$ .
1A2	5	7	I/O	Input/output 1A2. Referenced to $V_{CCA}$ .
1B1	13	15	I/O	Input/output 1B1. Referenced to $V_{CCB}$ .
1B2	12	14	I/O	Input/output 1B2. Referenced to $V_{CCB}$ .
1DIR	2	4	I	Direction-control input for '1' ports
1OE	15	1	I	3-state output-mode enables. Pull OE high to place '1' outputs in 3-state mode. Referenced to $V_{CCA}$ .
2A1	6	8	I/O	Input/output 2A1. Referenced to $V_{CCA}$ .
2A2	7	9	I/O	Input/output 2A2. Referenced to $V_{CCA}$ .
2B1	11	13	I/O	Input/output 2B1. Referenced to $V_{CCB}$ .
2B2	10	12	I/O	Input/output 2B2. Referenced to $V_{CCB}$ .
2DIR	3	5	I	Direction-control input for '2' ports
2OE	14	16	I	3-state output-mode enables. Pull OE high to place '2' outputs in 3-state mode. Referenced to $V_{CCA}$ .
GND	8, 9	10, 11	—	Ground
$V_{CCA}$	1	3	—	A-port power supply voltage. $1.2\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$
$V_{CCB}$	16	2	—	B-port power supply voltage. $1.2\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{CCA}$ $V_{CCB}$	Supply voltage range	-0.5	4.6	V	
$V_I$	Input voltage range <sup>(2)</sup>	I/O ports (A port)	-0.5	4.6	V
		I/O ports (B port)	-0.5	4.6	
		Control inputs	-0.5	4.6	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	-0.5	4.6	V
		B port	-0.5	4.6	
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current	$V_I < 0$		-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND			±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

### 6.2 Handling Ratings

		MIN	MAX	UNIT	
$T_{stg}$	Storage temperature range	-65	150	°C	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>		8	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		1	
		Machine model (C101)		150	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)(3)</sup>

		$V_{CCI}$	$V_{CCO}$	MIN	MAX	UNIT
$V_{CCA}$	Supply voltage			1.2	3.6	V
$V_{CCB}$	Supply voltage			1.2	3.6	V
$V_{IH}$	High-level input voltage	Data inputs <sup>(4)</sup>	1.2 V to 1.95 V	$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V	1.6		
			2.7 V to 3.6 V	2		
$V_{IL}$	Low-level input voltage	Data inputs <sup>(4)</sup>	1.2 V to 1.95 V	$V_{CCI} \times 0.35$		V
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
$V_{IH}$	High-level input voltage	DIR (referenced to $V_{CCA}$ ) <sup>(5)</sup>	1.2 V to 1.95 V	$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V	1.6		
			2.7 V to 3.6 V	2		
$V_{IL}$	Low-level input voltage	DIR (referenced to $V_{CCA}$ ) <sup>(5)</sup>	1.2 V to 1.95 V	$V_{CCA} \times 0.35$		V
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
$V_I$	Input voltage			0	3.6	V
$V_O$	Output voltage	Active state		0	$V_{CCO}$	V
		3-state		0	3.6	
$I_{OH}$	High-level output current		1.2 V	-3		mA
			1.4 V to 1.6 V	-6		
			1.65 V to 1.95 V	-8		
			2.3 V to 2.7 V	-9		
			3 V to 3.6 V	-12		
$I_{OL}$	Low-level output current		1.1 V to 1.2 V	3		mA
			1.4 V to 1.6 V	6		
			1.65 V to 1.95 V	8		
			2.3 V to 2.7 V	9		
			3 V to 3.6 V	12		
$\Delta t/\Delta v$	Input transition rise or fall rate				5	ns/V
$T_A$	Operating free-air temperature			-40	85	°C

(1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(3) All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

(4) For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCI} \times 0.7$  V,  $V_{IL}$  max =  $V_{CCI} \times 0.3$  V

(5) For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCA} \times 0.7$  V,  $V_{IL}$  max =  $V_{CCA} \times 0.3$  V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AVC4T245					UNIT
		D	DGV	PW	RGY	RSV	
		16 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.5	126.0	112.0	37.5	146.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.9	50.8	46.8	54.5	53.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	43.0	57.7	57.1	15.6	75.6	
$\Psi_{JT}$	Junction-to-top characterization parameter	13.4	5.7	5.7	0.5	13.5	
$\Psi_{JB}$	Junction-to-board characterization parameter	42.7	57.2	56.5	15.8	75.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	3.5	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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## 6.5 Electrical Characteristics<sup>(1)(2)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			–40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	V <sub>I</sub> = V <sub>IH</sub>	1.2 V to 3.6 V	1.2 V to 3.6 V			V <sub>CCO</sub> – 0.2		V
	I <sub>OH</sub> = –3 mA		1.2 V	1.2 V	0.95				
	I <sub>OH</sub> = –6 mA		1.4 V	1.4 V		1.05			
	I <sub>OH</sub> = –8 mA		1.65 V	1.65 V		1.2			
	I <sub>OH</sub> = –9 mA		2.3 V	2.3 V		1.75			
	I <sub>OH</sub> = –12 mA		3 V	3 V		2.3			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	V <sub>I</sub> = V <sub>IL</sub>	1.2 V to 3.6 V	1.2 V to 3.6 V				0.2	V
	I <sub>OL</sub> = 3 mA		1.2 V	1.2 V	0.25				
	I <sub>OL</sub> = 6 mA		1.4 V	1.4 V		0.35			
	I <sub>OL</sub> = 8 mA		1.65 V	1.65 V		0.45			
	I <sub>OL</sub> = 9 mA		2.3 V	2.3 V		0.55			
	I <sub>OL</sub> = 12 mA		3 V	3 V		0.7			
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.2 V to 3.6 V	1.2 V to 3.6 V	±0.025	±0.25		±1	μA
I <sub>off</sub>	A or B port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V	0 V to 3.6 V	±0.1	±1		±5	μA
			0 V to 3.6 V	0 V	±0.1	±1		±5	
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND, $\overline{OE}$ = V <sub>IH</sub>	3.6 V	3.6 V	±0.5	±2.5		±5	μA
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				8	μA
			0 V	0 V to 3.6 V				–2	
			0 V to 3.6 V	0 V				8	
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				8	μA
			0 V	0 V to 3.6 V				8	
			0 V to 3.6 V	0 V				–2	
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				16	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND	3.3 V	3.3 V	3.5			4.5	pF
C <sub>io</sub>	A or B port	V <sub>O</sub> = 3.3 V or GND	3.3 V	3.3 V	6			7	pF

(1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

## 6.6 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.2\text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.8\text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
$C_{pdA}$ (1)	A to B	Outputs enabled	$C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$	1	1	1	1.5	2	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		12	12.5	13	14	15	
		Outputs disabled		1	1	1	1	1	
$C_{pdB}$ (1)	A to B	Outputs enabled	$C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$	12	12.5	13	14	15	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	1	2	
		Outputs disabled		1	1	1	1	1	

(1) Power dissipation capacitance per transceiver

## 6.7 Switching Characteristics: $V_{CCA} = 1.2\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.2\text{ V}$  (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CCB} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CCB} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CCB} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$t_{PLH}$	A	B	3.4	2.9	2.7	2.6	2.8	ns
$t_{PHL}$			3.4	2.9	2.7	2.6	2.8	
$t_{PLH}$	B	A	3.6	3.1	2.8	2.6	2.6	ns
$t_{PHL}$			3.6	3.1	2.8	2.6	2.6	
$t_{PZH}$	$\overline{\text{OE}}$	A	5.6	4.7	4.3	3.9	3.7	ns
$t_{PZL}$			5.6	4.7	4.3	3.9	3.7	
$t_{PZH}$	$\overline{\text{OE}}$	B	5	4.3	3.9	3.6	3.6	ns
$t_{PZL}$			5	4.3	3.9	3.6	3.6	
$t_{PHZ}$	$\overline{\text{OE}}$	A	6.2	5.2	5.2	4.3	4.8	ns
$t_{PLZ}$			6.2	5.2	5.2	4.3	4.8	
$t_{PHZ}$	$\overline{\text{OE}}$	B	5.9	5.1	5	4.7	5.5	ns
$t_{PLZ}$			5.9	5.1	5	4.7	5.5	

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**6.8 Switching Characteristics:  $V_{CCA} = 1.5 V \pm 0.1 V$**

over recommended operating free-air temperature range,  $V_{CCA} = 1.5 V \pm 0.1 V$  (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 V$	$V_{CCB} = 1.5 V \pm 0.1 V$		$V_{CCB} = 1.8 V \pm 0.15 V$		$V_{CCB} = 2.5 V \pm 0.2 V$		$V_{CCB} = 3.3 V \pm 0.3 V$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	3.2	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
$t_{PHL}$			3.2	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	
$t_{PLH}$	B	A	3.3	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	ns
$t_{PHL}$			3.3	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
$t_{PZH}$	$\overline{OE}$	A	4.9	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	ns
$t_{PZL}$			4.9	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
$t_{PZH}$	$\overline{OE}$	B	4.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
$t_{PZL}$			4.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
$t_{PHZ}$	$\overline{OE}$	A	5.6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
$t_{PLZ}$			5.6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
$t_{PHZ}$	$\overline{OE}$	B	5.2	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns
$t_{PLZ}$			5.2	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

**6.9 Switching Characteristics:  $V_{CCA} = 1.8 V \pm 0.15 V$**

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 V \pm 0.15 V$  (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 V$	$V_{CCB} = 1.5 V \pm 0.1 V$		$V_{CCB} = 1.8 V \pm 0.15 V$		$V_{CCB} = 2.5 V \pm 0.2 V$		$V_{CCB} = 3.3 V \pm 0.3 V$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.9	0.1	6	0.1	4.9	0.1	3.9	0.3	3.9	ns
$t_{PHL}$			2.9	0.1	6	0.1	4.9	0.1	3.9	0.3	3.9	
$t_{PLH}$	B	A	3	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	ns
$t_{PHL}$			3	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	
$t_{PZH}$	$\overline{OE}$	A	4.4	1	7.4	1	7.3	0.6	7.3	0.4	7.2	ns
$t_{PZL}$			4.4	1	7.4	1	7.3	0.6	7.3	0.4	7.2	
$t_{PZH}$	$\overline{OE}$	B	4.1	1.2	9.2	1	7.4	0.8	5.3	0.8	4.6	ns
$t_{PZL}$			4.1	1.2	9.2	1	7.4	0.8	5.3	0.8	4.6	
$t_{PHZ}$	$\overline{OE}$	A	5.4	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7	ns
$t_{PLZ}$			5.4	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7	
$t_{PHZ}$	$\overline{OE}$	B	5	1.7	9.9	1.6	8.7	1.2	6.9	1	6.9	ns
$t_{PLZ}$			5	1.7	9.9	1.6	8.7	1.2	6.9	1	6.9	



### 6.10 Switching Characteristics: $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.8	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
$t_{PHL}$			2.8	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	
$t_{PLH}$	B	A	2.7	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
$t_{PHL}$			2.7	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	
$t_{PZH}$	$\overline{OE}$	A	4	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	ns
$t_{PZL}$			4	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	
$t_{PZH}$	$\overline{OE}$	B	3.8	0.9	8.8	0.8	7	0.6	4.8	0.6	4	ns
$t_{PZL}$			3.8	0.9	8.8	0.8	7	0.6	4.8	0.6	4	
$t_{PHZ}$	$\overline{OE}$	A	4.7	1	8.4	1	8.4	1	6.2	1	6.6	ns
$t_{PLZ}$			4.7	1	8.4	1	8.4	1	6.2	1	6.6	
$t_{PHZ}$	$\overline{OE}$	B	4.5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	ns
$t_{PLZ}$			4.5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	

### 6.11 Switching Characteristics: $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
$t_{PHL}$			2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	
$t_{PLH}$	B	A	2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	ns
$t_{PHL}$			2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	
$t_{PZH}$	$\overline{OE}$	A	3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	ns
$t_{PZL}$			3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	
$t_{PZH}$	$\overline{OE}$	B	3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns
$t_{PZL}$			3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	
$t_{PHZ}$	$\overline{OE}$	A	4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	ns
$t_{PLZ}$			4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	
$t_{PHZ}$	$\overline{OE}$	B	5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	ns
$t_{PLZ}$			5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	

### 6.12 Typical Characteristics

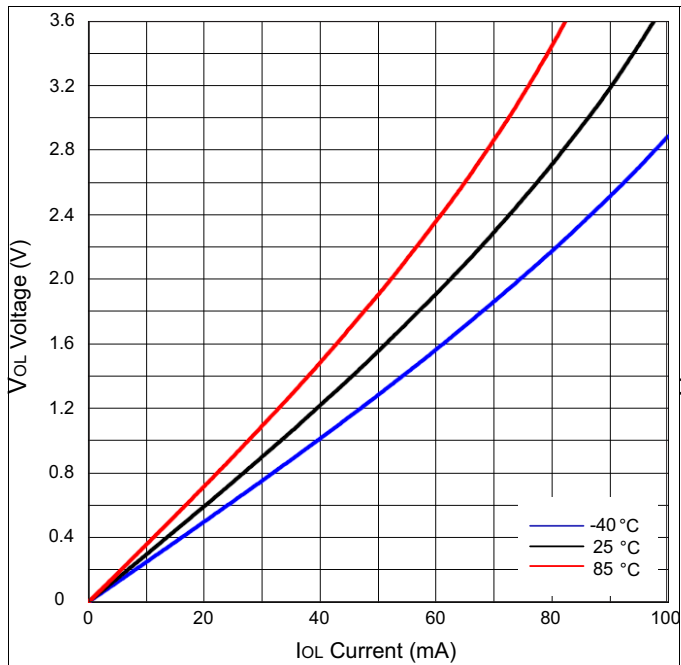


Figure 1. Low-Level Output Voltage ( $V_{OL}$ ) vs Low-Level Current ( $I_{OL}$ )

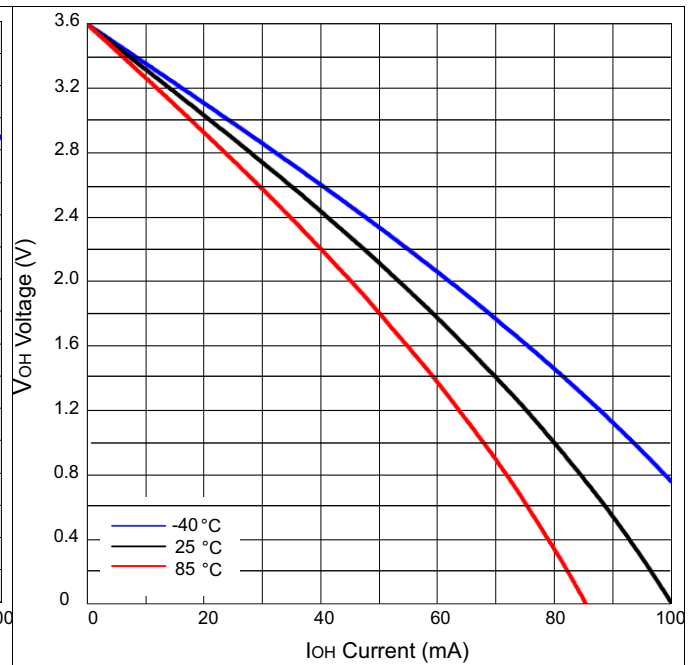
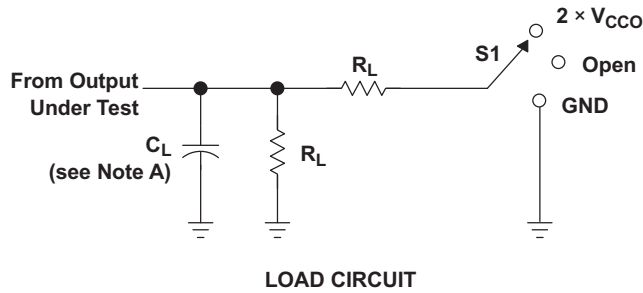


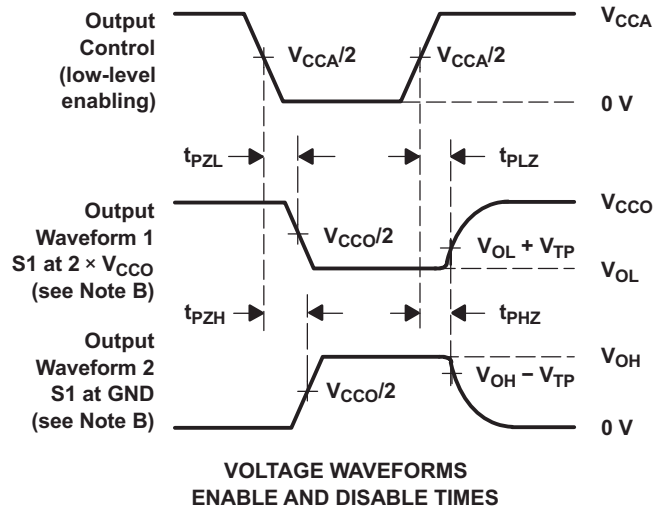
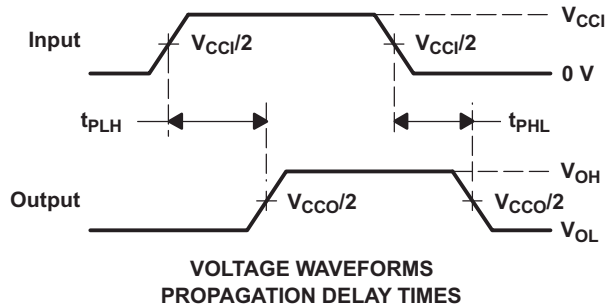
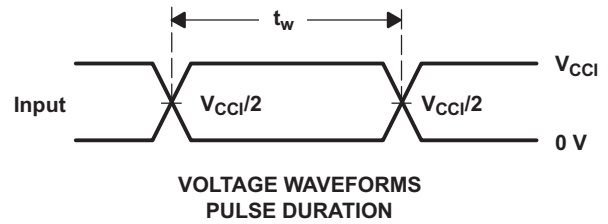
Figure 2. High-Level Output Voltage ( $V_{OH}$ ) vs High-Level Current ( $I_{OH}$ )

### 7 Parameter Measurement Information



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
1.2 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 k $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.  
 I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**Figure 3. Load and Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SN74AVC4T245 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (1DIR, 2DIR, 1OE, and 2OE) are supported by  $V_{CCA}$ , and Bx pins are supported by  $V_{CCB}$ . The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when OE is set to low. When OE is set to high, both Ax and Bx pins are in the high-impedance state.

### 8.2 Functional Block Diagram

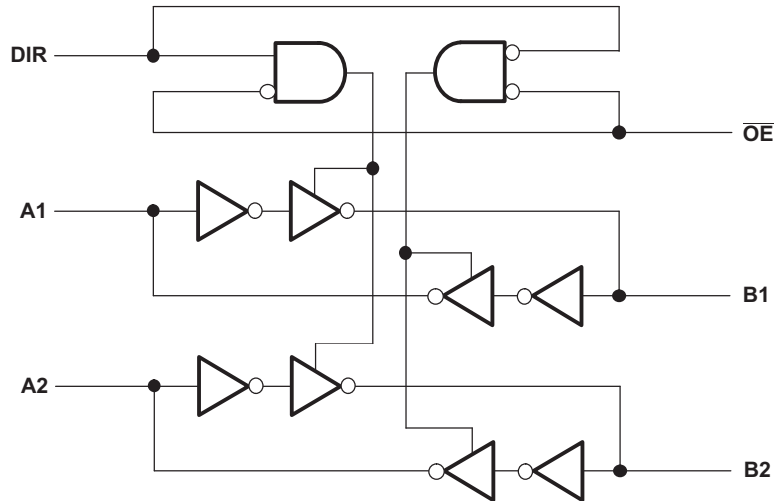


Figure 4. Logic Diagram (Positive Logic) for 1/2 of SN74AVC4T245

## 8.3 Feature Description

### 8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range

Both  $V_{CCA}$  and  $V_{CCB}$  can be supplied at any voltage between 1.2 V and 3.6 V; thus, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

### 8.3.2 Supports High Speed Translation

The SN74AVC4T245 device can support high data rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

### 8.3.3 $I_{off}$ Supports Partial-Power-Down Mode Operation

$I_{off}$  will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

## 8.4 Device Functional Modes

**Table 1. Function Table  
(Each 2-Bit Section)<sup>(1)</sup>**

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74AVC4T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T245 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

### 9.2 Typical Application

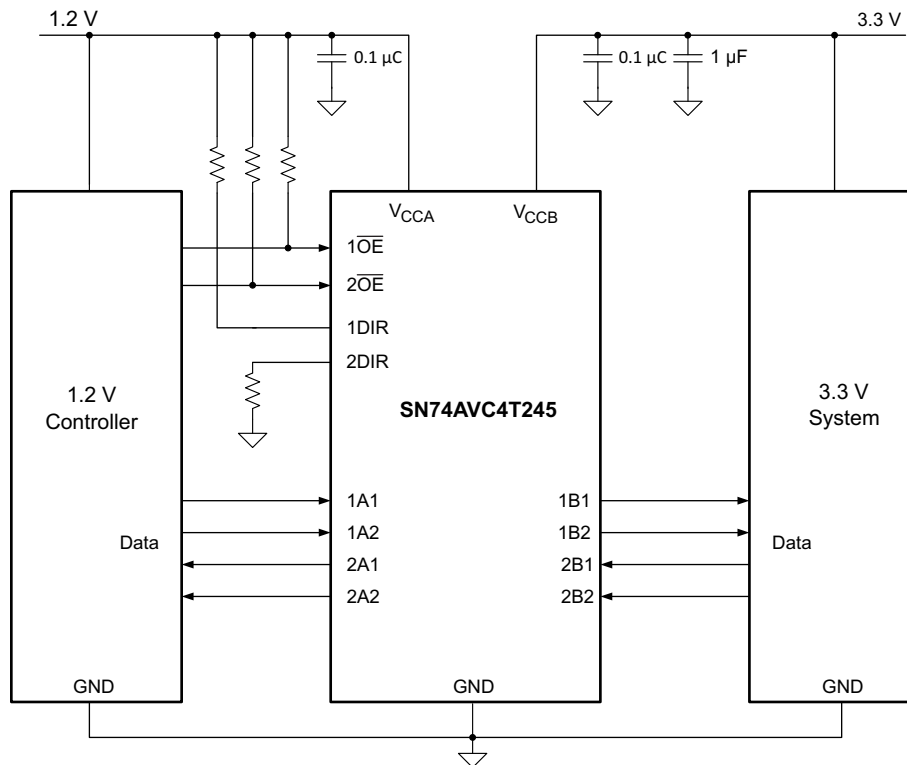


Figure 5. Typical Application Diagram

## Typical Application (continued)

### 9.2.1 Design Requirements

For the design example shown in *Typical Application*, use the parameters listed in [Table 2](#).

**Table 2. Design Parameters**

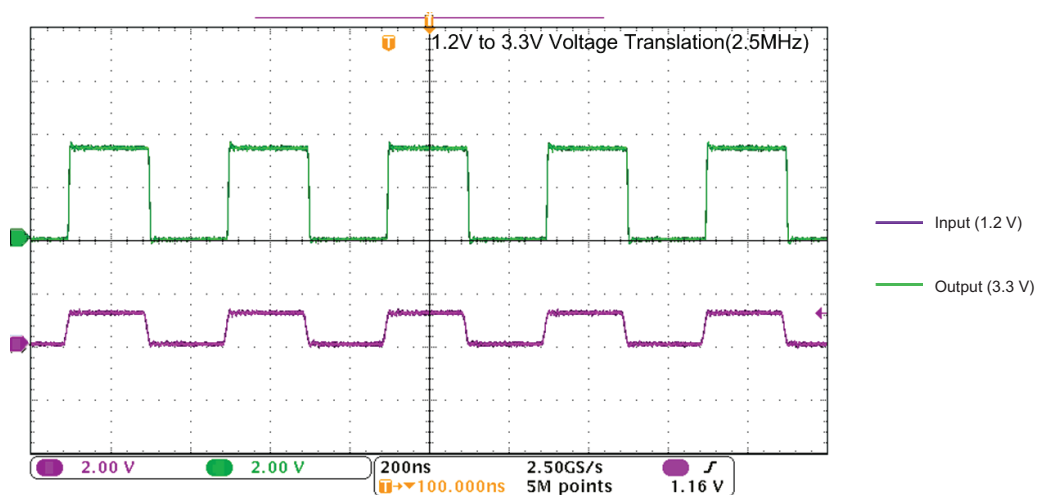
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T245 device to determine the input voltage range. For a valid logic high, the value must exceed the  $V_{IH}$  of the input port. For a valid logic low, the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T245 device is driving to determine the output voltage range.

### 9.2.3 Application Curves



**Figure 6. Translation Up (1.2 V to 3.3 V) at 2.5 MHz**

## 10 Power Supply Recommendations

The SN74AVC4T245 device uses two separate configurable power-supply rails,  $V_{CCA}$  and  $V_{CCB}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V and  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track  $V_{CCA}$  and  $V_{CCB}$  respectively allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable ( $\overline{OE}$ ) input circuit is designed so that it is supplied by  $V_{CCA}$  and when the  $\overline{OE}$  input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the  $\overline{OE}$  input pin must be tied to  $V_{CCA}$  through a pullup resistor and must not be enabled until  $V_{CCA}$  and  $V_{CCB}$  are fully ramped and stable. The minimum value of the pullup resistor to  $V_{CCA}$  is determined by the current-sinking capability of the driver.

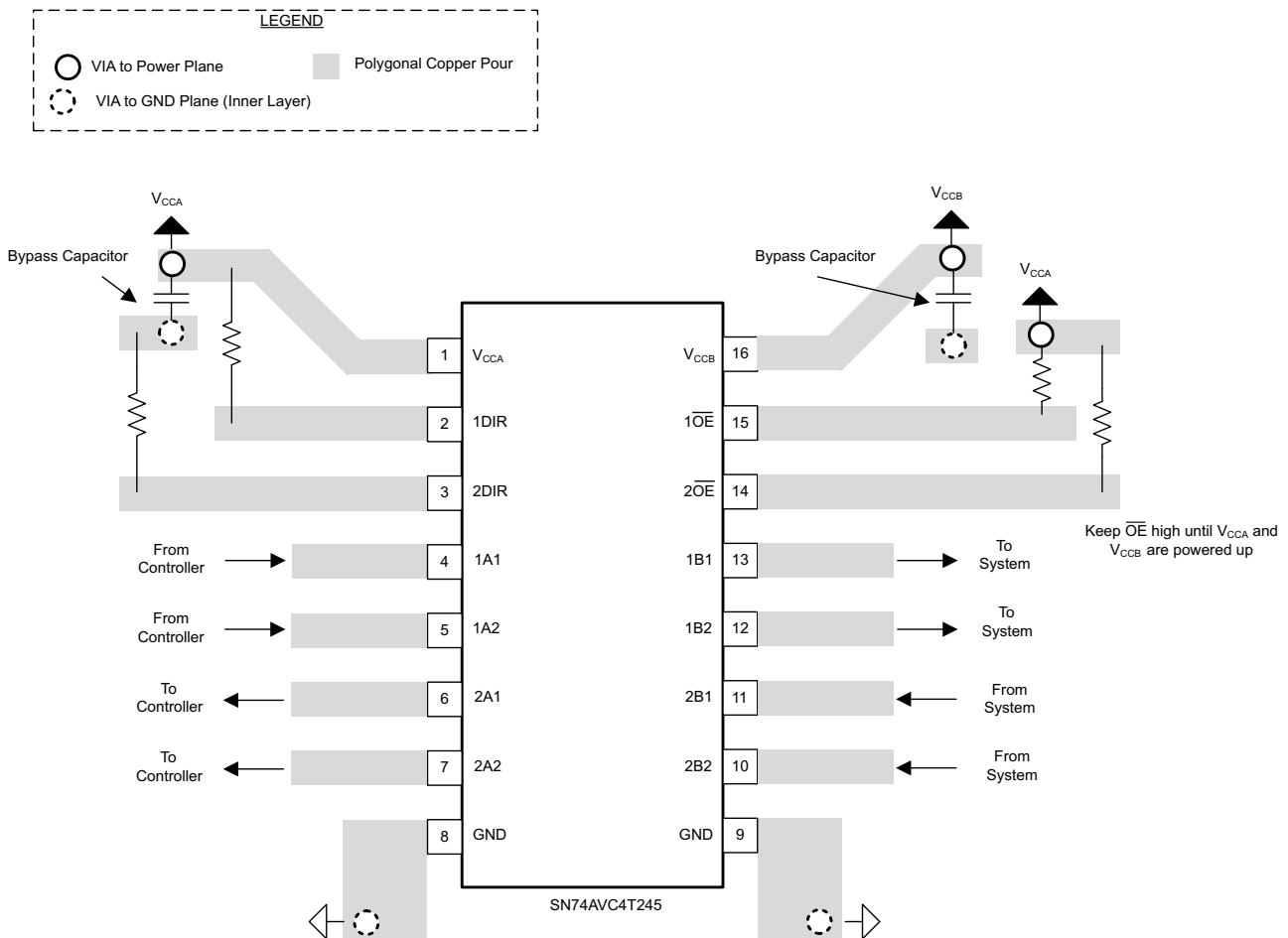
## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

### 11.2 Layout Example





## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

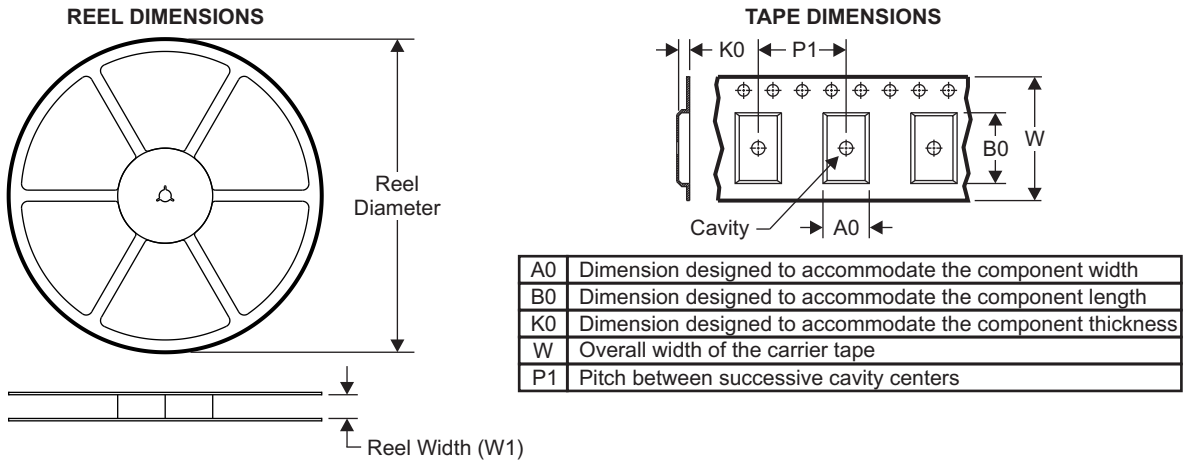
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# SN74AVC4T245

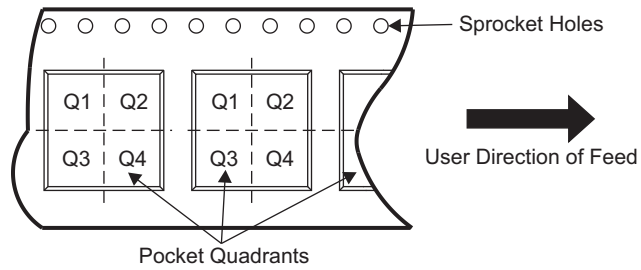
SCES576G – JUNE 2004 – REVISED NOVEMBER 2014

## 13.1 Package Materials Information

### 13.1.1 Tape and Reel Information

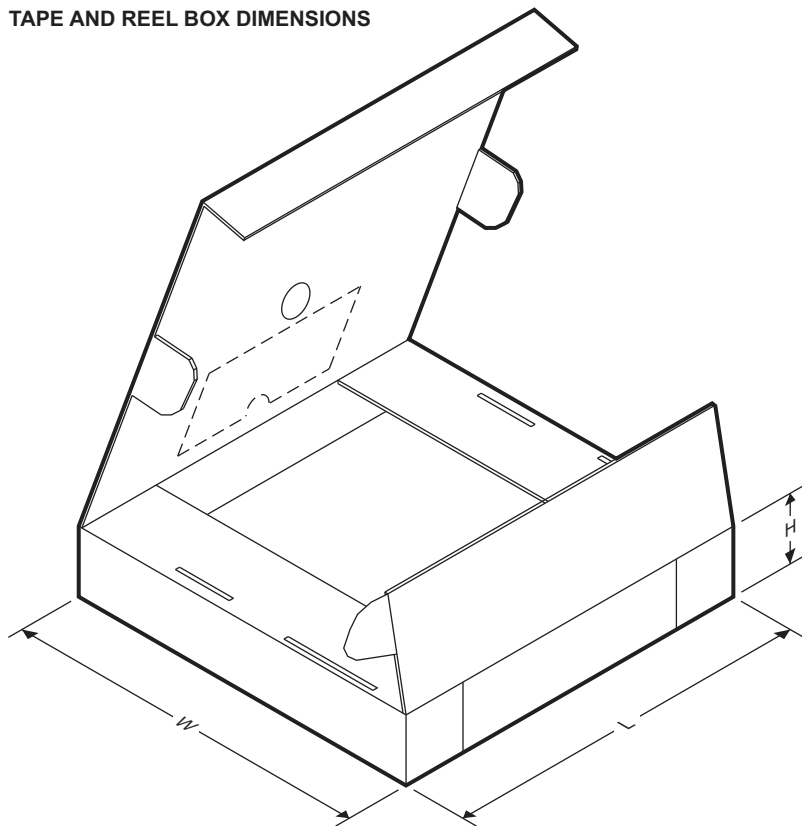


#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC4T245DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AVC4T245DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AVC4T245PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T245RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T245RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T245RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC4T245DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74AVC4T245DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AVC4T245PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74AVC4T245RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
SN74AVC4T245RGYR	VQFN	RGY	16	3000	355.0	350.0	50.0
SN74AVC4T245RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0

# PACKAGE OPTION ADDENDUM

10-Dec-2020

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC4T245DGVRE4	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
74AVC4T245RGYRG4	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT245	<a href="#">Samples</a>
74AVC4T245RSVR-NT	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU	<a href="#">Samples</a>
74AVC4T245RSVRG4	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU	<a href="#">Samples</a>
HPA00719RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU	<a href="#">Samples</a>
SN74AVC4T245D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	<a href="#">Samples</a>
SN74AVC4T245DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	<a href="#">Samples</a>
SN74AVC4T245DRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	<a href="#">Samples</a>
SN74AVC4T245DT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	<a href="#">Samples</a>
SN74AVC4T245PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245PWE4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245PWTE4	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245PWTG4	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT245	<a href="#">Samples</a>
SN74AVC4T245RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

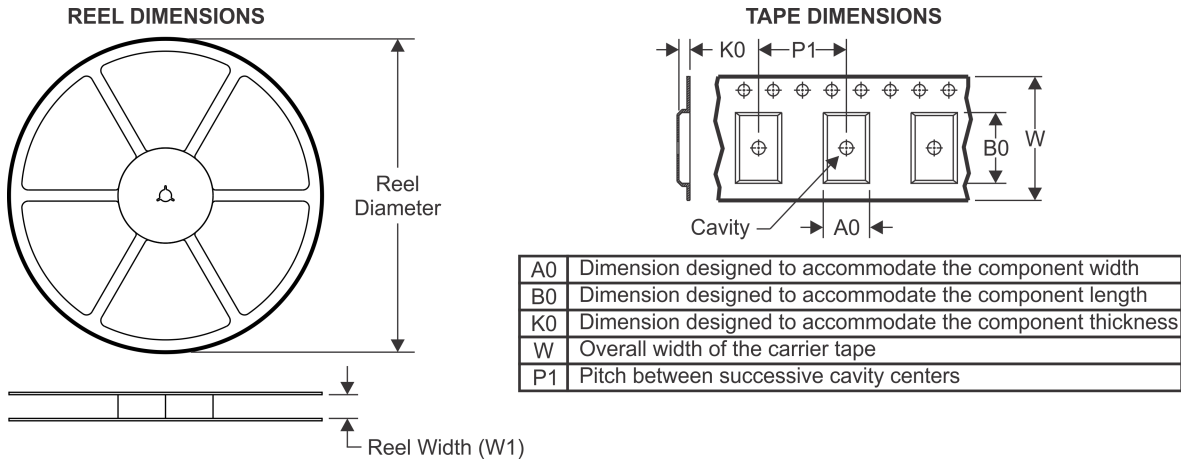
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

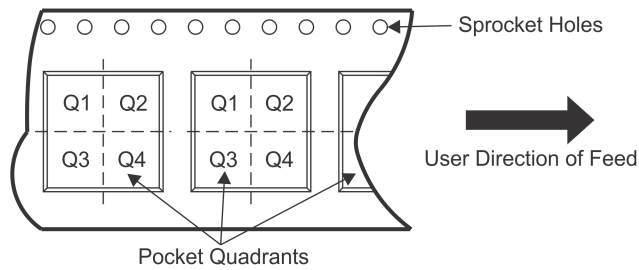
## OTHER QUALIFIED VERSIONS OF SN74AVC4T245 :

- Automotive: [SN74AVC4T245-Q1](#)

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



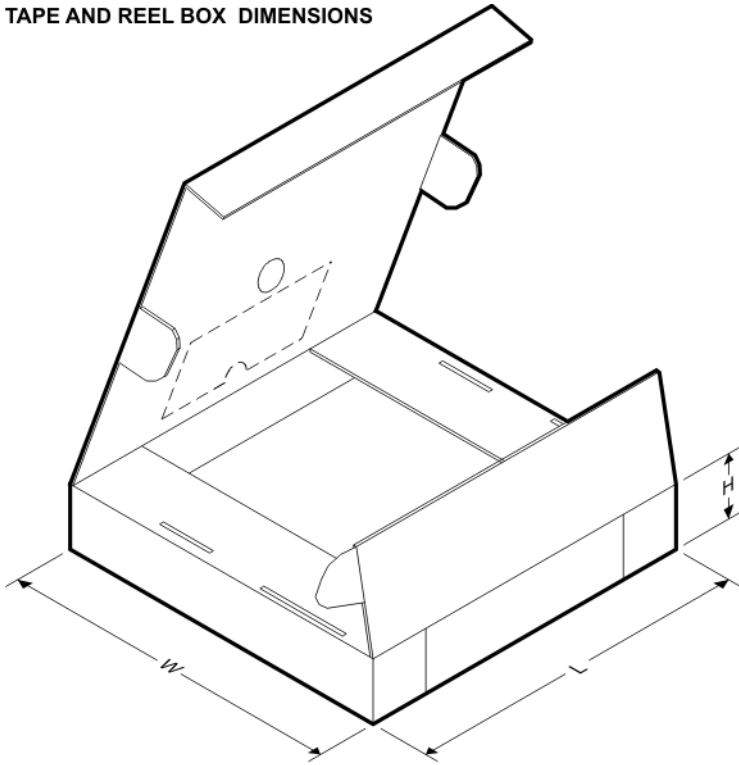
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVC4T245RSVR-NT	UQFN	RSV	16	3000	180.0	8.4	2.0	2.8	0.7	4.0	8.0	Q1
74AVC4T245RSVR-NT	UQFN	RSV	16	3000	180.0	9.5	2.1	2.9	0.75	4.0	8.0	Q1
SN74AVC4T245DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AVC4T245DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AVC4T245PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T245PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T245RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T245RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
SN74AVC4T245RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

# PACKAGE MATERIALS INFORMATION

27-Jul-2021

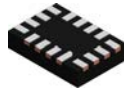
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T245RSVR-NT	UQFN	RSV	16	3000	200.0	183.0	25.0
74AVC4T245RSVR-NT	UQFN	RSV	16	3000	189.0	185.0	36.0
SN74AVC4T245DGVR	TVSOP	DGV	16	2000	853.0	449.0	35.0
SN74AVC4T245DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AVC4T245PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74AVC4T245PWT	TSSOP	PW	16	250	853.0	449.0	35.0
SN74AVC4T245RGYR	VQFN	RGY	16	3000	853.0	449.0	35.0
SN74AVC4T245RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
SN74AVC4T245RSVR	UQFN	RSV	16	3000	200.0	183.0	25.0

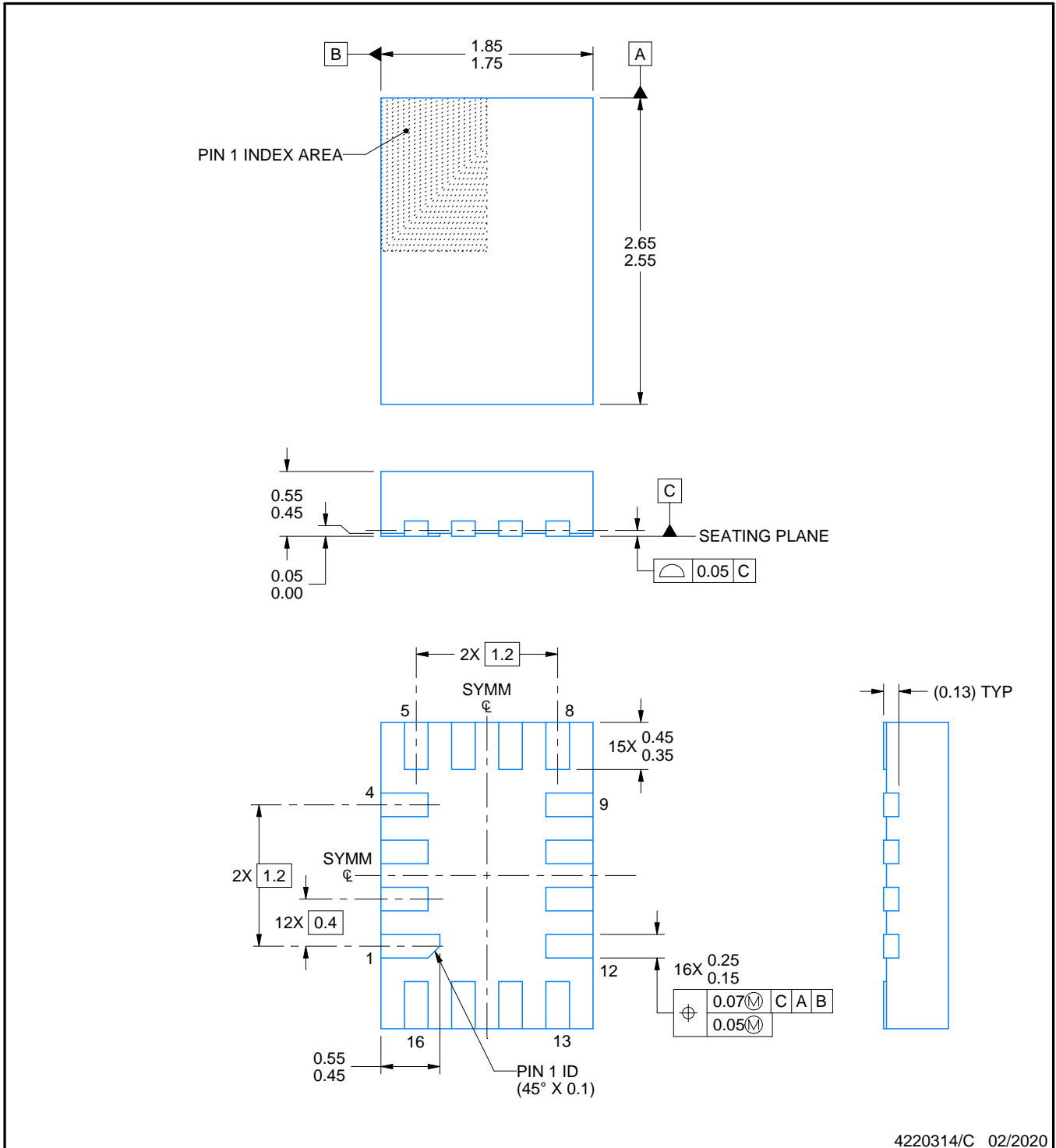
RSV0016A



# PACKAGE OUTLINE

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



4220314/C 02/2020

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

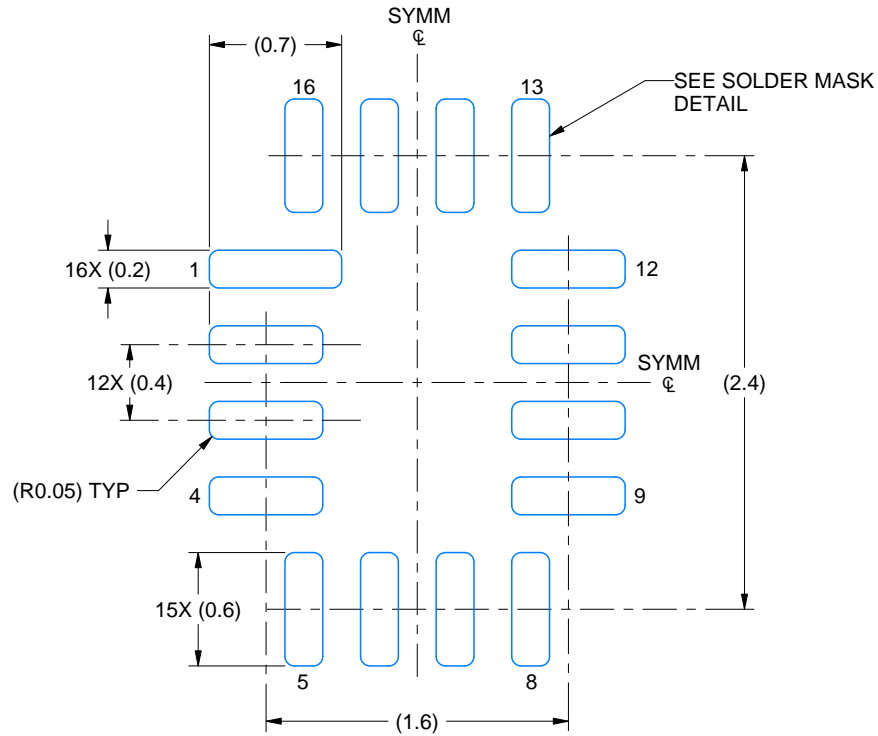


# EXAMPLE BOARD LAYOUT

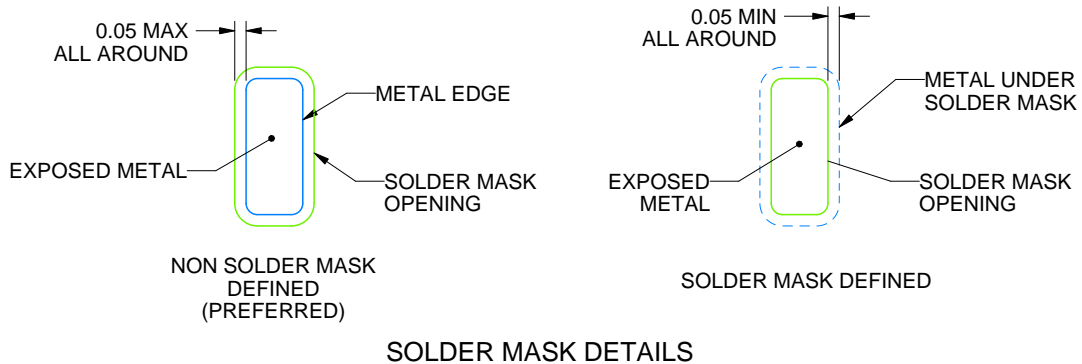
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

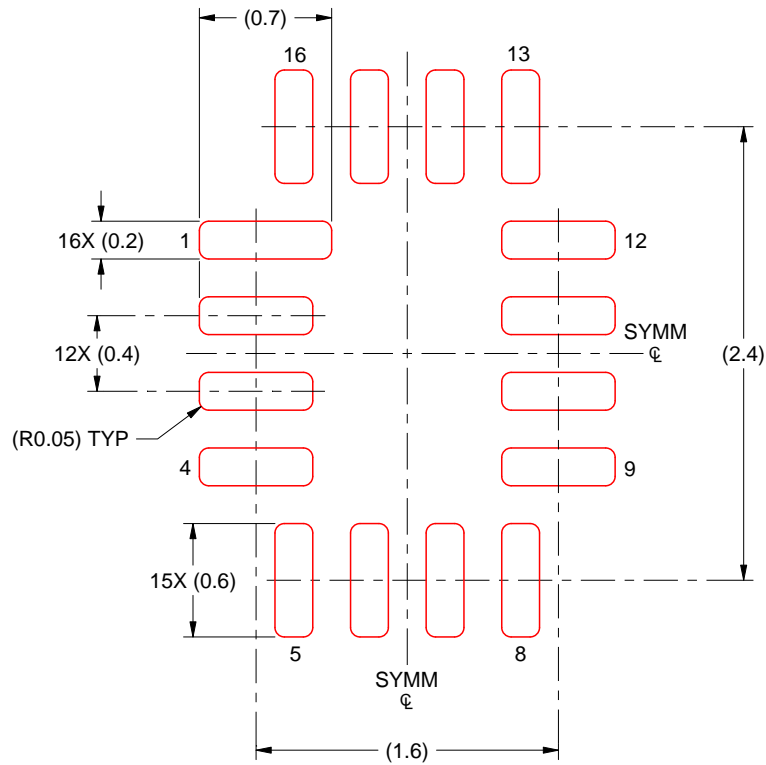
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



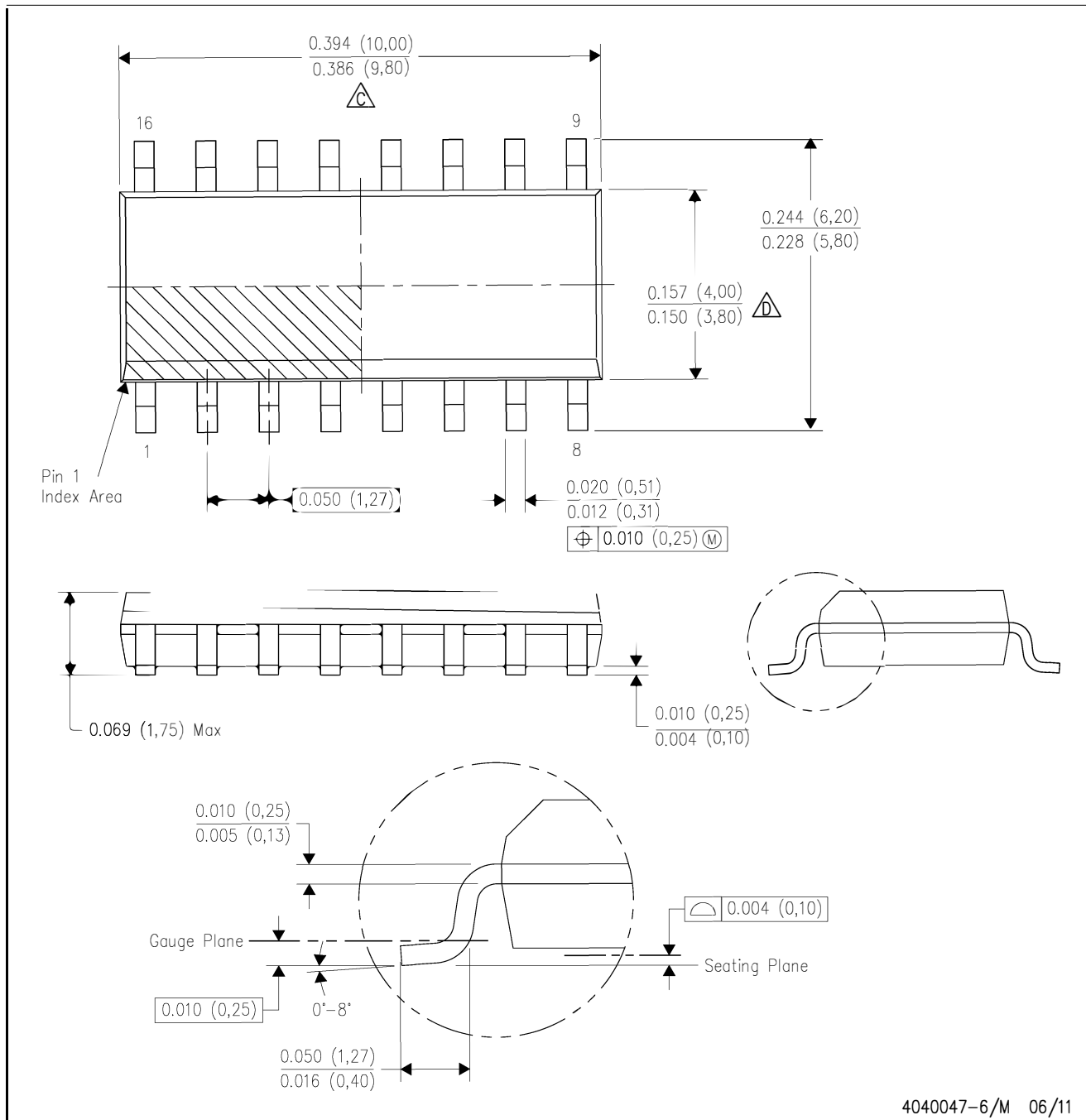
SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

D (R-PDSO-G16)

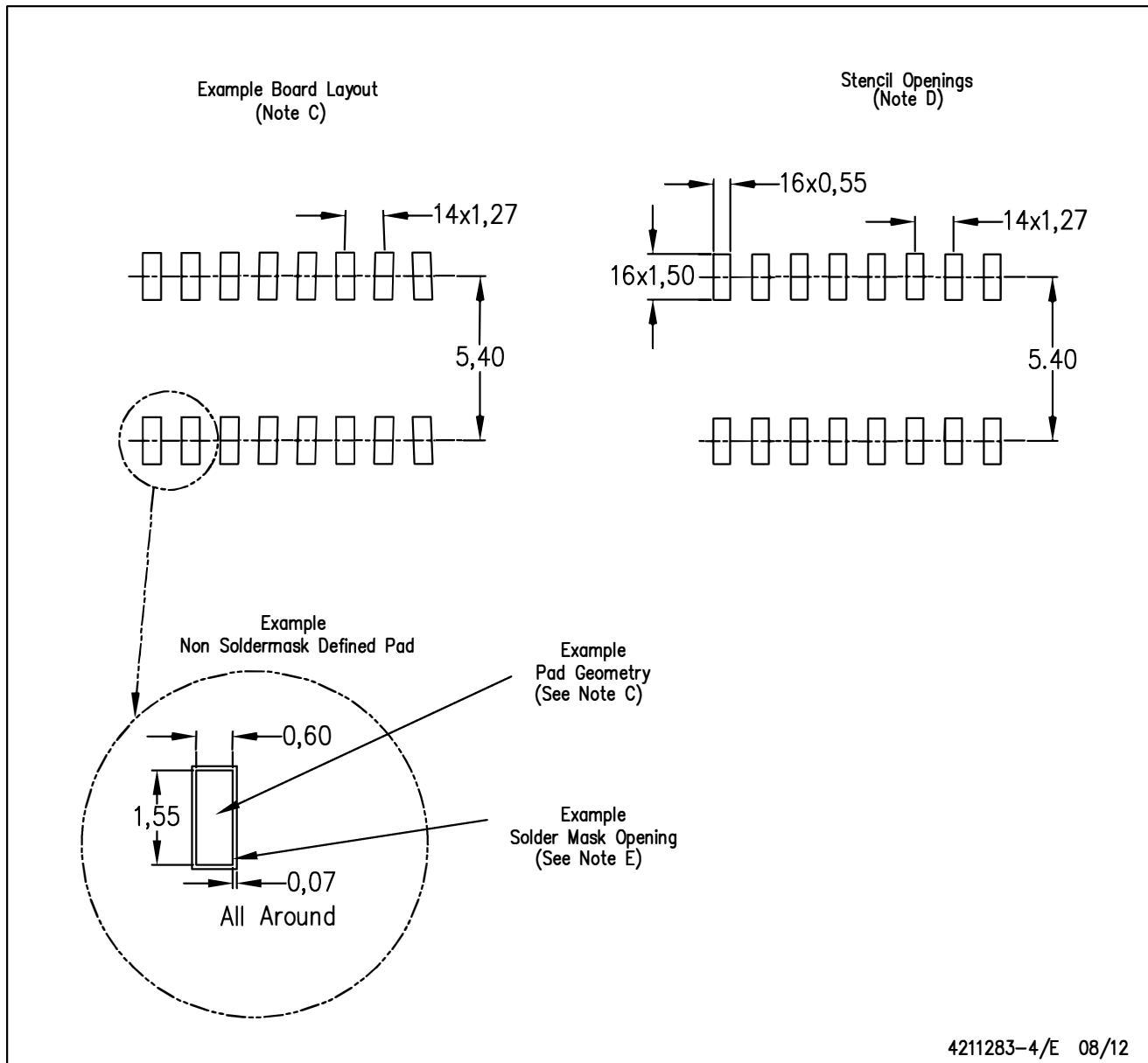
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW0016A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

### NOTES:

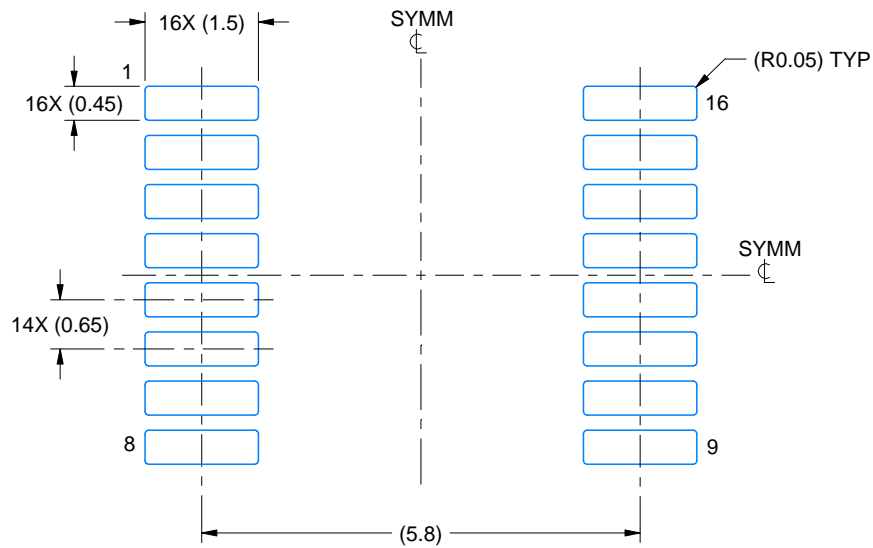
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

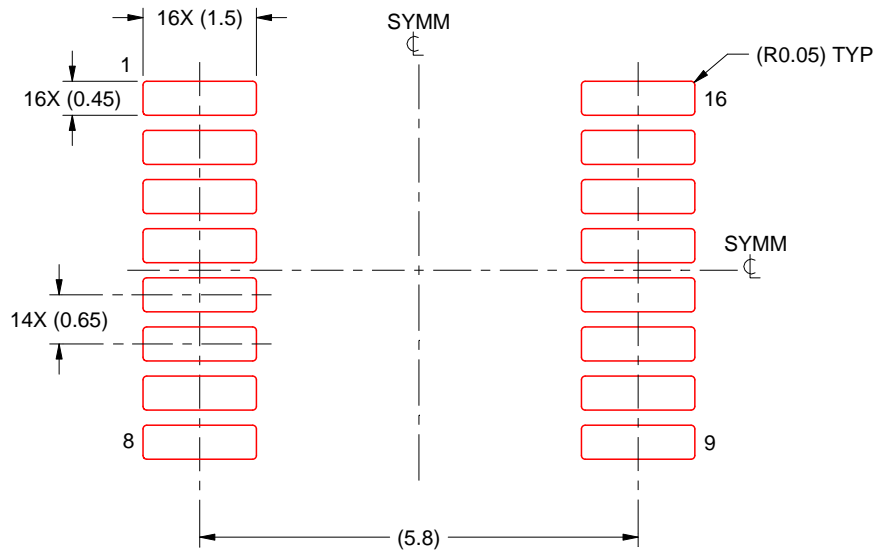
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

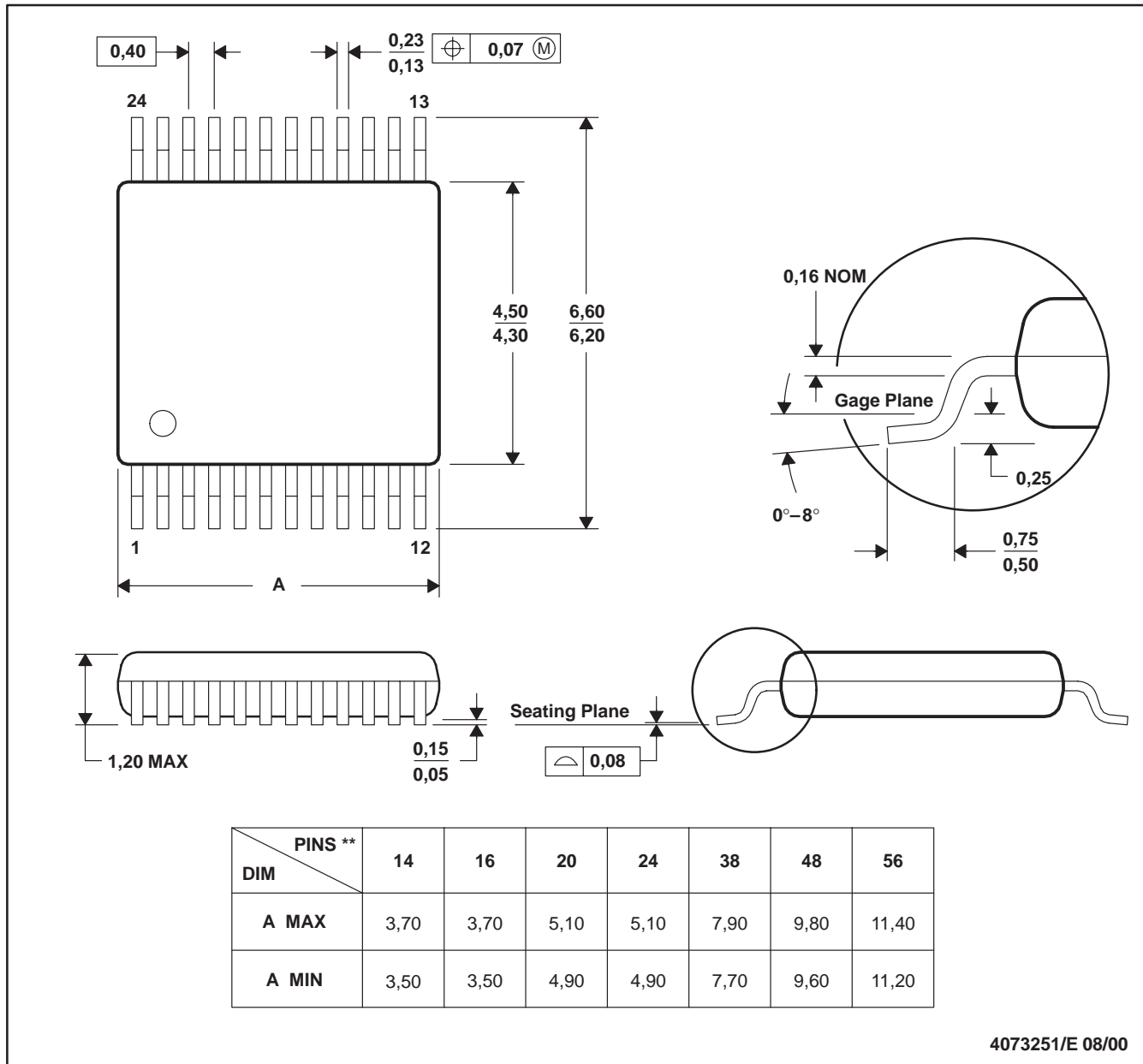
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

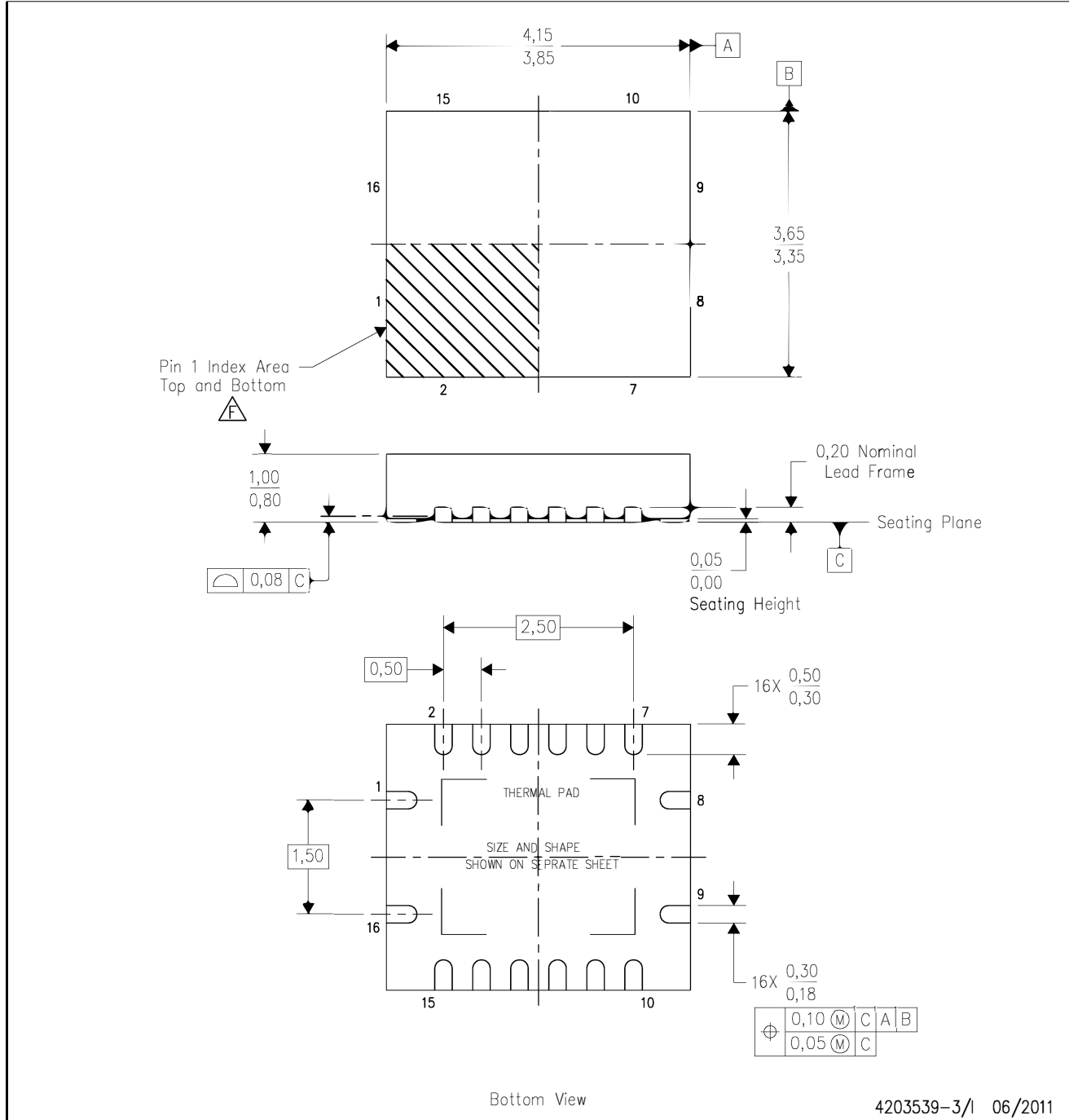



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
-  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.

RGY (R-PVQFN-N16)

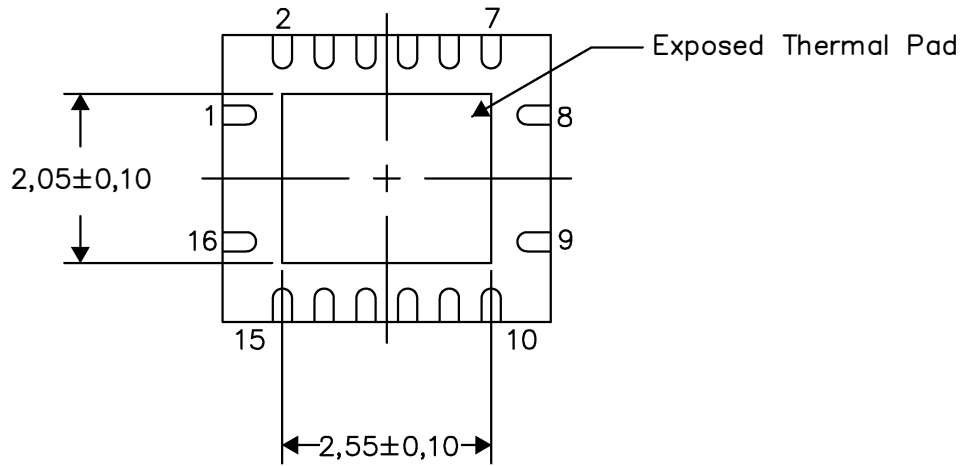
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

