具有可配置电压转换的 SN74AXC1T45 单比特位双电源总线收发器

1 特性

- 在 0.65V 至 3.6V 范围内进行上行和下行电平转换
- 工作温度：–40°C 至 +125°C
- 设计采用毛刺信号抑制电路以提高电源定序性能
- 最大静态电流 (I_{CCA} + I_{CCB}) 为 10μA（最高 85°C）和 16μA（最高 125°C）
- 从 1.8V 转换到 3.3V 时，支持高达 500Mbps 的转换速率
- V_{CC} 隔离特性
  - 如果任何一个 V_{CC} 输入低于 100mV，则所有 I/O 输出均禁用且处于高阻抗状态
- I_{off} 支持局部关断模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 8000V 人体放电模型
  - 1000V 充电器件模型

2 应用

- 企业与通信
- 工业
- 个人电子产品

3 说明

SN74AXC1T45 是一款采用两个独立可配置电源轨的单比特位同相总线收发器。V_{CCA} 和 V_{CCB} 电源电压低至 0.65V 时，该器件可正常工作。A 端口用于跟踪 V_{CCA}，该端口可支持 0.65V 至 3.6V 范围内的任何电源电压。B 端口用于跟踪 V_{CCB}，该端口也可支持 0.65V 至 3.6V 范围内的任何电源电压。

DIR 引脚决定信号传播的方向。DIR 引脚配置为高电平时，信号转换由端口 A 流向端口 B。DIR 配置为低电平时，则由端口 B 流向端口 A。DIR 引脚以 V_{CCA} 为基准，这意味着它的逻辑高电平和逻辑低电平阈值跟踪 V_{CCA} 电压。

该器件完全符合使用 I_{off} 电流的部分断电应用的规范要求。当器件断电时，I_{off} 保护电路可确保不从输入、输出或偏置到特定电压的组合 I/O 获取多余电流，也不向其提供多余电流。

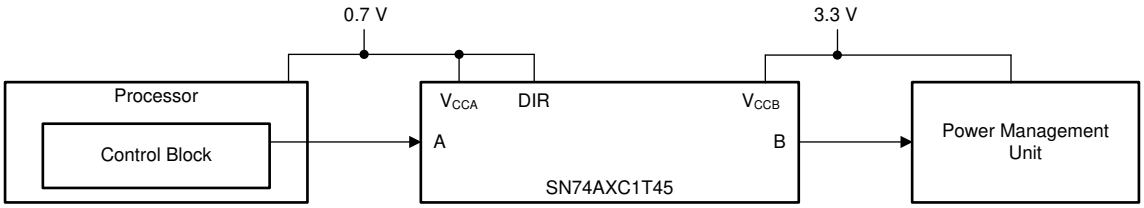
V_{CC} 隔离特性可确保当 V_{CCA} 或 V_{CCB} 低于 100mV 时，I/O 端口均禁用其输出并进入高阻态。

毛刺信号抑制电路使电源轨能以任何顺序打开或关断，从而提供强大的电源定序性能。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
SN74AXC1T45DBV	SOT-23 (6)	2.90mm × 1.60mm
SN74AXC1T45DCK	SC70 (6)	2.00mm × 1.25mm
SN74AXC1T45DRL	SOT-5X3 (6)	1.60mm × 1.20mm
SN74AXC1T45DEA	X2SON (6)	1.00mm x 1.00mm
SN74AXC1T45DTQ	X2SON (6)	1.00mm x 0.80mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (June 2018) to Revision C (September 2020) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 将所有表更新为最新的 3d 表格式 1
- Updated I_{CCA}, I_{CCB}, and I_{CCA} + I_{CCB} to reflect updated performance of device 6

Changes from Revision A (April 2018) to Revision B (June 2018) — **Page**

- 添加了 DEA 和 DTQ 作为可用封装选项 1
- 将产品状态从“量产混合”更改为“量产数据” 1

Changes from Revision * (December 2017) to Revision A (April 2018) — **Page**

- Added pinout drawing for DEA package 3
- Added pinout drawing for DTQ package 3

5 Pin Configuration and Functions

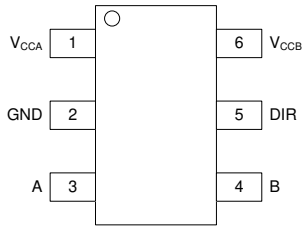


图 5-1. DBV Package 6-Pin SOT-23 Top View

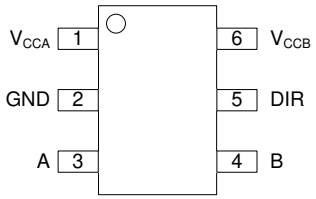


图 5-2. DCK Package 6-Pin SC70 Top View

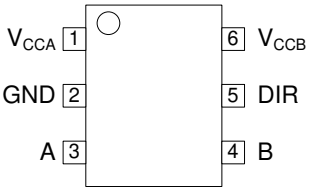


图 5-3. DTQ Package 6-Pin X2SON Transparent Top View

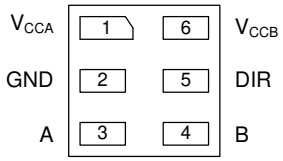


图 5-4. DRY Package 6-Pin SON Transparent Top View

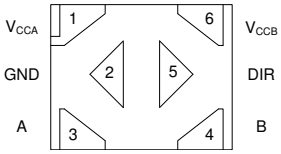


图 5-5. DRY Package 6-Pin SON Transparent Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_{CCA}	—	A-port supply voltage. 0.65V ⩽ V_{CCA} ⩽ 3.6 V.
2	GND	—	Ground.
3	A	I/O	Input/output A. This pin is referenced to V_{CCA}. When this pin is configured as an input, do not leave it floating.
4	B	I/O	Input/output B. This pin is referenced to V_{CCB}. When this pin is configured as an input, do not leave it floating.
5	DIR	I	Direction control signal. Set to Logic High for A-to-B level translation. Set to Logic Low for B-to-A level translation.
6	V_{CCB}	—	B-port supply voltage. 0.65V ⩽ V_{CCB} ⩽ 3.6 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.2	V
V_{CCB}	Supply voltage B		–0.5	4.2	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.2	V
		B Port	–0.5	V_{CCB} + 0.2	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_J	Junction Temperature			150	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			0.65	3.6	V
V_{CCB}	Supply voltage B			0.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} x 0.70		V
			V_{CCI} = 0.76 V - 1 V	V_{CCI} x 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} x 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control Input (DIR) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} x 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} x 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} x 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} x 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} x 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} x 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control Input (DIR) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} x 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} x 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} x 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
$\Delta t/\Delta v$	Input transition rate				100	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) VCCI is the VCC associated with the input port.
(2) VCCO is the VCC associated with the output port.
(3) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AXC1T45					UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT-5X3)	DEA (X2SON)	DTQ (X2SON)	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.2	235.3	298.9	358.0	327.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	137.2	160.5	148.4	201.0	194.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.2	76.9	165.0	221.8	248.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	64.0	59.7	20.7	26.1	24.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.4	77.1	164.9	220.8	247.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						– 40°C to 85°C			– 40°C to 125°C			
						MIN	TYP(3)	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = -100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = -50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = -200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = -500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_I	Input leakage current	Control input (DIR): V_I = V_{CCA} or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	– 1		1	– 1.5		1.5	µA
		A or B Port: Vi = V_{CCI} or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	– 4		4	– 8		8	
I_{off}	Partial power down current	A or B Port: Vi or Vo = 0 V - 3.6 V		0 V	0 V - 3.6 V	– 5		5	– 7.5		7.5	µA
				0 V - 3.6 V	0 V	– 5		5	– 7.5		7.5	
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			8			12	µA
				0 V	3.6 V	– 2			– 8			
				3.6 V	0 V			2			8	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			8			12	µA
				0 V	3.6 V			2			8	
				3.6 V	0 V	– 2			– 8			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			10			16	µA
C_I	Control input capacitance	V_I = 3.3 V or GND		3.3 V	3.3 V		4.4			4.4		pF
C_{IO}	Data I/O capacitance, A Port	V_O = 1.65V DC +1 MHz -16 dBm sine wave		3.3 V	0 V		5			5		pF
C_{IO}	Data I/O capacitance, B Port	V_O = 1.65V DC +1 MHz -16 dBm sine wave		0 V	3.3 V		5			5		pF

(1) VCCI is the VCC associated with the input port.
(2) VCCO is the VCC associated with the output port.
(3) All typical data is taken at 25°C.

6.6 Switching Characteristics

表 6-1. Switching Characteristics, V_{CCA} = 0.7 V

PARAMETER		FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	173	0.5	117	0.5	85	0.5	51	0.5	50	0.5	53	0.5	65	0.5	143	ns
				–40°C to 125°C	0.5	173	0.5	117	0.5	85	0.5	51	0.5	50	0.5	53	0.5	65	0.5	143	
		B	A	–40°C to 85°C	0.5	173	0.5	154	0.5	127	0.5	88	0.5	83	0.5	82	0.5	80	0.5	80	
				–40°C to 125°C	0.5	173	0.5	154	0.5	127	0.5	88	0.5	83	0.5	82	0.5	80	0.5	80	
t_{dis}	Disable time	DIR	A	–40°C to 85°C	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	ns
				–40°C to 125°C	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	
		DIR	B	–40°C to 85°C	0.5	163	0.5	123	0.5	100	0.5	50	0.5	45	0.5	49	0.5	61	0.5	109	
				–40°C to 125°C	0.5	163	0.5	123	0.5	100	0.5	50	0.5	45	0.5	49	0.5	61	0.5	109	
t_{en}	Enable time	DIR	A	–40°C to 85°C	0.5	389	0.5	331	0.5	287	0.5	143	0.5	134	0.5	137	0.5	147	0.5	200	ns
				–40°C to 125°C	0.5	406	0.5	333	0.5	287	0.5	143	0.5	134	0.5	137	0.5	147	0.5	200	
		DIR	B	–40°C to 85°C	0.5	369	0.5	313	0.5	281	0.5	247	0.5	246	0.5	249	0.5	261	0.5	339	
				–40°C to 125°C	0.5	395	0.5	339	0.5	307	0.5	273	0.5	272	0.5	275	0.5	287	0.5	365	

表 6-2. Switching Characteristics, V_{CCA} = 0.8 V

PARAMETER		FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	153	0.5	95	0.5	64	0.5	33	0.5	27	0.5	26	0.5	27	0.5	36	ns
				–40°C to 125°C	0.5	153	0.5	95	0.5	64	0.5	33	0.5	27	0.5	26	0.5	27	0.5	36	
		B	A	–40°C to 85°C	0.5	117	0.5	96	0.5	78	0.5	52	0.5	42	0.5	41	0.5	40	0.5	39	
				–40°C to 125°C	0.5	117	0.5	96	0.5	78	0.5	52	0.5	42	0.5	41	0.5	40	0.5	39	
t_{dis}	Disable time	DIR	A	–40°C to 85°C	0.5	100	0.5	100	0.5	100	0.5	100	0.5	100	0.5	100	0.5	100	0.5	100	ns
				–40°C to 125°C	0.5	100	0.5	100	0.5	100	0.5	100	0.5	100	0.5	100	0.5	100	0.5	100	
		DIR	B	–40°C to 85°C	0.5	151	0.5	111	0.5	88	0.5	38	0.5	32	0.5	30	0.5	30	0.5	38	
				–40°C to 125°C	0.5	151	0.5	111	0.5	88	0.5	38	0.5	32	0.5	30	0.5	30	0.5	38	
t_{en}	Enable time	DIR	A	–40°C to 85°C	0.5	321	0.5	261	0.5	226	0.5	96	0.5	80	0.5	78	0.5	76	0.5	87	ns
				–40°C to 125°C	0.5	341	0.5	266	0.5	229	0.5	97	0.5	80	0.5	78	0.5	76	0.5	87	
		DIR	B	–40°C to 85°C	0.5	309	0.5	251	0.5	220	0.5	189	0.5	183	0.5	182	0.5	183	0.5	192	
				–40°C to 125°C	0.5	317	0.5	259	0.5	228	0.5	197	0.5	191	0.5	190	0.5	191	0.5	200	

表 6-3. Switching Characteristics, V_{CCA} = 0.9 V

PARAMETER		FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V	
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	126	0.5	78	0.5	52	0.5	23	0.5	18	0.5	16	0.5	15	0.5	18	ns
				–40°C to 125°C	0.5	126	0.5	78	0.5	52	0.5	23	0.5	18	0.5	16	0.5	15	0.5	18	
		B	A	–40°C to 85°C	0.5	85	0.5	64	0.5	53	0.5	40	0.5	28	0.5	24	0.5	22	0.5	21	
				–40°C to 125°C	0.5	85	0.5	64	0.5	53	0.5	40	0.5	28	0.5	24	0.5	22	0.5	21	
t_{dis}	Disable time	DIR	A	–40°C to 85°C	0.5	75	0.5	75	0.5	75	0.5	75	0.5	75	0.5	75	0.5	75	0.5	75	ns
				–40°C to 125°C	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	
		DIR	B	–40°C to 85°C	0.5	144	0.5	105	0.5	82	0.5	32	0.5	25	0.5	24	0.5	21	0.5	23	
				–40°C to 125°C	0.5	144	0.5	105	0.5	83	0.5	36	0.5	28	0.5	26	0.5	21	0.5	23	
t_{en}	Enable time	DIR	A	–40°C to 85°C	0.5	282	0.5	223	0.5	195	0.5	77	0.5	59	0.5	54	0.5	48	0.5	54	ns
				–40°C to 125°C	0.5	304	0.5	229	0.5	199	0.5	81	0.5	62	0.5	56	0.5	49	0.5	54	
		DIR	B	–40°C to 85°C	0.5	262	0.5	214	0.5	188	0.5	159	0.5	154	0.5	152	0.5	151	0.5	154	
				–40°C to 125°C	0.5	269	0.5	221	0.5	195	0.5	166	0.5	161	0.5	159	0.5	158	0.5	161	

表 6-4. Switching Characteristics, V_{CCA} = 1.2 V

PARAMETER		FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V	
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	87	0.5	52	0.5	39	0.5	15	0.5	9	0.5	8	0.5	7	0.5	7	ns
				–40°C to 125°C	0.5	87	0.5	52	0.5	39	0.5	15	0.5	10	0.5	9	0.5	7	0.5	8	
		B	A	–40°C to 85°C	0.5	51	0.5	33	0.5	23	0.5	15	0.5	12	0.5	10	0.5	7	0.5	7	
				–40°C to 125°C	0.5	51	0.5	33	0.5	23	0.5	15	0.5	12	0.5	10	0.5	8	0.5	7	

表 6-4. Switching Characteristics, V_{CCA} = 1.2 V (continued)

PARAMETER	FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	22	0.5	22	0.5	22	0.5	22	0.5	22	0.5	22	0.5	22	0.5	22	ns
			–40°C to 125°C	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	
	DIR	B	–40°C to 85°C	0.5	137	0.5	98	0.5	74	0.5	24	0.5	18	0.5	16	0.5	13	0.5	13	
			–40°C to 125°C	0.5	137	0.5	98	0.5	78	0.5	30	0.5	23	0.5	21	0.5	17	0.5	16	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	240	0.5	185	0.5	157	0.5	45	0.5	36	0.5	33	0.5	26	0.5	29	ns
			–40°C to 125°C	0.5	265	0.5	193	0.5	164	0.5	51	0.5	41	0.5	37	0.5	30	0.5	32	
	DIR	B	–40°C to 85°C	0.5	115	0.5	80	0.5	67	0.5	43	0.5	37	0.5	36	0.5	35	0.5	35	
			–40°C to 125°C	0.5	121	0.5	86	0.5	73	0.5	49	0.5	44	0.5	43	0.5	41	0.5	42	

表 6-5. Switching Characteristics, V_{CCA} = 1.5 V

PARAMETER		FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	83	0.5	42	0.5	28	0.5	12	0.5	8	0.5	7	0.5	5	0.5	5	ns
				–40°C to 125°C	0.5	83	0.5	42	0.5	28	0.5	12	0.5	9	0.5	8	0.5	6	0.5	6	
		B	A	–40°C to 85°C	0.5	50	0.5	28	0.5	18	0.5	10	0.5	8	0.5	7	0.5	5	0.5	4	
				–40°C to 125°C	0.5	50	0.5	28	0.5	18	0.5	10	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis}	Disable time	DIR	A	–40°C to 85°C	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	ns
				–40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	
		DIR	B	–40°C to 85°C	0.5	136	0.5	96	0.5	72	0.5	22	0.5	16	0.5	14	0.5	11	0.5	11	
				–40°C to 125°C	0.5	136	0.5	96	0.5	76	0.5	29	0.5	21	0.5	19	0.5	15	0.5	14	
t_{en}	Enable time	DIR	A	–40°C to 85°C	0.5	238	0.5	178	0.5	151	0.5	38	0.5	30	0.5	28	0.5	22	0.5	24	ns
				–40°C to 125°C	0.5	263	0.5	186	0.5	157	0.5	44	0.5	36	0.5	33	0.5	26	0.5	27	
		DIR	B	–40°C to 85°C	0.5	104	0.5	63	0.5	49	0.5	33	0.5	29	0.5	28	0.5	26	0.5	26	
				–40°C to 125°C	0.5	109	0.5	68	0.5	54	0.5	38	0.5	35	0.5	34	0.5	32	0.5	32	

表 6-6. Switching Characteristics, V_{CCA} = 1.8 V

PARAMETER		FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	81	0.5	41	0.5	24	0.5	10	0.5	7	0.5	6	0.5	5	0.5	4	ns
				–40°C to 125°C	0.5	81	0.5	41	0.5	24	0.5	10	0.5	8	0.5	7	0.5	5	0.5	5	
		B	A	–40°C to 85°C	0.5	53	0.5	26	0.5	16	0.5	8	0.5	7	0.5	6	0.5	5	0.5	4	
				–40°C to 125°C	0.5	53	0.5	26	0.5	16	0.5	9	0.5	7	0.5	7	0.5	5	0.5	4	

表 6-6. Switching Characteristics, V_{CCA} = 1.8 V (continued)

PARAMETER	FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	ns
			–40°C to 125°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	
	DIR	B	–40°C to 85°C	0.5	136	0.5	96	0.5	72	0.5	22	0.5	15	0.5	14	0.5	11	0.5	11	
			–40°C to 125°C	0.5	136	0.5	96	0.5	75	0.5	28	0.5	20	0.5	18	0.5	14	0.5	13	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	241	0.5	176	0.5	148	0.5	35	0.5	28	0.5	26	0.5	21	0.5	24	ns
			–40°C to 125°C	0.5	266	0.5	184	0.5	155	0.5	42	0.5	33	0.5	32	0.5	24	0.5	26	
	DIR	B	–40°C to 85°C	0.5	101	0.5	61	0.5	44	0.5	30	0.5	27	0.5	26	0.5	25	0.5	24	
			–40°C to 125°C	0.5	105	0.5	65	0.5	48	0.5	34	0.5	32	0.5	31	0.5	29	0.5	29	

表 6-7. Switching Characteristics, V_{CCA} = 2.5 V

PARAMETER		FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	80	0.5	40	0.5	22	0.5	7	0.5	5	0.5	5	0.5	4	0.5	4	ns
				–40°C to 125°C	0.5	80	0.5	40	0.5	22	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	
		B	A	–40°C to 85°C	0.5	66	0.5	27	0.5	15	0.5	7	0.5	5	0.5	5	0.5	4	0.5	3	
				–40°C to 125°C	0.5	66	0.5	27	0.5	15	0.5	7	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis}	Disable time	DIR	A	–40°C to 85°C	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	ns
				–40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	
		DIR	B	–40°C to 85°C	0.5	136	0.5	95	0.5	71	0.5	21	0.5	14	0.5	13	0.5	10	0.5	10	
				–40°C to 125°C	0.5	136	0.5	95	0.5	75	0.5	27	0.5	20	0.5	17	0.5	13	0.5	12	
t_{en}	Enable time	DIR	A	–40°C to 85°C	0.5	254	0.5	176	0.5	147	0.5	33	0.5	25	0.5	24	0.5	19	0.5	22	ns
				–40°C to 125°C	0.5	278	0.5	185	0.5	153	0.5	39	0.5	31	0.5	29	0.5	23	0.5	25	
		DIR	B	–40°C to 85°C	0.5	99	0.5	55	0.5	41	0.5	22	0.5	24	0.5	20	0.5	23	0.5	19	
				–40°C to 125°C	0.5	98	0.5	58	0.5	40	0.5	26	0.5	24	0.5	23	0.5	23	0.5	22	

表 6-8. Switching Characteristics, V_{CCA} = 3.3 V

PARAMETER		FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	79	0.5	39	0.5	22	0.5	7	0.5	4	0.5	4	0.5	3	0.5	3	ns
				–40°C to 125°C	0.5	79	0.5	39	0.5	22	0.5	7	0.5	5	0.5	4	0.5	4	0.5	4	
		B	A	–40°C to 85°C	0.5	144	0.5	36	0.5	18	0.5	7	0.5	5	0.5	4	0.5	4	0.5	3	
				–40°C to 125°C	0.5	144	0.5	36	0.5	18	0.5	8	0.5	6	0.5	5	0.5	4	0.5	4	

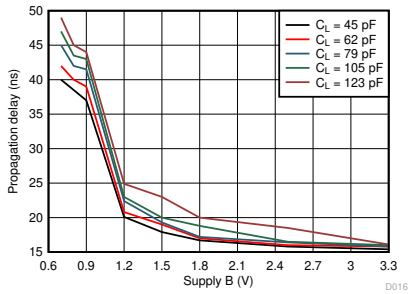
表 6-8. Switching Characteristics, V_{CCA} = 3.3 V (continued)

PARAMETER	FROM	TO	TEST CONDITIONS	B – PORT SUPPLY VOLTAGE (V_{CCB})														UNIT
				0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	ns
			–40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	
	DIR	B	–40°C to 85°C	0.5	136	0.5	95	0.5	71	0.5	21	0.5	14	0.5	12	0.5	10	0.5	10	
			–40°C to 125°C	0.5	136	0.5	95	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	331	0.5	185	0.5	149	0.5	33	0.5	25	0.5	23	0.5	19	0.5	22	ns
			–40°C to 125°C	0.5	356	0.5	93	0.5	156	0.5	40	0.5	31	0.5	29	0.5	22	0.5	24	
	DIR	B	–40°C to 85°C	0.5	98	0.5	58	0.5	41	0.5	26	0.5	23	0.5	23	0.5	22	0.5	22	
			–40°C to 125°C	0.5	99	0.5	59	0.5	42	0.5	27	0.5	25	0.5	24	0.5	24	0.5	24	

6.7 Operating Characteristics: T_A = 25°C

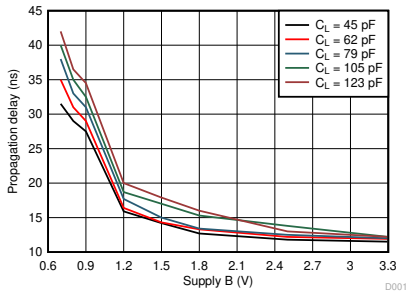
PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	0.7 V	0.7 V		1.3		pF
			0.8 V	0.8 V		1.3		
			0.9 V	0.9 V		1.3		
			1.2 V	1.2 V		1.3		
			1.5 V	1.5 V		1.3		
			1.8 V	1.8 V		1.4		
			2.5 V	2.5 V		1.7		
			3.3 V	3.3 V		2.1		
	Power Dissipation Capacitance per transceiver (B to A)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	0.7 V	0.7 V		9.2		pF
			0.8 V	0.8 V		9.4		
			0.9 V	0.9 V		9.4		
			1.2 V	1.2 V		9.8		
			1.5 V	1.5 V		10.1		
			1.8 V	1.8 V		11.0		
			2.5 V	2.5 V		14.4		
			3.3 V	3.3 V		18.6		
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	0.7 V	0.7 V		9.2		pF
			0.8 V	0.8 V		9.3		
			0.9 V	0.9 V		9.4		
			1.2 V	1.2 V		9.7		
			1.5 V	1.5 V		10.1		
			1.8 V	1.8 V		11.0		
			2.5 V	2.5 V		14.4		
			3.3 V	3.3 V		18.3		
	Power Dissipation Capacitance per transceiver (B to A)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	0.7 V	0.7 V		1.3		pF
			0.8 V	0.8 V		1.3		
			0.9 V	0.9 V		1.3		
			1.2 V	1.2 V		1.3		
			1.5 V	1.5 V		1.3		
			1.8 V	1.8 V		1.4		
			2.5 V	2.5 V		1.7		
			3.3 V	3.3 V		2.1		

6.8 Typical Characteristics



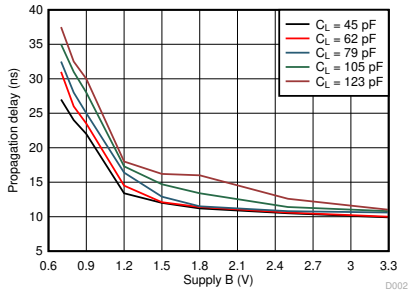
T_A = 25°C V_{CCA} = 0.7 V

图 6-1. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



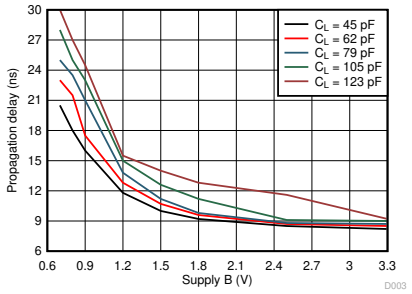
T_A = 25°C V_{CCA} = 0.8 V

图 6-2. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



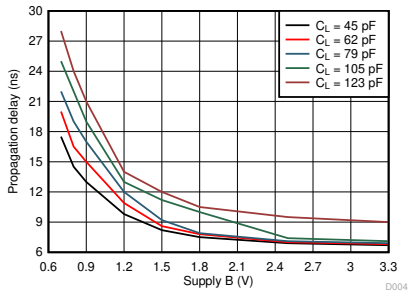
T_A = 25°C V_{CCA} = 0.9 V

图 6-3. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



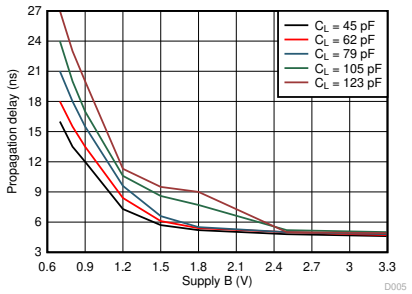
T_A = 25°C V_{CCA} = 1.2 V

图 6-4. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



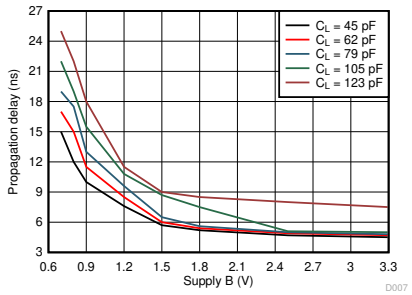
T_A = 25°C V_{CCA} = 1.5 V

图 6-5. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



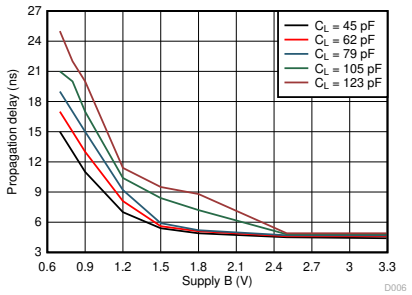
T_A = 25°C V_{CCA} = 1.8 V

图 6-6. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



T_A = 25°C V_{CCA} = 3.3 V

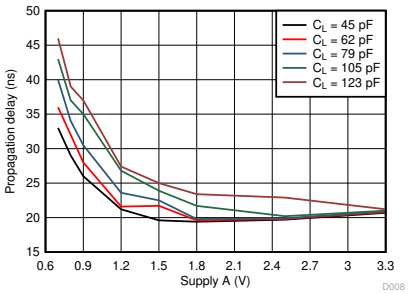
图 6-7. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



T_A = 25°C V_{CCA} = 2.5 V

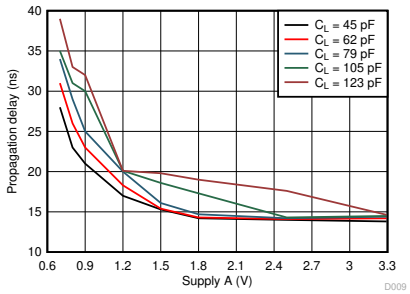
图 6-8. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance

6.8 Typical Characteristics (continued)



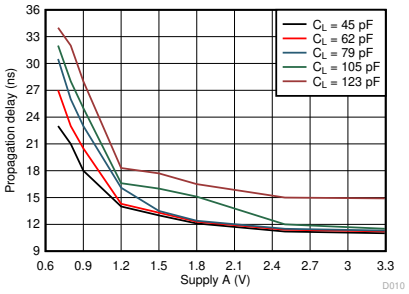
T_A = 25°C V_{CCA} = 0.7 V

图 6-9. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



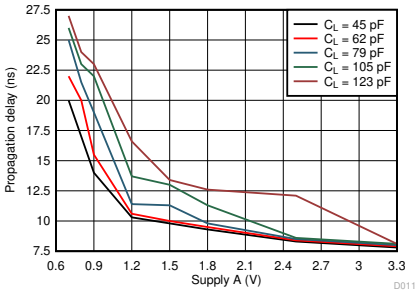
T_A = 25°C V_{CCA} = 0.8 V

图 6-10. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



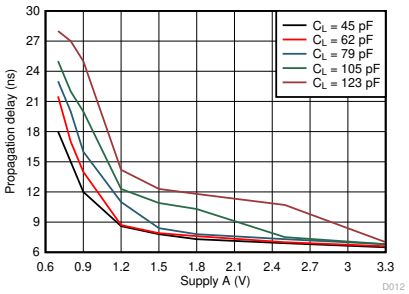
T_A = 25°C V_{CCA} = 0.9 V

图 6-11. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



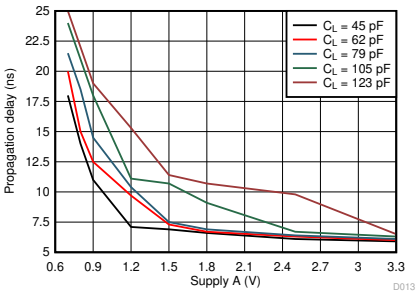
T_A = 25°C V_{CCA} = 1.2 V

图 6-12. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



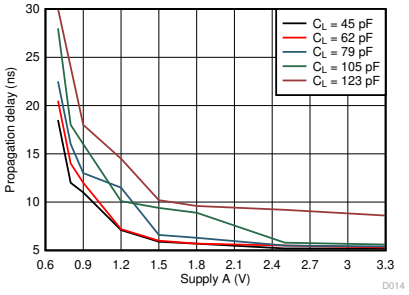
T_A = 25°C V_{CCA} = 1.5 V

图 6-13. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



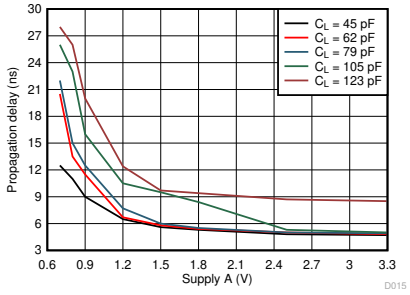
T_A = 25°C V_{CCA} = 1.8 V

图 6-14. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



T_A = 25°C V_{CCA} = 2.5 V

图 6-15. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



T_A = 25°C V_{CCA} = 3.3 V

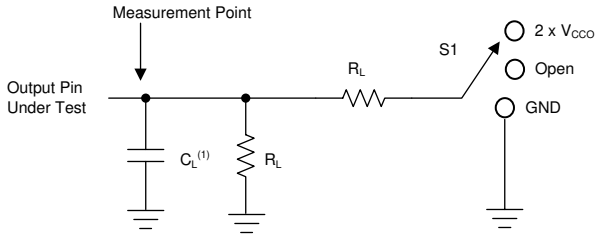
图 6-16. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

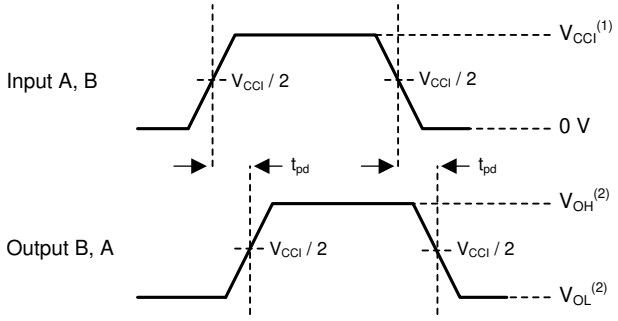


A. C_L includes probe and jig capacitance.

图 7-1. Load Circuit

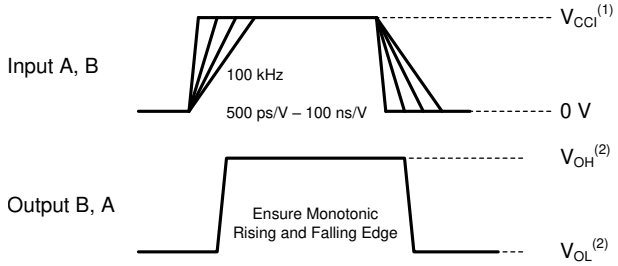
表 7-1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
Δt/Δv	Input transition rise or fall rate	0.65 V – 3.6 V	1 MΩ	15 pF	Open	N/A
t_{pd}	Propagation (delay) time	1.1 V – 3.6 V	2 kΩ	15 pF	Open	N/A
		0.65 V – 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	2 × V_{CCO}	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	2 × V_{CCO}	0.1 V
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	GND	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	GND	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	GND	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	GND	0.1 V



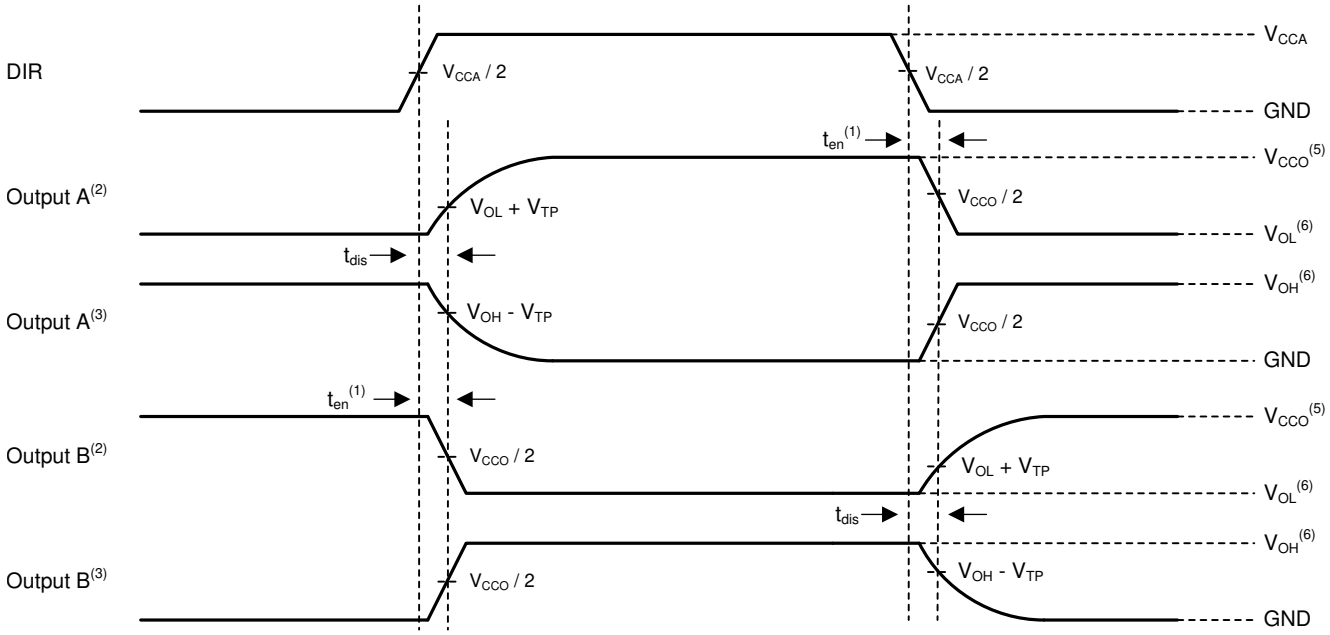
1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

图 7-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

图 7-3. Input Transition Rise or Fall Rate



1. Illustrative purposes only. Enable Time is a calculation as described in the data sheet.
2. Output waveform on the condition that input is driven to a valid Logic Low.
3. Output waveform on the condition that input is driven to a valid Logic High.
4. V_{CCI} is the supply pin associated with the input port
5. V_{CCO} is the supply pin associated with the output port.
6. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

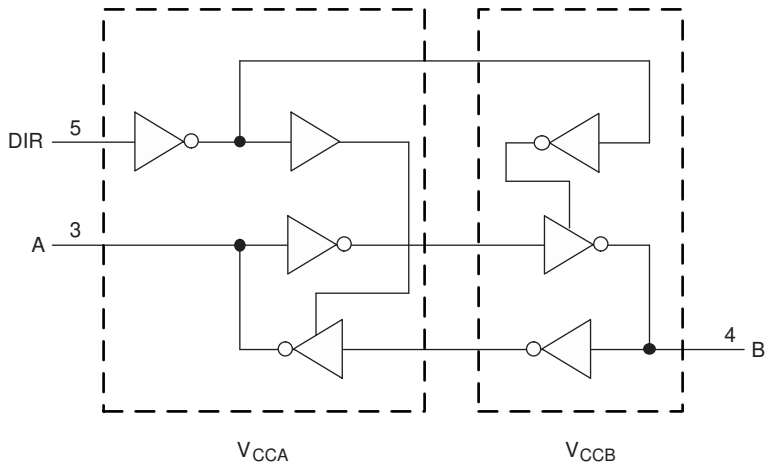
图 7-4. Disable and Enable Time

8 Detailed Description

8.1 Overview

The SN74AXC1T45 is single-bit, dual-supply, noninverting voltage level translation. Pin A and the direction control pin are support by V_{CCA} and pin B is support by V_{CCB}. The A port can accept I/O voltages ranging from 0.65 V to 3.6 V, and the B port can accept I/O voltages from 0.65 V to 3.6 V. A high logic on the DIR pin allows data transmission from A to B and a logic low on the DIR pin allows data transmission from B to A.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 0.65-V to 3.6-V Power-Supply Range

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V and 3.3 V).

8.3.2 Support High-Speed Translation

The SN74AXC1T45 device can support high data-rate applications. The translated signal data rate can be up to 500 Mbps when signal is translated from 1.8 V to 3.3 V.

8.3.3 I_{off} Supports Partial-Power-Down Mode Operation

The I_{off} circuit prevents backflow current by disabling the I/O output circuits when the device is in partial-power-down mode.

8.4 Device Functional Modes

表 8-1 lists the device functions for the DIR input.

表 8-1. Function Table

INPUT(1) DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AXC1T45 device can be used in level-translation applications for interfacing devices or systems with one another when they are operating at different interface voltages. The maximum data rate can be up to 500 Mbps when the device translate signal is from 1.8 V to 3.3 V.

9.1.1 Enable Times

Calculate the enable times for the SN74AXC1T45 using the following formulas:

$$t_{A\_en}\ (\text{DIR to A}) = t_{dis}\ (\text{DIR to B}) + t_{pd}\ (\text{B to A}) \quad (1)$$

$$t_{B\_en}\ (\text{DIR to B}) = t_{dis}\ (\text{DIR to A}) + t_{pd}\ (\text{A to B}) \quad (2)$$

In a bidirectional application, these enable times provide the maximum delay time from the time the DIR bit is switched until an output is expected. For example, if the SN74AXC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled ($t_{dis)}$ before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay (t_{pd}). To avoid bus contention care should be taken to not apply an input signal prior to the output port being disabled (t_{dis} max).

9.2 Typical Applications

9.2.1 Unidirectional Logic Level-Shifting Application

图 9-1 shows an example of the SN74AXC1T45 being used in a unidirectional logic level-shifting application.

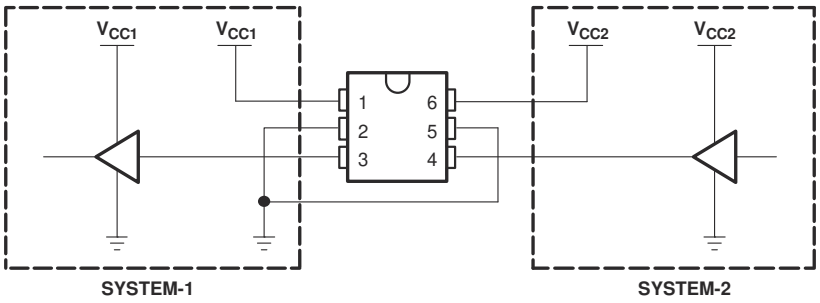


图 9-1. Unidirectional Logic Level-Shifting Application

表 9-1. Unidirectional Level Shifting Function

PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (0.65 V to 3.6 V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V_{CC1} voltage.
4	B	IN	Input threshold value depends on V_{CC2} voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (0.65 V to 3.6 V)

9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-2.

表 9-2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC1T45 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC1T45 device is driving to determine the output voltage range.

9.2.1.3 Application Curve

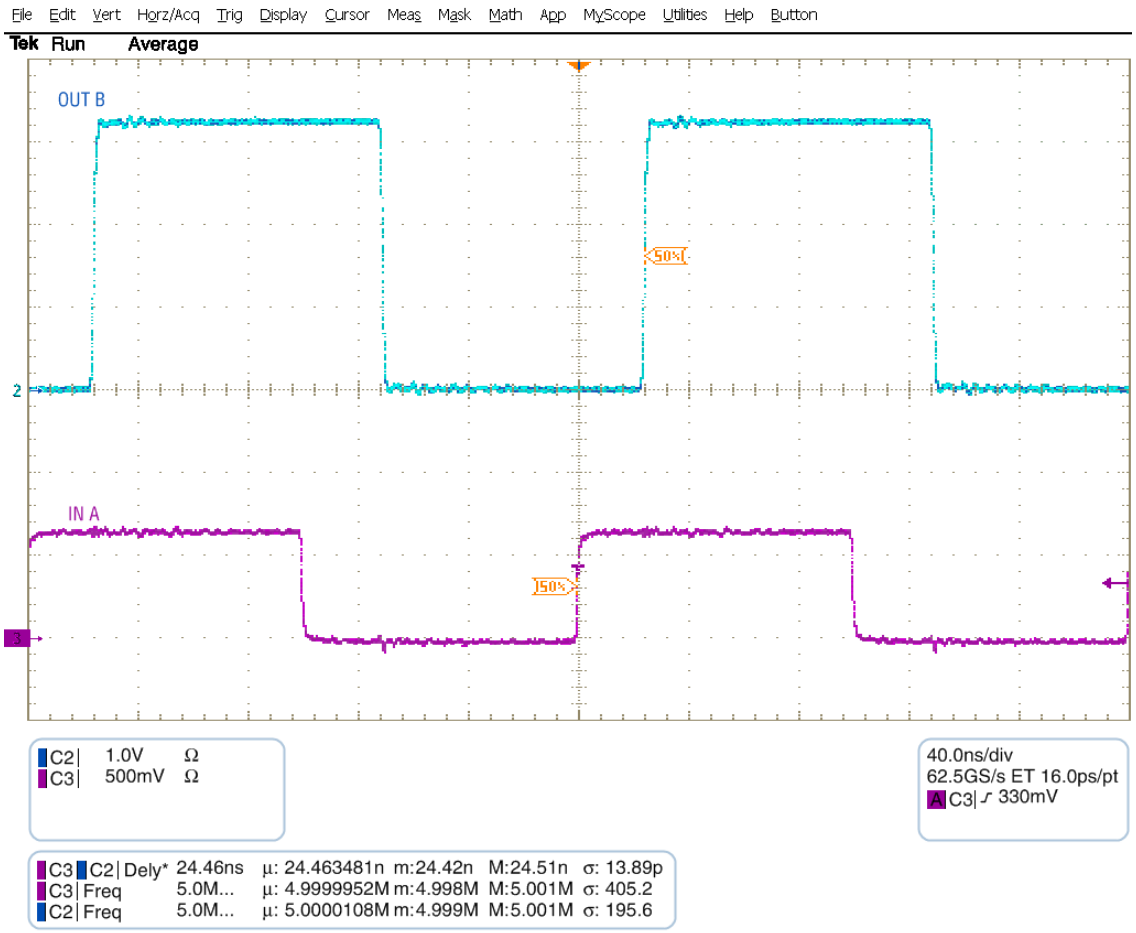


图 9-2. Up Translation at 2.5 MHz (0.7 V to 3.3 V)

9.2.2 Bidirectional Logic Level-Shifting Application

图 9-3 shows the SN74AXC1T45 being used in a bidirectional logic level-shifting application. Because the SN74AXC1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

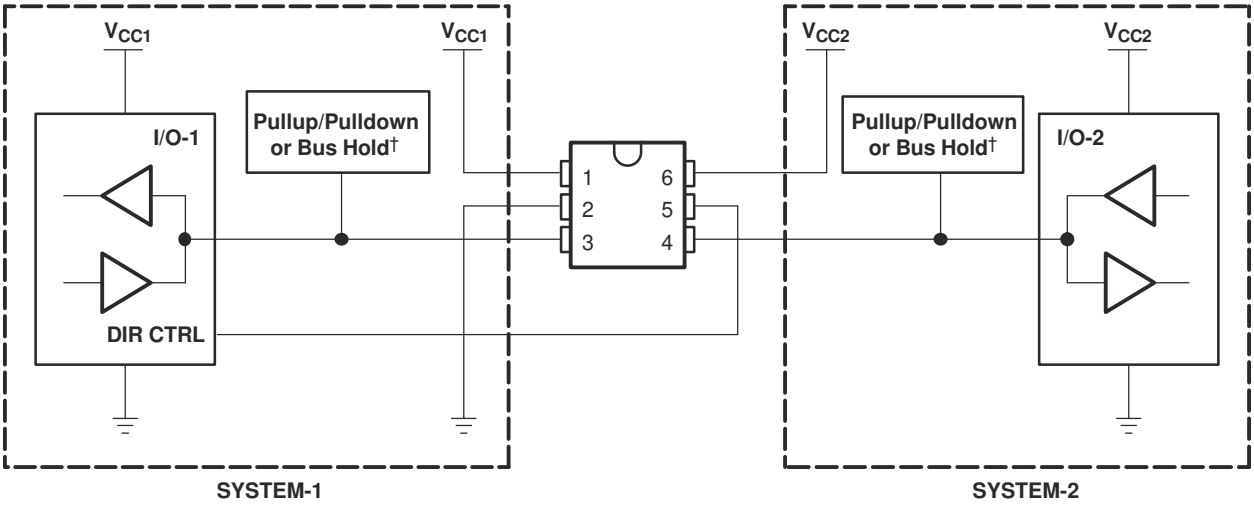


图 9-3. Bidirectional Logic Level-Shifting Application

表 9-3 lists the data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

表 9-3. Data Transmission: SYSTEM-1 and SYSTEM-2

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2.
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown resistors.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown resistors.(1)
4	L	In	Out	SYSTEM-2 data to SYSTEM-1.

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, essentially, both pullup or both pulldown.

9.2.2.1 Design Requirements

Refer to *Design Requirements*.

9.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

9.2.2.3 Application Curve

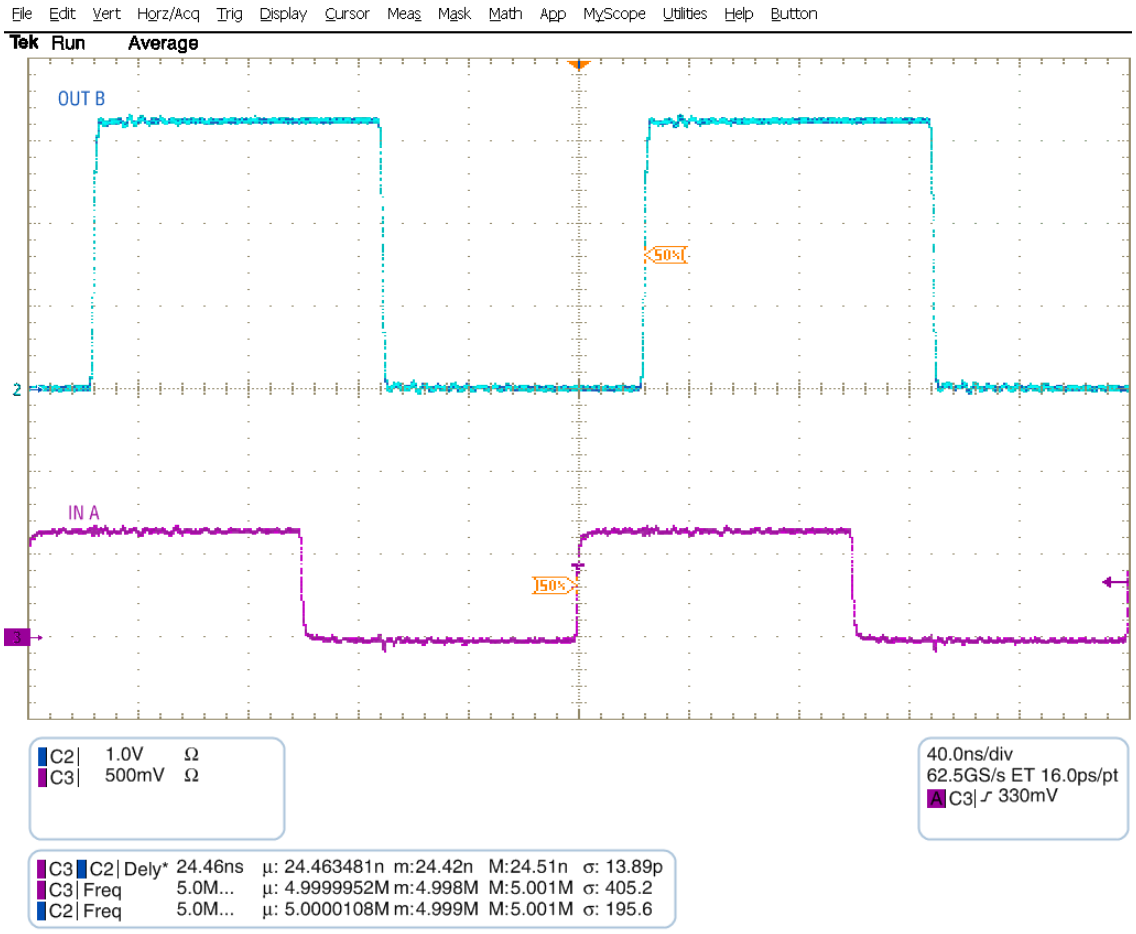


图 9-4. Up Translation at 2.5 MHz (0.7 V to 3.3 V)

10 Power Supply Recommendations

The SN74AXC1T45 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. The V_{CCA} power-supply rail accepts any supply voltage from 0.65 V to 3.6 V and the V_{CCB} power-supply rail accepts any supply voltage from 0.65 V to 3.6 V. The A port and B port are designed to track the V_{CCA} and V_{CCB} supplies respectively allowing for low-voltage, bidirectional translation between any of the 0.7-V, 0.8-V, 0.9-V, 1.2-V, 1.5 - V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

10.1 Power-Up Considerations

A proper power-up sequence must be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect the ground before any supply voltage is applied.
2. Power up the V_{CCA} and V_{CCB} supplies. The V_{CCA} and V_{CCB} supplies can be ramped in any order.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

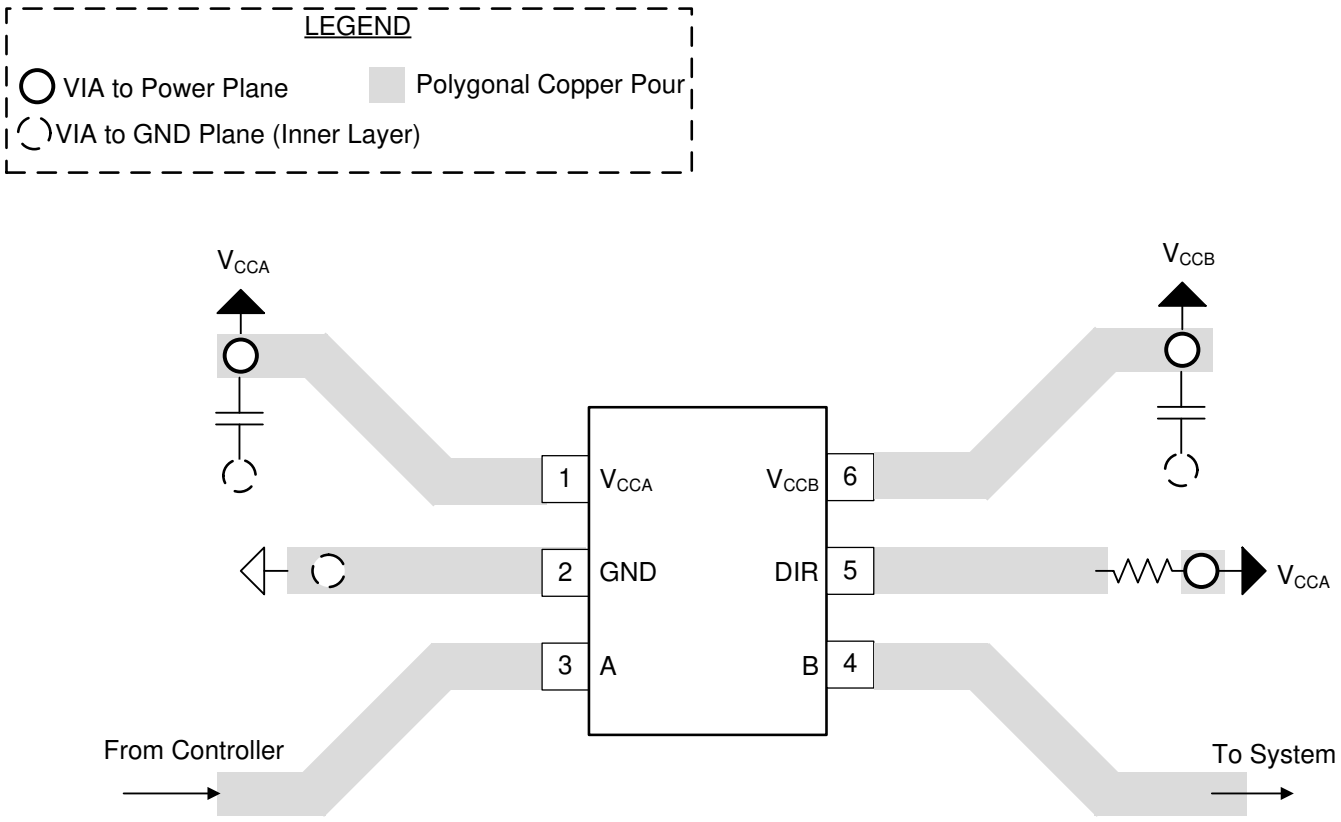


图 11-1. PCB Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Evaluate SN74AXC1T45DRL Using a Generic EVM* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Power Sequencing for the AXC Family of Devices* application report

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXC1T45DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GRL	Samples
SN74AXC1T45DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1A3	Samples
SN74AXC1T45DEAR	ACTIVE	X2SON	DEA	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CR	Samples
SN74AXC1T45DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1A1	Samples
SN74AXC1T45DTQR	ACTIVE	X2SON	DTQ	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

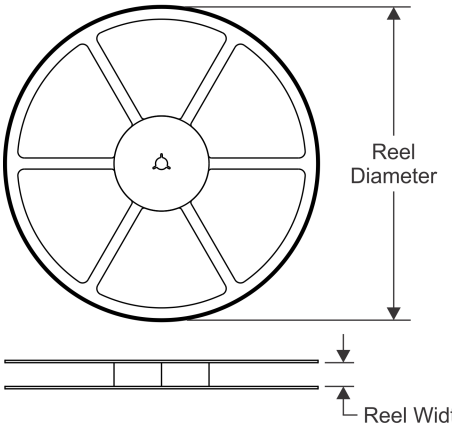
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

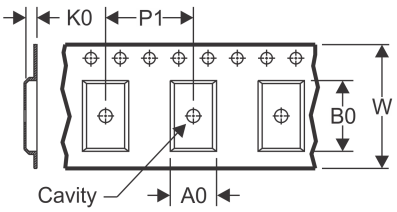
9-Sep-2020

TAPE AND REEL INFORMATION

REEL DIMENSIONS

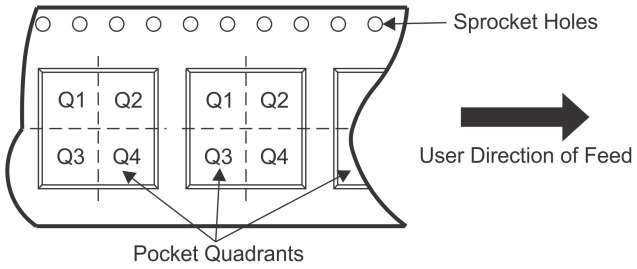


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



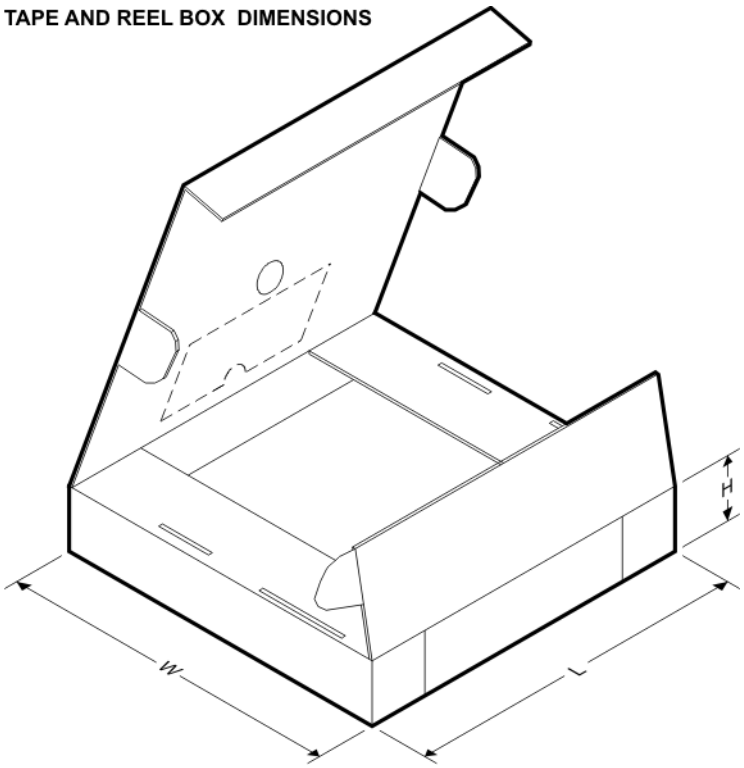
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXC1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AXC1T45DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AXC1T45DEAR	X2SON	DEA	6	5000	180.0	9.5	1.13	1.13	0.5	4.0	8.0	Q3
SN74AXC1T45DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AXC1T45DTQR	X2SON	DTQ	6	3000	180.0	9.5	0.94	1.13	0.5	2.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

9-Sep-2020

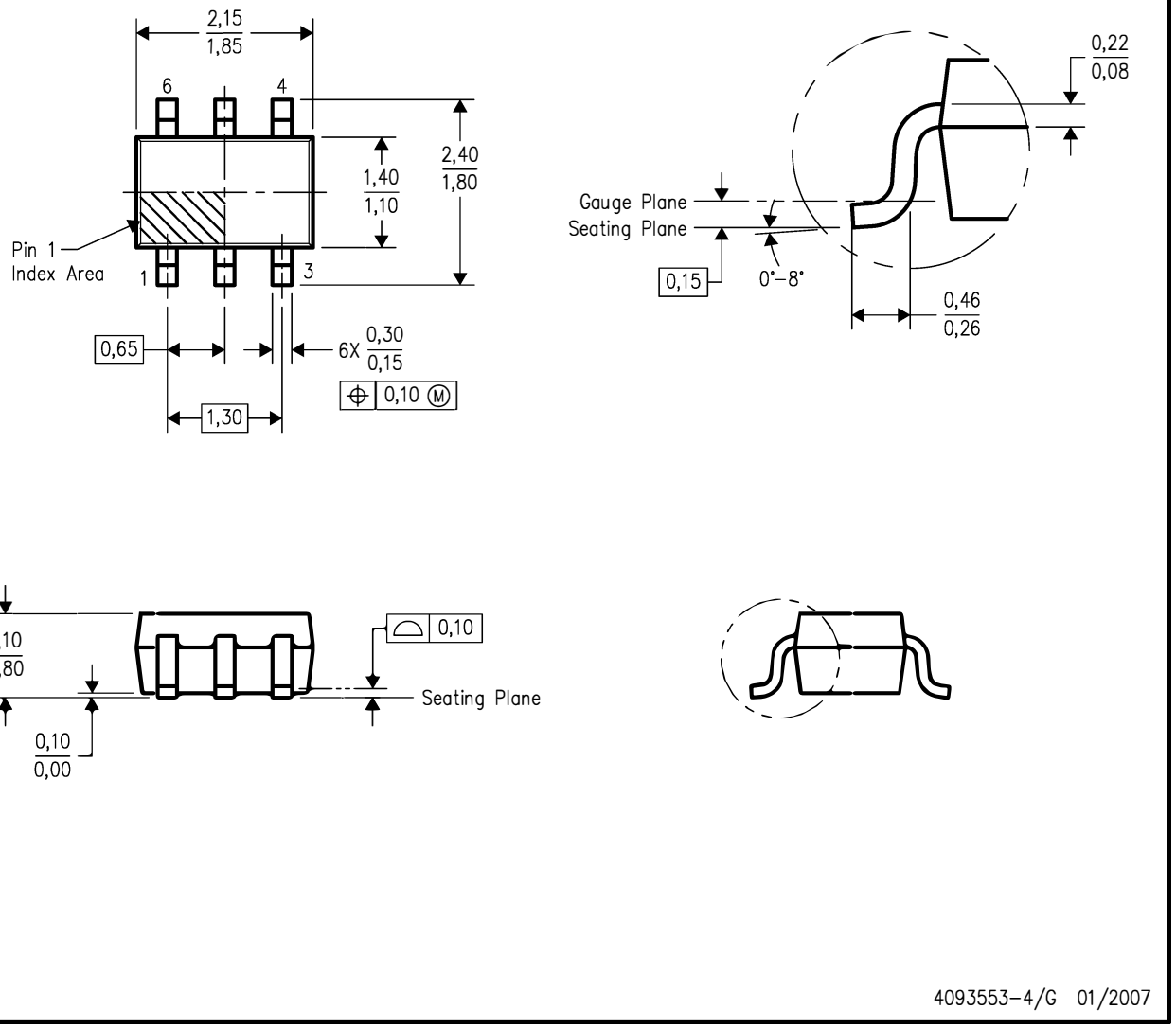
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

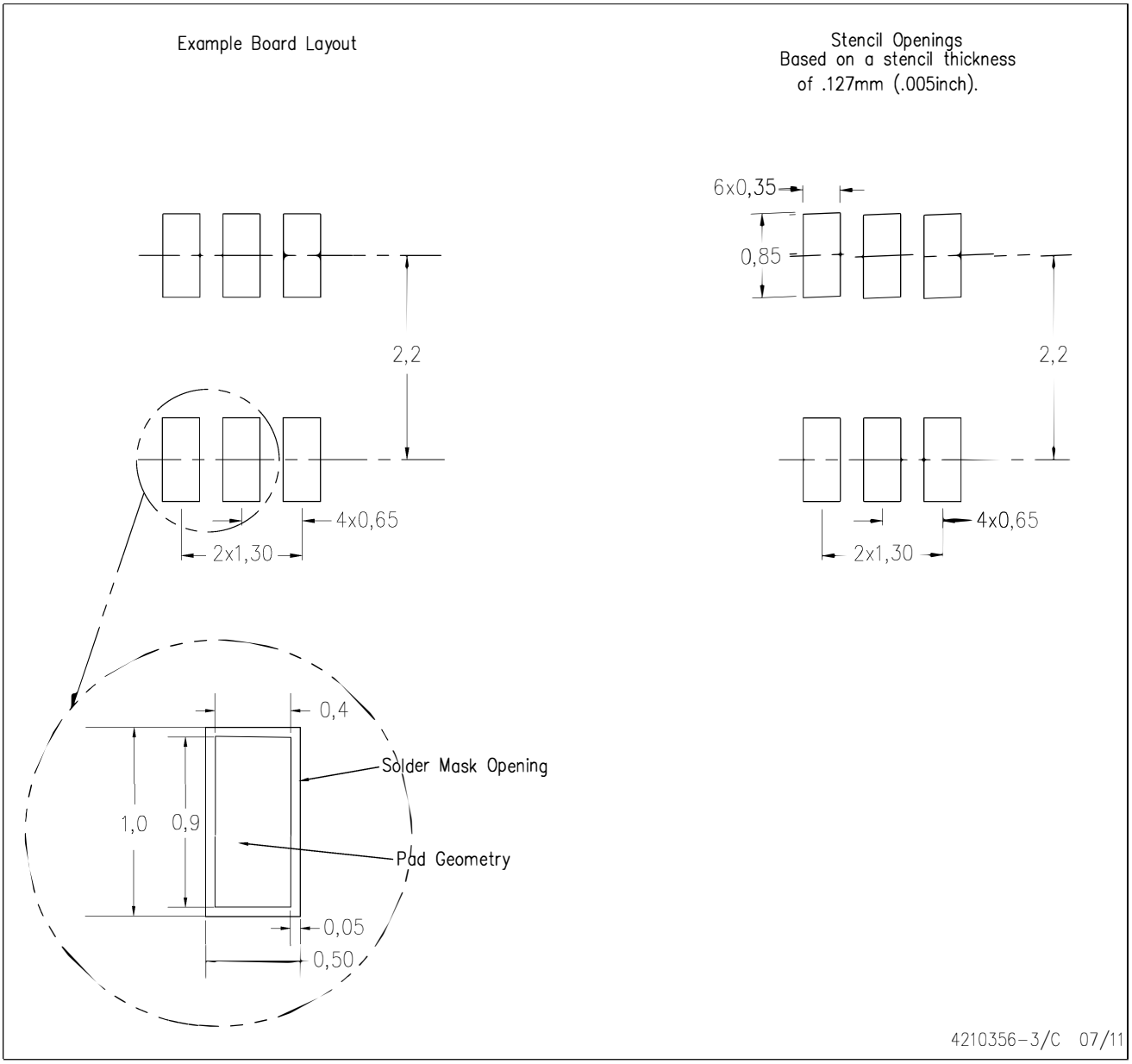
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXC1T45DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74AXC1T45DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AXC1T45DEAR	X2SON	DEA	6	5000	189.0	185.0	36.0
SN74AXC1T45DRLR	SOT-5X3	DRL	6	4000	183.0	183.0	20.0
SN74AXC1T45DTQR	X2SON	DTQ	6	3000	189.0	185.0	36.0

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



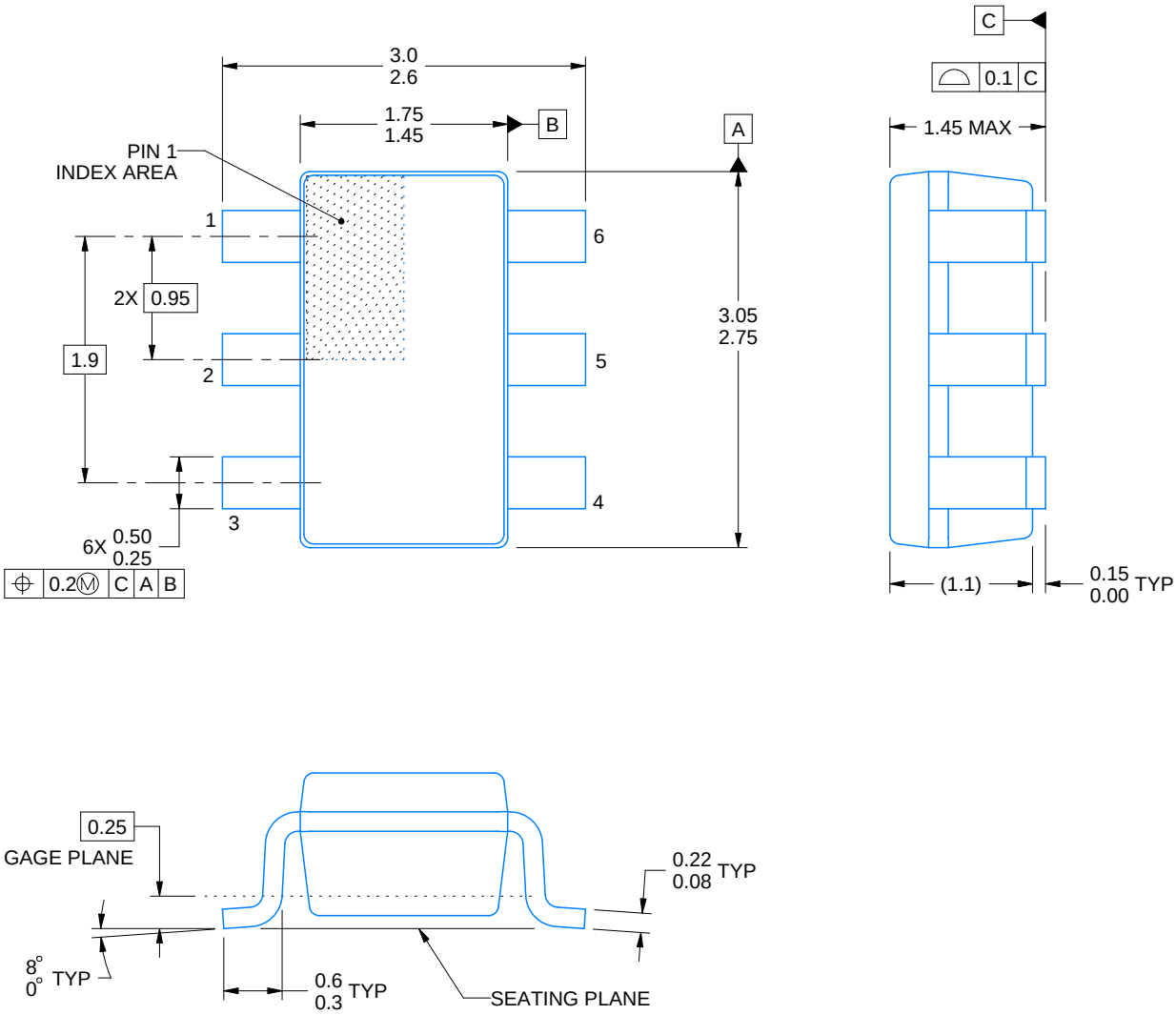
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/C 06/2021

NOTES:

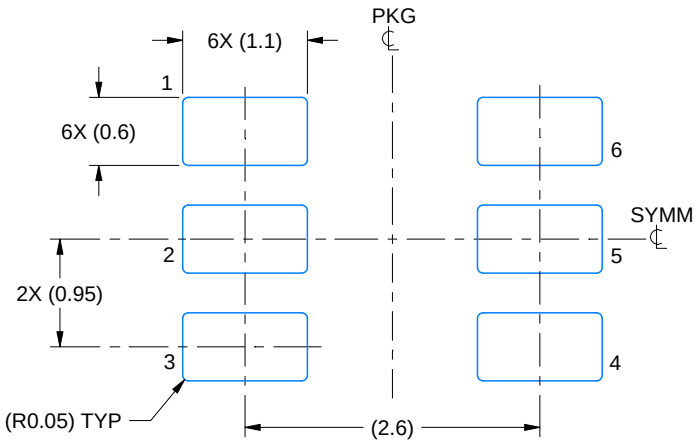
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

EXAMPLE BOARD LAYOUT

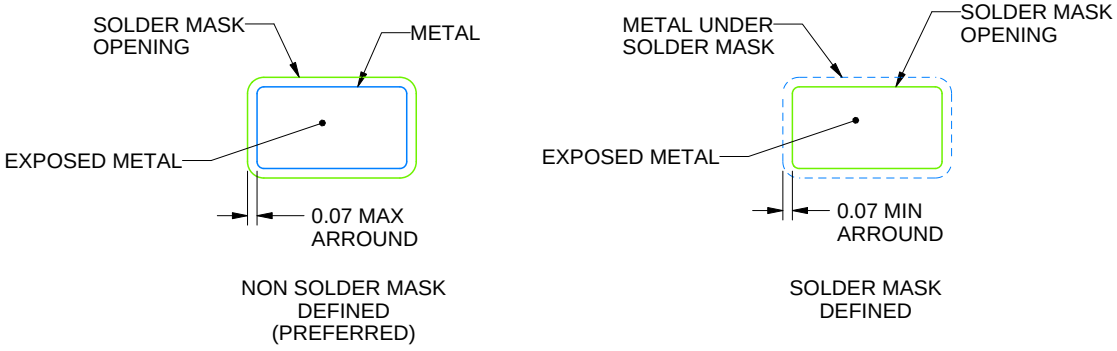
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

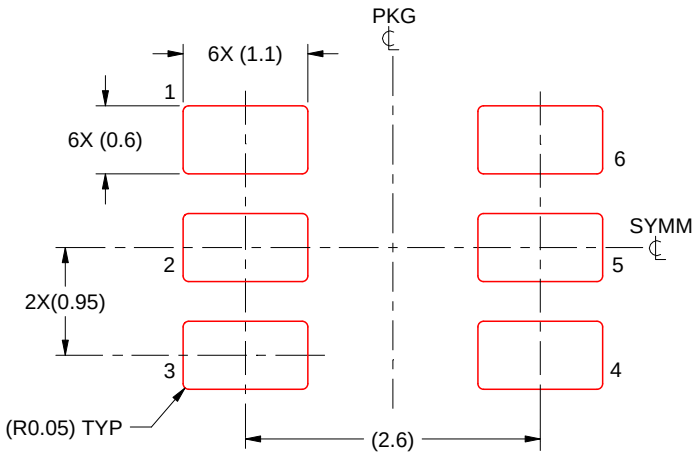
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

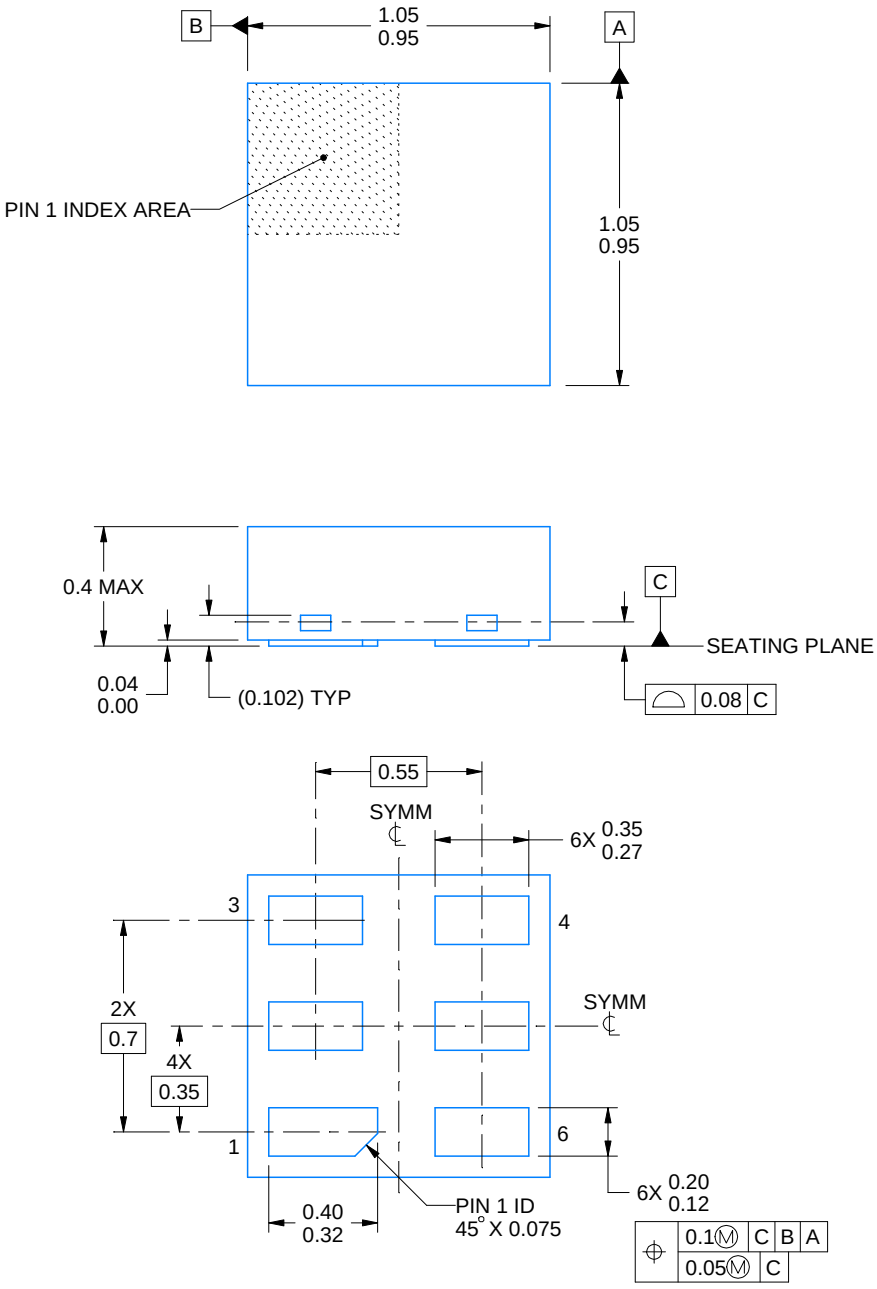
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DEA0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4223910/C 12/2017

NOTES:

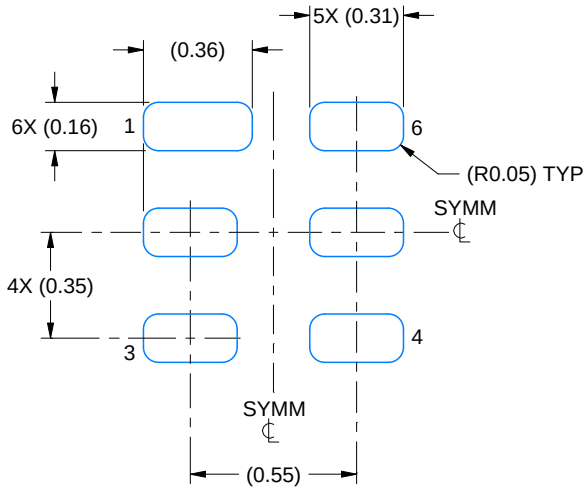
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

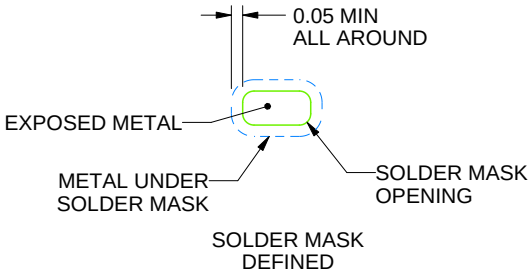
DEA0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4223910/C 12/2017

NOTES: (continued)

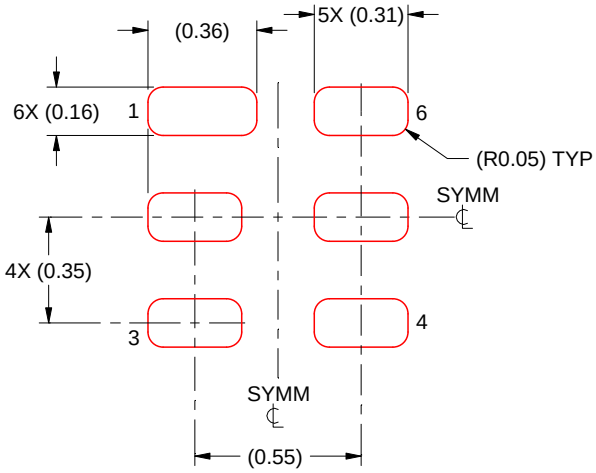
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DEA0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE:40X

4223910/C 12/2017

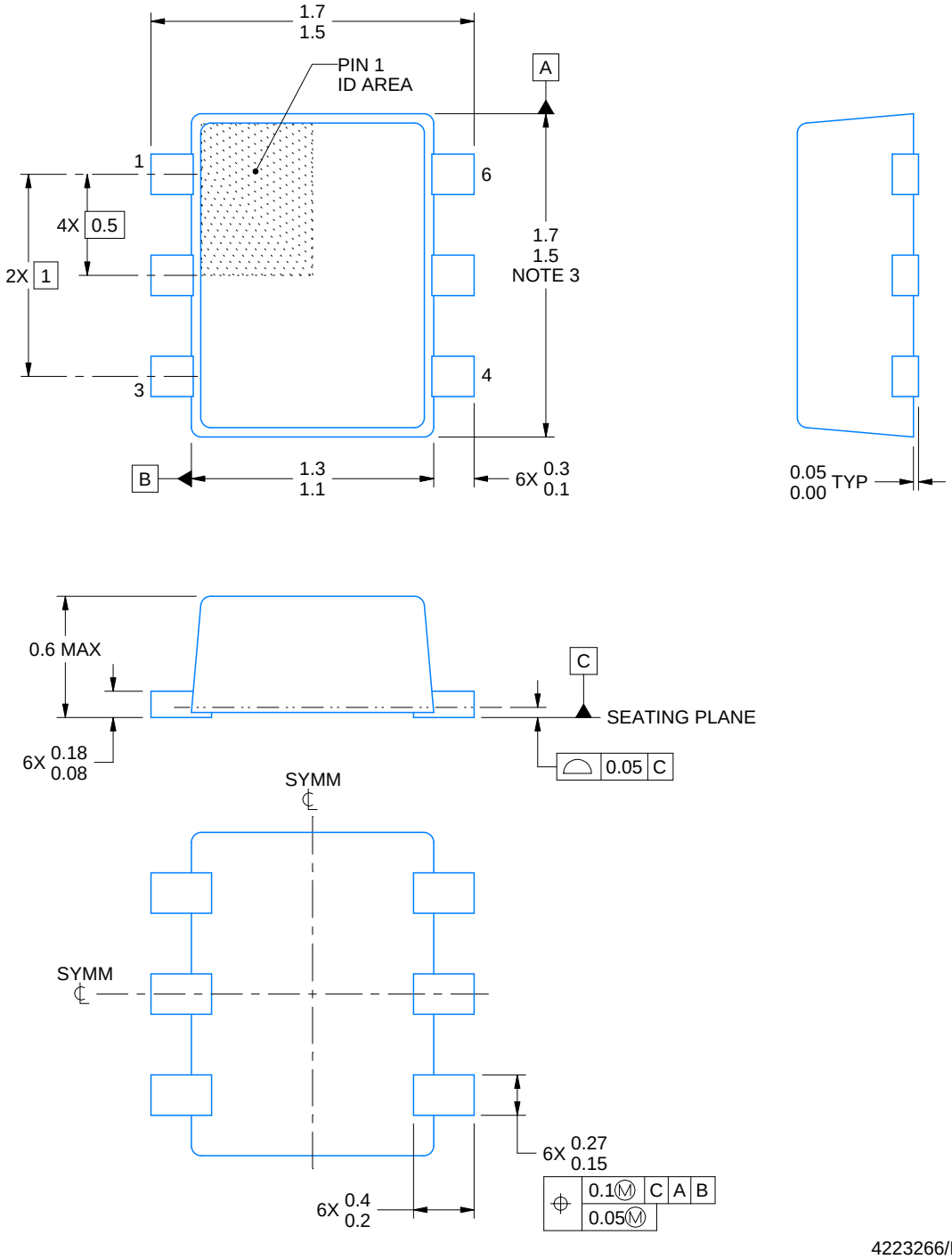
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

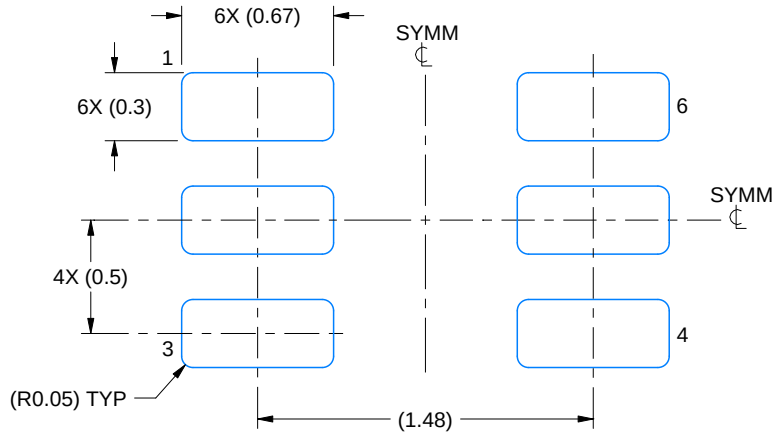
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

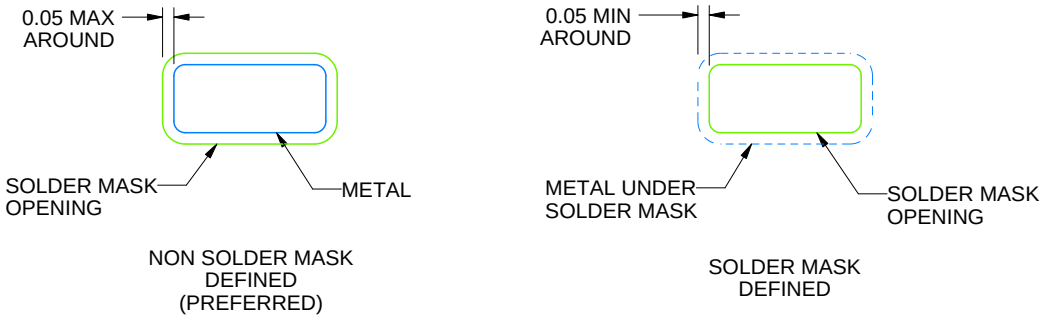
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/B 12/2020

NOTES: (continued)

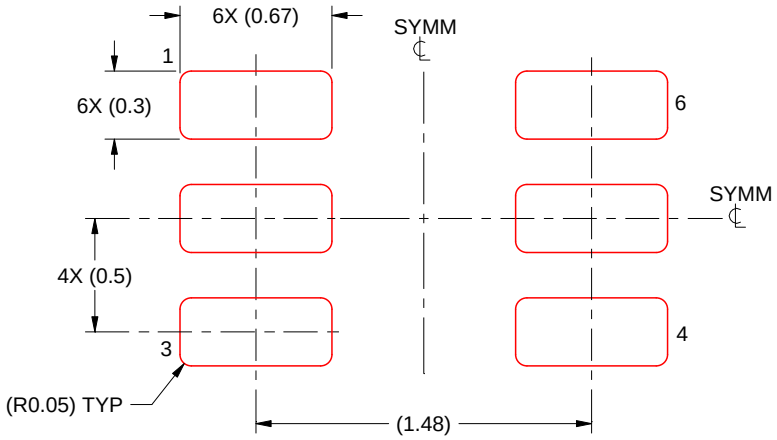
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/B 12/2020

NOTES: (continued)

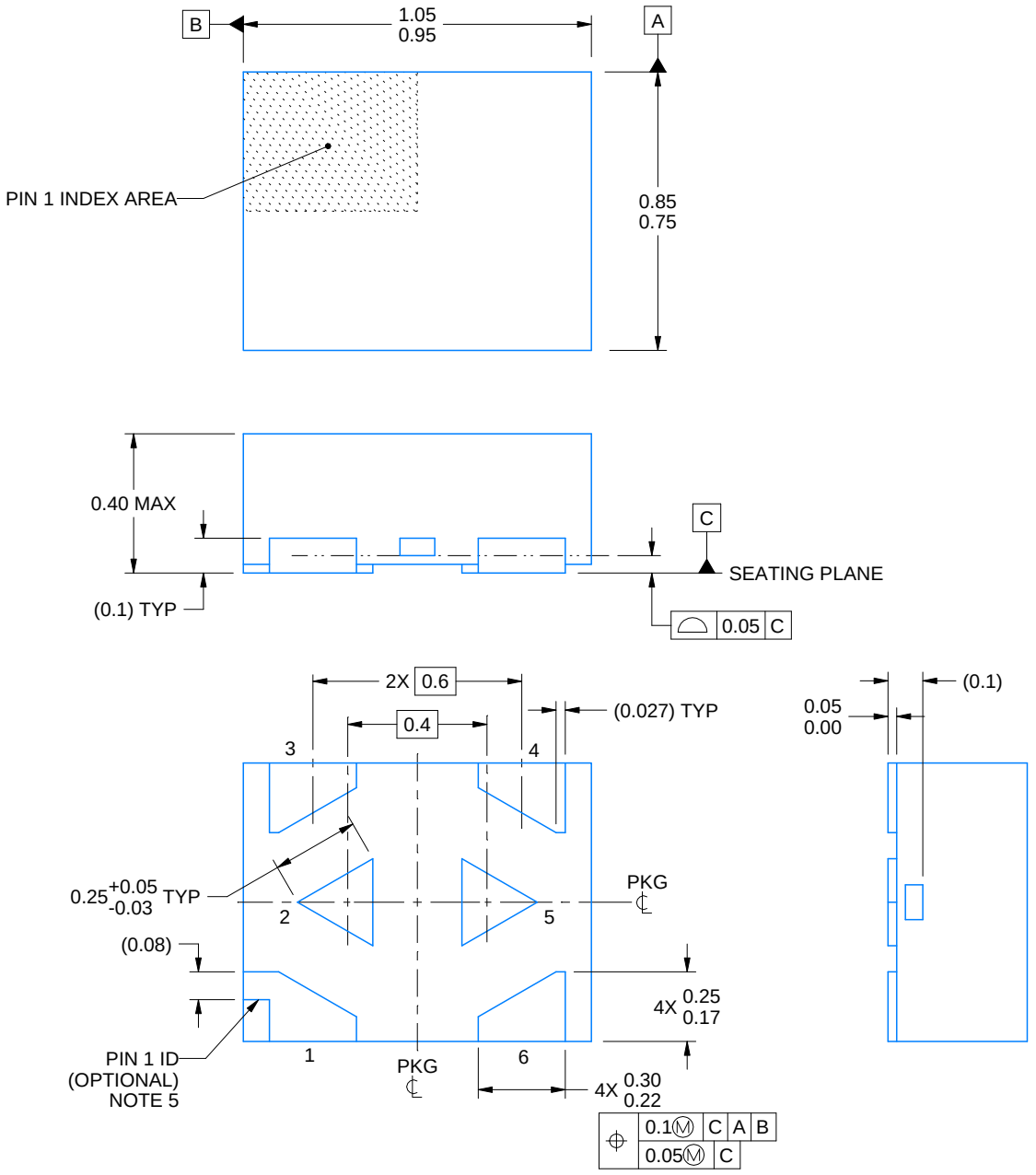
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DTQ0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4224056/A 11/2017

NOTES:

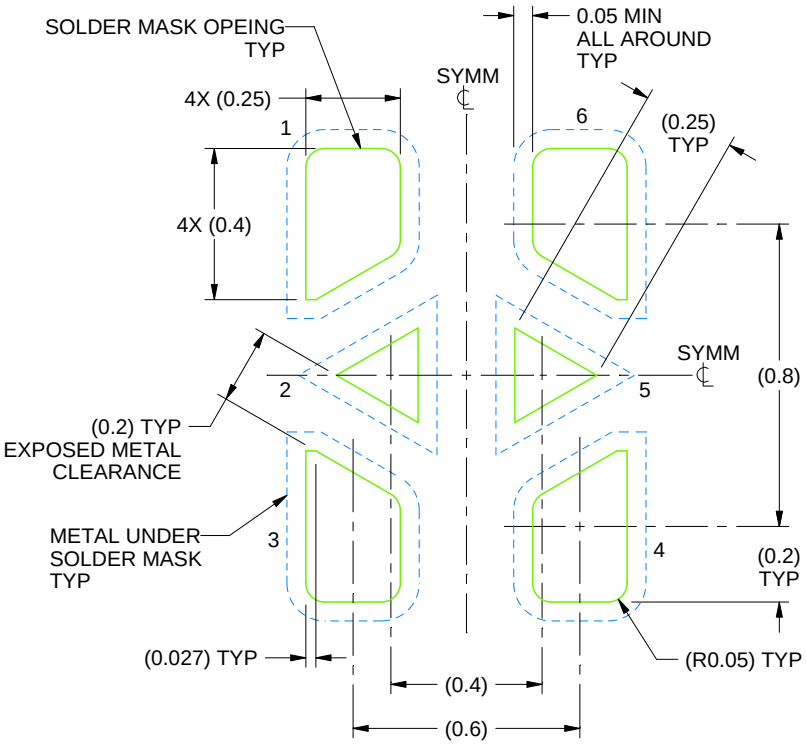
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

EXAMPLE BOARD LAYOUT

DTQ0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4224056/A 11/2017

NOTES: (continued)

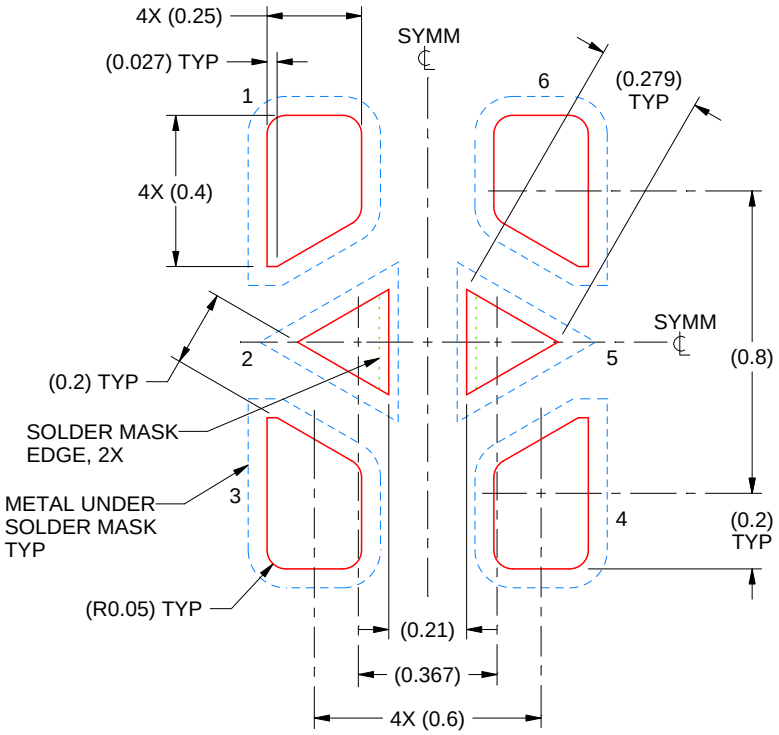
6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DTQ0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4224056/A 11/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.