74LVC1G125
Bus Buffer/Line Driver with 3-State Output

GENERAL DESCRIPTION

The 74LVC1G125 is a single buffer/line driver with a non-inverting 3-state output and it is designed for 1.65V to 5.5V V_{CC} operation. The 3-state output is controlled by the output enable input ($\overline{OE}$). When $\overline{OE}$ is low, the device passes data from the A input to the Y output. When $\overline{OE}$ is high, the output is in the high-impedance state.

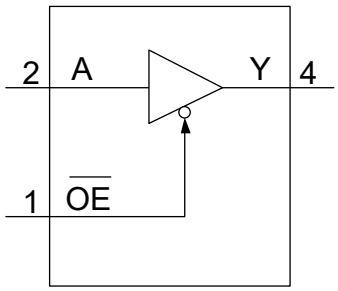
The input can be driven from either 3.3V or 5V devices. This feature allows the use of this device in a mixed 3.3V and 5V environment.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

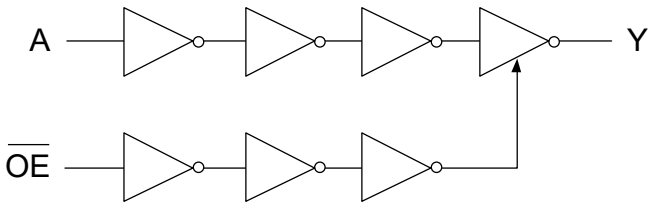
FEATURES

- **Wide Supply Voltage Range: 1.65V to 5.5V**
- **High Noise Immunity**
- **±24mA Output Drive at V_{CC} = 3.0V**
- **CMOS Low Power Consumption**
- **Inputs Accept Voltages Up to 5V**
- **Direct Interface with TTL Levels**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SC70-5 Package**

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUT		OUTPUT
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	*X*	Z

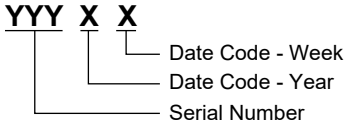
H = High Voltage Level
L = Low Voltage Level
Z = High-Impedance State
X = Don't Care

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC1G125	SC70-5	-40℃ to +125℃	74LVC1G125XC5G/TR	R56XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 6.5V
Input Voltage, V_I (2) ..... -0.5V to 6.5V
Output Voltage, V_O (2) (3)
Active Mode .....-0.5V to V_{CC} + 0.5V
Power-Down Mode .....-0.5 to 6.5V
Input Clamping Current, I_{IK} (V_I < 0V).....-50mA
Output Clamping Current, I_{OK} (V_O > V_{CC} or V_O < 0V)
.....±50mA
Output Current, I_O (V_O = 0V to V_{CC}) .....±50mA
Supply Current, I_{CC} 50mA
Ground Current, I_{GND}.....-50mA
Junction Temperature (4) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} .....1.65V to 5.5V
Input Voltage, V_I.....0V to 5.5V
Output Voltage, V_O
Active Mode ..... 0V to V_{CC}
Power-Down Mode, V_{CC} = 0V .....0V to 5.5V
Input Transition Rise and Fall Rate, Δt/ΔV
V_{CC} = 1.65V to 2.7V ..... 20ns/V (MAX)
V_{CC} = 2.7V to 5.5V ..... 10ns/V (MAX)
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. When V_{CC} = 0V (power-down mode), the output voltage can be 5.5V in normal operation.

4. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

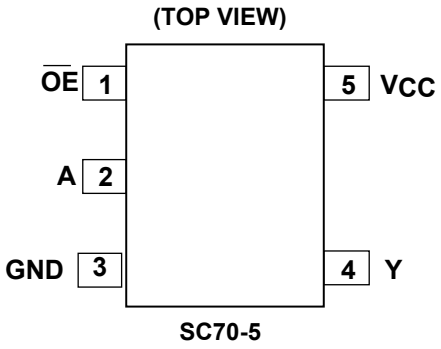
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$\overline{OE}$	Output Enable Input.
2	A	Data Input.
3	GND	Ground.
4	Y	Data Output.
5	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.65V to 1.95V		Full	0.65 × V_{CC}			V
		V_{CC} = 2.3V to 2.7V		Full	1.7			
		V_{CC} = 2.7V to 3.6V		Full	2			
		V_{CC} = 4.5V to 5.5V		Full	0.7 × V_{CC}			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.65V to 1.95V		Full			0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V		Full			0.7	
		V_{CC} = 2.7V to 3.6V		Full			0.8	
		V_{CC} = 4.5V to 5.5V		Full			0.3 × V_{CC}	
High-Level Output Voltage	V_{OH}	V_I = V_{IH}	V_{CC} = 1.65V to 5.5V, I_O = -100μA	Full	V_{CC} - 0.05	V_{CC} - 0.01		V
			V_{CC} = 1.65V, I_O = -4mA	Full	1.43	1.55		
			V_{CC} = 2.3V, I_O = -8mA	Full	2.02	2.18		
			V_{CC} = 2.7V, I_O = -12mA	Full	2.38	2.56		
			V_{CC} = 3.0V, I_O = -24mA	Full	2.52	2.74		
			V_{CC} = 4.5V, I_O = -32mA	Full	4	4.22		
Low-Level Output Voltage	V_{OL}	V_I = V_{IL}	V_{CC} = 1.65V to 5.5V, I_O = 100μA	Full		0.01	0.05	V
			V_{CC} = 1.65V, I_O = 4mA	Full		0.1	0.22	
			V_{CC} = 2.3V, I_O = 8mA	Full		0.12	0.28	
			V_{CC} = 2.7V, I_O = 12mA	Full		0.16	0.34	
			V_{CC} = 3.0V, I_O = 24mA	Full		0.3	0.56	
			V_{CC} = 4.5V, I_O = 32mA	Full		0.32	0.6	
Input Leakage Current	I_I	V_{CC} = 0V to 5.5V, V_I = 5.5V or GND		Full		±0.01	±1	μA
Off-State Output Current	I_{OZ}	V_{CC} = 3.6V, V_I = V_{IH} or V_{IL}, V_O = 5.5V or GND		Full		±0.01	±1	μA
Power-Off Leakage Current	I_{OFF}	V_{CC} = 0V, V_I or V_O = 5.5V		Full		±0.01	±1	μA
Supply Current	I_{CC}	V_{CC} = 1.65V to 5.5V, V_I = 5.5V or GND, I_O = 0A		Full		0.01	1	μA
Additional Supply Current	ΔI_{CC}	Per pin, V_{CC} = 2.3V to 5.5V, V_I = V_{CC} - 0.6V, I_O = 0A		Full		0.05	10	μA
Input Capacitance	C_I	V_{CC} = 3.3V, V_I = GND to V_{CC}		+25℃		3.5		pF

DYNAMIC CHARACTERISTICS

(For test circuit, see Figure 1. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃ and V_{CC} = 1.8V, 2.5V, 2.7V, 3.3V and 5.0V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	A to Y, see Figure 2	V_{CC} = 1.65V to 1.95V	Full	0.5	6.4	15.0	ns
			V_{CC} = 2.3V to 2.7V	Full	0.5	3.6	7.5	
			V_{CC} = 2.7V	Full	0.5	3.3	7.5	
			V_{CC} = 3.0V to 3.6V	Full	0.5	3.1	6.5	
			V_{CC} = 4.5V to 5.5V	Full	0.5	2.7	5.0	
Enable Time (3)	t_{EN}	$\overline{OE}$ to Y, see Figure 3	V_{CC} = 1.65V to 1.95V	Full	0.5	6.9	16.5	ns
			V_{CC} = 2.3V to 2.7V	Full	0.5	3.7	8.0	
			V_{CC} = 2.7V	Full	0.1	3.6	8.0	
			V_{CC} = 3.0V to 3.6V	Full	0.1	3	6.5	
			V_{CC} = 4.5V to 5.5V	Full	0.1	2.6	4.5	
Disable Time (4)	t_{DIS}	$\overline{OE}$ to Y, see Figure 3	V_{CC} = 1.65V to 1.95V	Full	0.5	6.4	12.5	ns
			V_{CC} = 2.3V to 2.7V	Full	0.5	3.6	6.5	
			V_{CC} = 2.7V	Full	0.5	4.2	6.5	
			V_{CC} = 3.0V to 3.6V	Full	0.5	4.2	6.5	
			V_{CC} = 4.5V to 5.5V	Full	0.5	3.5	5.0	
Power Dissipation Capacitance (5)	C_{PD}	Per buffer, V_I = GND to V_{CC}	Output enabled	+25℃		18.9		pF
			Output disabled	+25℃		0.5		

NOTES:

1. Specified by design and characterization; not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}.
3. t_{EN} is the same as t_{PZH} and t_{PZL}.
4. t_{DIS} is the same as t_{PLZ} and t_{PHZ}.
5. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC} \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

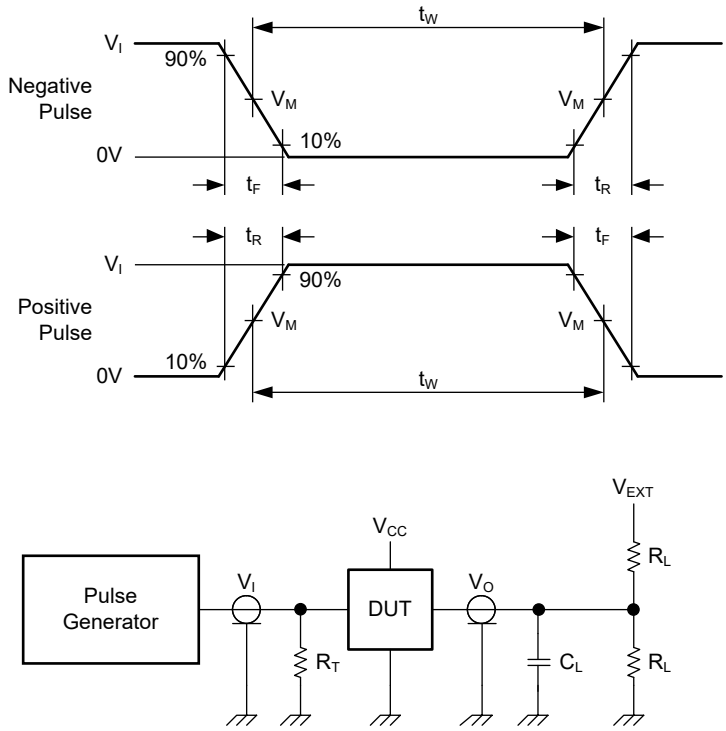
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generator.

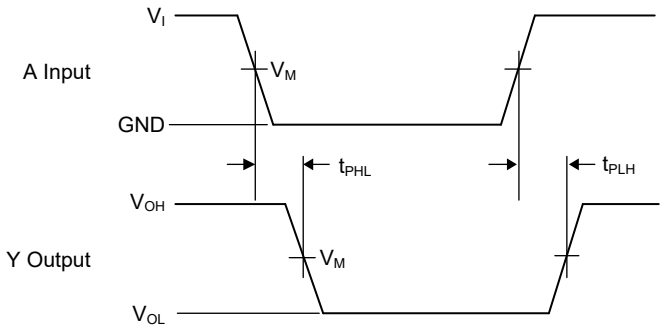
V_{EXT} = External voltage for measuring switching times.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

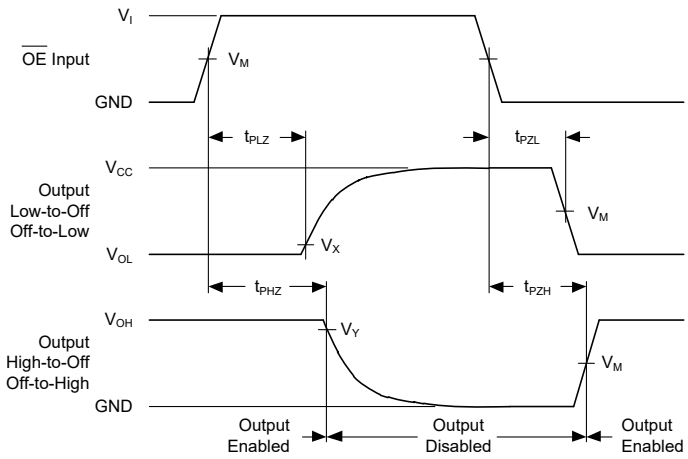
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ	Open	$2V_{CC}$	GND
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω	Open	$2V_{CC}$	GND
2.7V	2.7V	≤ 2.5ns	50pF	500Ω	Open	6V	GND
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	Open	6V	GND
4.5V to 5.5V	V_{CC}	≤ 2.5ns	50pF	500Ω	Open	$2V_{CC}$	GND

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input A to Output Y Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. 3-State Enable and Disable Times

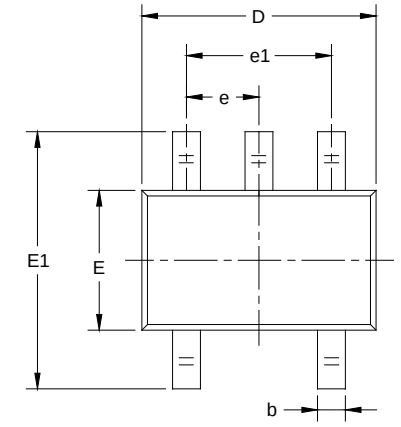
Table 2. Measurement Points

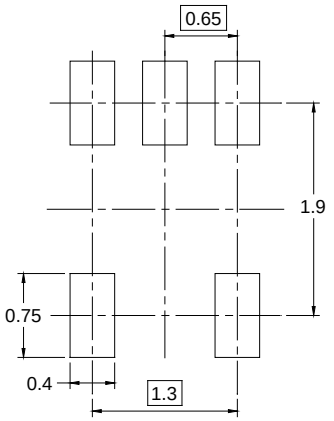
SUPPLY VOLTAGE	INPUT	OUTPUT		
V_{CC}	V_M (1)	V_M	V_X	V_Y
1.65V to 1.95V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15V	V_{OH} - 0.15V
2.3V to 2.7V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15V	V_{OH} - 0.15V
2.7V	1.5V	1.5V	V_{OL} + 0.3V	V_{OH} - 0.3V
3.0V to 3.6V	1.5V	1.5V	V_{OL} + 0.3V	V_{OH} - 0.3V
4.5V to 5.5V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

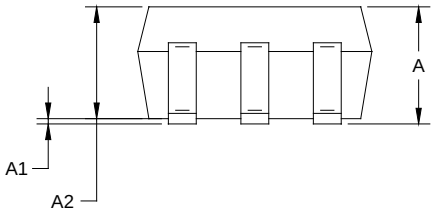
PACKAGE OUTLINE DIMENSIONS

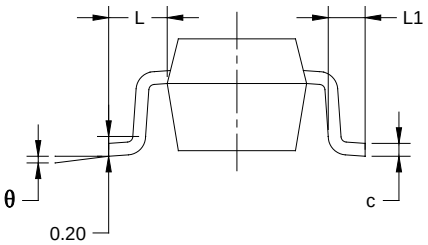
SC70-5





RECOMMENDED LAND PATTERN (Unit: mm)

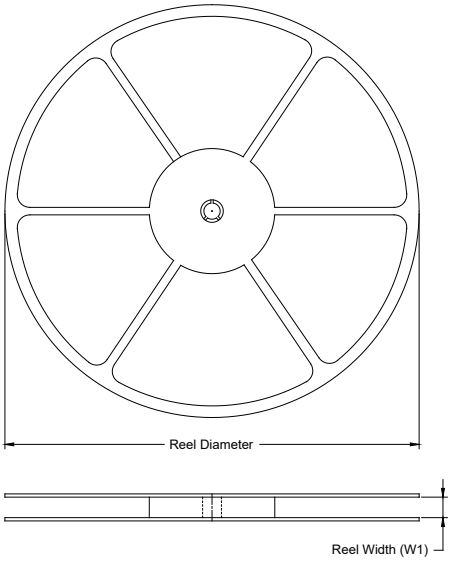




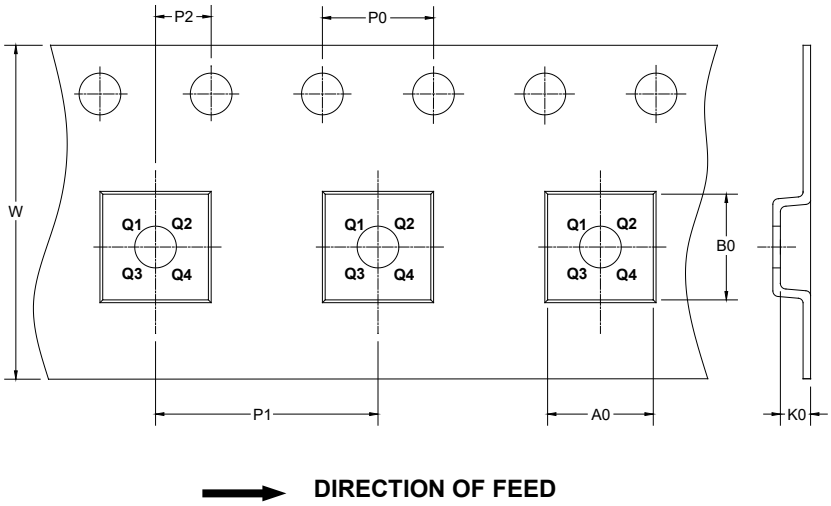
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.220	0.003	0.009
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.65 TYP		0.026 TYP	
e1	1.300 BSC		0.051 BSC	
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



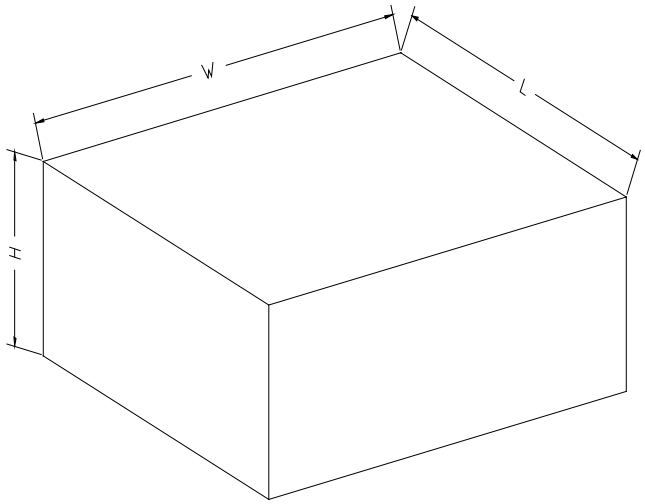
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-5	7″	9.5	2.25	2.55	1.20	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002