# SN74LVC1GU04 Single Inverter Gate

## 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Unbuffered Output
- Maximum $t_{pd}$ of 3.7 ns at 3.3 V
- Low Power Consumption, 10-μA Maximum $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Pro Audio Mixers
- Smoke Detectors
- Solid-State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablets: Enterprise
- Audio Docks: Portable
- DLP Front Projection Systems
- DVR and DVS
- Digital Picture Frame (DPF)
- Digital Still Cameras

## 3 Description

This single inverter gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC1GU04 device contains one inverter with an unbuffered output and performs the Boolean function $Y = \overline{A}$.

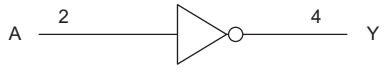
NanoFree package technology is a major breakthrough in device packaging concepts, using the die as the package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC1GU04DBV | SOT-23 (5) | 2.90 mm × 1.60 mm |
| SN74LVC1GU04DCK | SC70 (5) | 2.00 mm × 1.25 mm |
| SN74LVC1GU04DRL | SOT-5X3 (5) | 1.60 mm × 1.20 mm |
| SN74LVC1GU04DRY | SON (6) | 1.45 mm × 1.00 mm |
| SN74LVC1GU04DSF | SON (6) | 1.00 mm × 1.00 mm |
| SN74LVC1GU04YZP | DSBGA (5) | 1.44 mm × 0.94 mm |
| SN74LVC1GU04YZV | DSBGA (4) | 0.91 mm × 0.91 mm |
| SN74LVC1GU04DPW | X2SON (5) | 0.80 mm × 0.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision X (November 2017) to Revision Y** **Page**

- Updated input voltage minimum from 0.5 V to –0.5 V in Absolute Maximum Ratings table. ... 5

**Changes from Revision W (January 2016) to Revision X** **Page**

- Changed values in the Thermal Information table to align with JEDEC standards. ... 6
- Updated Feature Description to include more detailed information about specific device features. ... 9
- Changed Typical Application to oscillator circuit. ... 11
- Added DPW layout example ... 13

**Changes from Revision V (November 2013) to Revision W** **Page**

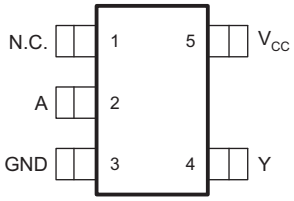
- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

**Changes from Revision U (June 2011) to Revision V** **Page**

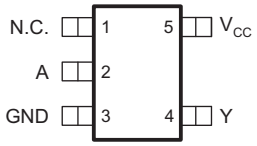
- Updated document to new TI data sheet format. ... 1
- Updated operating free-air temperature range in Recommended Operating Conditions table. ... 5

# 5 Pin Configuration and Functions

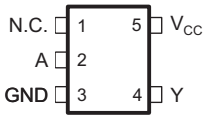
**DBV Package**
**5-Pin SOT-23**
**Top View**



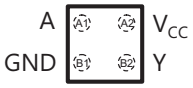

**DCK Package**
**5-Pin SC70**
**Top View**



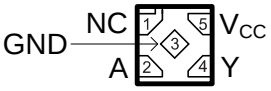

**DRL Package**
**5-Pin SOT**
**Top View**




**YZV Package**
**4-Pin DSBGA**
**Top View**




**DPW Package**
**5-Pin SON**
**Top View**

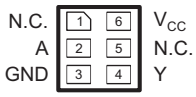



**Pin Functions**[1][2]

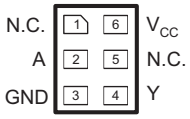
| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DBV, DRL, DCK, DPW | YZV | | |
| A | 2 | A1 | I | Input |
| GND | 3 | B1 | — | Ground |
| NC | 1 | – | — | Not connected |
| $V_{CC}$ | 5 | A2 | — | Positive Supply |
| Y | 4 | B2 | O | Output |

(1) NC – No internal connection
(2) See *Mechanical, Packaging, and Orderable Information* for dimensions

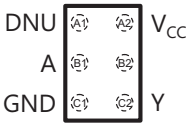
**DSF Package**
**6-Pin SON**
**Top View**




**DRY Package**
**6-Pin SON**
**Top View**




**YZP Package**
**6-Pin DSBGA**
**Top View**




DNU – Do not use

## Pin Functions (1) (2)

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DSF, DRY | YZP | | |
| A | 2 | B1 | I | Input |
| GND | 3 | C1 | — | Ground |
| NC | 1, 5 | A1, B2 | — | Not connected |
| $V_{CC}$ | 6 | A2 | — | Positive Supply |
| Y | 4 | C2 | O | Output |

(1) NC – No internal connection
(2) See *Mechanical, Packaging, and Orderable Information* for dimensions

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Maximum junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in *Recommended Operating Conditions* .

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 | ±1000 | |

## 6.3 Recommended Operating Conditions

See (1).

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $I_O$ = –100 μA | 0.75 × $V_{CC}$ | | V |
| $V_{IL}$ | Low-level input voltage | $I_O$ = 100 μA | | 0.25 × $V_{CC}$ | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –16 | |
| | | | | –24 | |
| | | $V_{CC}$ = 4.5 V | | –32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. For more information, see the *Implications of Slow or Floating CMOS Inputs* application report.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74LVC1GU04 | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | DRL (SOT-5X3) | DRY (SON) | DSF (SON) | DPW (X2SON) | YZV (DSBGA) | YZP (DSBGA) | |
| | | 5 PINS | 5 PINS | 5 PINS | 5 PINS | 5 PINS | 5 PINS | 4 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 231.5 | 276.1 | 296.2 | 369.6 | 410.3 | 511 | 168.2 | 144.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 139.4 | 178.9 | 137.3 | 257.6 | 208.4 | 241.9 | 2.1 | 1.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 71.1 | 70.9 | 145.3 | 230.8 | 262.6 | 374.2 | 55.9 | 39.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 45.2 | 47 | 14.7 | 77.2 | 36 | 45 | 1.1 | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 70.7 | 69.3 | 145.9 | 231 | 262.3 | 373.3 | 56.3 | 39.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | 168.0 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range, $T_A$ = –40°C to +125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{IL}$ = 0 V, $I_{OH}$ = –100 µA, $V_{CC}$ = 1.65 V to 5.5 V | $V_{CC}$ – 0.1 | | | V |
| | | $V_{IL}$ = 0 V, $I_{OH}$ = –4 mA, $V_{CC}$ = 1.65 V | 1.2 | | | |
| | | $V_{IL}$ = 0 V, $I_{OH}$ = –8 mA, $V_{CC}$ = 2.3 V | 1.9 | | | |
| | | $V_{IL}$ = 0 V, $I_{OH}$ = –16 mA, $V_{CC}$ = 3 V | 2.4 | | | |
| | | $V_{IL}$ = 0 V, $I_{OH}$ = –24 mA, $V_{CC}$ = 3 V | 2.3 | | | |
| | | $V_{IL}$ = 0 V, $I_{OH}$ = –32 mA, $V_{CC}$ = 4.5 V | 3.8 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IH}$ = $V_{CC}$, $I_{OL}$ = 100 µA, $V_{CC}$ = 1.65 V to 5.5 V | | | 0.1 | V |
| | | $V_{IH}$ = $V_{CC}$, $I_{OL}$ = 4 mA, $V_{CC}$ = 1.65 V | | | 0.45 | |
| | | $V_{IH}$ = $V_{CC}$, $I_{OL}$ = 8 mA, $V_{CC}$ = 2.3 V | | | 0.3 | |
| | | $V_{IH}$ = $V_{CC}$, $I_{OL}$ = 16 mA, $V_{CC}$ = 3 V | | | 0.4 | |
| | | $V_{IH}$ = $V_{CC}$, $I_{OL}$ = 24 mA, $V_{CC}$ = 3 V | | | 0.55 | |
| | | $V_{IH}$ = $V_{CC}$, $I_{OL}$ = 32 mA, $V_{CC}$ = 4.5 V | | | 0.55 | |
| $I_I$ | Input leakage current | A Input: $V_I$ = 5.5 V or GND, $V_{CC}$ = 0 V to 5.5 V | | | ±5 | µA |
| $I_{CC}$ | Supply current | $V_I$ = 5.5 V or GND, $I_O$ = 0, $V_{CC}$ = 1.65 V to 5.5 V | | | 10 | µA |
| $C_I$ | Input capacitance | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 3.3 V, $T_A$ = –40°C to 85°C | | 7 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 6.6 Switching Characteristics: $T_A$ = –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (See Figure 2)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay | A-to-Y | $V_{CC}$ = 1.8 V ± 0.15 V | 1.3 | 5 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 4 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.1 | 3.7 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3 | |

## 6.7 Switching Characteristics: $T_A$ = –40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (See Figure 2)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay | A-to-Y | $V_{CC}$ = 1.8 V ± 0.15 V | 1.3 | 5.5 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 4.5 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.1 | 4.2 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.5 | |

## 6.8 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | $V_{CC}$ = 1.8 V | 9 | pF |
| | | | $V_{CC}$ = 2.5 V | 11 | |
| | | | $V_{CC}$ = 3.3 V | 13 | |
| | | | $V_{CC}$ = 5 V | 27 | |

## 6.9 Typical Characteristic

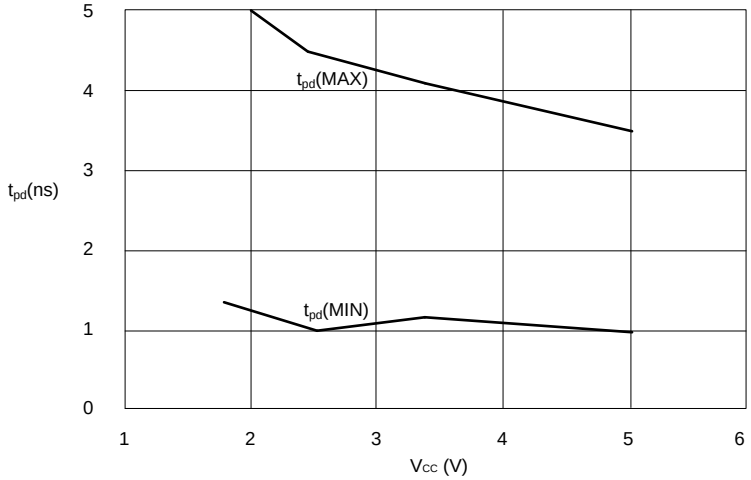
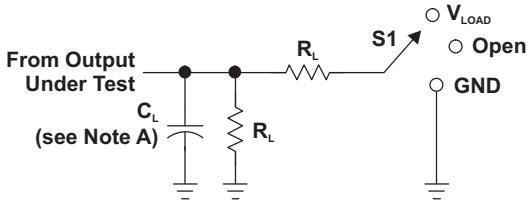



**Figure 1. $t_{pd}$ vs $V_{CC}$**

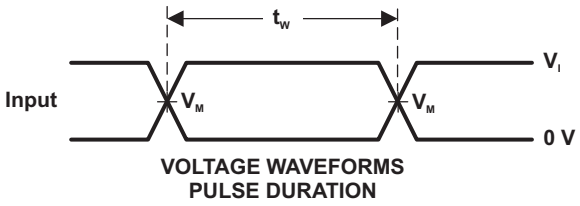
# 7 Parameter Measurement Information



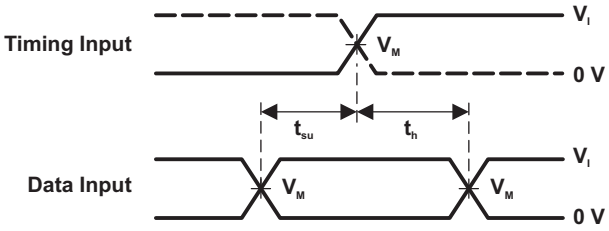

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

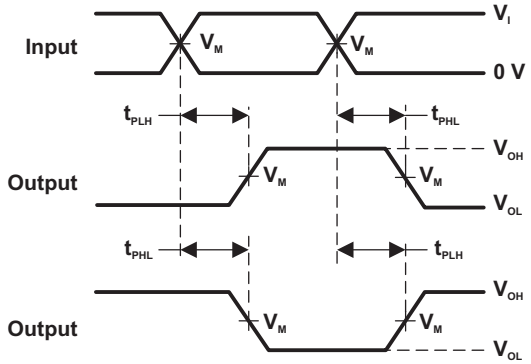
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



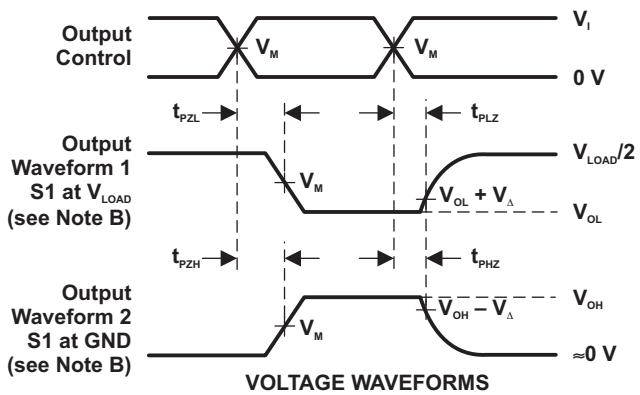

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SN74LVC1GU04 device contains one inverter with an unbuffered output with a maximum sink current of 32 mA.

## 8.2 Functional Block Diagram

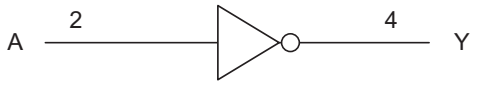



**Figure 3. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

### 8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high-drive capability of this device creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst-case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

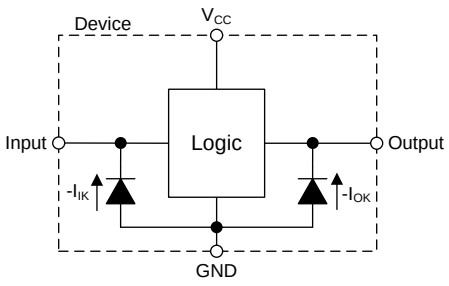
Signals that are applied to the inputs need to have fast edge rates, as shown by $\Delta t/\Delta v$ in the *Recommended Operating Conditions*, to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

### 8.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in Figure 4.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



## Feature Description (continued)

### 8.3.4 Partial Power Down ($I_{off}$)

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off}$ in the *Electrical Characteristics*.

### 8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

### 8.3.6 Unbuffered Logic

A standard CMOS logic function typically consists of at least three stages: the input inverter, the logic function, and the output inverter. Some devices have multiple stages at the input or output for various reasons. An unbuffered CMOS logic function eliminates the extra input and output stages; the device only contains the required logic function which is directly driven from the inputs and directly drives the outputs.

The unbuffered inverter is commonly used in oscillator circuits because it is less sensitive to parameter changes in the oscillator circuit due to having lower total gain than a buffered equivalent. To learn more about how to use an unbuffered inverter in an oscillator circuit, see *Use of the CMOS Unbuffered Inverter in Oscillator Circuits*.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1GU04.

**Table 1. Function Table**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The unbuffered inverter is commonly used in oscillator circuits because it is less sensitive to parameter changes in the oscillator circuit due to having lower total gain than a buffered equivalent. An example application circuit is shown in Figure 5. To learn more about how to use an unbuffered inverter in an oscillator circuit, refer to the *Use of the CMOS Unbuffered Inverter in Oscillator Circuits* application report.

## 9.2 Typical Application

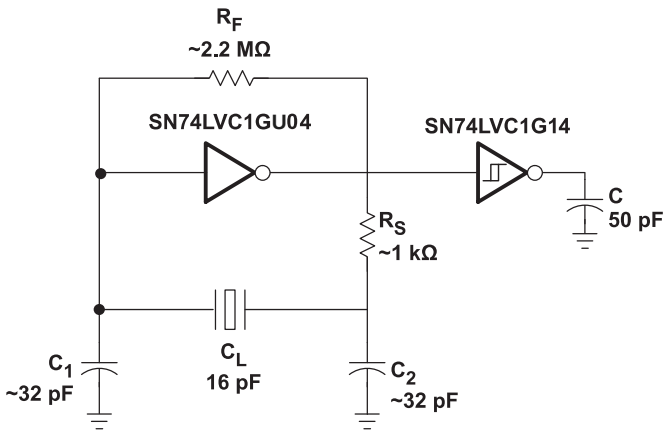





**Figure 5. Typical Application Diagram**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

To learn more about how to use an unbuffered inverter in an oscillator circuit, refer to the *Use of the CMOS Unbuffered Inverter in Oscillator Circuits* application report.

1. Recommended Input Conditions
   - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as ($V_I$ max) in *Recommended Operating Conditions* at any valid $V_{CC}$.
2. Absolute Maximum Output Conditions
   - Load currents must not exceed ($I_O$ max) per output and must not exceed (Continuous current through $V_{CC}$ or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
   - Outputs must not be pulled above the voltage rated in the *Absolute Maximum Ratings*.

## Typical Application (continued)

### 9.2.3 Application Curve

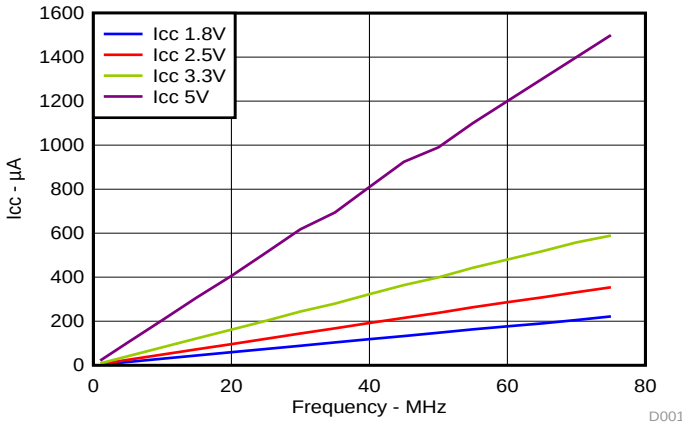



**Figure 6. $I_{CC}$ vs Frequency**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

The $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

# 11 Layout

## 11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 7 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 8 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

## 11.2 Layout Example

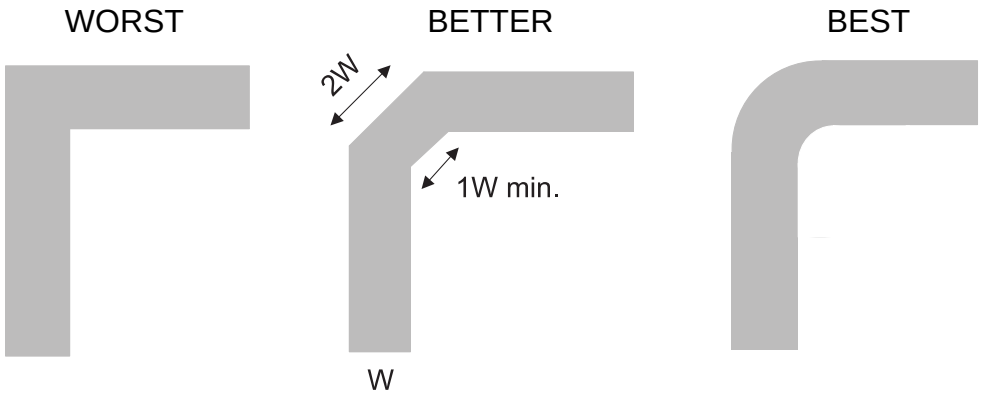



**Figure 7. Trace Example**

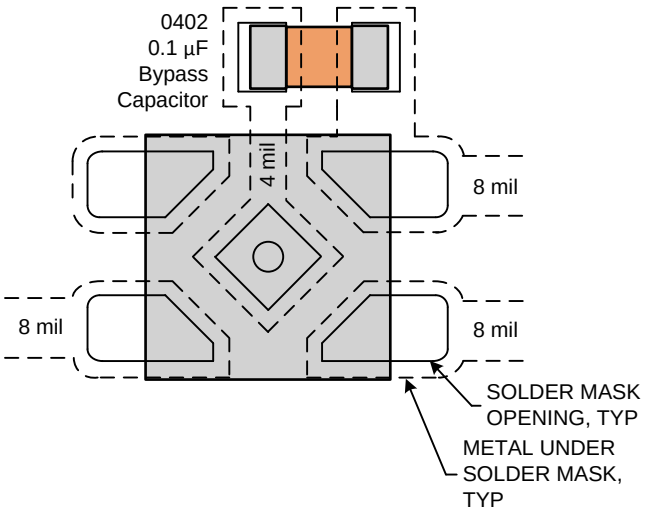



**Figure 8. Example Layout With DPW (X2SON-5) Package**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

## 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

# PACKAGE OPTION ADDENDUM

10-Dec-2020

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74LVC1GU04DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CU4F | Samples |
| 74LVC1GU04DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CU4F | Samples |
| 74LVC1GU04DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CU4F | Samples |
| 74LVC1GU04DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CD5<br>CDS | Samples |
| 74LVC1GU04DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CD5<br>CDS | Samples |
| 74LVC1GU04DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CD5<br>CDS | Samples |
| 74LVC1GU04DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CD5<br>CDS | Samples |
| 74LVC1GU04DRLRG4 | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CDR | Samples |
| SN74LVC1GU04DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (CU45, CU4F, CU4J, CU4R, CU4T)<br>(CU4H, CU4P, CU4S) | Samples |
| SN74LVC1GU04DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (CU45, CU4F, CU4J, CU4R)<br>(CU4H, CU4P, CU4S) | Samples |
| SN74LVC1GU04DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (CD5, CDF, CDJ, CDK, CDR, CDT)<br>(CDH, CDP, CDS) | Samples |
| SN74LVC1GU04DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (CD5, CDF, CDJ, CDK, CDR, CDT)<br>(CDH, CDP, CDS) | Samples |
| SN74LVC1GU04DPWR | ACTIVE | X2SON | DPW | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CM | Samples |
| SN74LVC1GU04DRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CDR | Samples |
| SN74LVC1GU04DRY2 | ACTIVE | SON | DRY | 6 | 5000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CD | Samples |

# PACKAGE OPTION ADDENDUM

10-Dec-2020

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1GU04DRYR | ACTIVE | SON | DRY | 6 | 5000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CD | Samples |
| SN74LVC1GU04DSFR | ACTIVE | SON | DSF | 6 | 5000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CD | Samples |
| SN74LVC1GU04YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CDN | Samples |
| SN74LVC1GU04YZVR | ACTIVE | DSBGA | YZV | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CD (7, N) | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

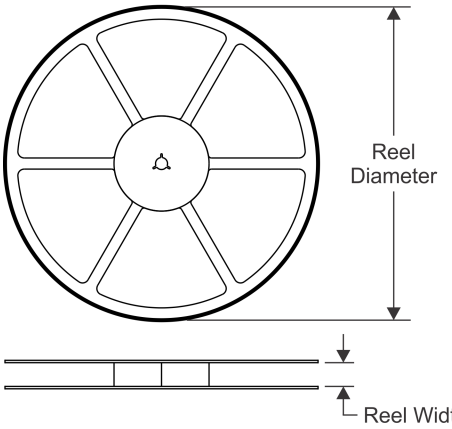
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

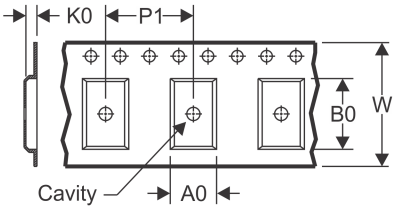
24-Jul-2020

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

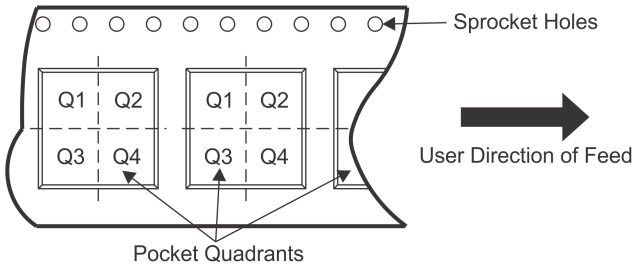



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

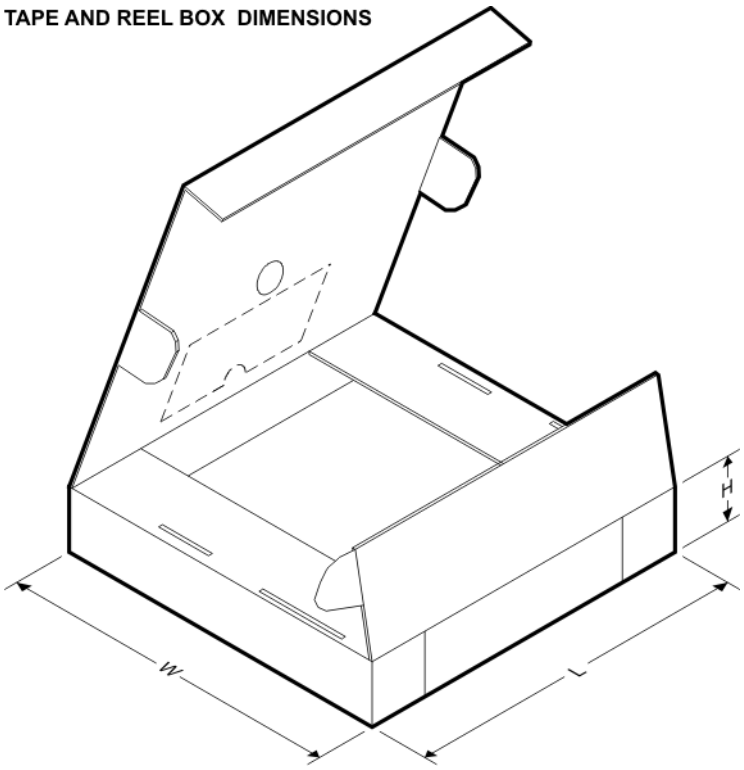
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74LVC1GU04DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| 74LVC1GU04DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| 74LVC1GU04DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| 74LVC1GU04DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |

# PACKAGE MATERIALS INFORMATION

24-Jul-2020

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1GU04DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DRY2 | SON | DRY | 6 | 5000 | 180.0 | 8.4 | 1.65 | 1.2 | 0.7 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DRY2 | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.6 | 1.15 | 0.75 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1GU04DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1GU04YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |
| SN74LVC1GU04YZVR | DSBGA | YZV | 4 | 3000 | 178.0 | 9.2 | 1.0 | 1.0 | 0.63 | 4.0 | 8.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74LVC1GU04DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| 74LVC1GU04DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| 74LVC1GU04DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| 74LVC1GU04DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |

# PACKAGE MATERIALS INFORMATION

24-Jul-2020

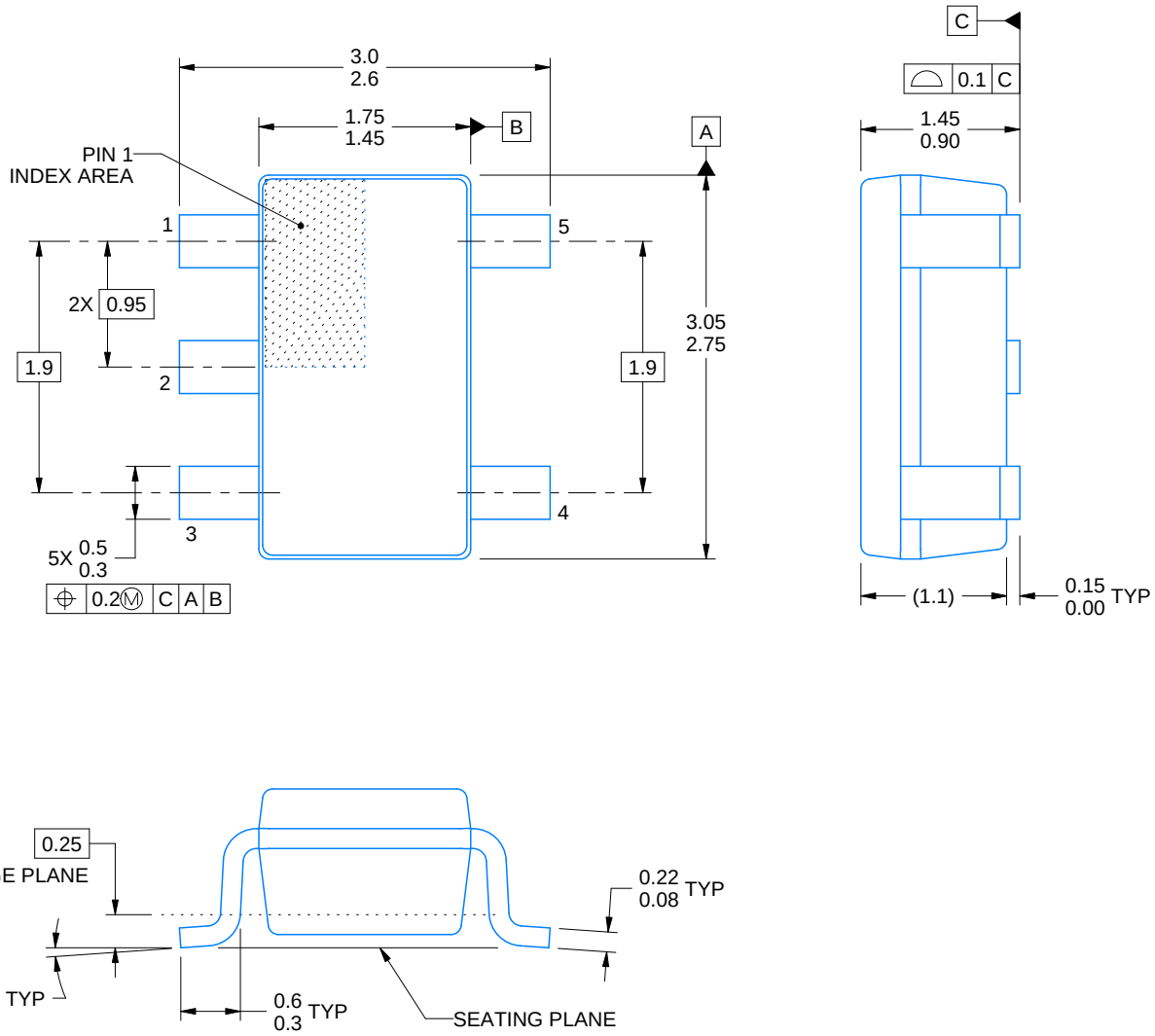
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1GU04DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DRY2 | SON | DRY | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DRY2 | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1GU04DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1GU04DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1GU04YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74LVC1GU04YZVR | DSBGA | YZV | 4 | 3000 | 220.0 | 220.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR




4214839/F 06/2021

NOTES:

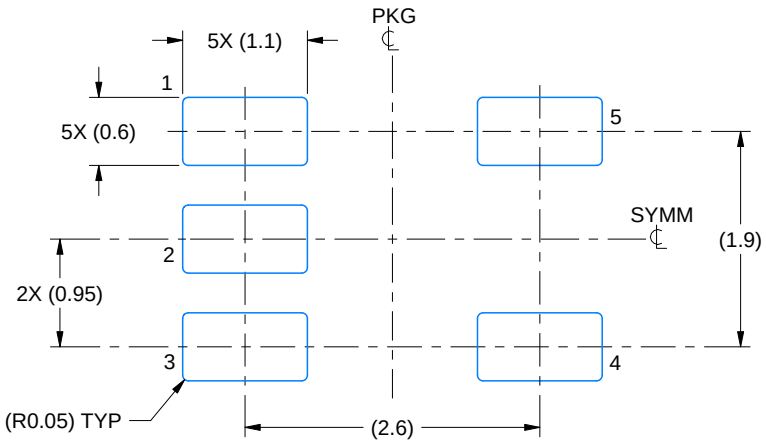
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

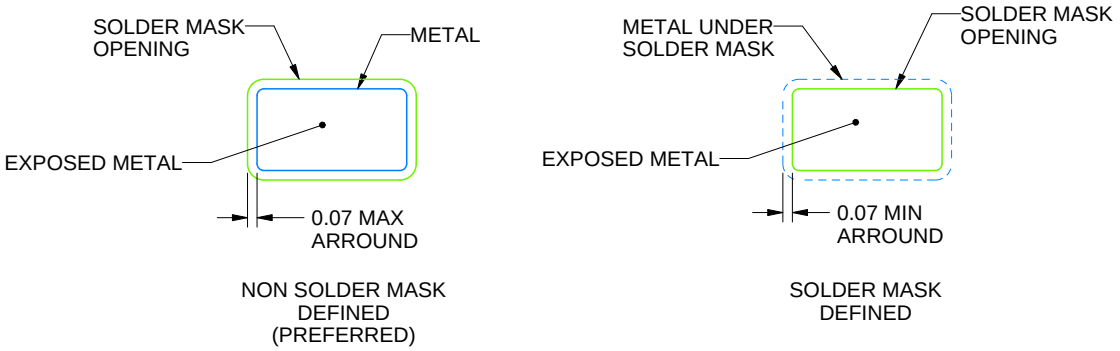
## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

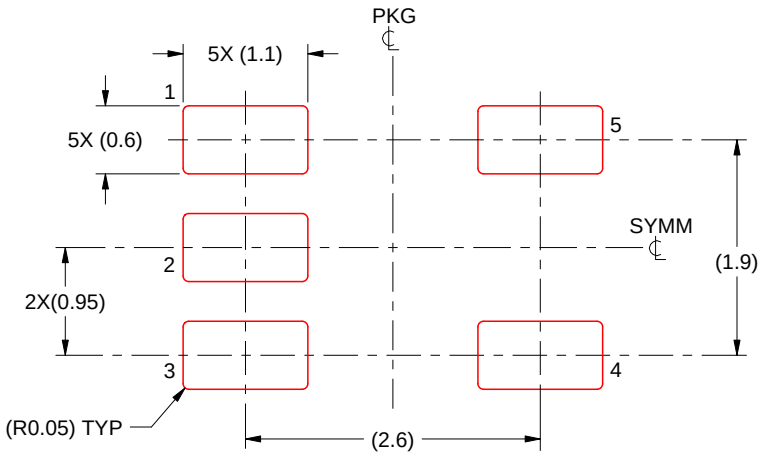
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



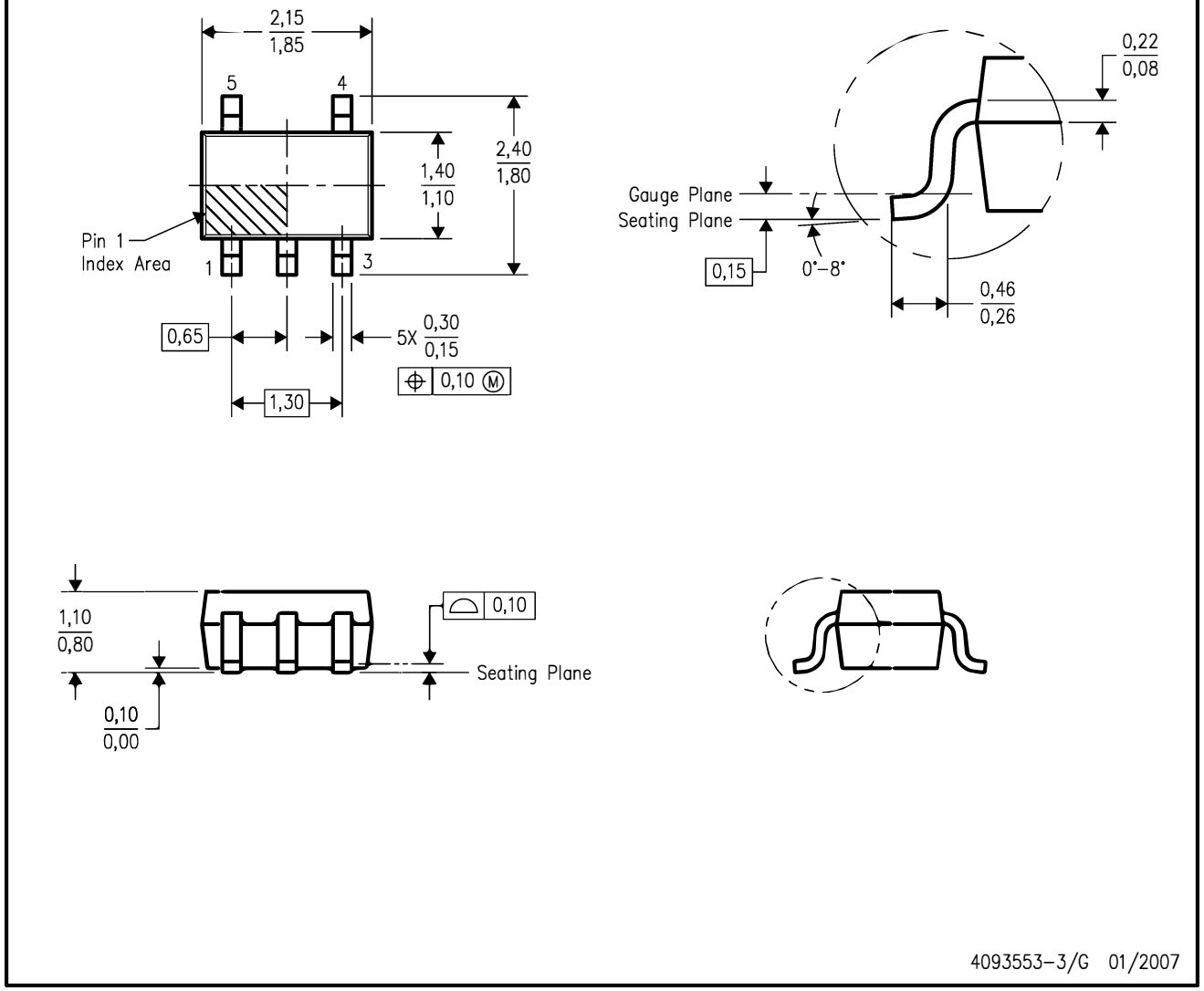

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

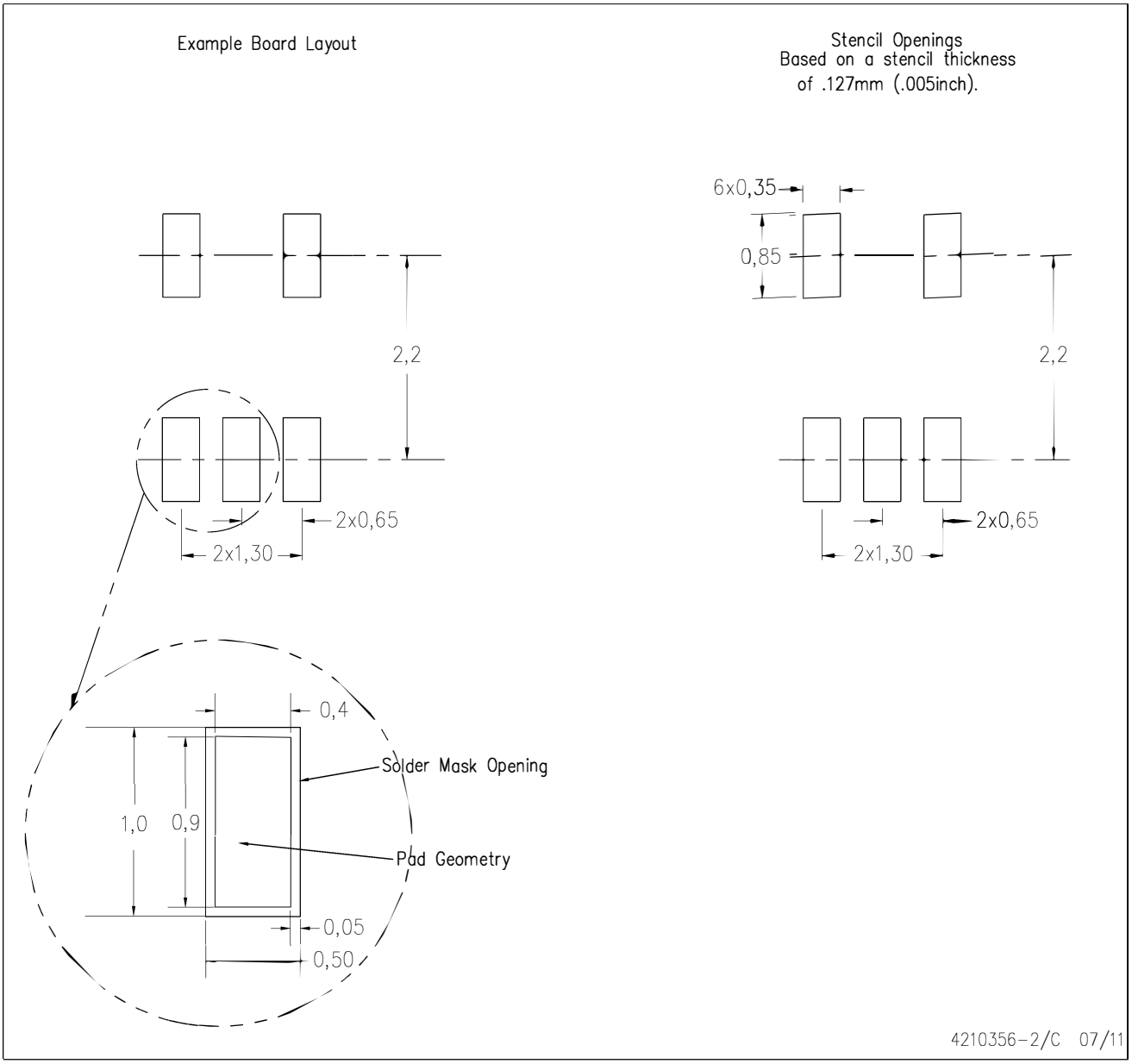
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



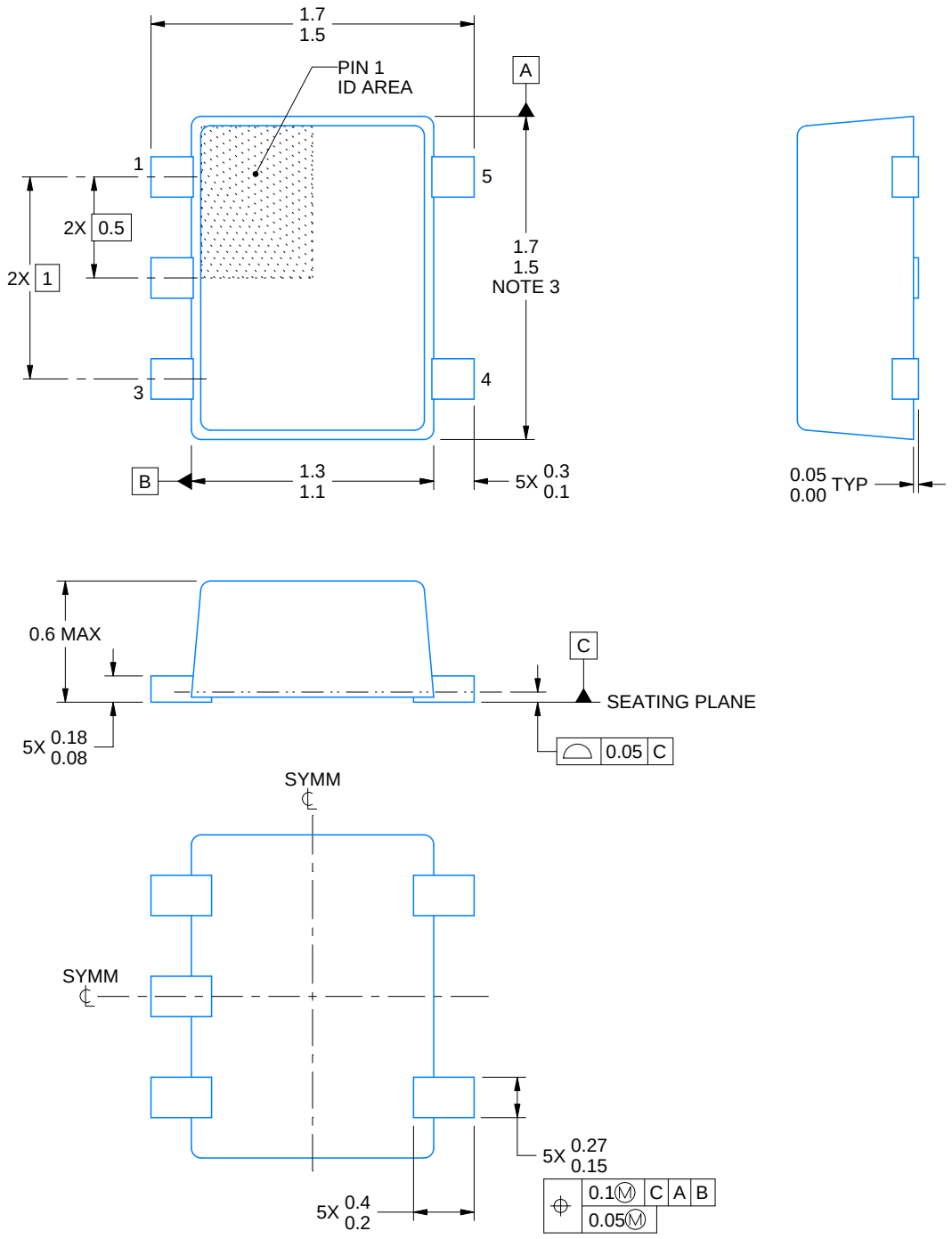

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

# PACKAGE OUTLINE

## DRL0005A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




4220753/B 12/2020

NOTES:

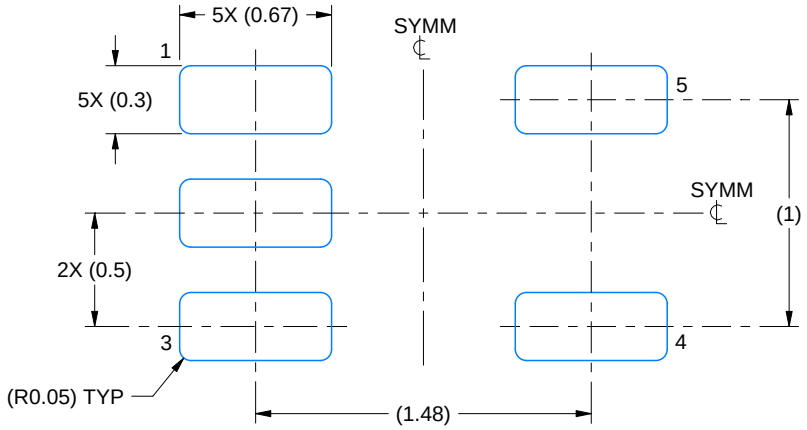
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

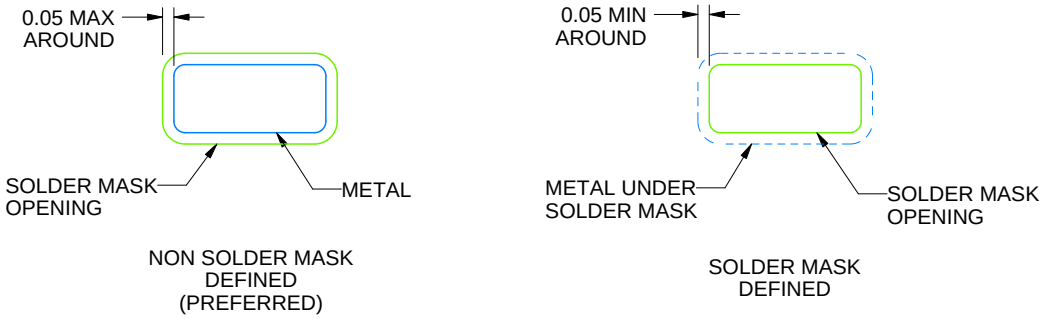
## DRL0005A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
SCALE:30X




SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

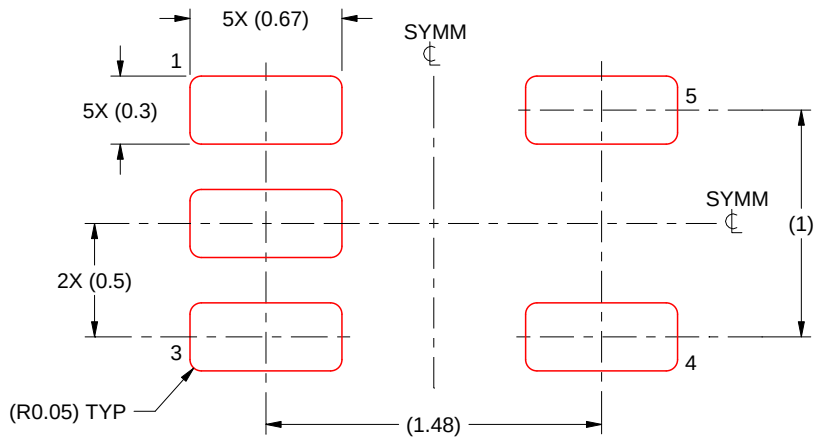
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DRL0005A

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

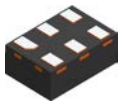
# DRY 6

# USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

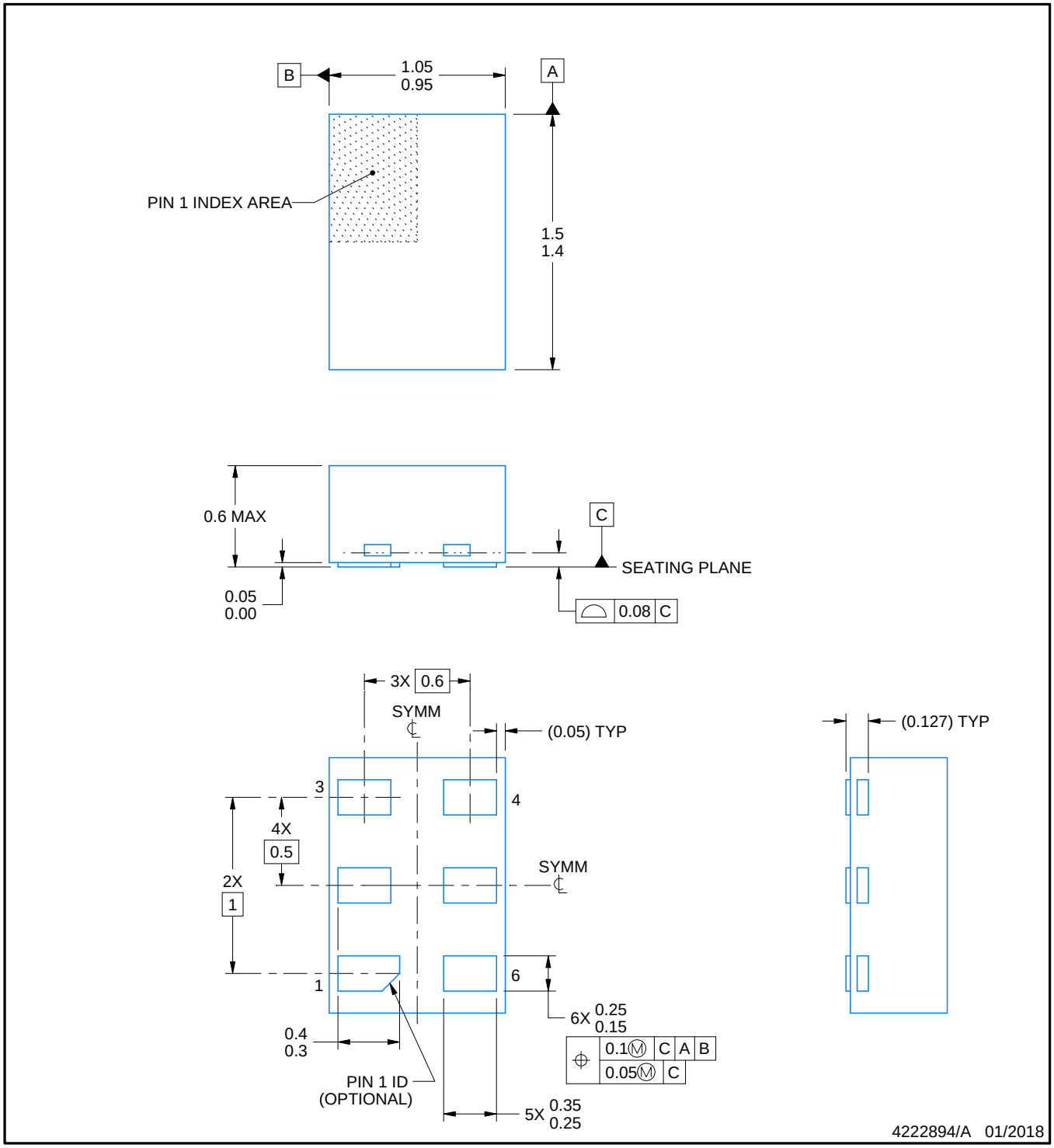
# DRY0006A



# PACKAGE OUTLINE

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

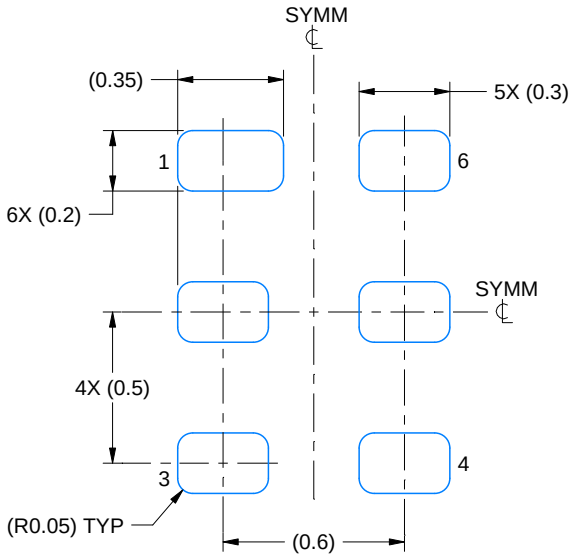
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

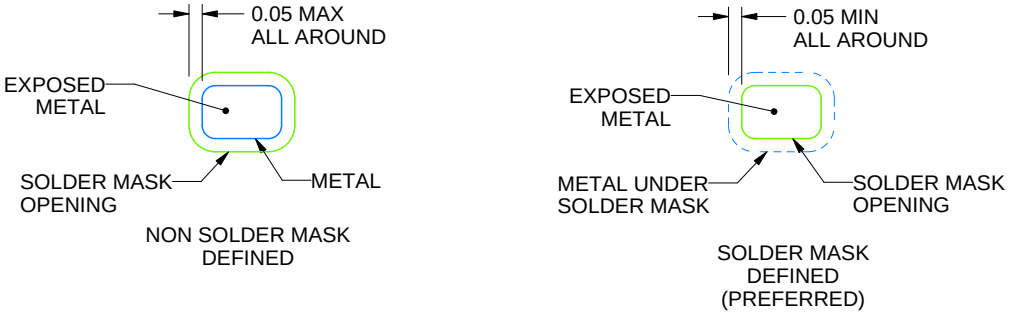
## DRY0006A

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

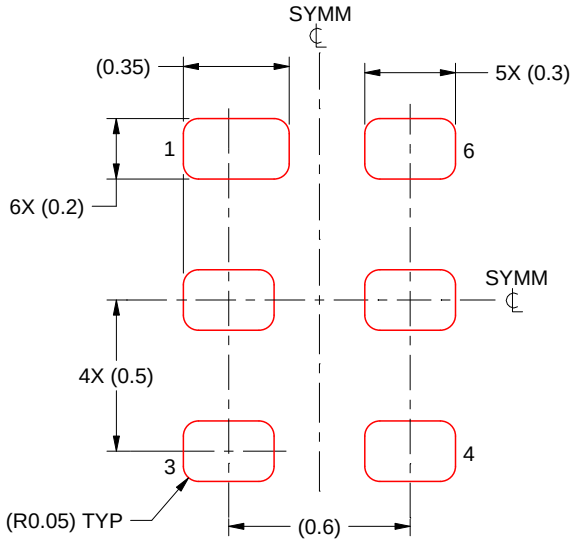
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DRY0006A

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

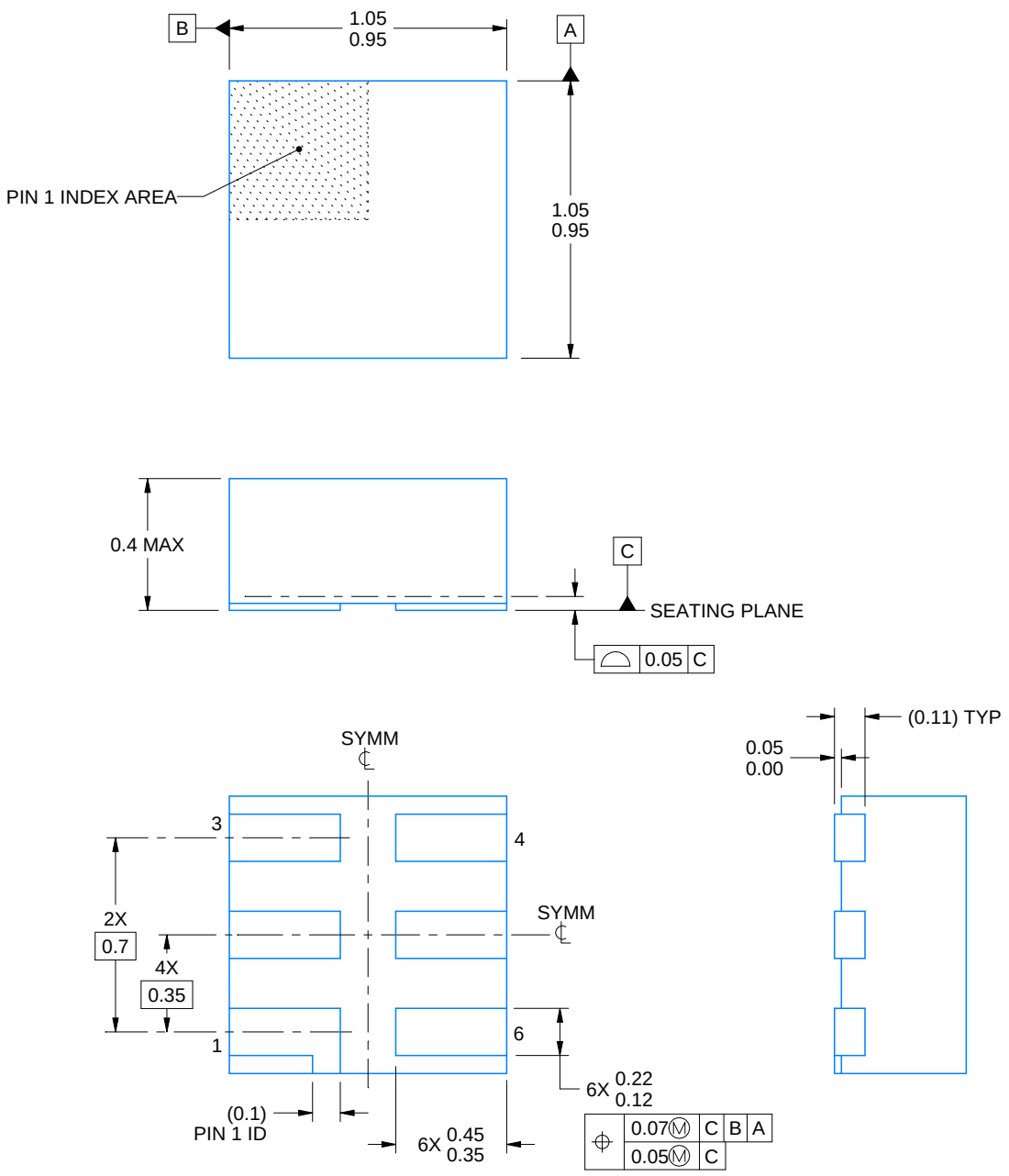
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




4220597/A 06/2017

NOTES:

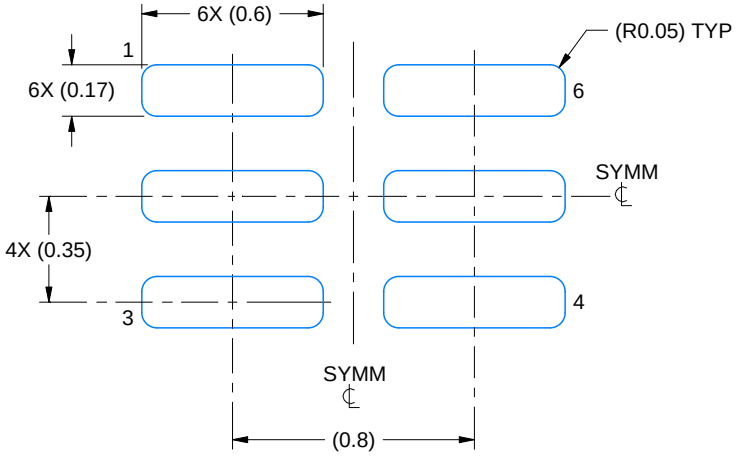
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

# EXAMPLE BOARD LAYOUT

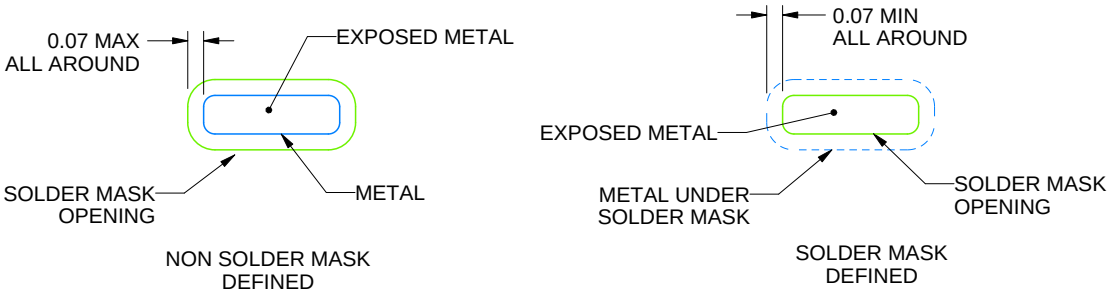
## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

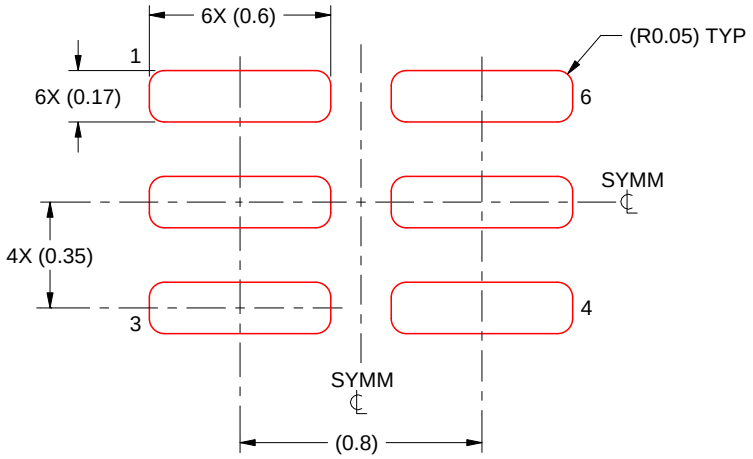
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# GENERIC PACKAGE VIEW

## DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

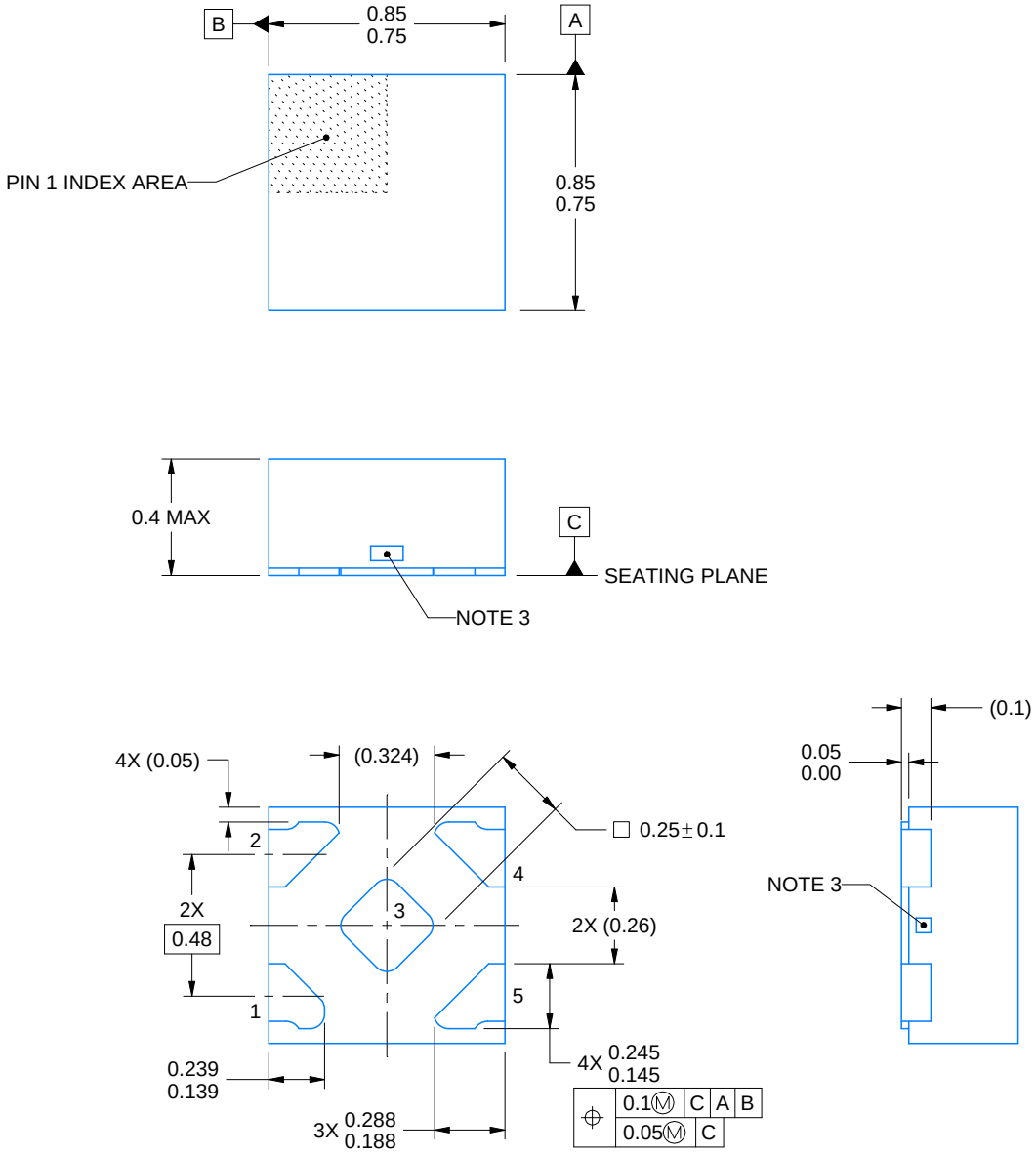

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DPW0005A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




4223102/C 06/2021

NOTES:

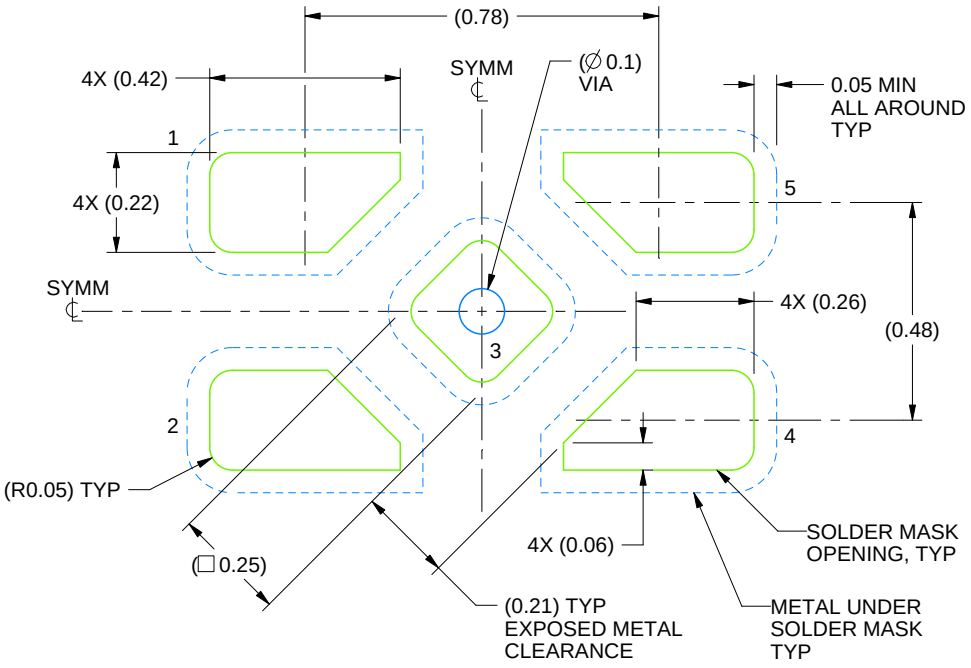
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

# EXAMPLE BOARD LAYOUT

## DPW0005A

### X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/C 06/2021

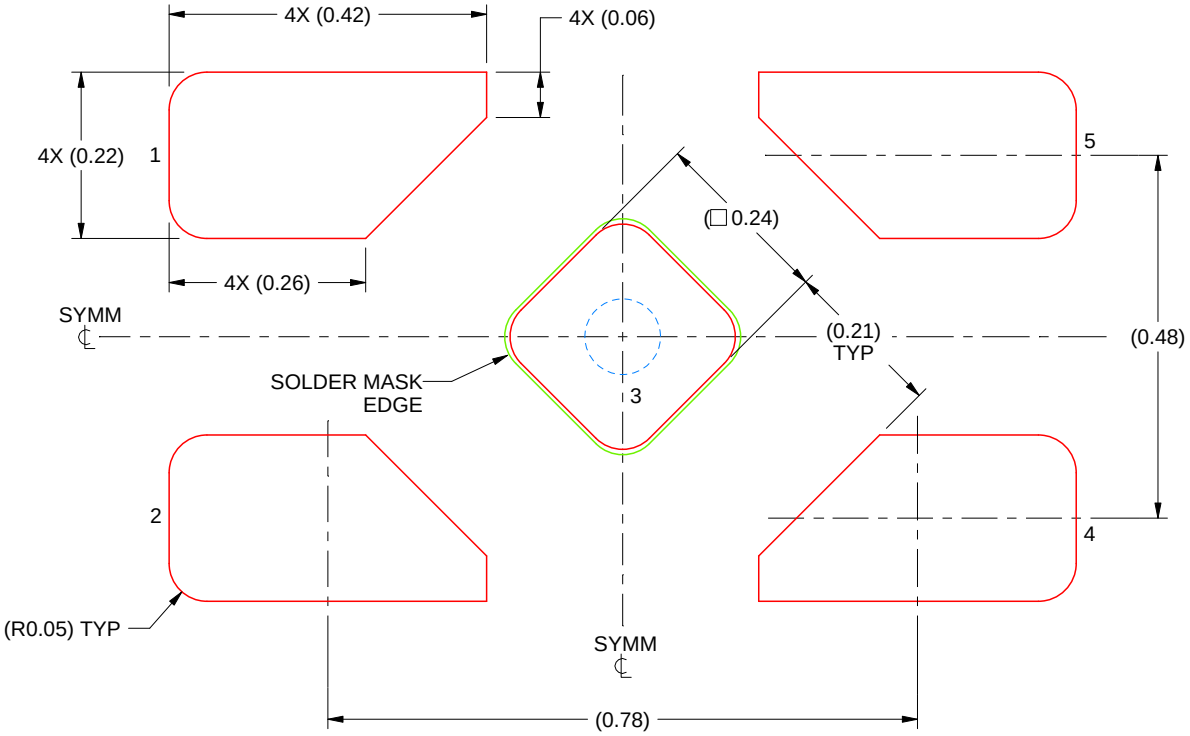
NOTES: (continued)

# EXAMPLE STENCIL DESIGN

## DPW0005A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/C 06/2021

NOTES: (continued)

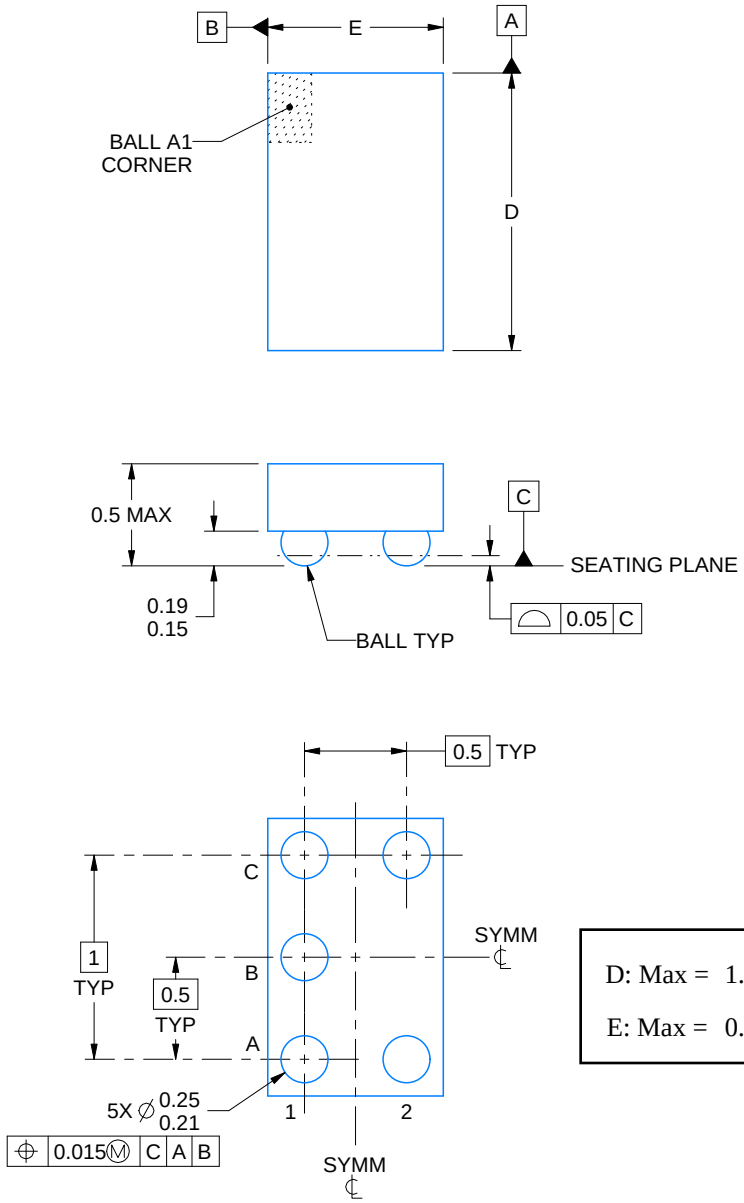
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## YZP0005

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




D: Max = 1.44 mm, Min = 1.38 mm

E: Max = 0.94 mm, Min = 0.88 mm

4219492/A 05/2017

NOTES:

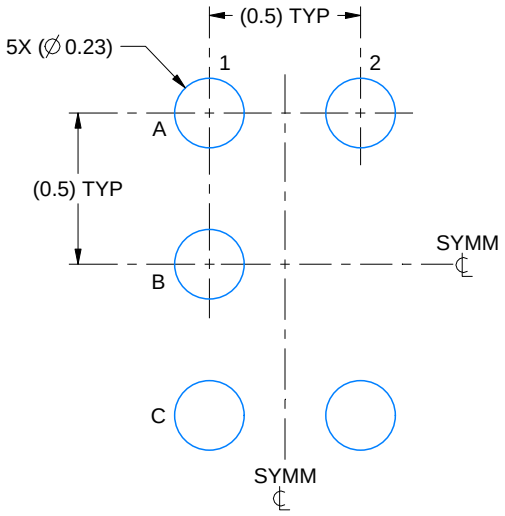
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

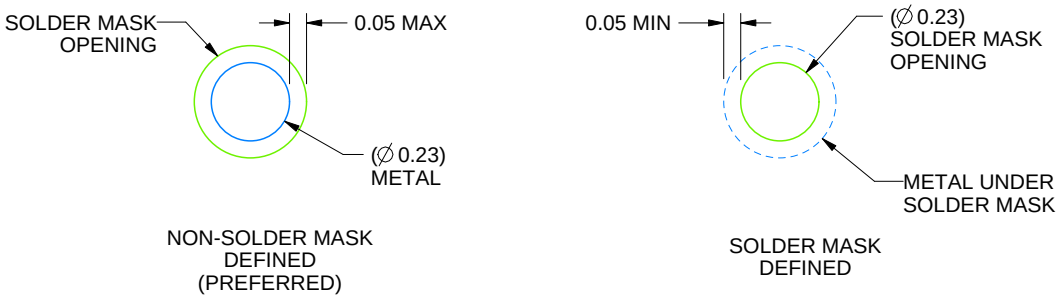
## YZP0005

### DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




LAND PATTERN EXAMPLE
SCALE:40X




SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

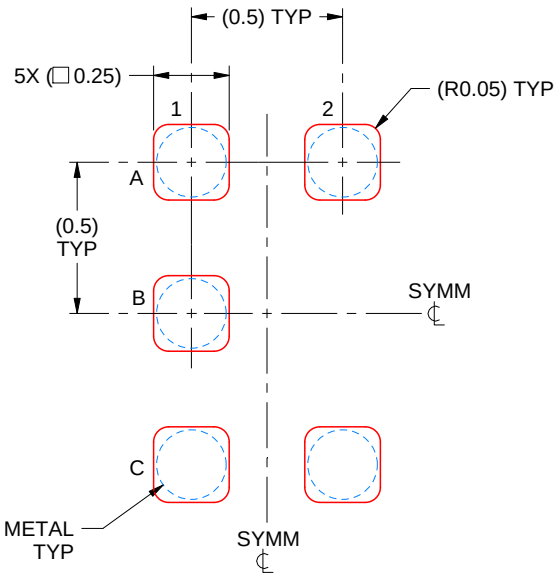
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

# EXAMPLE STENCIL DESIGN

## YZP0005

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



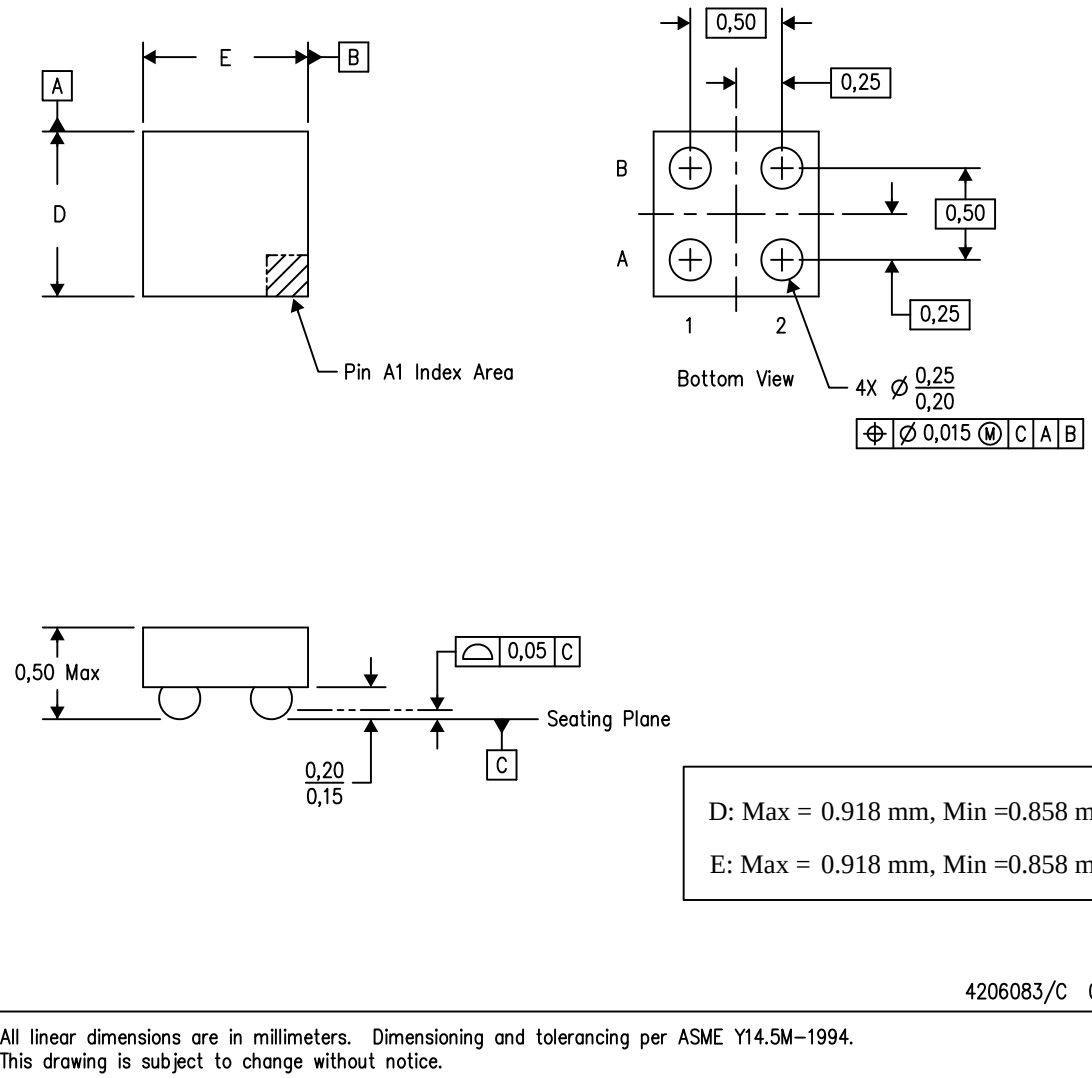

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.