74AHC123
Dual Retriggerable Monostable Multivibrator with Reset

GENERAL DESCRIPTION

The 74AHC123 is a high-speed silicon-gate CMOS device. The device is a dual retriggerable monostable multivibrator designed for 2.0V to 5.5V V_{CC} operation.

The 74AHC123 edge-triggered multivibrator features with output pulse width control by three methods. In the first method, the $n\overline{A}$ input is low, and the nB input goes high. In the second method, the nB input is high, and the $n\overline{A}$ input goes low. In the third method, the $n\overline{A}$ input is low, the nB input is high, and the $n\overline{R}D$ input goes high.

Once triggered, the basic output pulse width may be extended by retriggering the gated active low-going edge ($n\overline{A}$) input or the active high-going edge (nB) input. By repeating this process, the output pulse period (nQ = high, $n\overline{Q}$ = low) can be made as long as desired. Alternatively an output delay can be terminated at any time by a low-going edge on $n\overline{R}D$ input, which also inhibits the triggering.

An internal connection from $n\overline{R}D$ to the input gate makes it possible to trigger the circuit by a high-going signal at $n\overline{R}D$ input as shown in function table. Figure 3 and Figure 4 illustrate pulse control by retriggering and early reset.

The output pulse duration is programmed by selecting external resistance (R_{EXT}) and capacitance (C_{EXT}) values.

When $C_{EXT} \geq 10nF$, the typical output pulse width is defined as: $t_W = R_{EXT} \times C_{EXT}$ where t_W = pulse width in ns; R_{EXT} = external resistor in kΩ; C_{EXT} = external capacitor in pF. Schmitt-trigger action at all inputs makes the circuit highly tolerant to slower input rise and fall times.

FEATURES

- **All Inputs Have a Schmitt-Trigger Action**
- **Inputs Accept Voltages Higher than V_{CC}**
- **Edge-Triggered from Active High or Active Low Gated Logic Inputs**
- **Retriggerable for Very Long Pulses up to 100% Duty Factor**
- **Direct Reset Terminates Output Pulse**
- **Operates with CMOS Input Levels**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOIC-16 Package**

FUNCTION TABLE

INPUT			OUTPUT	
$n\overline{R}D$	**$n\overline{A}$**	**nB**	**nQ**	**$n\overline{Q}$**
L	*X*	*X*	L	H
X	H	*X*	L*	H*
X	*X*	L	L*	H*
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = High Voltage Level

L = Low Voltage Level

↑ = Low-to-High Transition

↓ = High-to-Low Transition

⎍ = One High Level Output Pulse

⎎ = One Low Level Output Pulse

X = Don't Care

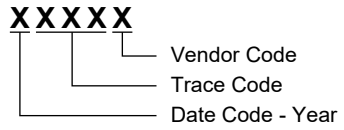
* If the monostable multivibrator was triggered before this condition was established, the pulse will continue as programmed.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AHC123	SOIC-16	-40℃ to +125℃	74AHC123XS16G/TR	74AHC123XS16 XXXXX	Tape and Reel, 2500

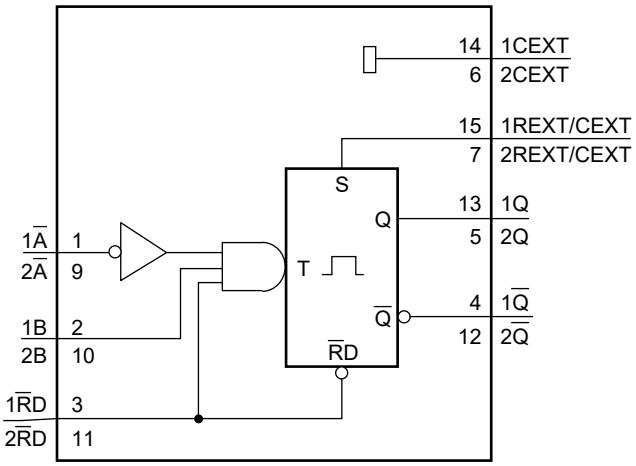
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

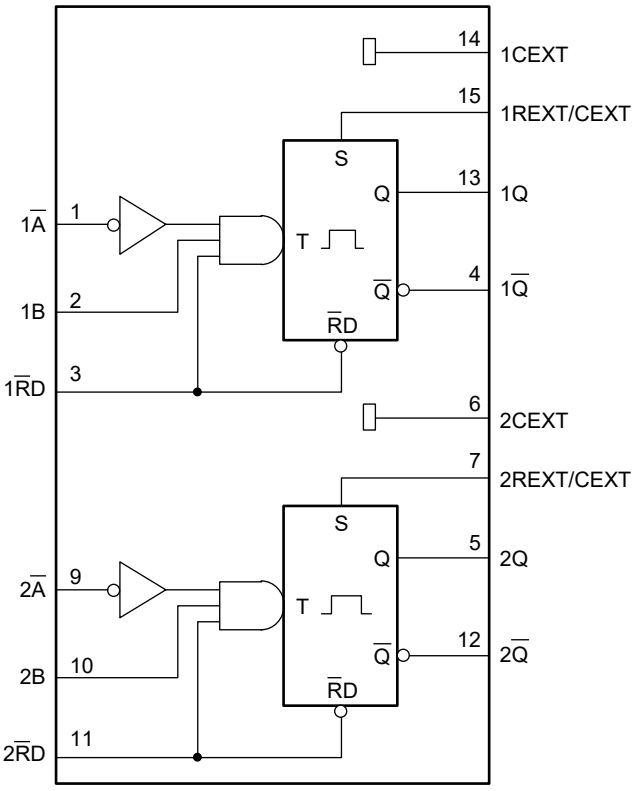


Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

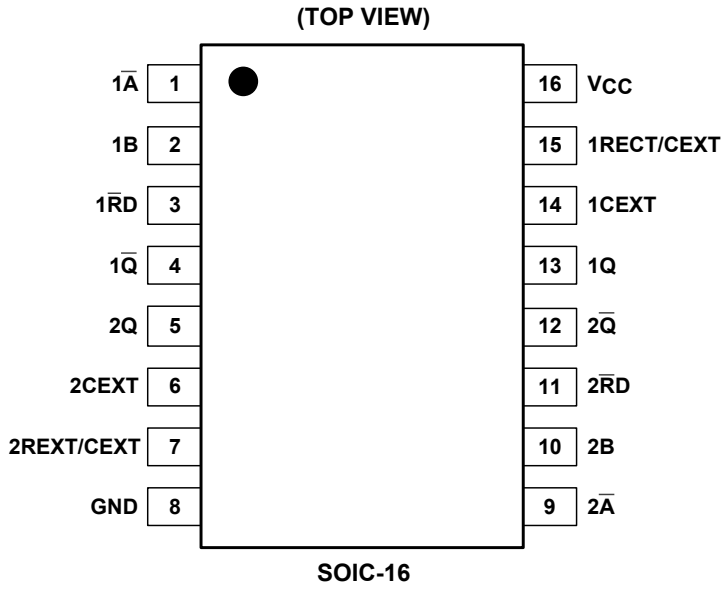
LOGIC SYMBOL



LOGIC DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 9	1$\overline{A}$, 2$\overline{A}$	Negative-Edge Triggered Inputs.
2, 10	1B, 2B	Positive-Edge Triggered Inputs.
3, 11	1$\overline{R}$D, 2$\overline{R}$D	Direct Reset Low and Positive-Edge Triggered Inputs.
4, 12	1$\overline{Q}$, 2$\overline{Q}$	Active Low Outputs.
13, 5	1Q, 2Q	Active High Outputs.
14, 6	1CEXT, 2CEXT	External Capacitor Connections.
15, 7	1REXT/CEXT, 2REXT/CEXT	External Resistor and Capacitor Connections.
8	GND	Ground.
16	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(All typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V		1.5			V
		V_{CC} = 3.0V		2.1			V
		V_{CC} = 5.5V		3.85			V
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V				0.5	V
		V_{CC} = 3.0V				0.9	V
		V_{CC} = 5.5V				1.65	V
High-Level Output Voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O = -50μA, V_{CC} = 2.0V		1.995		V
			I_O = -50μA, V_{CC} = 3.0V		2.995		V
			I_O = -50μA, V_{CC} = 4.5V		4.495		V
			I_O = -4.0mA, V_{CC} = 3.0V		2.8		V
			I_O = -8.0mA, V_{CC} = 4.5V		4.2		V
Low-Level Output Voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O = 50μA, V_{CC} = 2.0V		0.005		V
			I_O = 50μA, V_{CC} = 3.0V		0.005		V
			I_O = 50μA, V_{CC} = 4.5V		0.005		V
			I_O = 4.0mA, V_{CC} = 3.0V		0.2		V
			I_O = 8.0mA, V_{CC} = 4.5V		0.3		V
Input Leakage Current	I_I	V_{CC} = 0V to 5.5V, V_I = 5.5V or GND	nREXT/CEXT (1)		0.01		μA
			Pins n$\overline{A}$, nB and n$\overline{R}$D		0.01		μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A			0.01		μA
		Active state (per circuit) (1) V_I = V_{CC} or GND	V_{CC} = 3.0V		220		μA
			V_{CC} = 4.5V		320		μA
			V_{CC} = 5.5V		400		μA
Input Capacitance	C_I				5		pF
Output Capacitance	C_O						pF

NOTE:
1. Voltage on nREXT/CEXT = 0.5 × V_{CC} and pin nREXT/CEXT in off-state during test.

DYNAMIC CHARACTERISTICS

(For test circuit, see Figure 1. All typical values are measured at T_A = +25°C, V_{CC} = 3.3V and V_{CC} = 5.0V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Propagation Delay [1]	t_{PD}	$n\overline{A}$ and nB to nQ and $n\overline{Q}$, see Figure 2	V_{CC} = 3.0V to 3.6V	C_L = 15pF		7.6		ns
				C_L = 50pF		10.5		ns
			V_{CC} = 4.5V to 5.5V	C_L = 15pF		5.4		ns
				C_L = 50pF		7.3		ns
		$n\overline{R}D$ to nQ and $n\overline{Q}$, see Figure 2	V_{CC} = 3.0V to 3.6V	C_L = 15pF		8.2		ns
				C_L = 50pF		11.7		ns
			V_{CC} = 4.5V to 5.5V	C_L = 15pF		5.6		ns
				C_L = 50pF		8.1		ns
		$n\overline{R}D$ to nQ and $n\overline{Q}$ (reset), see Figure 2	V_{CC} = 3.0V to 3.6V	C_L = 15pF		6.8		ns
				C_L = 50pF		9.2		ns
			V_{CC} = 4.5V to 5.5V	C_L = 15pF		4.8		ns
				C_L = 50pF		6.3		ns
Pulse Width	t_W	Inputs, $n\overline{A}$ = low, see Figure 2	V_{CC} = 3.0V to 3.6V			5		ns
			V_{CC} = 4.5V to 5.5V			5		ns
		Inputs, nB = high, see Figure 2	V_{CC} = 3.0V to 3.6V			5		ns
			V_{CC} = 4.5V to 5.5V			5		ns
		Inputs, $n\overline{R}D$ = low, see Figure 2	V_{CC} = 3.0V to 3.6V			5		ns
			V_{CC} = 4.5V to 5.5V			5		ns
		Outputs, $n\overline{Q}$= low and nQ = high, C_L = 50pF, see Figure 2, 3, 4, 5 [2]	V_{CC} = 3.0V to 3.6V	C_{EXT} = 28pF, R_{EXT} = 2kΩ		230		ns
			V_{CC} = 4.5V to 5.5V			230		ns
			V_{CC} = 3.0V to 3.6V	C_{EXT} = 0.01μF, R_{EXT} = 10kΩ		100		μs
			V_{CC} = 4.5V to 5.5V			100		μs
			V_{CC} = 3.0V to 3.6V	C_{EXT} = 0.1μF, R_{EXT} = 10kΩ		1		ms
			V_{CC} = 4.5V to 5.5V			1		ms
Retrigger Time	t_{RTRIG}	$n\overline{A}$ to nB, C_L = 50pF, see Figure 3 and Figure 5	V_{CC} = 3.0V to 3.6V	C_{EXT} = 100pF, R_{EXT} = 1kΩ		60		ns
			V_{CC} = 4.5V to 5.5V			55		ns
			V_{CC} = 3.0V to 3.6V	C_{EXT} = 0.01μF, R_{EXT} = 1kΩ		0.5		μs
			V_{CC} = 4.5V to 5.5V			0.5		μs
Power Dissipation Capacitance [3]	C_{PD}	C_L = 50pF, f_i = 1MHz, V_{IN} = GND to V_{CC}				110		pF
External Resistance	R_{EXT}	V_{CC} = 2.0V			5			kΩ
		V_{CC} > 3.0V			1			kΩ
External Capacitance [4]	C_{EXT}	V_{CC} = 2.0V						pF
		V_{CC} > 3.0V						pF

NOTES:

1. t_{PD} is the same as t_{PLH} and t_{PHL}.
2. For $C_{EXT} \geq 10$nF, the typical value of the pulse width t_W (μs) = C_{EXT} (nF) × R_{EXT} (kΩ).
3. C_{PD} is used to determine the dynamic power dissipation (PD in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = input frequency in MHz.

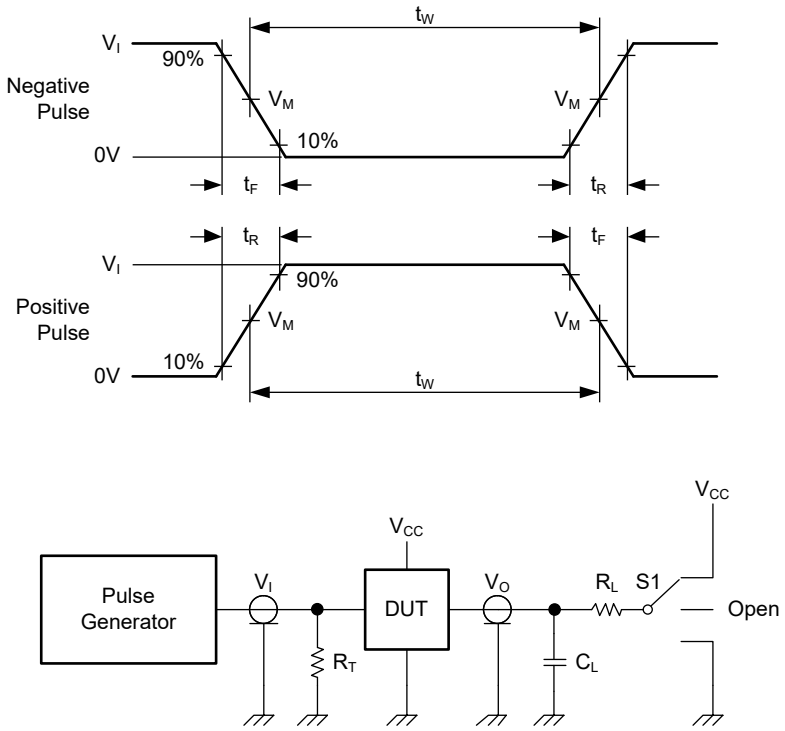
   f_o = output frequency in MHz.

   C_L = output load capacitance in pF.

   V_{CC} = supply voltage in Volts.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.
4. C_{EXT} has no limits.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator.

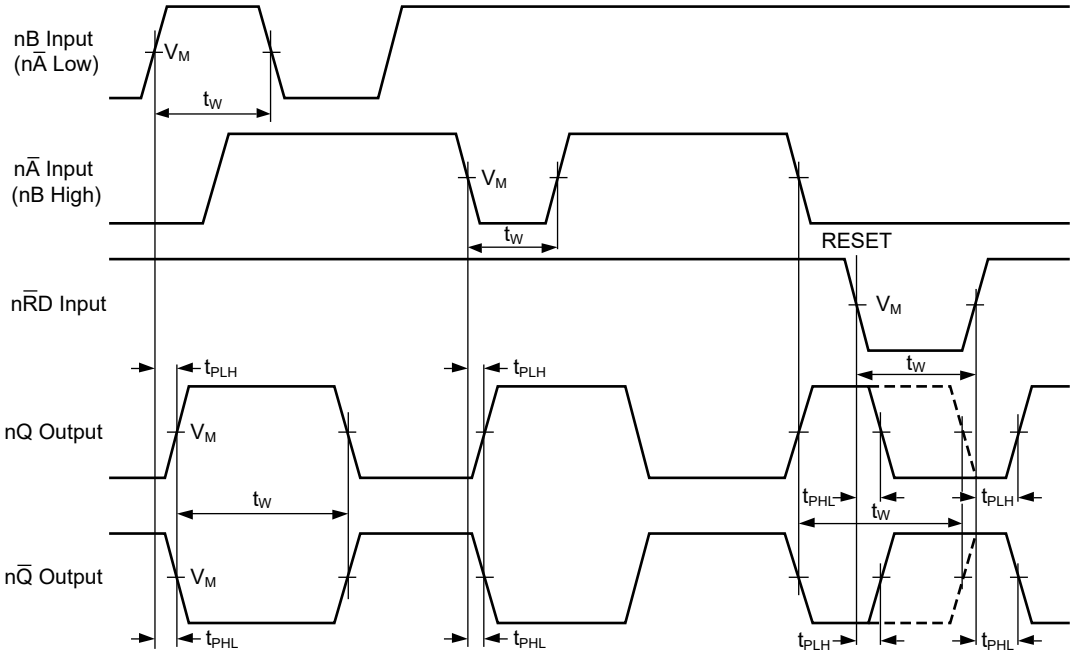
S1 = Test selection switch.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

INPUT		LOAD		S1 POSITION		
V_I	t_R, t_F	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	3.0ns	15pF, 50pF	1kΩ	Open	GND	V_{CC}

WAVEFORMS

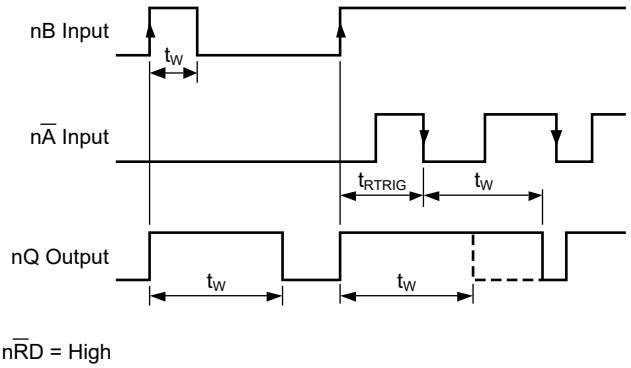


Test conditions are given in Table 1.
Measurement points are given in Table 2.

Figure 2. Propagation Delay Inputs (nA̅, nB and nR̅D) to Outputs (nQ and nQ̅)

Table 2. Measurement Points

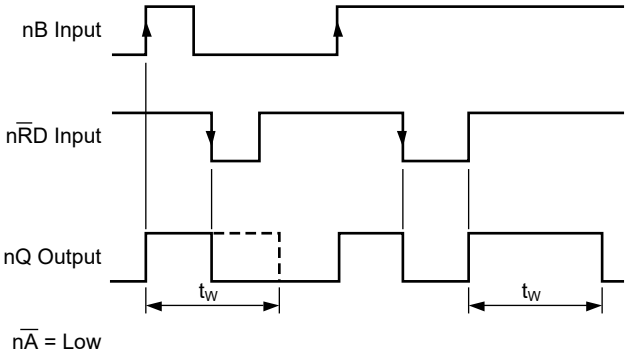
INPUT	OUTPUT
V_M	**V_M**
0.5 × V_{CC}	0.5 × V_{CC}



Test conditions are given in Table 1.

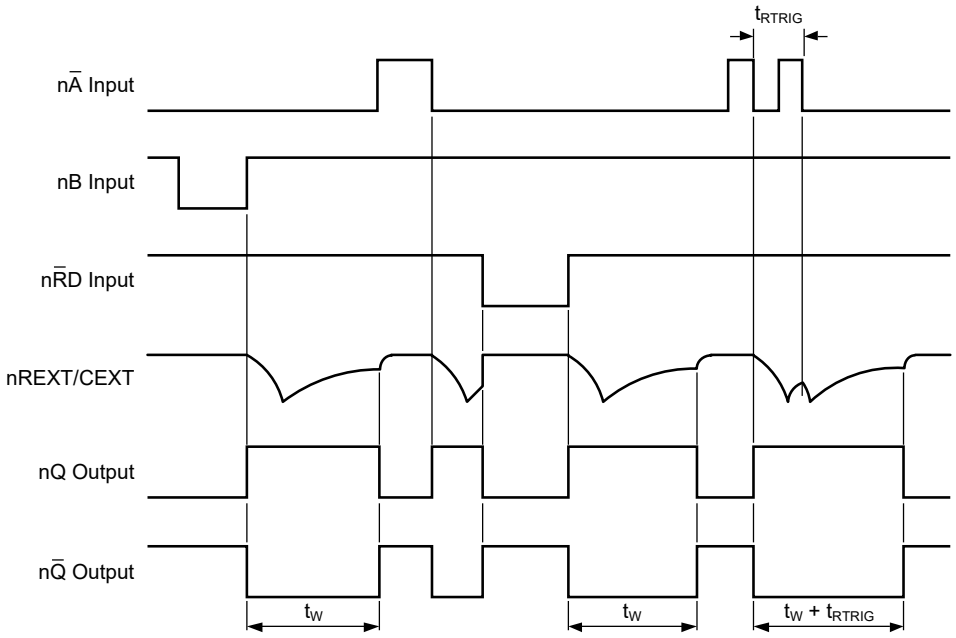
Figure 3. Output Pulse Control Using Retrigger Pulse

WAVEFORMS (continued)



Test conditions are given in Table 1.

Figure 4. Output Pulse Control Using Reset Input nR̄D



Test conditions are given in Table 1.

Figure 5. Input and Output Timing

WAVEFORMS (continued)

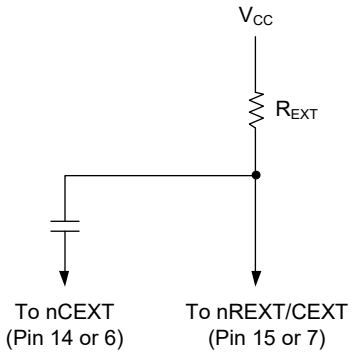
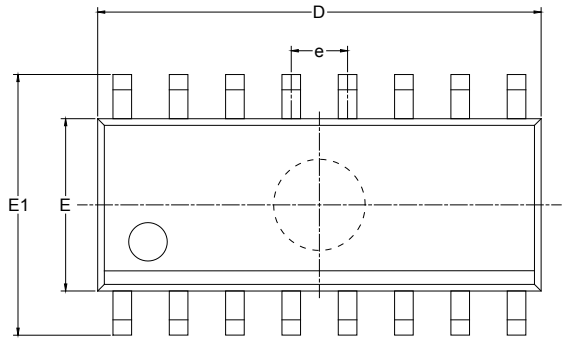
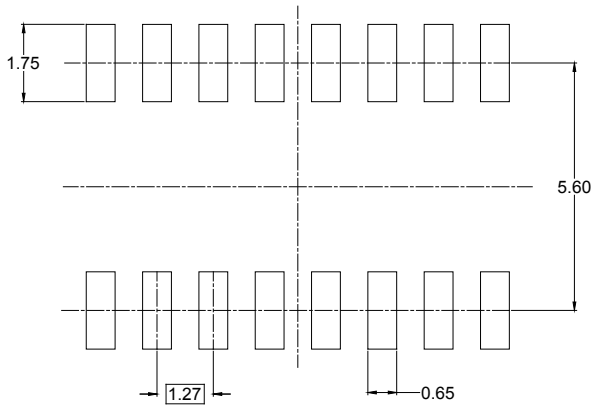


Figure 6. Timing Component Connections

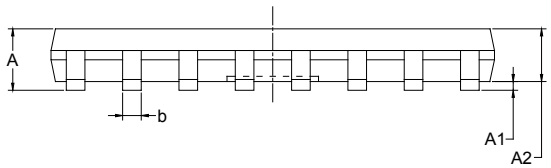
PACKAGE OUTLINE DIMENSIONS

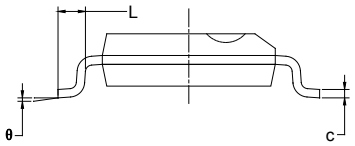
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)

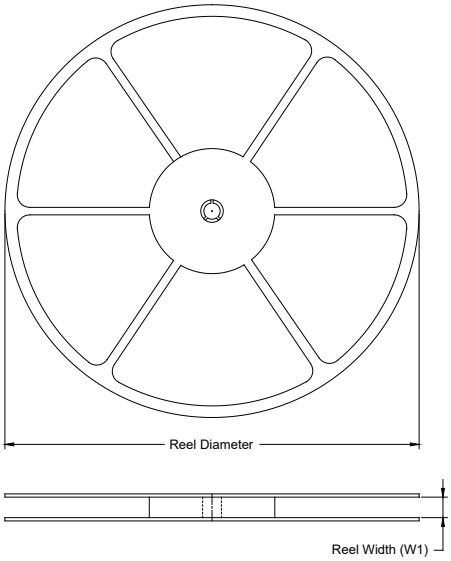




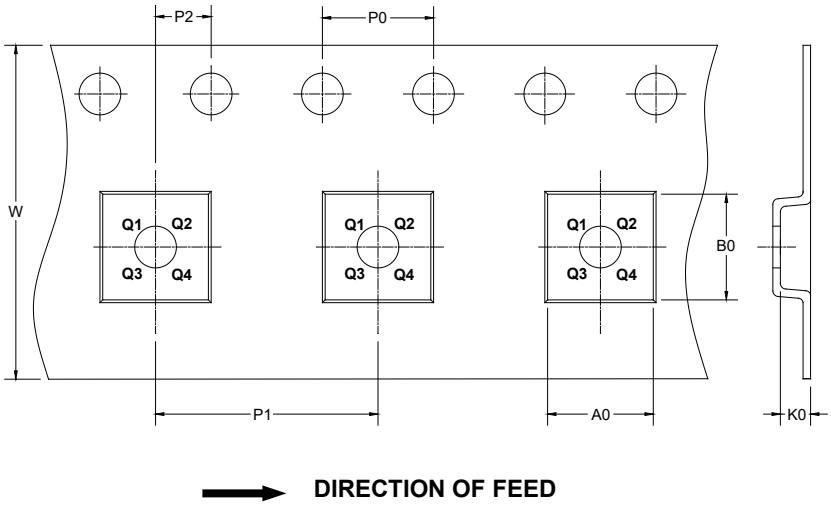
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

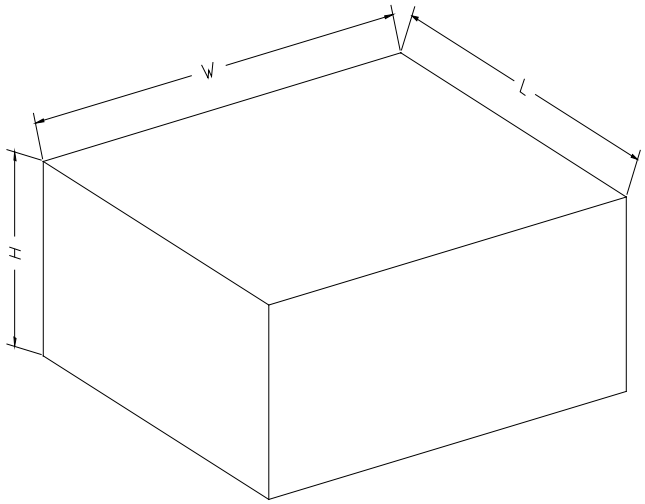
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13″	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002