SGM2054
Sink and Source DDR Termination Regulator

GENERAL DESCRIPTION

The SGM2054 device is a sink and source DDR (double data rate) termination regulator. It is specifically designed for low-cost and low-external component count systems.

Other features include logic-controlled shutdown mode, output current limit and thermal shutdown protection. The SGM2054 has an EN signal that can be used to discharge VO when EN is less than 0.3V.

With fast transient response, remote sensing, and soft-start capabilities to reduce inrush current, the SGM2054 ensures the optimal system performance for powering the DDR2, DDR3, Low-Power DDR3, DDR3L, DDR4 and DDR5 VTT bus termination.

The SGM2054 is available in a Green TDFN-3×3-10L package. It operates over an operating temperature range of -40℃ to +125℃.

FEATURES

- **VLDOIN Voltage Range: 1.1V to 3.5V**
- **Low Input Voltages: 2.5V Rail and 3.3V Rail**
- **Minimum VO Effective Capacitance: 20μF**
- **Open-Drain Power-Good (PG) Output**
- **EN Logic Control**
- **Buffered Reference: ±10mA**
- **Soft-Start Inrush Control**
- **Remote Sensing**
- **Fast Load Transient Response**
- **Under-Voltage Lockout**
- **Output Current Limit**
- **Thermal Shutdown Protection**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TDFN-3×3-10L Package**

APPLICATIONS

LCD TV
STB
Wireless Base Station
Server, Notebook and Desktop PC
Printer

TYPICAL APPLICATION

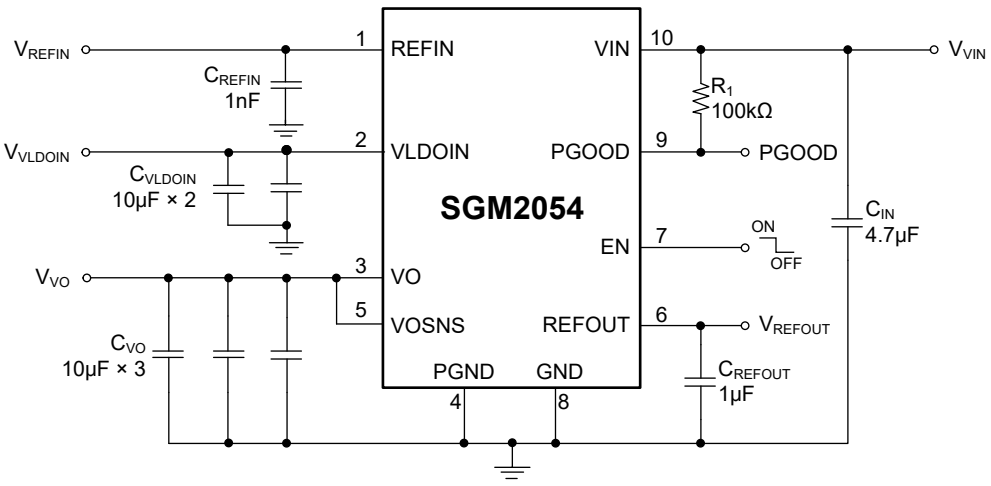


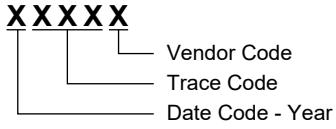
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2054	TDFN-3×3-10L	-40℃ to +125℃	SGM2054XTD10G/TR	SGM 2054D XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

REFIN, VIN, VLDOIN, VOSNS to GND ..... -0.3V to 3.6V
EN, PGOOD to GND ..... -0.3V to 3.6V
PGND to GND ..... -0.3V to 0.3V
REFOUT to GND ..... -0.3V to (V_{REFOUT} + 0.3V)
VO to GND ..... -0.3V to (V_{LDOIN} + 0.3V)
Package Thermal Resistance
TDFN-3×3-10L, θ_{JA} ..... 56℃/W
TDFN-3×3-10L, θ_{JB} ..... 26℃/W
TDFN-3×3-10L, $\theta_{JC(TOP)}$ ..... 59℃/W
TDFN-3×3-10L, $\theta_{JC(BOT)}$ ..... 10℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 7000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

VIN to GND ..... 2.375V to 3.5V
VLDOIN to GND ..... 1.1V to 3.5V
EN, PGOOD, VO, VOSNS to GND ..... 0V to 3.5V
REFIN to GND ..... 0.5V to 1.8V
REFOUT to GND ..... 0V to 1.8V
PGND to GND 0V
VLDOIN Effective Capacitance, C_{LDOIN} ..... 15μF (MIN)
VIN Effective Capacitance, C_{IN} ..... 1μF (MIN)
VO Effective Capacitance, C_{VO} ..... 20μF to 100μF
REFOUT Effective Capacitance, C_{REFOUT} ..... 0.1μF to 1μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

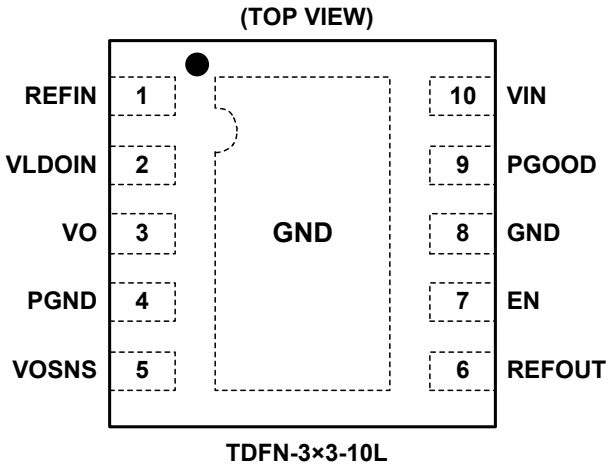
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	REFIN	I	Reference Input Pin.
2	VLDOIN	I	Regulator Supply Voltage Pin. It is recommended to use a ceramic capacitor with a minimum effective capacitance of 15μF from VLDOIN pin to ground.
3	VO	O	Regulator Output Pin. It is recommended to use output capacitor with effective capacitance in the range of 20μF to 100μF.
4	PGND	G	Regulator Power Ground.
5	VOSNS	I	Voltage Sense Input Pin. Connect to the remote voltage sensing point of load powered by VO.
6	REFOUT	O	Reference Output Pin. It is recommended to use output capacitor with effective capacitance in the range of 0.1μF to 1μF.
7	EN	I	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator.
8	GND	G	Signal Ground.
9	PGOOD	O	Power-Good Indicator Output Pin. An open-drain output and active high when the output voltage reaches $V_{TH(PG)}$ of the target.
10	VIN	I	Input Voltage Supply Pin. It is recommended to use a ceramic capacitor with a minimum effective capacitance of 1μF from VIN pin to ground.
Exposed Pad	GND	G	Exposed Pad. Connect it to GND internally. Connect it to a large ground plane to maximize thermal performance; this pad is not an electrical connection point.

NOTE: I = Input, O = Output, G = Ground.

ELECTRICAL CHARACTERISTICS

(V_{VIN} = 3.3V, V_{VLDOIN} = 1.8V, V_{REFIN} = 0.9V, V_{EN} = V_{VIN}, C_{VO} = 3 × 10μF, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current							
Supply Current	I_{VIN}	V_{EN} = 3.3V, no load			0.7	1	mA
Shutdown Current	I_{SHDN}	V_{EN} = 0V, V_{REFIN} = 0V, no load			50	65	μA
		V_{EN} = 0V, V_{REFIN} > 0.4V, no load			165	240	
Supply Current of VLDOIN	I_{VLDOIN}	V_{EN} = 3.3V, no load			1	50	μA
Shutdown Current of VLDOIN	$I_{VLDOIN(SHDN)}$	V_{EN} = 0V, no load			0.1	10	μA
Input Current							
Input Current of REFIN	I_{REFIN}	V_{EN} = 3.3V				0.5	μA
VO Output							
Output DC Voltage of VO	V_{VO}	V_{REFOUT} = 0.9V (DDR2), I_{VO} = 0A	T_J = +25℃		0.9		V
			T_J = -40℃ to +125℃	-12		12	mV
		V_{REFOUT} = 0.75V (DDR3), I_{VO} = 0A	T_J = +25℃		0.75		V
			T_J = -40℃ to +125℃	-12		12	mV
		V_{REFOUT} = 0.675V (DDR3L), I_{VO} = 0A	T_J = +25℃		0.675		V
			T_J = -40℃ to +125℃	-12		12	mV
		V_{REFOUT} = 0.6V (DDR4), I_{VO} = 0A	T_J = +25℃		0.6		V
			T_J = -40℃ to +125℃	-12		12	mV
		V_{REFOUT} = 0.55V (DDR5), I_{VO} = 0A	T_J = +25℃		0.55		V
			T_J = -40℃ to +125℃	-12		12	mV
Output Voltage Tolerance to REFOUT	V_{OTOL}	-2A < I_{VO} < 2A		-12		12	mV
VO Source Current Limit	I_{VOSRCL}	With reference to REFOUT, V_{OSNS} = 90% × V_{REFOUT}, T_J = -40℃ to +85℃		3		5.5	A
VO Sink Current Limit	I_{VOSNCL}	With reference to REFOUT, V_{OSNS} = 110% × V_{REFOUT}, T_J = -40℃ to +85℃		-5.7		-3.5	A
Discharge Resistance of VO	R_{DIS}	V_{REFIN} = 0V, V_{VO} = 0.3V, V_{EN} = 0V			16	30	Ω
Power-Good Comparator							
VO PGOOD Threshold	$V_{TH(PG)}$	PGOOD window lower threshold with respect to REFOUT		-24	-20	-16	%
		PGOOD window upper threshold with respect to REFOUT		16	20	26	
		PGOOD hysteresis			5		
PGOOD Start-Up Delay	$t_{PGSTUPDLY}$	Start-up rising edge, VOSNS within 15% of REFOUT			2		ms
Output Low Voltage	$V_{PGOODLOW}$	I_{SINK} = 4mA				0.4	V
PGOOD Bad Delay	$t_{PBADDLY}$	VOSNS is outside of the ±20% PGOOD window			0.2		μs
Leakage Current	$I_{PGOODLKG}$	V_{OSNS} = V_{REFIN} (PGOOD high impedance), V_{PGOOD} = V_{IN} + 0.2V				1	μA

ELECTRICAL CHARACTERISTICS (continued)

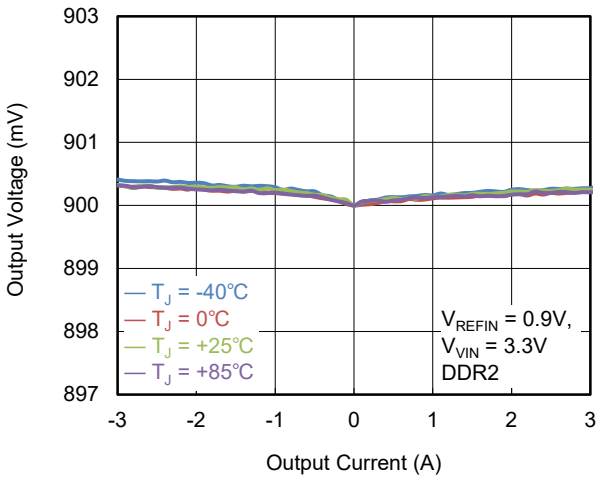
(V_{VIN} = 3.3V, V_{VLDOIN} = 1.8V, V_{REFIN} = 0.9V, V_{EN} = V_{VIN}, C_{VO} = 3 × 10μF, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFIN and REFOUT							
REFIN Voltage Range	V_{REFIN}			0.5		1.8	V
REFIN Under Voltage Lockout	$V_{REFINUVLO}$	REFIN rising		350	380	410	mV
REFIN Under Voltage Lockout Hysteresis	$V_{REFINUVHYS}$				20		mV
REFOUT Voltage	V_{REFOUT}				REFIN		V
REFOUT Voltage Tolerance to V_{REFIN}	$V_{REFOUTTOL}$	-1mA < I_{REFOUT} < 1mA	V_{REFIN} = 1.25V	-12		12	mV
			V_{REFIN} = 0.9V	-12		12	
			V_{REFIN} = 0.75V	-12		12	
			V_{REFIN} = 0.675V	-12		12	
			V_{REFIN} = 0.6V	-12		12	
			V_{REFIN} = 0.55V	-12		12	
REFOUT Source Current Limit	$I_{REFOUTSRCL}$	V_{REFOUT} = 0V		20	40		mA
REFOUT Sink Current Limit	$I_{REFOUTSNCL}$	V_{REFOUT} = V_{IN}		20	40		mA
UVLO and EN Logic Threshold							
UVLO Threshold	V_{UVLO}	Wake up		2.15	2.25	2.35	V
		Hysteresis			80		mV
High-Level Input Voltage	V_{ENIH}	Enable		1			V
Low-Level Input Voltage	V_{ENIL}	Enable				0.5	
Hysteresis Voltage	V_{ENYST}	Enable			0.03		
Logic Input Leakage Current	I_{EN-LKG}	EN		-1		1	μA
Start-Up Time	t_{STR}	C_{OUT} = 100μF, $V_{VO(NOM)}$ = 0.6V, EN turns on to V_{VO} = 90% × $V_{VO(NOM)}$			27		μs
Thermal Shutdown							
Thermal Shutdown Temperature	T_{SHDN}				150		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}				20		

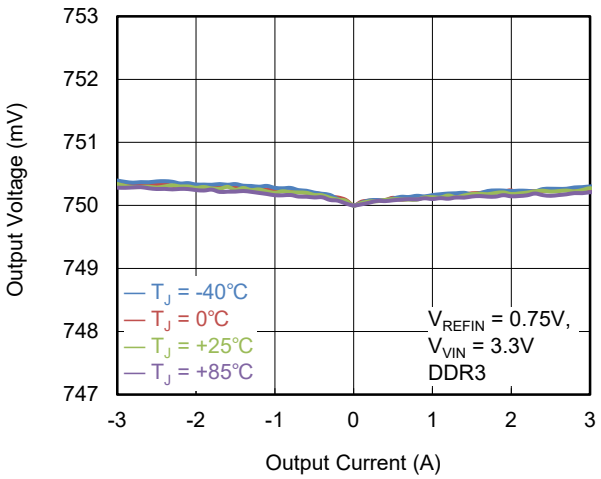
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{VLDOIN} = 1.8V, V_{VOSNS} = 0.9V, V_{EN} = V_{VIN}, C_{VO} = 3 × 10μF, unless otherwise noted.

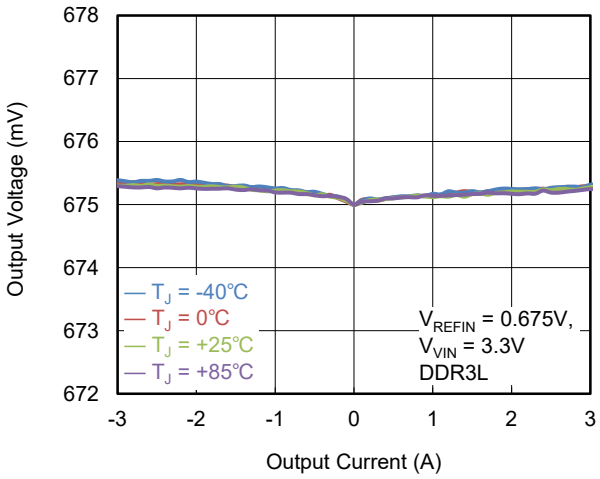
VO Load Regulation



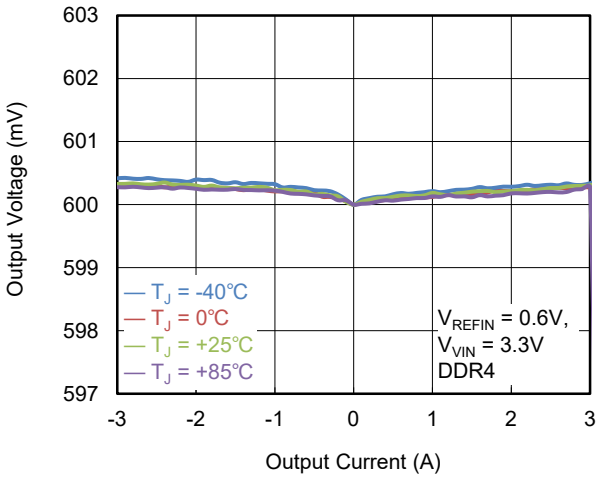
VO Load Regulation



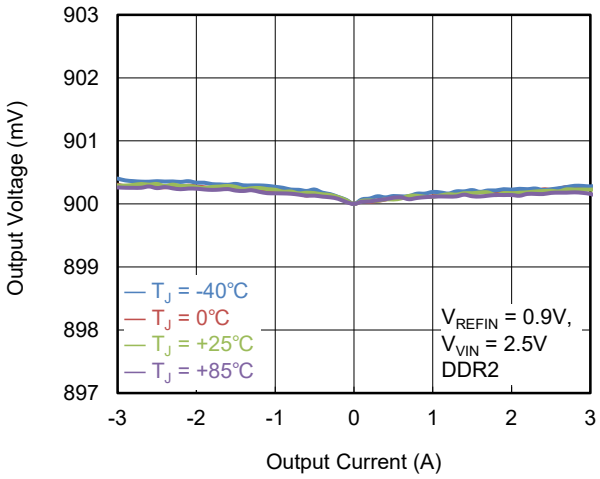
VO Load Regulation



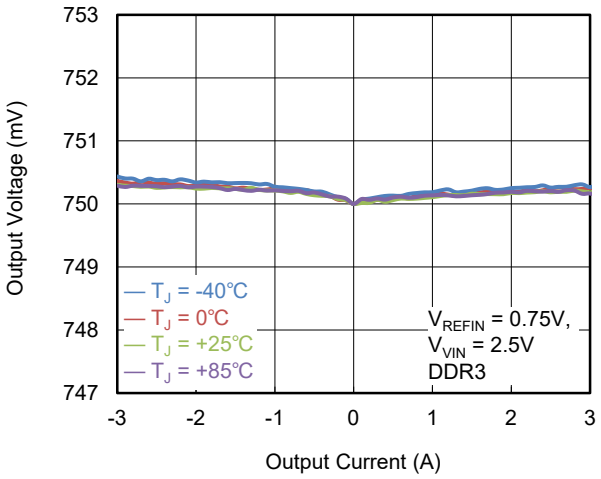
VO Load Regulation



VO Load Regulation



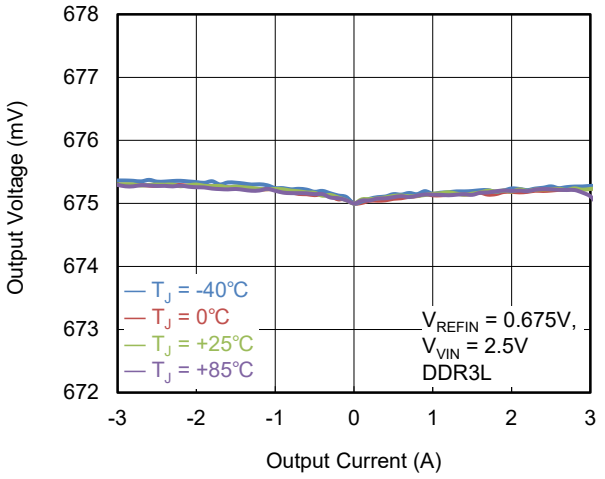
VO Load Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{VLDOIN} = 1.8V, V_{VOSNS} = 0.9V, V_{EN} = V_{VIN}, C_{VO} = 3 × 10μF, unless otherwise noted.

VO Load Regulation



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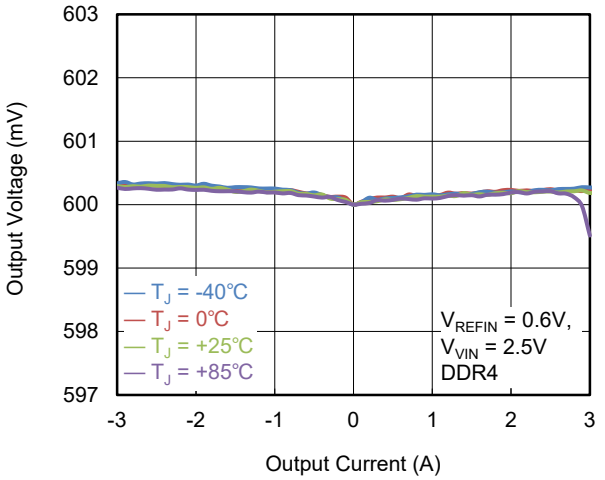
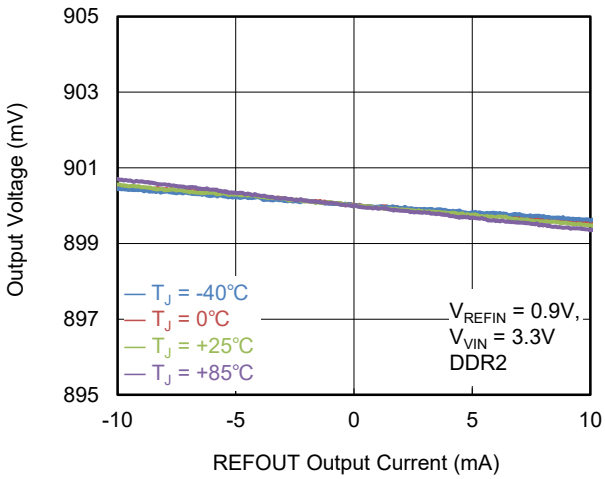


REFOUT Load Regulation



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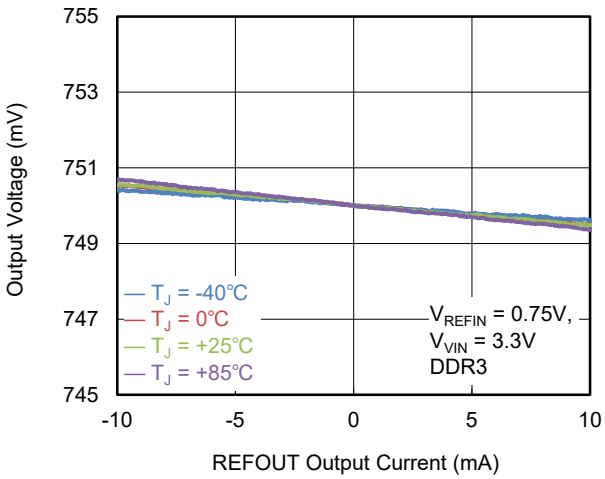

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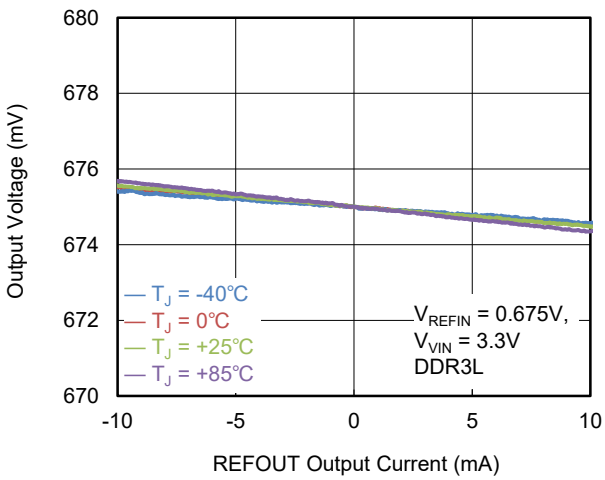
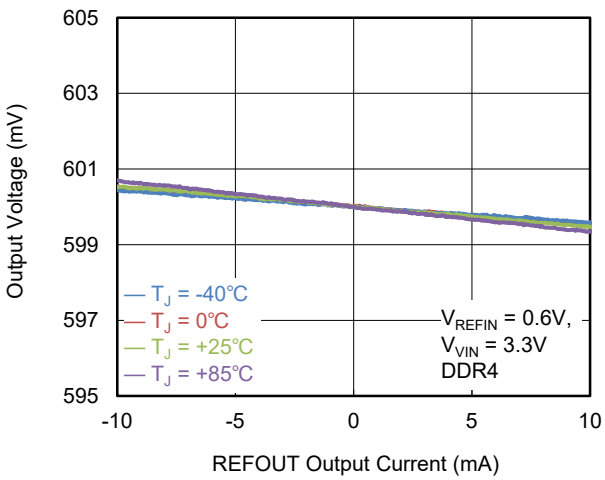


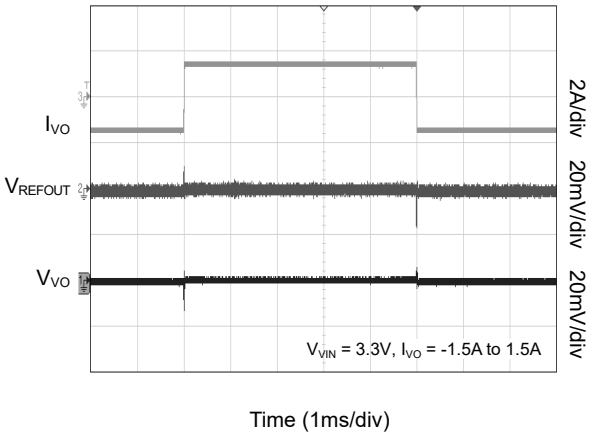
REFOUT Load Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{VLDOIN} = 1.8V, V_{VOSNS} = 0.9V, V_{EN} = V_{VIN}, C_{VO} = 3 × 10μF, unless otherwise noted.

Load Transient Response



FUNCTIONAL BLOCK DIAGRAM

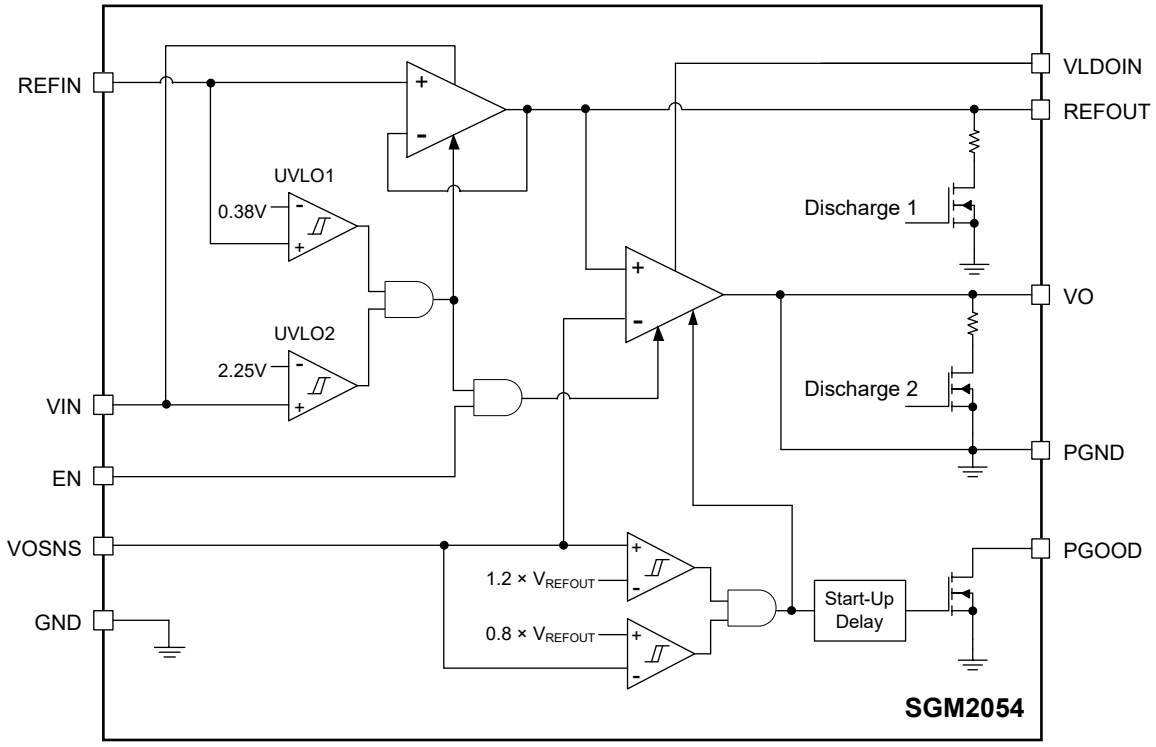


Figure 2. Block Diagram

DETAILED DESCRIPTION

Sink and Source Regulator (VO Pin is the Output)

The SGM2054 is an ultra-low dropout voltage, sink and source linear regulator which is specifically designed as the termination voltage of DDR memory. It can provide up to 3A output current capability.

The SGM2054 has a built-in high-side N-MOSFET for current sourcing and a low-side N-MOSFET for current sinking. To support the fast load transient response of DDR memory, the feedback loop of the SGM2054 is very fast, it can get fast load transient response using small ceramic capacitors and save cost. The VOSNS remote sensing pin is used to compensate the dropout voltage generated by the PCB trace resistance and it should be connected to the remote node of load which is powered by VO.

Reference Input (REFIN Pin)

The input voltage range of the REFIN pin is from 0.5V to 1.8V and it is used to generate the reference voltage (V_{REFOUT}) of DDR memory. It is set by an external equivalent ratio voltage divider connected to the memory power supply bus (V_{DDQ}). In application, V_{REFOUT}, V_{TT} and V_{DDQ} must meet the equation:

$$V_{REFOUT} = V_{TT} = V_{DDQ} / 2$$

REFOUT and VO must track the reference input at the REFIN pin.

Reference Output (REFOUT Pin)

REFOUT is independent of the EN pin state. The output voltage is tightly regulated to track the reference voltage applied at the REFIN pin. When REFIN voltage rises to 380mV and V_{VIN} is above the UVLO threshold, REFOUT will become active. When V_{REFOUT} is lower than 360mV, REFOUT is disabled, and it will be discharged to GND by an internal 130Ω (TYP) MOSFET.

REFOUT can source and sink 10mA to/from load. It is used as DDR termination voltage (V_{TT}) of DDR memory.

Soft-Start

The VO pin has soft-start function using current clamp method. It limits inrush current when charging the output capacitors. The soft-start function and over-current protection are completely symmetrical for sourcing and sinking current. For sourcing, it charges output capacitors from the VLDOIN pin to the REFOUT and VO pins. For sinking, it discharges output capacitors from the REFOUT and VO pins to GND. When VO is outside of the power-good window, the clamping current is one-half of the full over-current limit (OCL). When VO is inside the power-good window, the clamping current will switch to the full OCL.

Enable Control

The SGM2054 uses the EN pin to enable/disable the device. When the EN pin voltage is lower than 0.5V, the device is in shutdown state. In this state, the internal discharge transistor is active to pull the output voltage to ground through a 16Ω (TYP) resistor.

When the EN pin voltage is higher than 1V, the device is in active state, the input voltage is regulated to the output voltage and the internal discharge transistor is turned off.

Power-Good

The PGOOD pin is an open-drain that asserts high with 2ms (TYP) delay time after the VO enters power-good window which is V_{VO} within +20% of V_{REFOUT}. When the VO is outside the PGOOD window, PGOOD de-asserts within 0.2μs (TYP). 100kΩ (TYP) pull-up resistor is recommended, which should be connected to a stable and right power supply to interface with digital controller.

Output Current Limit

When overload events happen, the output current is internally limited.

Under-Voltage Lockout (UVLO)

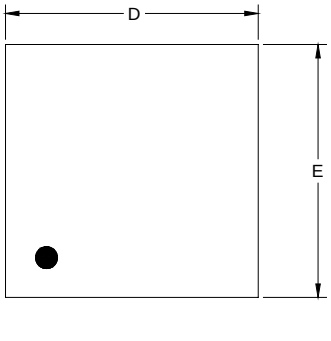
The UVLO circuit monitors the input voltage to prevent the device from turning on before V_{VIN} rises above the V_{UVLO} threshold. The UVLO circuit responds quickly to glitches on the VIN pin and attempts to disable the output of the device if any of these rails collapses. The local input capacitance prevents severe brownouts in most applications.

Thermal Shutdown

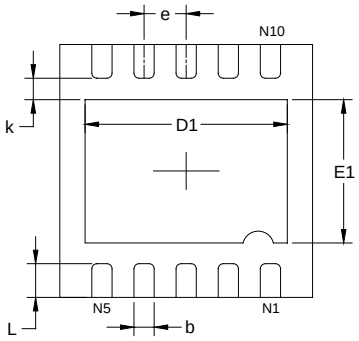
The SGM2054 can detect the temperature of die. When the die temperature exceeds the threshold value of thermal shutdown, the SGM2054 will be in shutdown state and remain in this state until the die temperature decreases to +130℃.

PACKAGE OUTLINE DIMENSIONS

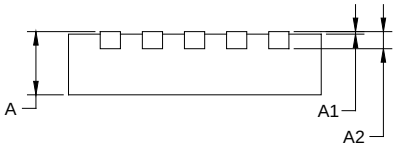
TDFN-3×3-10L



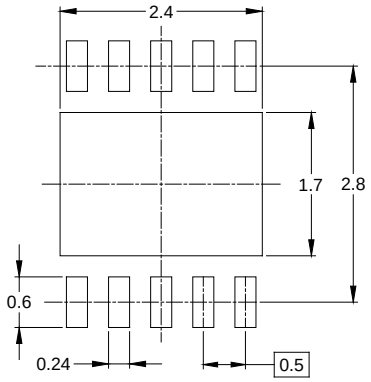
TOP VIEW



BOTTOM VIEW



SIDE VIEW



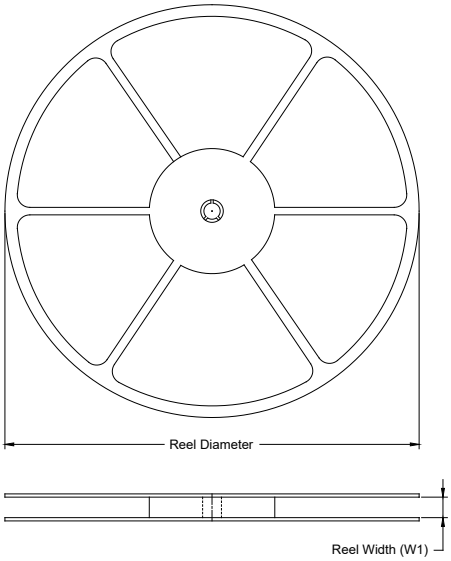
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

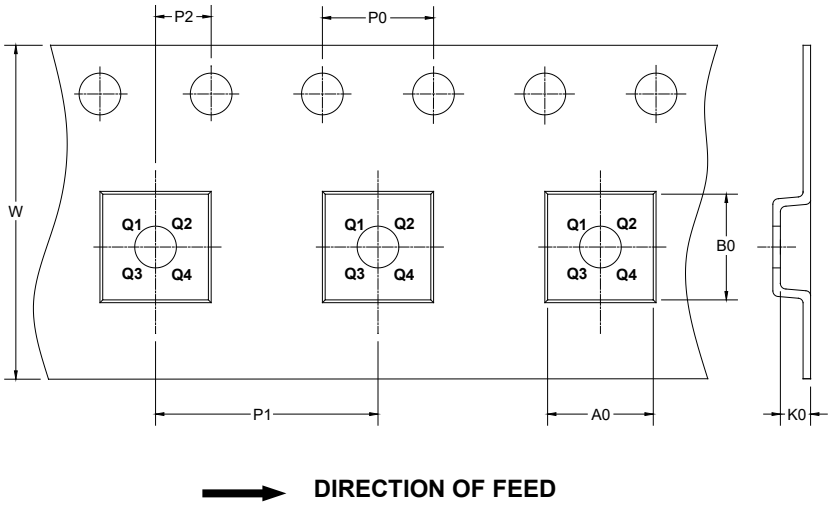
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



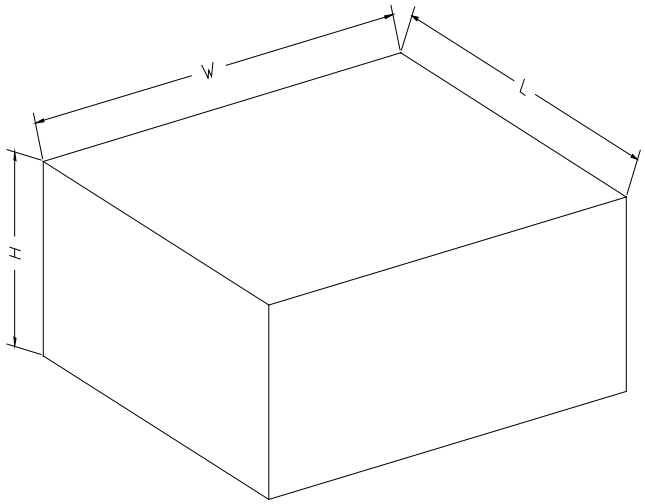
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-10L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002