SGM25711B
2.5V to 18V High-Efficiency Power-Limiting Hot Swap Controller

GENERAL DESCRIPTION

The SGM25711B is a hot swap controller that allows a board to be safely inserted or removed from a live backplane. An internal circuit drives an external N-MOSFET switch to control supply voltage from 2.5V to 18V.

The SGM25711B features programmable current limit and fault time to protect the power supply from current at all times. If the supply remains at current limit for more than a programmable fault time, the external MOSFET is turned off. The SGM25711B restarts automatically after a fault timeout delay. The low, 25mV current sense threshold is highly accurate and allows using smaller sense resistors yielding lower power loss and smaller size.

The SGM25711B offers programmable power-limiting to ensure that the external MOSFET operates inside its safe operating area (SOA) at all times. This feature allows the user to easily design a high reliability system. Power good and fault outputs are provided for status monitoring and downstream load control.

SGM25711B is available in a Green MSOP-10 package.

FEATURES

- **Input Voltage Range from 2.5V to 18V**
- **Programmable MOSFET SOA Protection**
- **Accurate Current Limit at All Times**
- **Accurate 25mV Current Sense Threshold**
- **Power Good Output**
- **Fast Circuit-Breaker for Short-Circuit Protection**
- **Programmable Fault Timer**
- **Programmable Under-Voltage Threshold**
- **Active-Low for nPG and nFLT Pins**
- **Available in a Green MSOP-10 Package**

APPLICATIONS

Server Line Cards
Storage Area Networks (SAN)
Medical Systems
Plug-In Modules
Base Stations

TYPICAL APPLICATION

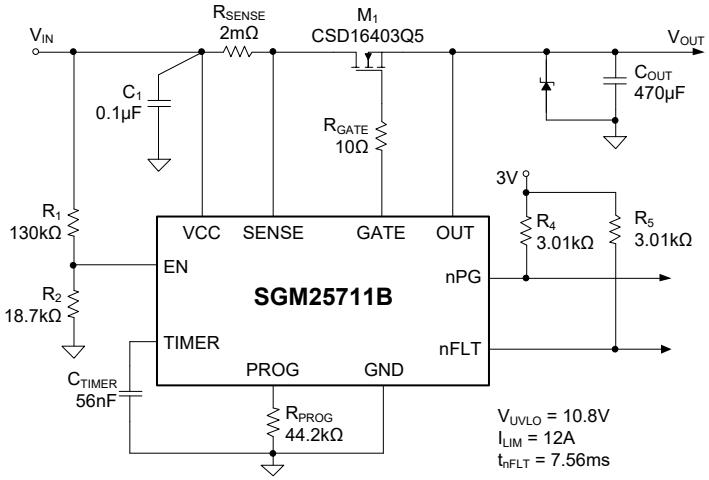


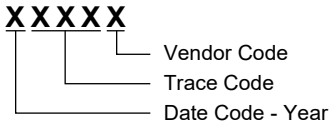
Figure 1. Typical Application Circuit (12V/10A)

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25711B	MSOP-10	-40℃ to +125℃	SGM25711BXMS10G/TR	SGMRB7 XMS10 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range
EN, nFLT (1), nPG (1), GATE, OUT, SENSE, VCC ..... -0.3V to 30V
PROG (1) ..... -0.3V to 3.6V
SENSE to VCC ..... -0.3V to 0.3V
TIMER ..... -0.3V to 5V
Sinking Current
nFLT, nPG 5mA
Sourcing Current
PROG ..... Internally limited
Package Thermal Resistance
MSOP-10, θ_{JA} ..... 164℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

NOTE: 1. Do not apply voltages directly to these pins.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range
SENSE, VCC ..... 2.5V to 18V
EN, nFLT, nPG, OUT ..... 0V to 18V
Sinking Current
nFLT, nPG ..... 0mA to 2mA
Resistance, R_{PROG} ..... 4.99kΩ to 500kΩ
External Capacitance, C_{TIMER} ..... 1nF (MIN)
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

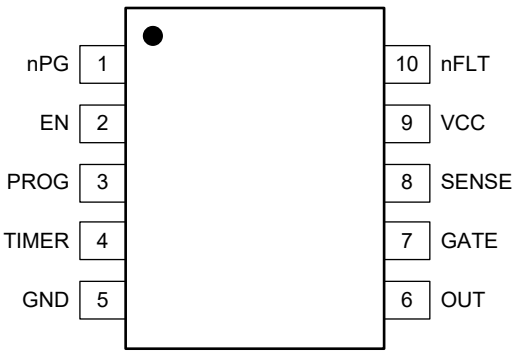
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



MSOP-10

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	nPG	Power Good Indicator Pin. Active-low, open-drain power good indicator. Status is determined by the voltage across the MOSFET.
2	EN	Enable Pin. Active-high enable input. Connect to resistor divider.
3	PROG	Power-Limiting Programmable Pin. A resistor from this pin to GND sets the maximum power dissipation for the MOSFET.
4	TIMER	Fault Timer Pin. A capacitor connected from this pin to GND programs the timeout period.
5	GND	Ground.
6	OUT	Power Output Pin. Output voltage sensor for monitoring MOSFET power.
7	GATE	Gate Driver Output. Gate driver output for external MOSFET.
8	SENSE	Current Sense Pin. Current sense input for resistor shunt from VCC to SENSE.
9	VCC	Power Input Pin. Input voltage sense and power supply.
10	nFLT	Fault Event Indicator Pin. Active-low, open-drain output indicates overload fault timer has turned MOSFET off.

ELECTRICAL CHARACTERISTICS

(-40℃ ≤ T_J ≤ +125℃, V_{CC} = 12V, V_{EN} = 3V and R_{PROG} = 50kΩ to GND. All voltages referenced to GND, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC					
UVLO Threshold Voltage, Rising		2.25	2.35	2.45	V
UVLO Threshold Voltage, Falling		2.17	2.27	2.37	V
Hysteresis			85		mV
Supply Current, Enabled	I_{OUT} + I_{VCC} + I_{SENSE}		0.32	0.5	mA
Supply Current, Disabled	V_{EN} = 0V, I_{OUT} + I_{VCC} + I_{SENSE}		4		μA
EN					
Enable Threshold Voltage, Falling		1.25	1.3	1.35	V
Hysteresis			55		mV
Input Leakage Current	V_{EN} = 0V to 30V	-1	0	1	μA
nFLT					
Output Low Voltage	Sinking 2mA		35	65	mV
Input Leakage Current	V_{nFLT} = 0V or 30V	-1	0	1	μA
nPG					
nPG Threshold Voltage	$V_{(SENSE - OUT)}$ rising, nPG going high	235	315	395	mV
Hysteresis	$V_{(SENSE - OUT)}$ falling, nPG going low		85		mV
Output Low Voltage	Sinking 2mA		35	65	mV
Input Leakage Current	V_{nPG} = 0V or 30V	-1	0	1	μA
PROG					
Bias Voltage	Sourcing 10μA	0.65	0.68	0.71	V
Input Leakage Current	V_{PROG} = 1.5V	-0.2	0	0.2	μA
TIMER					
Sourcing Current	V_{TIMER} = 0V	8	10	12	μA
Sinking Current	V_{TIMER} = 2V	8	10	12	μA
	V_{EN} = 0V, V_{TIMER} = 2V	4.5	7	9.5	mA
TIMER Threshold Voltage, Rising		1.3	1.35	1.4	V
TIMER Threshold Voltage, Falling		0.33	0.35	0.38	V
Timer Activation Voltage	Raise GATE until I_{TIMER} sinking, measure $V_{(GATE - VCC)}$, V_{CC} = 12V	5.3	5.6	5.9	V
OUT					
Input Bias Current	V_{OUT} = 12V		1		μA
GATE					
Output Voltage	V_{OUT} = 12V	24.5	25.5	26.5	V
Clamp Voltage	Inject 10μA into GATE, measure $V_{(GATE - VCC)}$	12	13.5	15	V
Sourcing Current	V_{GATE} = 12V	20	33	46	μA
Sinking Current	Fast turn-off, V_{GATE} = 0.2V	33	63	93	mA
	Sustained, V_{GATE} = 4V to 23V	6	11	16	mA
Pull-Down Resistance	Thermal shutdown	11.5	17.5	23.5	kΩ
SENSE					
Input Bias Current	V_{SENSE} = 12V, sinking current		15	25	μA
Current Limit Threshold	V_{OUT} = 12V, -20℃ ≤ T_J ≤ +125℃	23	25	27	mV
	V_{OUT} = 12V, -40℃ ≤ T_J ≤ +125℃	22.5	25	27.5	
Power-Limiting Threshold	V_{OUT} = 7V, R_{PROG} = 50kΩ	10	14	18	mV
	V_{OUT} = 2V, R_{PROG} = 25kΩ	10	14	18	
Fast-Trip Shutdown Threshold		52.3	61.5	70.7	mV
Over-Temperature Shutdown (OTSD)					
Threshold, Rising			145		℃
Hysteresis			15		℃

TIMING REQUIREMENTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EN					
Deglitch Time	EN↑	10	39.5	80	μs
Disable Delay Time ($t_{pff50-90}$)	EN↓ to GATE↓, C_{GATE} = 0, see Figure 2	0.33	0.665	1	μs
nPG					
Delay (Deglitch) Time	Rising or falling edge	2	4	6	ms
GATE					
Fast Turn-Off Duration		9	13.5	18	μs
Turn-On Delay Time ($t_{prr50-50}$)	V_{CC} rising to GATE sourcing, see Figure 3		125	250	μs
SENSE					
Fast Turn-Off Duration		9	13.5	18	μs
Fast Turn-Off Delay Time ($t_{prf50-50}$)	$V_{(VCC-SENSE)}$ = 80mV, C_{GATE} = 0pF, see Figure 4		250		ns

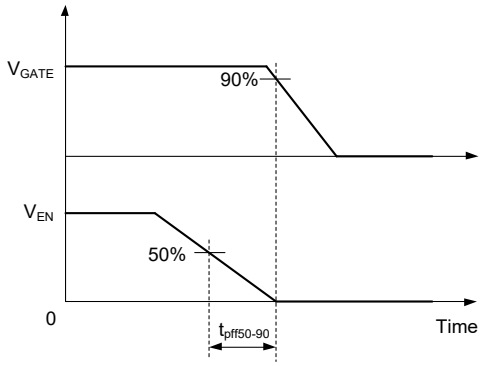


Figure 2. $t_{pff50-90}$ Timing Definition

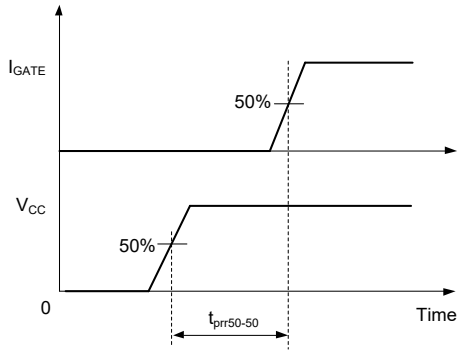


Figure 3. $t_{prr50-50}$ Timing Definition

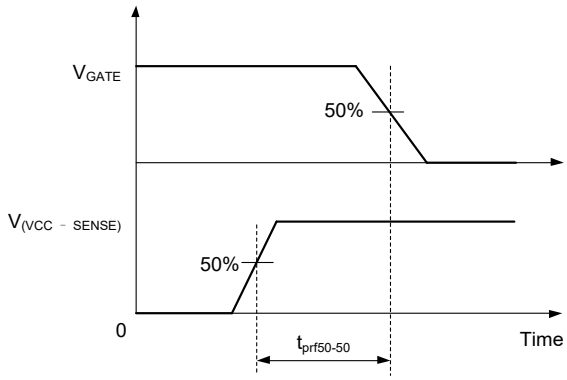
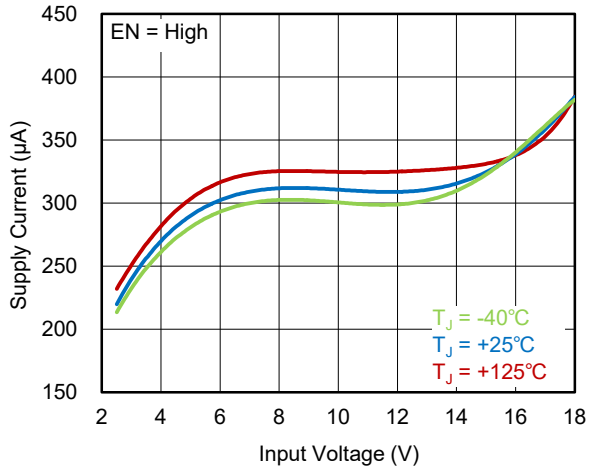


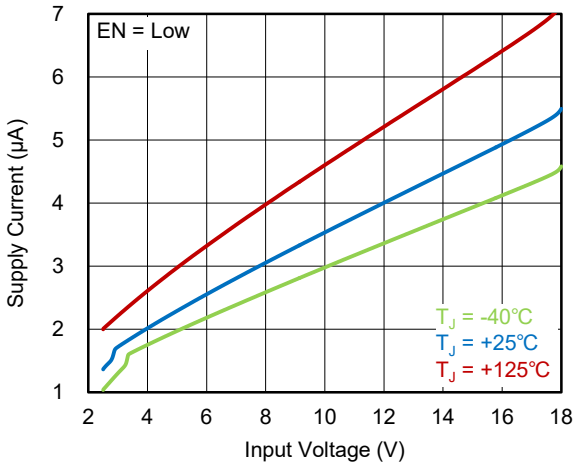
Figure 4. $t_{prf50-50}$ Timing Definition

TYPICAL PERFORMANCE CHARACTERISTICS

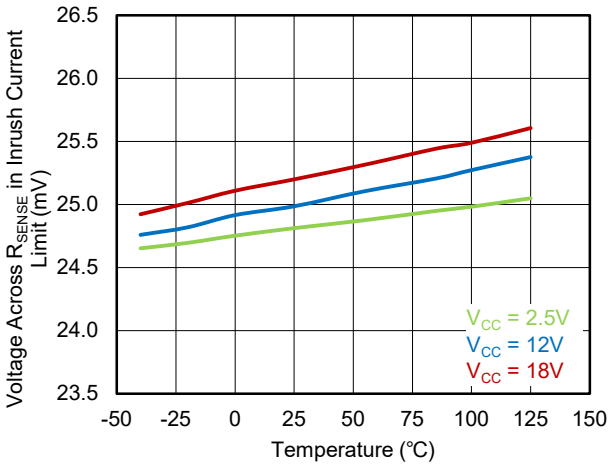
Supply Current vs. Input Voltage at Normal Operation



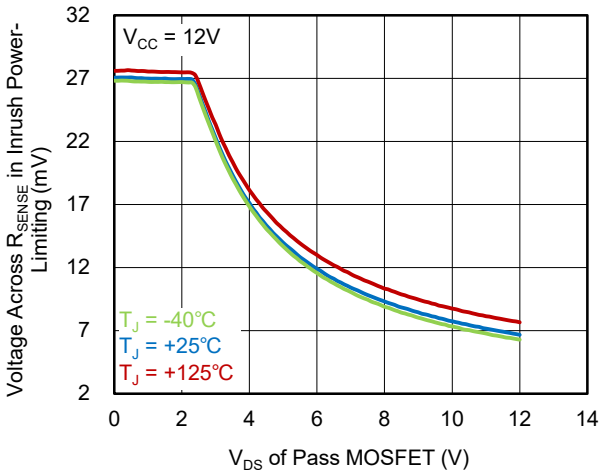
Supply Current vs. Input Voltage at Shutdown



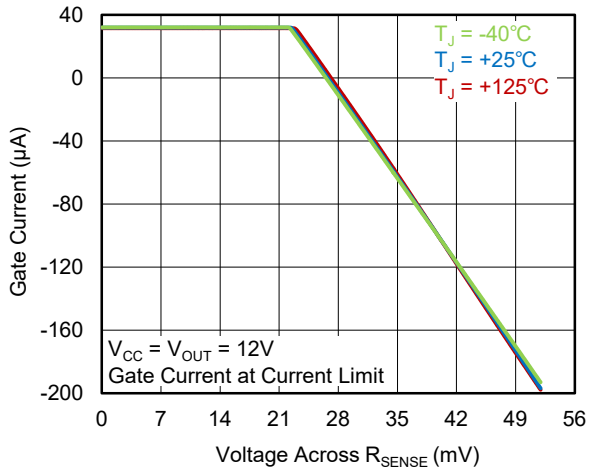
Voltage Across R_{SENSE} in Inrush Current Limit vs. Temperature



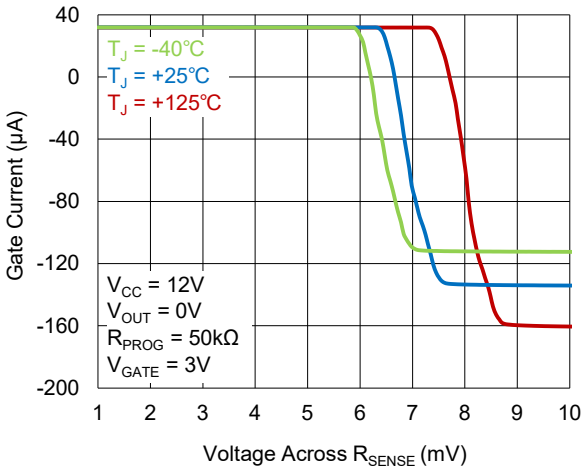
Voltage Across R_{SENSE} in Inrush Power-Limiting vs. V_{DS} of Pass MOSFET



Gate Current vs. Voltage Across R_{SENSE}

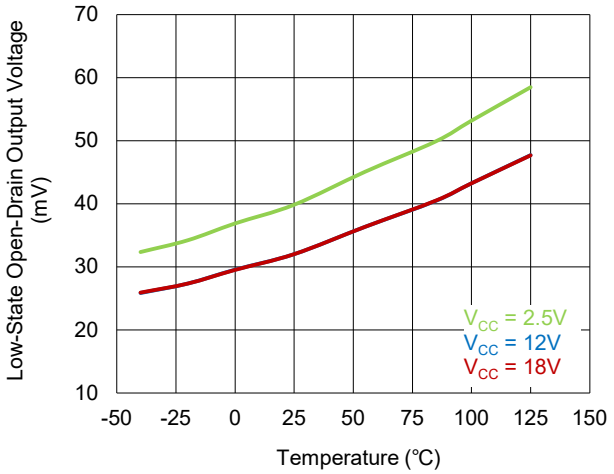


Gate Current vs. Voltage Across R_{SENSE}

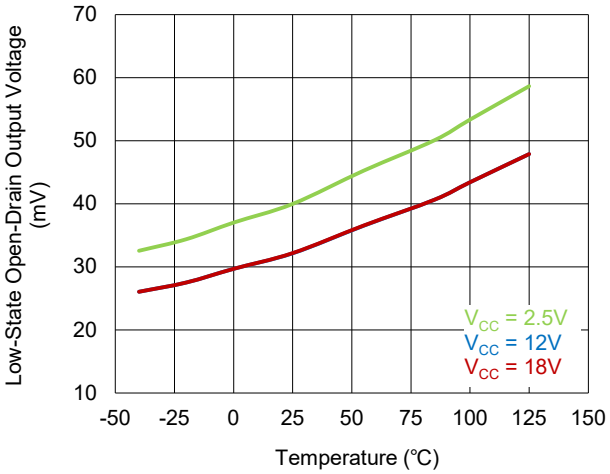


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

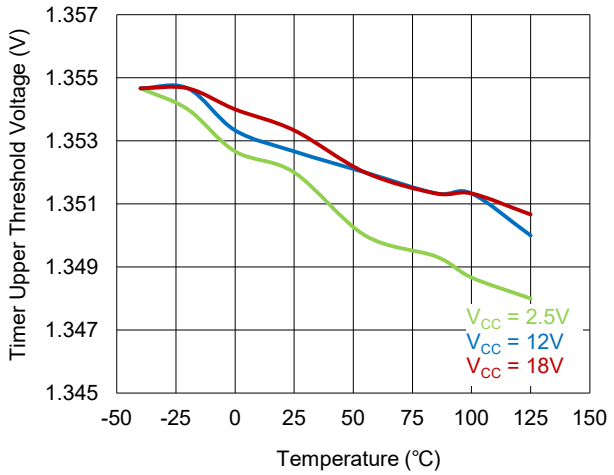
nPG Open-Drain Output Voltage in Low-State vs. Temperature



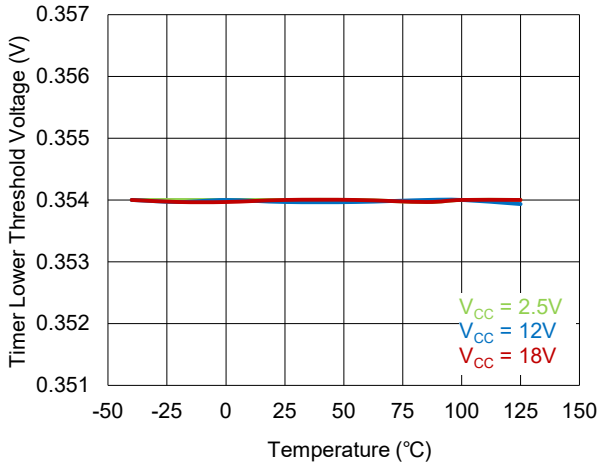
nFLT Open-Drain Output Voltage in Low-State vs. Temperature



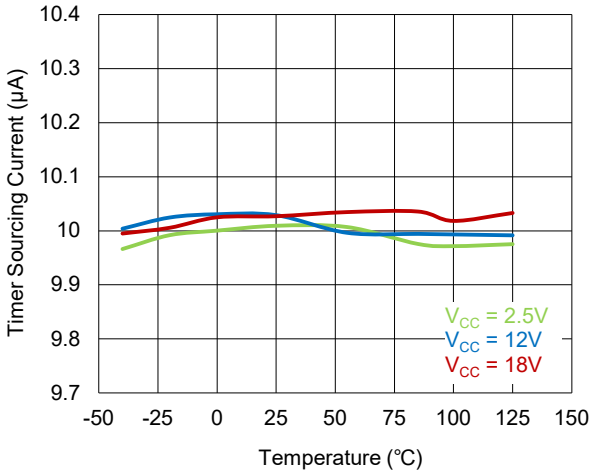
Timer Upper Threshold Voltage vs. Temperature



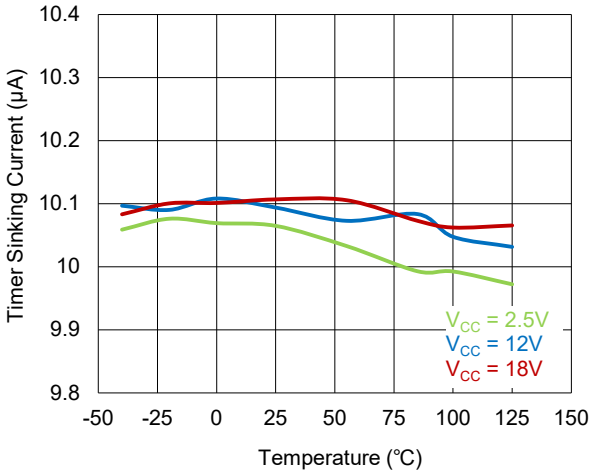
Timer Lower Threshold Voltage vs. Temperature



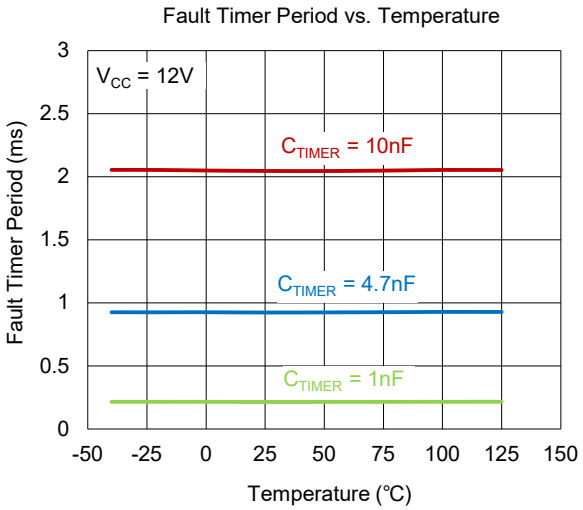
Timer Sourcing Current vs. Temperature

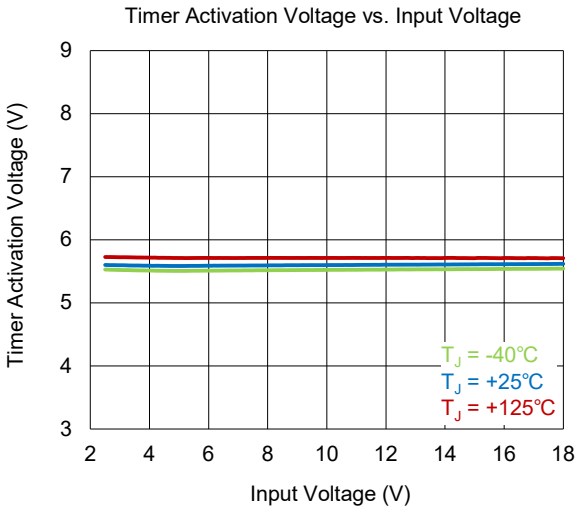


Timer Sinking Current vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)





FUNCTIONAL BLOCK DIAGRAM

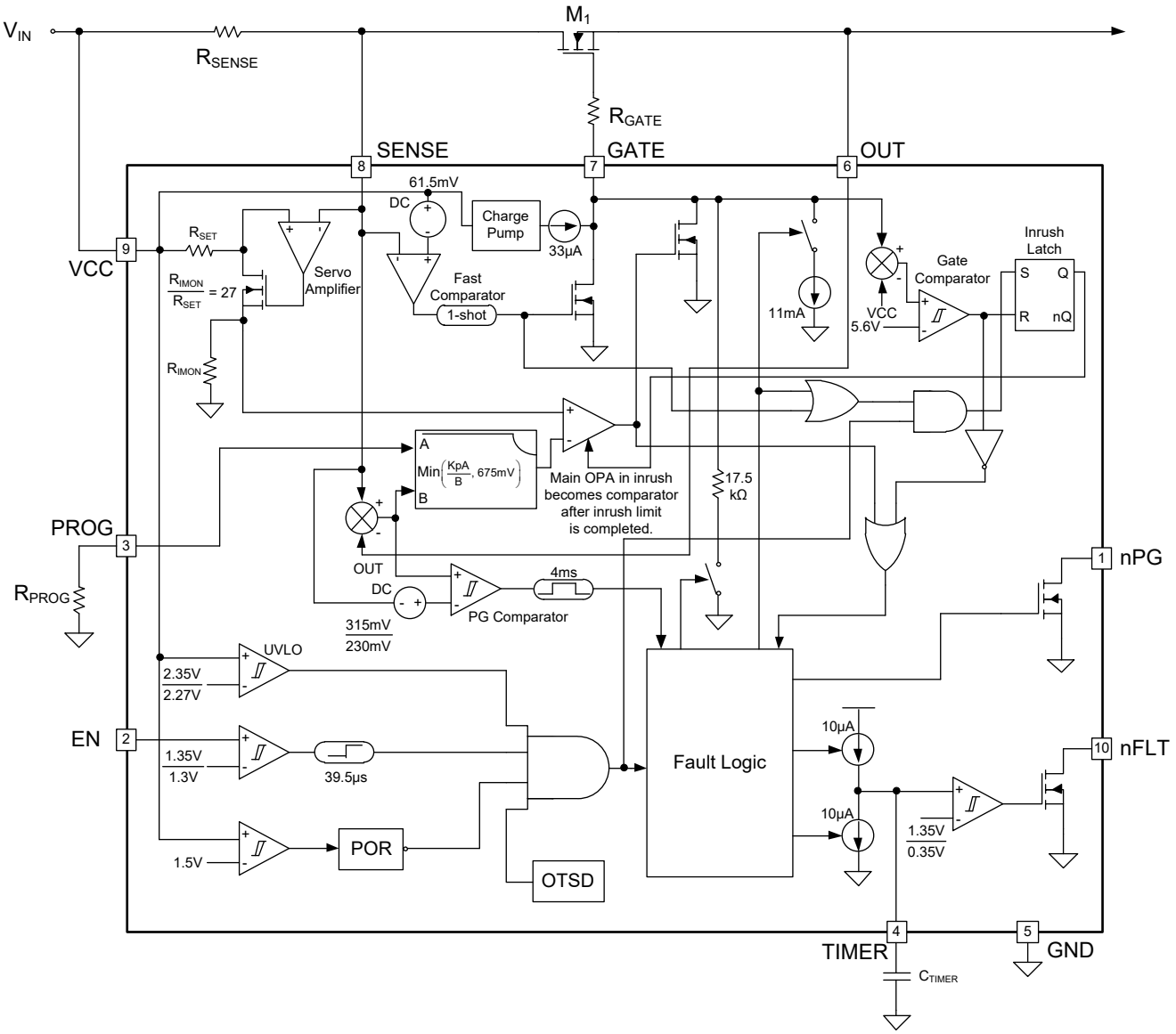


Figure 5. Block Diagram

DETAILED DESCRIPTION

The following description relies on the typical application circuit (12V/10A), as well as the functional block diagram in Figure 5.

EN

A voltage of 1.35V or higher is applied to this pin to enable the gate driver. The addition of an external resistor divider allows the EN pin to be used as an under-voltage monitor. Cycling EN low and then back to high resets the SGM25711B that has latched off due to a fault condition. This pin should not be left floating.

nFLT

The nFLT pin is assigned for SGM25711B. When the SGM25711B remains within the current limit long enough for the fault timer to expire, the low open-drain output will be pulled low. The SGM25711B operates in auto-retry mode. In auto-retry mode, a fault timeout first disables the external MOSFET (M_1), then waits for 16 cycles of timer charging and discharging, and finally tries to restart. This process repeats as long as the fault persists. The nFLT pin is pulled low whenever the M_1 is disabled by the fault timer. In a continuous fault, the nFLT waveform becomes a series of pulses. The nFLT pin does not assert if the M_1 is disabled by EN, OTSD, or UVLO. This pin can be left floating when not used.

GATE

This pin drives the gate of the M_1. A charge pump sources 33μA to enhance the M_1. A 13.5V clamp between GATE and VCC pins limits the gate-to-source voltage, because V_{CC} is very close to V_{OUT} in normal operation. During startup, a trans-conductance amplifier regulates the gate voltage of M_1 to provide inrush current limit. The TIMER pin charges timer capacitor (C_{TIMER}) with 10μA during the inrush. Inrush current is limited until the $V_{(GATE - VCC)}$ exceeds the timer activation voltage (5.6V for V_{CC} = 12V). Then the SGM25711B enters into circuit-breaker mode. When $V_{(GATE - VCC)}$ exceeds the timer activation voltage, the TIMER pin stops sourcing current and begins sinking current. In the circuit-breaker mode, the current flowing through the R_{SENSE} is compared with the current limit threshold derived from the MOSFET power-limiting scheme (see PROG section). If the current flowing through the R_{SENSE} exceeds the current limit threshold, then M_1 is turned off. The GATE pin is disabled by the following three conditions:

1. GATE is pulled down by an 11mA current source, when:
- The fault timer expires during an overload current fault ($V_{(VCC - SENSE)}$ > 25mV)
- V_{EN} is below its falling threshold
- V_{CC} drops below the UVLO threshold

2. GATE is pulled down by a 3.3Ω resistor when V_{EN} is below its falling threshold or when a hard output short occurs and $V_{(VCC - SENSE)}$ is greater than the fast-trip shutdown threshold (61.5mA). After fast-trip shutdown is complete, an 11mA sustaining current ensures that the M_1 remains off.

3. GATE is discharged by a 17.5kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold. GATE attempts a restart periodically in auto-retry mode.

No external resistor should be directly connected from GATE to GND or from GATE to OUT pins.

OUT

This pin allows the device to measure the drain-to-source voltage across the M_1. The power good indicator relies on this information as much as the power-limiting engine. The OUT pin should be protected from negative voltage transients by a clamping diode. A Schottky diode of 3A/40V in a SMC package is recommended as a clamping diode for high power applications. The OUT pin should be bypassed to GND with a low-impedance ceramic capacitor.

nPG

This active-low, open-drain output pulls low after the drain-to-source voltage of the MOSFET has fallen below 230mV and a 4ms deglitch delay has expired. It goes open-drain when V_{DS} exceeds 315mV. nPG assumes high-impedance status after a 4ms deglitch delay once V_{DS} of M_1 rises up, resulting from GATE being pulled to GND at any of the following conditions:

- An overload fault occurs ($V_{(VCC - SENSE)}$ > 25mV).
- A hard output short occurs, leading to $V_{(VCC - SENSE)}$ greater than the fast-trip shutdown threshold (61.5mV) has been exceeded.
- V_{EN} is below its falling threshold.
- V_{CC} drops below the UVLO threshold.
- The device temperature exceeds the OTSD threshold.

This pin can be left floating when not used.

DETAILED DESCRIPTION (continued)

GND

This pin is connected to system ground.

PROG

A resistor from this pin to GND sets the maximum power allowed in the M_1 during inrush. Do not apply a voltage to this pin. If the constant power-limiting is not desired, use a R_{PROG} resistor of 4.99kΩ. To set the maximum power, use Equation 1.

$$R_{PROG} = \frac{3500}{P_{LIM} \times R_{SENSE}} \quad (1)$$

To compute the power-limiting based on an existing $R_{PROG,}$ use Equation 2.

$$P_{LIM} = \frac{3500}{R_{PROG} \times R_{SENSE}} \quad (2)$$

where P_{LIM} is the allowed power-limiting of M_1. R_{SENSE} is the current sense resistor connected between the VCC pin and the SENSE pin. R_{PROG} is the resistor connected from the PROG pin to GND. Both R_{PROG} and R_{SENSE} are in Ω and P_{LIM} is in W. P_{LIM} is determined by the maximum allowed thermal stress of M_1, given by Equation 3.

$$P_{LIM} < \frac{T_{J(MAX)} - T_{C(MAX)}}{R_{\theta JC(MAX)}} \quad (3)$$

where $T_{J(MAX)}$ is the maximum desired transient junction temperature and $T_{C(MAX)}$ is the maximum case temperature prior to a start or restart. $R_{\theta JC(MAX)}$ is the junction-to-case thermal impedance of the pass MOSFET in units of ℃/W. Both $T_{J(MAX)}$ and $T_{C(MAX)}$ are in ℃.

SENSE

This pin connects to the negative terminal of R_{SENSE}. It sets the current limit by sensing the voltage across this resistor. The current limit I_{LIM} is set by Equation 4.

$$I_{LIM} < \frac{25mV}{R_{SENSE}} \quad (4)$$

A fast-trip shutdown occurs when $V_{(VCC - SENSE)}$ exceeds 61.5mV.

TIMER

A capacitor C_{TIMER} connected from the TIMER pin to GND determines the overload fault timing. When the overload occurs, the timer charges the C_{TIMER} with 10μA current, otherwise discharges the C_{TIMER} with 10μA current. When V_{TIMER} reaches 1.35V, the M_1 is turned off. This capacitor also determines the auto-retry period after a fault. A minimum timing capacitance of 1nF is recommended to ensure proper operation of the fault timer. The value of C_{TIMER} can be calculated from the desired fault time t_{nFLT}, use Equation 5.

$$C_{TIMER} = \frac{10\mu A}{1.35V} \times t_{nFLT} \quad (5)$$

The M_1 is disabled for 16 cycles of timer charging and discharging if the load current exceeds the current limit threshold or the fast-trip shutdown threshold. The TIMER pin is pulled to GND by a 7mA current source at the end of the 16^{th} cycle of charging and discharging. The M_1 is then re-enabled. The C_{TIMER} can also be discharged to GND by a 7mA current source whenever any of the following conditions:

- V_{EN} is below its falling threshold.
- V_{CC} drops below the UVLO threshold.

VCC

This pin performs three functions. First, it provides power to the integrated circuit. Second, it serves as an input to the power-on reset (POR) and under-voltage lockout (UVLO) functions. The VCC trace should connect directly to the positive terminal of R_{SENSE} to minimize the voltage sensing error. Bypass capacitor C_1, shown in the typical application circuit, see Figure 1, should be connected to the positive terminal of R_{SENSE}. A 0.1μF capacitor is recommended.

DETAILED DESCRIPTION (continued)

Device Functional Modes

The SGM25711B provides all the features needed for a positive hot swap controller. These features include:

- Under-voltage lockout
- Adjustable (system-level) enable
- Turn-on inrush limiting
- High-side gate drive for an external MOSFET
- MOSFET protection by power-limiting
- Adjustable overload timeout - also called an electronic circuit-breaker mode
- Charge-complete indicator for downstream DC/DC converter coordination
- Auto-retry mode

Figure 6 to Figure 8 and Figure 10 to Figure 12 respectively show the typical application (12V/10A) and oscilloscope plots. They demonstrate many of the functions described previously.

Board Plug-In

Figure 6 and Figure 7 illustrate the inrush current that flows when the hot swap board is inserted into the system bus under the control of the SGM25711B. The SGM25711B is held inactive for a short period while internal voltages are stable. During this period, GATE, PROG, TIMER are held low and nPG, nFLT are held open-drain. When the V_{CC} rail voltage exceeds approximately 1.5V, the power-on reset (POR) circuit initializes the SGM25711B and is ready for the startup process.

GATE, PROG, TIMER, nPG, and nFLT are released after the internal voltages have stabilized and the external EN (enable) thresholds have been exceeded. The device begins sourcing current from the GATE pin to turn on M_1. The SGM25711B monitors both the drain-to-source voltage across M_1 and the drain current passing through it. Based on these measurements, the SGM25711B limits the drain current by controlling the gate voltage, so that the power dissipation in the M_1 will not exceed the power-limiting set by the user. The current increases as the voltage across the M_1 decreases until finally the current reaches the current limit I_{LIM}.

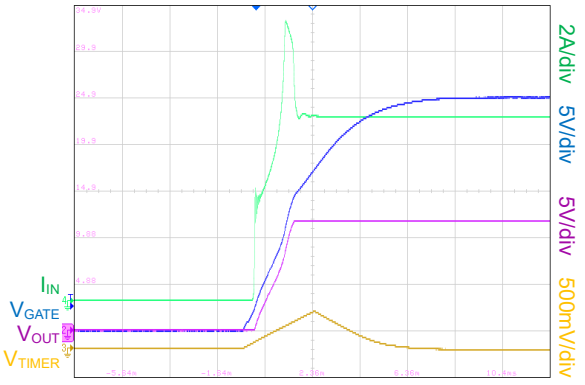


Figure 6. Inrush Mode at Hot Swap Circuit Insertion

Inrush Operation

After the initialization described in the Board Plug-In section of SGM25711B is completed and EN is active, GATE pin begins sourcing current, V_{GATE} starts increasing. When the V_{GATE} reaches the threshold voltage of M_1, the current flows into the output capacitor of the device. When this current exceeds the limit set by the power-limiting engine, the gate voltage of M_1 is regulated by a feedback loop to keep the M_1 current under control. A more complete explanation of the power-limiting scheme is given in the Action of the Constant Power Engine section. When GATE pin begins sourcing current, the TIMER pin begins to charge the timing capacitor (C_{TIMER}) with an approximate 10μA current. The TIMER pin continues to charge C_{TIMER} until $V_{(GATE - VCC)}$ reaches the timer activation voltage (5.6V for V_{CC} = 12V). The TIMER then begins to discharge C_{TIMER} with an approximate 10μA current. The inrush mode is finished. If the V_{TIMER} exceeds its upper threshold of 1.35V before $V_{(GATE - VCC)}$ reaches the timer activation voltage, the GATE pin is pulled to GND and the hot swap circuit enters the auto-retry mode.

The power-limiting feature is disabled once the inrush operation is finished and the hot swap circuit enters the circuit-breaker mode. Once the load exceeds the current limit threshold, the SGM25711B will turn off M_1 after a fault timer period.

DETAILED DESCRIPTION (continued)

Action of the Constant Power Engine

Figure 7 illustrates the operation of the constant power engine during startup. The circuit used to generate the waveforms of Figure 7 is programmed to a power-limiting of 54W by means of the resistor connected between PROG and GND pins. At the moment, current begins to flow through the MOSFET, a 12V voltage appears across it (V_{CC} = 12V), and the constant power engine therefore allows a current of 4.5A (equal to 54W divided by 12V) to flow. This current increases in inverse ratio as the drain-to-source voltage decreases, so as to maintain a constant dissipation of 54W. The constant power engine adjusts the current by altering the reference signal fed to the current limit amplifier. The lower part of Figure 8 shows the measured power dissipated within the MOSFET, labeled FET PWR, remaining substantially constant during this period of operation, which ends when the current through the MOSFET reaches the current limit (I_{LIM}). This constant power engine allows the MOSFET to operate near its maximum SOA, thus reducing the startup time and minimizing the size and cost of the required MOSFET.

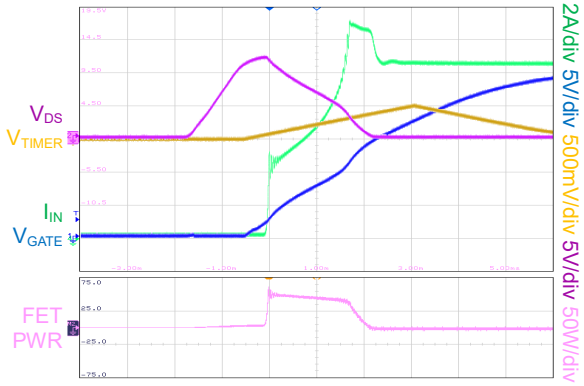


Figure 7. Computation of M_1 Power Stress during Startup

Circuit-Breaker and Fast-Trip

By sensing the voltage across R_{SENSE}, the SGM25711B monitors load current. The SGM25711B offers two limit thresholds: a current limit threshold and a fast-trip shutdown threshold.

The circuit-breaker mode and fast-trip turn-off are shown in Figure 8 through Figure 11.

Figure 8 shows the behavior of the SGM25711B when the load current is above the current limit but less than the fast-trip shutdown threshold. When the load current exceeds the current limit threshold, the gate voltage is regulated to limit the current passing through R_{SENSE} to the settled current limit value. Meanwhile an approximate 10μA begins to charge C_{TIMER}. If the V_{TIMER} reaches 1.35V, the M_1 will be turned off. The SGM25711B commences a restart cycle, the fault pin nFLT pulls low to signal a fault condition. This turn-off scheme is sometimes called an electronic circuit-breaker mode.

The fast-trip shutdown threshold protects the system from a severe overload or a permanent hard short. When the voltage across the sense resistor (R_{SENSE}) exceeds the fast-trip shutdown threshold, the GATE pin immediately pulls the M_1 gate to ground with an approximately resistor of 3.2Ω. This extremely rapid turn-off may generate destructive transient in the system, in which case the turn-off current can be adjusted by using a low value resistor inserted between the GATE pin and the MOSFET gate. The fast-trip circuit holds the MOSFET off for a few ms, after which the gate voltage ramps up slowly, the current limit feedback loop will take over the gate control of M_1. Then the SGM25711B operates in auto-retry mode. Figure 10 and Figure 11 illustrate the behavior of the system implementing SGM25711B when the current exceeds the fast-trip shutdown threshold.

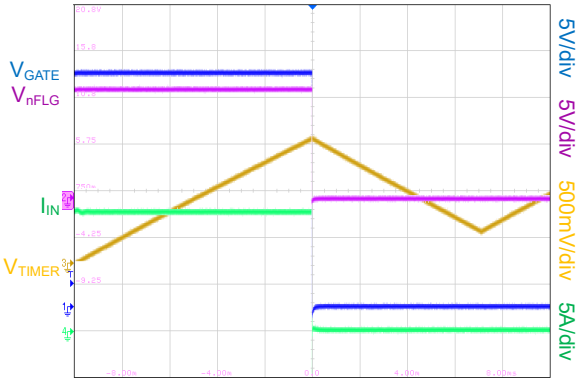


Figure 8. Circuit-Breaker Mode during Overload

DETAILED DESCRIPTION (continued)

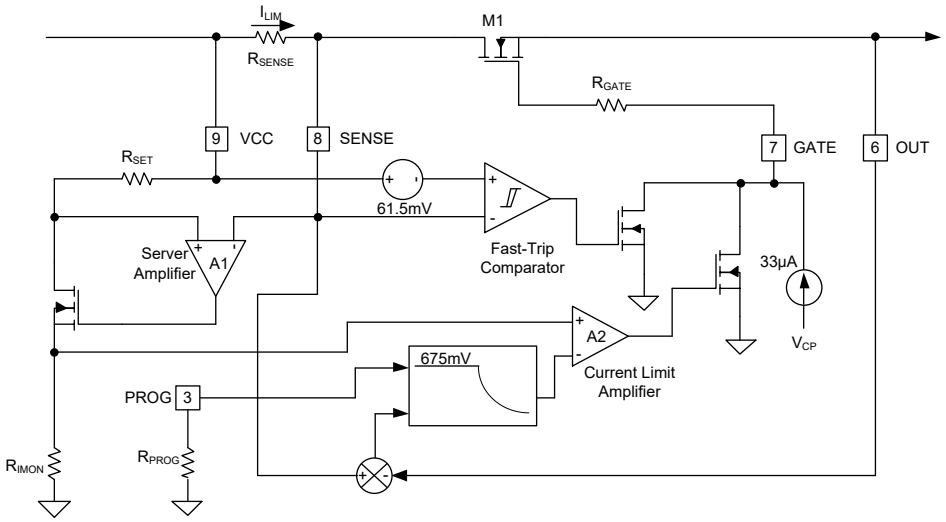
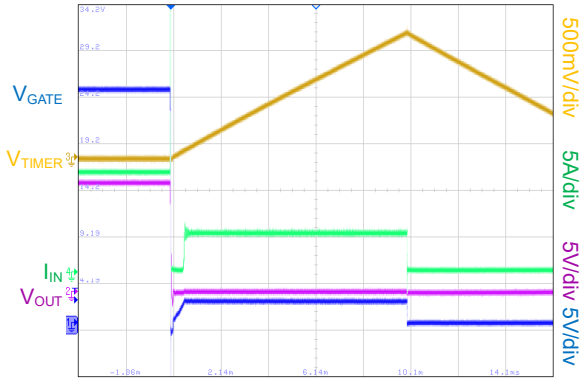
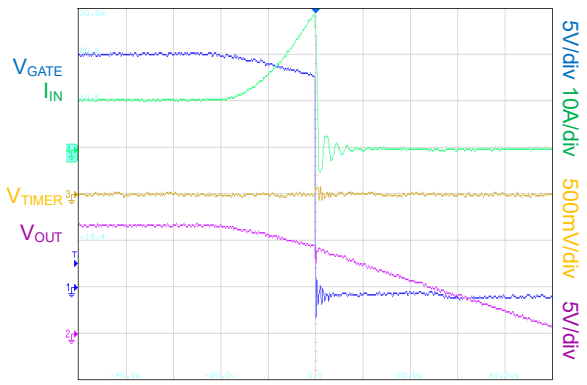


Figure 9. Partial Diagram of the SGM25711B with Selected External Components



Time (2ms/div)

Figure 10. Current Limit during Output Load Short-Circuit Condition (Overview)

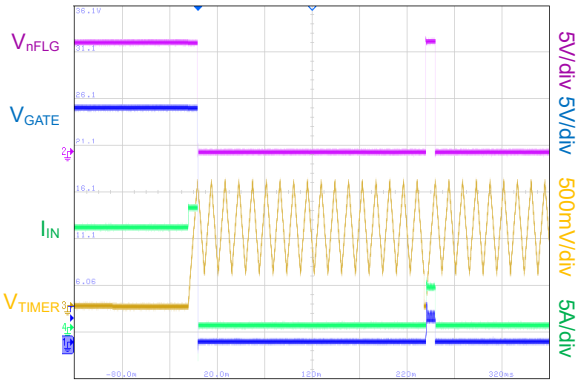


Time (10μs/div)

Figure 11. Current Limit during Output Load Short-Circuit Condition (Onset)

Auto-Retry

The SGM25711B will auto retry after a fault has caused it to turn off the M_1. Internal circuits control C_{TIMER} to count 16 cycles before re-enabling M_1 as shown in Figure 12. This sequence repeats if the fault persists. The timer has a 1:1 charge-to-discharge current ratio. For the first cycle, the TIMER pin starts from 0V and rises to the upper threshold of 1.35V and then falls to 0.35V. For the following 16 cycles, 0.35V is used as the lower threshold. This small duty cycle often reduces the average short-circuit power dissipation to the normal operation level and eliminates special thermal considerations for the persistent output short.



Time (50ms/div)

Figure 12. Auto-Retry Cycle Timing

DETAILED DESCRIPTION (continued)

nPG, nFLT and TIMER Operations

The nPG provides a deglitched indication of end-of-inrush based on the voltage across M_1. nPG is used to prevent a downstream power supply from operating while its input capacitor C_{OUT} is still charging. nPG goes active low about 4ms after C_{OUT} is charged. This delay allows M_1 to fully turn on before the downstream power supply starts up.

Care should be taken to ensure that the MOSFET on-resistance is small enough to ensure that the voltage drop across this transistor is less than the minimum power good threshold of 235mV. After the hot swap circuit successfully starts up, as long as the drain-to-source voltage of M_1 exceeds its upper threshold of 315mV, nPG can return to the high-impedance state, thus sending a warning flag to the downstream power supply. This flag may occur as a result of overload fault, output short fault, input over-voltage, higher die temperature, or the gate shutdown by UVLO and EN.

The nFLT indicates the set fault timer period expired. When the load current exceeds the programmed current limit (not the fast-trip shutdown threshold), an approximate 10μA begins to charge the C_{TIMER}, and the fault timer starts. When the voltage of C_{TIMER} reaches the upper threshold of V_{TIMER} (1.35V), nFLT pulls low. Otherwise, nFLT keeps a high-impedance state.

The fault timer is the charging time of C_{TIMER} from 0V to its upper threshold of 1.35V. The fault timer begins to count under any of the following conditions:

1. In the inrush mode, the device begins to charge the C_{TIMER} when M_1 is enabled. When $V_{(GATE - VCC)}$ exceeds the timer activation voltage (see the Inrush Operation section), the device begins to discharge the C_{TIMER}. If $V_{(GATE - VCC)}$ does not reach the timer activation voltage before V_{TIMER} reaches 1.35V, then the SGM25711B turns off the M_1. After the MOSFET is turned off, the timer goes into auto-retry mode.

2. In an overload fault, the device begins to charge the C_{TIMER} when the load current exceeds the programmed current limits. When the timer capacitor voltage reaches its upper threshold of 1.35V, from the device begins to discharge the $C_{TIMER,}$ and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into auto-retry mode.

3. In output short fault, the device begins to charge the C_{TIMER} when the load current exceeds the programmed current limits following a fast-trip shutdown of M_1. When the timer capacitor voltage reaches its upper threshold of 1.35V, the device begins to discharge the C_{TIMER}, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into auto-retry mode.

If the load current drops below the programmed current limit within the fault timer period, V_{TIMER} decreases and the pass MOSFET fully turns on again.

If the timer capacitor reaches the upper threshold of 1.35V, then timer charges and discharges C_{TIMER} between the lower threshold of 0.35V and the upper threshold of 1.35V for 16 cycles before the SGM25711B attempts to restart. The TIMER pin is pulled to GND at the end of the 16^{th} cycle of charging and discharging and then ramps from 0V to 1.35V for the initial half-cycle in which the GATE pin sources current. This periodic pattern is stopped once the overload fault is removed or the SGM25711B is disabled by UVLO or EN.

Over-Temperature Shutdown (OTSD)

The SGM25711B includes a built-in over-temperature shutdown circuit. If the die temperature exceeds approximately +145℃, the device will turn off the M_1 and nFLT, nPG pins go to high-impedance states. Normal operation resumes once the die temperature has fallen approximately 15℃.

Startup of Hot Swap Circuit by VCC or EN

When the V_{CC} is above UVLO upper threshold and EN is higher than its upper threshold, the device will source current to the GATE pin. After an inrush period, SGM25711B fully turns on M_1.

By any of the following conditions, the M_1 can be disabled: UVLO, EN, load current above current limit threshold, output hard short, or OTSD. Three separate conditions pull down the GATE pin:

1. GATE is pulled down by an 11mA current source when any of the following occurs.

- The fault timer expires during an overload current fault ($V_{(VCC - SENSE)}$ > 25mV).
- V_{EN} is below its falling threshold.
- V_{CC} drops below the UVLO threshold.

2. GATE is pulled down by an N-MOSFET (3.2Ω when V_{DS} = 0.2V) for 13.5μs when a output hard output short occurs and $V_{(VCC - SENSE)}$ is greater than the fast-trip shutdown threshold (61.5mV). After fast-trip shutdown is complete, an 11mA sustaining current ensures that the external MOSFET remains off.

3. GATE is discharged by a 17.5kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

APPLICATION INFORMATION

The SGM25711B is a hot swap controller used to manage inrush current and provide load fault protection. When designing hot swap solutions, three key scenarios should be considered:

- Startup
- Output of a hot swap is shorted to ground when the hot swap is on.
- Powering-up a board when the output and ground are shorted. This is usually called a start-into-short.

Each of these scenarios places stress on the hot swap MOSFET. Take special care when designing the hot swap circuit to keep the MOSFET within its SOA. The following design example is provided as a guide.

Typical Application

This section provides an application example utilizing power limited startup and MOSFET SOA protection. The design parameters are listed in the Design Requirements section and represent a more moderate level of fault current.

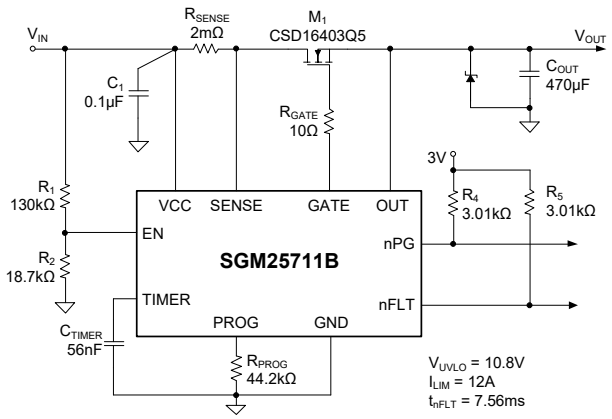


Figure 13. Typical Application (12V at 10A)

Design Requirements

For this design example, use the parameters shown in Table 1.

Table 1. Design Parameters

Parameter	Value
Input Voltage	12V ± 2V
Maximum Operating Load Current	10A
Operating Temperature	+20℃ to +50℃
Fault Trip Current	12A
Load Capacitance	470µF

Power-Limiting Startup

This design example assumes a 12V system voltage with an operating tolerance of ±2V. The rated load current is 10A, corresponding to a DC load of 1.2Ω. If the current exceeds 12A, then the controller should shut down and then attempt to restart. Ambient temperatures may range from +20°C to +50°C. The load has a minimum input capacitance of 470µF. Figure 14 shows a simplified system block diagram of the proposed application.

This design procedure seeks to control the junction temperature of M_1 under both static and transient conditions by proper selection of package, cooling, R_{DSON}, current limit, fault timeout, and power-limiting. The design procedure further assumes that a unit running at full load and maximum ambient temperature experiences a brief input power interruption sufficient to discharge C_{OUT}, but short enough to keep M_1 from cooling. A full C_{OUT} recharge then takes place. Adjust this procedure to fit your application and design criteria.

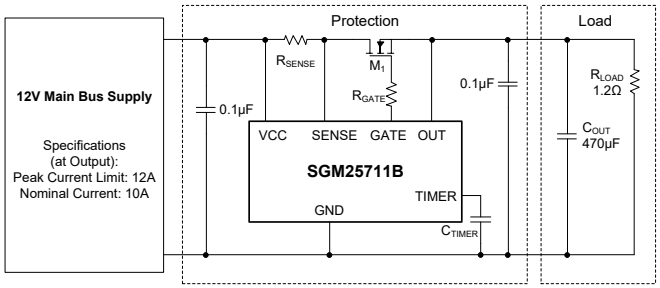


Figure 14. Simplified Block Diagram of the System Constructed in the Design Example

APPLICATION INFORMATION (continued)

STEP 1. Choose R_{SENSE}

From the SGM25711B Electrical Characteristics section, the current limit threshold voltage is around 25mV. A resistance of 2mΩ is selected for the peak current limit of 12A, while dissipating only 200mW at the rated 10A current (see Equation 6). This represents a 0.17% power loss.

$$R_{SENSE} = \frac{V_{(VCC\ -\ SENSE)}}{I_{LIM}}$$

therefore,

$$R_{SENSE} = \frac{25mV}{12A} \approx 2m\Omega \quad (6)$$

STEP 2. Choose M_1

The next design step is to select M_1. The SGM25711B is designed to use a MOSFET with a gate-to-source voltage rating of 20V.

Devices with lower gate-to-source voltage ratings can be used if a Zener diode is connected so as to limit the maximum gate-to-source voltage across the transistor.

The next factor to consider is the drain-to-source voltage rating of the MOSFET. Although the MOSFET only sees 12V DC, it may experience much higher transient voltages during extreme conditions, such as the abrupt shutoff that occurs during a fast-trip. A TVS may be required to limit inductive transients under such conditions. A transistor with a $V_{DS(MAX)}$ rating of at least twice the nominal input power supply voltage is recommended regardless of whether a TVS is used or not.

Next select the on-resistance of the transistor (R_{DSON}). The maximum on-resistance must not generate a voltage greater than the minimum power good threshold voltage of 235mV. Assuming a current limit of 12A, a maximum R_{DSON} of 19mΩ is required. Also consider the effect of R_{DSON} upon the maximum operating temperature $T_{J(MAX)}$ of the MOSFET. Equation 7 computes the value of $R_{DSON(MAX)}$ at a junction temperature of $T_{J(MAX)}$. Most manufacturers list $R_{DSON(MAX)}$ at +25°C and provide a derating curve from which values at other temperatures can be derived. Use Equation 7 to compute the maximum allowable on-resistance, $R_{DSON(MAX)}$.

$$R_{DSON(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{I_{MAX}^{\ 2} \times R_{\theta JA}}$$

therefore,

$$R_{DSON(MAX)} = \frac{150℃\ -\ 50℃}{(12A)^2 \times 51℃/W} = 13.6m\Omega \quad (7)$$

Taking these factors into consideration, the CSD16403Q5 was selected for this example. This transistor has a $V_{GS(MAX)}$ rating of 16V, a $V_{DS(MAX)}$ rating of 25V, and a maximum R_{DSON} of 2.8mΩ at room temperature. During normal circuit operation, the MOSFET can have up to 10A flowing through it. The power dissipation of the MOSFET equates to 0.24W and a 9.6℃ rise in junction temperature. This is well within the datasheet limits for the MOSFET. The power dissipated during a fault (output short) is far larger than the steady-state power. The power handling capability of the MOSFET must be checked during fault conditions.

STEP 3. Choose Power-Limiting Value (P_{LIM}) and R_{PROG}

The M_1 dissipates large amounts of power during inrush. The power-limiting of the SGM25711B should be set to prevent the die temperature from exceeding a short-term maximum temperature ($T_{J(MAX)2}$). The short-term $T_{J(MAX)2}$ could be set as high as 130℃ while still leaving ample margin to the usual manufacturer's rating of 145℃. Equation 8 is an expression for calculating P_{LIM}.

$$P_{LIM} \le 0.8 \times \frac{T_{J(MAX)2} - \left[\left(I_{MAX}^{\ 2} \times R_{DSON} \times R_{\theta CA}\right) + T_{A(MAX)}\right]}{R_{\theta JC}}$$

therefore,

$$P_{LIM} \le 0.8 \times \frac{130℃ - \left[\left(12A^2 \times 0.002\Omega \times (51℃/W\text{-}1.8℃/W\right) + 50℃\right]}{1.8℃/W} = 29.3W \quad (8)$$

where $R_{\theta JC}$ is the junction-to-case thermal resistance of the MOSFET, R_{DSON} is the resistance at the maximum operating temperature, and the factor of 0.8 represents the tolerance of the constant power engine. For an ambient temperature of 50℃, the calculated maximum P_{LIM} is 29.3W. From Equation 2, a 59.7kΩ, 1% resistor is selected for R_{PROG} (see Equation 9).

$$R_{PROG} = \frac{3500}{P_{LIM} \times R_{SENSE}}$$

therefore,

$$R_{PROG} = \frac{3500}{29.3W \times 0.002\Omega} = 59.7k\Omega \quad (9)$$

APPLICATION INFORMATION (continued)

STEP 4. Choose Output Voltage Rising Time (t_{ON}), C_{TIMER}

The maximum output voltage rise time (t_{ON}), set by the timer capacitor (C_{TIMER}) must suffice to fully charge the load capacitance (C_{OUT}) without triggering the fault circuitry. Equation 10 defines t_{ON} for two possible inrush cases.

Assuming that only the load capacitance draws current during startup.

$$t_{ON} = \begin{cases} \frac{C_{OUT} \times P_{LIM}}{2 \times I_{LIM}^2} + \frac{C_{OUT} \times V_{CC(MAX)}^2}{2 \times P_{LIM}} - \frac{C_{OUT} \times V_{CC(MAX)}}{I_{LIM}} & \text{if } P_{LIM} < I_{LIM} \times V_{CC(MAX)} \\ \frac{C_{OUT} \times V_{CC(MAX)}}{I_{LIM}} & \text{if } P_{LIM} > I_{LIM} \times V_{CC(MAX)} \end{cases}$$

therefore,

$$t_{ON} = \frac{470\mu F \times 29.3W}{2 \times (12A)^2} + \frac{470\mu F \times (12V)^2}{2 \times 29.3W} - \frac{470\mu F \times 12V}{12A} = 0.73ms \quad (10)$$

The next step is to determine the minimum fault-timer period. In Equation 10, the output rise time is t_{ON}. This is the amount of time it takes to charge the output capacitor up to the final output voltage. However, the fault timer uses the difference between the input voltage and the gate voltage to determine if the SGM25711B is still in inrush limit. The fault timer continues to run until V_{GS} rises 5.6V (for V_{CC} = 12V) above the input voltage. Some additional time must be added to the charge time to account for this additional gate voltage rise. The minimum fault time can be calculated using Equation 11.

$$t_{nFLT} = t_{ON} + \frac{5.6V \times C_{ISS}}{I_{GATE}}$$

therefore,

$$t_{nFLT} = 0.73ms + \frac{5.6V \times 2040pF}{20\mu A} = 1.3ms \quad (11)$$

where C_{ISS} is the MOSFET input capacitance, I_{GATE} is the minimum gate sourcing current of SGM25711B, or 20μA. Using the example parameters in Equation 11 and the CSD16403Q5 leads to a minimum fault time of 1.3ms. This time is derived considering the tolerances of C_{OUT}, C_{ISS}, I_{LIM}, P_{LIM}, I_{GATE}, and $V_{CC(MAX)}$. The fault timer must be set to a value higher than 1.3ms to avoid turning off during startup, but lower than any maximum fault time limit determined by the SOA curve derated for operating junction temperature.

For this example, select 7ms to allow for variation of system parameters such as temperature, load, component tolerance, and input voltage. The timing capacitor is calculated in Equation 12 as 52nF. Selecting the next-highest standard value, 56nF, yields a 7.56ms fault time (see Equation 12).

$$C_{TIMER} = \frac{10\mu A}{1.35V} \times t_{nFLT}$$

therefore,

$$C_{TIMER} = \frac{10\mu A}{1.35V} \times 7ms = 52nF \quad (12)$$

STEP 5. Calculate the Auto-Retry Mode Duty Ratio

In auto-retry mode, the SGM25711B is on for 1 charging cycle and off for 16 charge and discharge cycles, as can be seen in Figure 12. The first C_{TIMER} charging cycle is from 0V to 1.35V, which gives 7.56ms. The first C_{TIMER} discharging cycle is from 1.35V to 0.35V, which gives 5.6ms. Therefore, the total time is 7.56ms + 33 × 5.6ms = 192.36ms. As a result, the auto-retry mode duty ratio is 7.56ms/192.36ms = 3.93%.

STEP 6. Select R_1 and R_2 for Under-Voltage

Next, select the values of the UV resistors, R_1 and R_2, as shown in Figure 1. From the SGM25711B electrical specifications, V_{ENTH} = 1.35V. The V_{UV} is the under-voltage trip voltage, which for this example equals 10.7V.

$$V_{ENTH} = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad (13)$$

Assume R_1 is 130kΩ and use Equation 13 to solve for the R_2 value of 18.7kΩ.

STEP 7. Choose R_{GATE}, R_4, R_5 and C_1

In the typical application diagram on the page 1, the gate resistor (R_{GATE}) is intended to suppress high frequency oscillations. A resistor of 10Ω will serve for most applications, but if M_1 has a C_{ISS} below 200pF, then 33Ω is recommended. Applications with larger MOSFETs and very short wiring may not require R_{GATE}. R_4 and R_5 are required only if nPG and nFLT are used; these resistors serve as pull-ups for the open-drain output drivers. The current sunk by each of these pins should not exceed 2mA (see the Recommended Operating Conditions section). C_1 is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise while in the disabled state. Where acceptable, a value in the range of 0.001μF to 0.1μF is recommended.

APPLICATION INFORMATION (continued)

Use of nPG

Use the nPG pin to control and coordinate a downstream DC/DC converter. If this is not done, then a long time delay is needed to allow C_{OUT} to fully charge before the converter starts. An undesirable latch-up condition can be created between the SGM25711B output characteristic and the DC/DC converter input characteristic if the converter starts while C_{OUT} is still charging, the nPG pin is a way to avoid this.

Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during a current limit event. The OUT pin ratings can be satisfied by connecting a diode from OUT pin to GND. The diode should be selected to control the negative voltage at the full short-circuit current. Schottky diodes are generally recommended for this application.

Gate Clamp Diode

The SGM25711B has a relatively well-regulated gate voltage of 12V to 15.5V with a supply voltage V_{CC} higher than 4V. A small clamp Zener from GATE to source of M_1 is recommended if V_{GS} of M_1 is rated below 12V. A series resistance of several hundred ohms or a series silicon diode is recommended to prevent the output capacitance from discharging through the gate driver to ground.

High-Gate-Capacitance Applications

Gate voltage overstress and abnormally large fault current spikes can be caused by large gate capacitance. An external gate clamp Zener diode is recommended to assist the internal Zener if the total gate capacitance of M_1 exceeds about 4000pF.

Bypass Capacitors

It is a good practice to provide low-impedance ceramic capacitor bypassing of the VCC and OUT pins. Values in the range of 10nF to 1μF are recommended. Some system topologies are insensitive to the values of these capacitors; however, some are not and require minimization of the value of the bypass capacitor. Input capacitance on a plug-in board may cause a large inrush current as the capacitor charges through the low-impedance power bus when inserted. This stresses the connector contacts and causes a short voltage sag on the input bus. Small amounts of capacitance (10nF to 0.1μF) are often tolerable in these systems.

Output Short-Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in this datasheet. Every setup is different.

Using Soft-Start with SGM25711B

In some applications, it may be desired to have a constant dV/dt ramp on the output of the SGM25711B to ensure a constant inrush current. This is often accomplished by adding a capacitor from GATE to GND as shown in Figure 15. This limits the gate ramp speed, which in turn limits the ramp of the output.

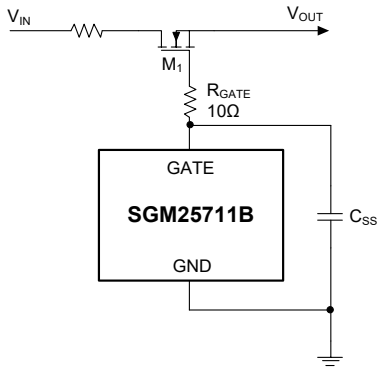


Figure 15. Simplified Diagram for Using Soft-Start

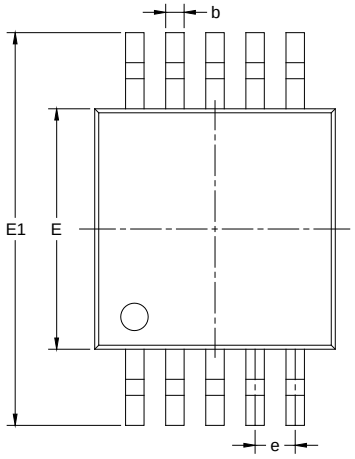
Due to the nature of the timer and the gate driver, there are several considerations that must be taken into account when using this type of a design.

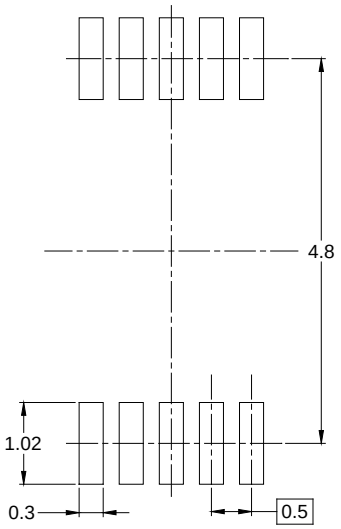
Power Supply Recommendations

Use a 10nF to 1μF ceramic capacitor to bypass the VCC pin to GND. When the input bus power feed is inductive, then a transient voltage suppressor (TVS) may also be required.

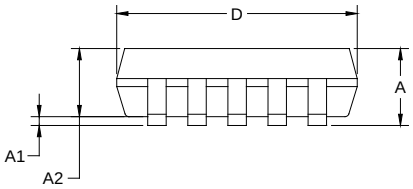
PACKAGE OUTLINE DIMENSIONS

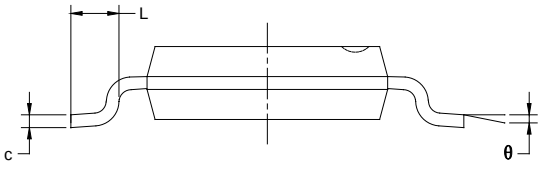
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



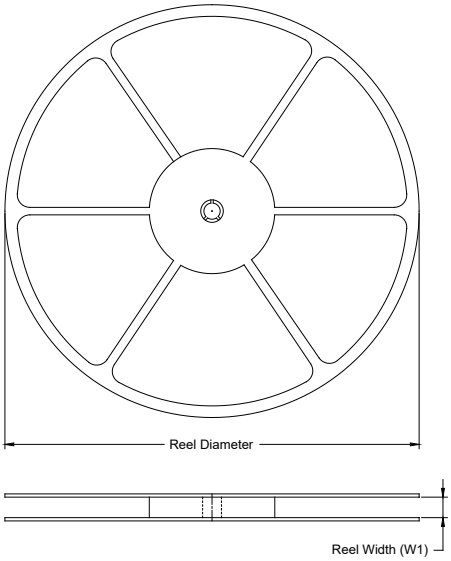


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

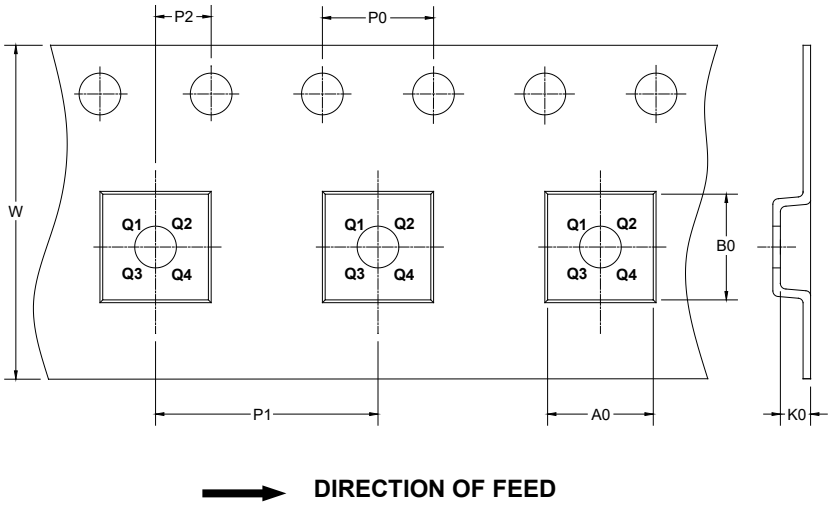
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



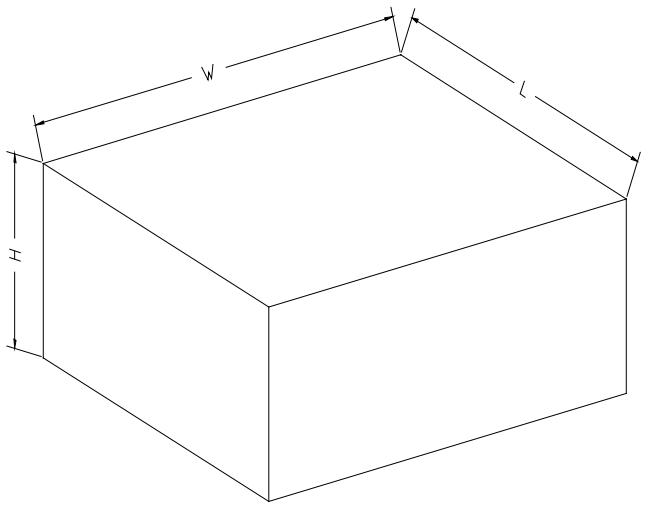
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13″	12.4	5.20	3.30	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002