# TMP275-Q1 Automotive Grade ±0.5°C Temperature Sensor with I$^2$C and SMBus Interface in Industry-Standard LM75 Form Factor and Pinout

## 1 Features

- AEC-Q100 Qualified with:
  - Temperature Grade 1: –40°C to +125°C Ambient Operation Temperature Range
  - HBM ESD Classification Level 2
  - CDM ESD Classification Level C6
- High Accuracy:
  - ±0.5°C (Maximum) from −20°C to +100°C
  - ±1°C (Maximum) from −40°C to +125°C
- Low Quiescent Current:
  - 50 µA (Typical)
  - 0.1 µA (Standby)
- Resolution: 9 to 12 Bits, User-Selectable
- Digital Output: SMBus™, Two-Wire, and I$^2$C Interface Compatibility
- 8 I$^2$C, SMBus Addresses
- Wide Supply Range: 2.7 V to 5.5 V
- Small 8-Pin VSSOP and SOIC Packages
- No Specified Power-Up Sequence Required, Two-Wire Bus Pullups Can Be Enabled Before V+

## 2 Applications

- Climate Controls
- Infotainment Processor Management
- Airflow Sensors
- Battery Control Units
- Engine Control Units
- UREA Sensors
- Water Pumps
- HID Lamps
- Airbag Control Units

## 3 Description

The TMP275-Q1 is a ±0.5°C, accurate integrated digital temperature sensor with a 12-bit, analog-to-digital converter (ADC) that can operate on a supply voltage as low as 2.7 V and is pin- and register-compatible with the Texas Instruments' LM75, TMP75, TMP75B, and TMP175 devices. The TMP275-Q1 device is available in 8-pin SOIC and VSSOP packages and requires no external components to sense temperature. The device is capable of reading temperatures with a maximum resolution of 0.0625°C (12 bits) and as low as 0.5°C (9 bits), thus allowing the user to maximize efficiency by programming for higher resolution or faster conversion time. The device is specified over the temperature range of –40°C to +125°C.
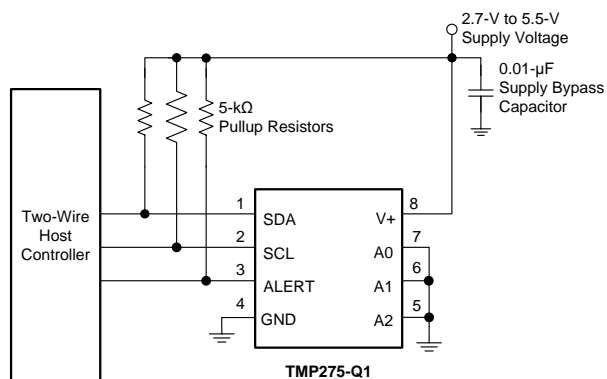
The TMP275-Q1 device features SMBus and two-wire interface compatibility, and allows up to eight devices on the same bus with the SMBus overtemperature alert function. The factory-calibrated temperature accuracy and the noise-immune digital interface make the TMP275-Q1 the preferred solution for temperature compensation of other sensors and electronic components, without the need for additional system-level calibration or elaborate board layout for distributed temperature sensing.
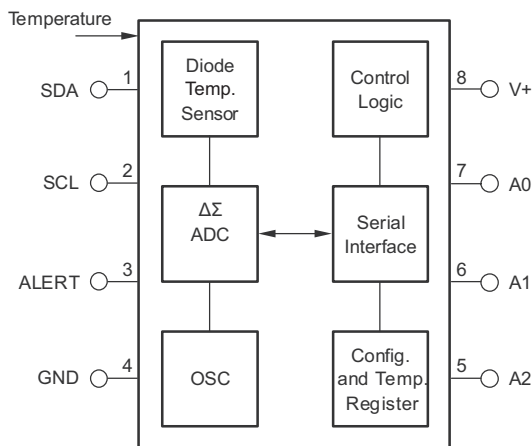
**Device Information[1]**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TMP275-Q1 | SOIC (8) | 4.90 mm × 3.91 mm |
| | VSSOP (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

**Simplified Schematic**



**Internal Block Diagram**

# Table of Contents

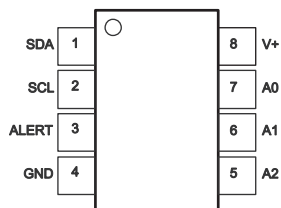# 4 Revision History

**Changes from Original (November 2015) to Revision A**         **Page**

• Changed *Thermal Information* table specifications ................................................................................................. 4

# 5 Pin Configuration and Functions

**D, DGK Packages**
**8-Pin SOIC, VSSOP**
**Top View**



**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | SDA | I/O | Serial data. Open-drain output; requires a pullup resistor. |
| 2 | SCL | I | Serial clock. Open-drain output; requires a pullup resistor. |
| 3 | ALERT | O | Overtemperature alert. Open-drain output; requires a pullup resistor. |
| 4 | GND | — | Ground |
| 5 | A2 | I | |
| 6 | A1 | I | Address select. Connect to GND or V+. |
| 7 | A0 | I | |
| 8 | V+ | I | Supply voltage, 2.7 V to 5.5 V |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

|  | MIN | MAX | UNIT |
|---|---|---|---|
| Power supply, V+ |  | 7 | V |
| Input voltage[2] | −0.5 | 7 | V |
| Input current |  | 10 | mA |
| Operating temperature | −55 | 127 | °C |
| Junction temperature, $T_J$ max |  | 150 | °C |
| Storage temperature, $T_{stg}$ | −60 | 130 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2500 | V |
|  |  | Charged device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 |  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | 2.7 |  | 5.5 | V |
| Operating free-air temperature, $T_A$ | −40 |  | 125 | °C |

## 6.4 Thermal Information

|  | THERMAL METRIC[1] | TMP275-Q1 | | UNIT |
|---|---|---|---|---|
|  |  | D (SOIC) | DGK (VSSOP) |  |
|  |  | 8 PINS | 8 PINS |  |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 121.6 | 185 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 70.5 | 76.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 62 | 106.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 23 | 14.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 61.5 | 104.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

at $T_A$ = –40°C to +125°C and V+ = 2.7 V to 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TEMPERATURE INPUT** | | | | | | |
| Range | | | –40 | | 125 | °C |
| Accuracy (temperature error) | | –20°C to 100°C, V+ = 3.3 V | | ±0.125 | ±0.5 | °C |
| | | 0°C to 100°C, V+ = 3 V to 3.6 V | | ±0.125 | ±0.75 | |
| | | –40°C to 125°C, V+ = 3 V to 3.6 V | | ±0.125 | ±1 | |
| | | 25°C to 100°C, V+ = 3.3 V to 5.5 V | | 0.2 | ±1.5 | |
| Resolution[1] | | Selectable | | 0.0625 | | °C |
| **DIGITAL INPUT/OUTPUT** | | | | | | |
| Input capacitance | | | | 3 | | pF |
| $V_{IH}$ | High-level input logic | | 0.7 (V+) | | 6 | V |
| $V_{IL}$ | Low-level input logic | | –0.5 | | 0.3 (V+) | V |
| $I_{IN}$ | Leakage input current | 0 V ≤ $V_{IN}$ ≤ 6 V | | | 1 | μA |
| Input voltage hysteresis | | SCL and SDA pins | | 500 | | mV |
| $V_{OL}$ | Low-level output logic | SDA | $I_{OL}$ = 3 mA | 0 | 0.15 | 0.4 | V |
| | | ALERT | $I_{OL}$ = 4 mA | 0 | 0.15 | 0.4 | |
| Resolution | | Selectable | | 9 to 12 | | Bits |
| Conversion time | | 9 bits | | 27.5 | 37.5 | ms |
| | | 10 bits | | 55 | 75 | |
| | | 11 bits | | 110 | 150 | |
| | | 12 bits | | 220 | 300 | |
| Time-out time | | | 25 | 54 | 74 | ms |
| **POWER SUPPLY** | | | | | | |
| Operating range | | | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Serial bus inactive | | 50 | 85 | μA |
| | | Serial bus active, SCL frequency = 400 kHz | | 100 | | |
| | | Serial bus active, SCL frequency = 3.4 MHz | | 410 | | |
| $I_{SD}$ | Shutdown current | Serial bus inactive | | 0.1 | 3 | μA |
| | | Serial bus active, SCL frequency = 400 kHz | | 60 | | |
| | | Serial bus active, SCL frequency = 3.4 MHz | | 380 | | |
| **TEMPERATURE RANGE** | | | | | | |
| Specified range | | | –40 | | 125 | °C |
| Operating range | | | –55 | | 127 | °C |

(1)  Specified for 12-bit resolution.

## 6.6 Timing Requirements

see the *Timing Diagrams* section for timing diagrams[1]

| | | | FAST MODE | | HIGH-SPEED MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{(SCL)}$ | SCL operating frequency | V+ | 0.001 | 0.4 | 0.001 | 2.38 | MHz |
| $t_{(BUF)}$ | Bus-free time between STOP and START condition | See the *Timing Diagrams* section | 1300 | | 160 | | ns |
| $t_{(HDSTA)}$ | Hold time after repeated START condition. After this period, the first clock is generated. | | 600 | | 160 | | ns |
| $t_{(SUSTA)}$ | repeated start condition setup time | | 600 | | 160 | | ns |
| $t_{(SUSTO)}$ | STOP Condition Setup Time | | 600 | | 160 | | ns |
| $t_{(HDDAT)}$ | Data hold time | | 4 | 900 | 4 | 120 | ns |
| $t_{(SUDAT)}$ | Data setup time | | 100 | | 10 | | ns |
| $t_{(LOW)}$ | SCL-clock low period | V+ , see the *Timing Diagrams* section | 1300 | | 280 | | ns |
| $t_{(HIGH)}$ | SCL-clock high period | See the *Timing Diagrams* section | 600 | | 60 | | ns |
| $t_FD$ | Data fall time | See the *Timing Diagrams* section | | 300 | | 150 | ns |
| $t_RC$ | Clock rise time | See the *Two-Wire Timing Diagrams* section | | 300 | | 40 | ns |
| | | SCLK ≤ 100 kHz, see the *Timing Diagrams* section | | 1000 | | | ns |
| $t_FC$ | Clock fall time | See the *Two-Wire Timing Diagrams* section | | 300 | | 40 | ns |

(1) Values are based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not specified and are not production tested.

## 6.7 Typical Characteristics

at $T_A$ = 25°C and V+ = 5 V (unless otherwise noted)
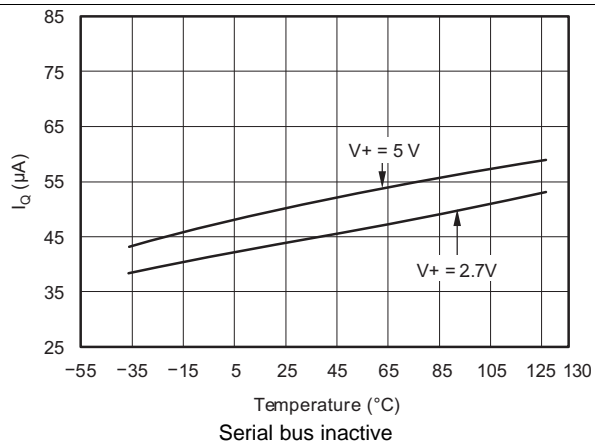


Figure 1. Quiescent Current vs Temperature
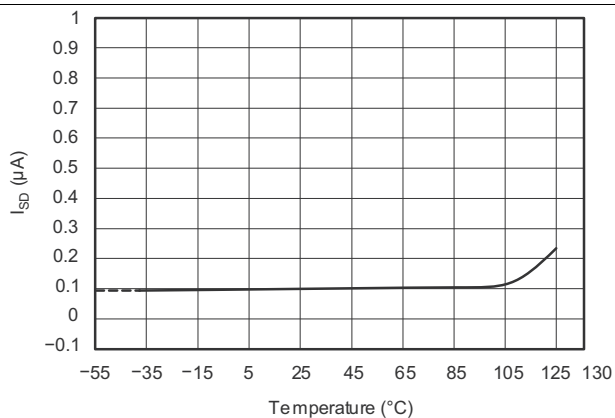


Figure 2. Shutdown Current vs Temperature
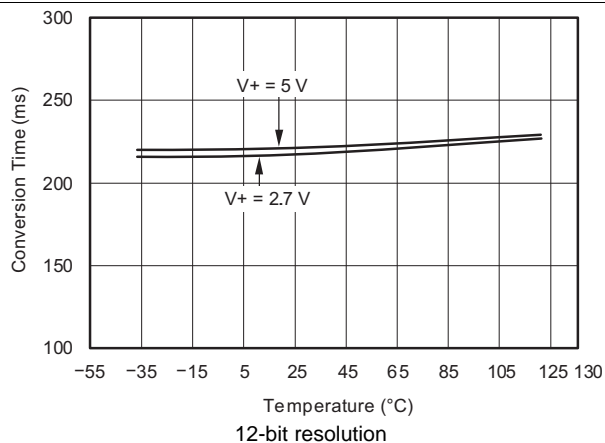


Figure 3. Conversion Time vs Temperature
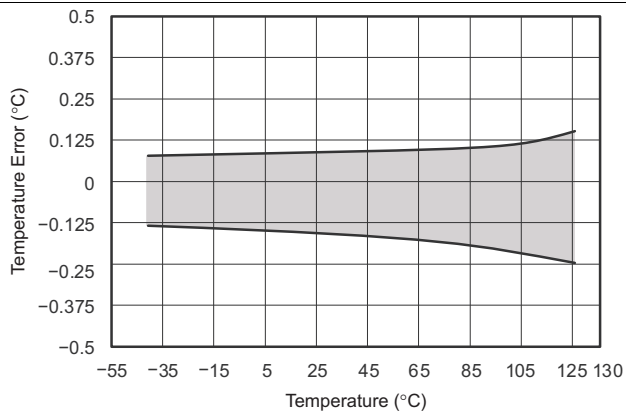


Figure 4. Temperature Error vs Temperature
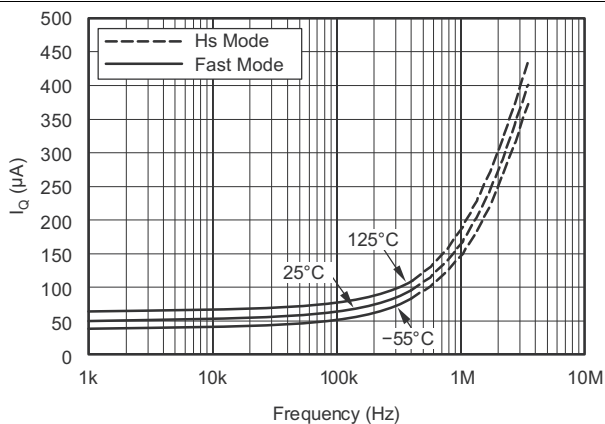


Figure 5. Quiescent Current with Bus Activity vs Temperature
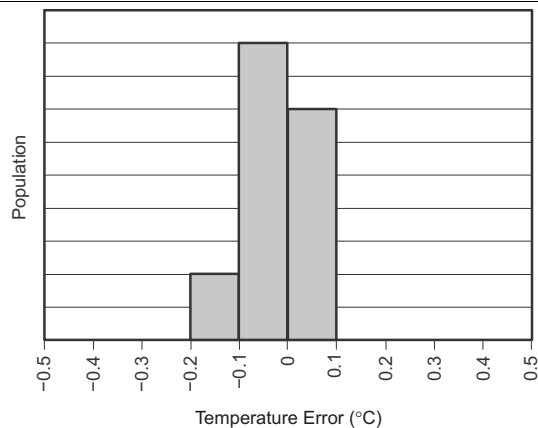


Figure 6. Temperature Error at 25°C

# 7 Detailed Description

## 7.1 Overview

The TMP275-Q1 is a digital temperature sensor that is optimal for thermal management and thermal protection applications. The TMP275-Q1 is two-wire, SMBus, and I$^2$C interface compatible, and is specified over the temperature range of –40°C to +125°C. The temperature sensor in the TMP275-Q1 is the device itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal; see the *Functional Block Diagram* section for the internal block diagram of the TMP275-Q1 device.

## 7.2 Functional Block Diagram
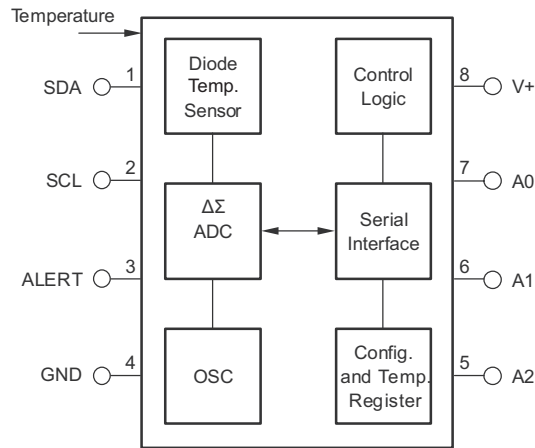
## 7.3 Feature Description

### 7.3.1 Digital Temperature Output

The temperature register of the TMP275-Q1 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 5 and Table 6. Note that byte 1 is the most significant byte and is followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 1. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete. The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits (MSBs) in the Temperature register are used with the unused least significant bits (LSBs) set to zero.

**Table 1. Temperature Data Format**

| TEMPERATURE (°C) | DIGITAL OUTPUT | |
|---|---|---|
| | BINARY | HEX |
| 128 | 0111 1111 1111 | 7FF |
| 127.9375 | 0111 1111 1111 | 7FF |
| 100 | 0110 0100 0000 | 640 |
| 80 | 0101 0000 0000 | 500 |
| 75 | 0100 1011 0000 | 4B0 |
| 50 | 0011 0010 0000 | 320 |
| 25 | 0001 1001 0000 | 190 |
| 0.25 | 0000 0000 0100 | 004 |
| 0 | 0000 0000 0000 | 000 |
| −0.25 | 1111 1111 1100 | FFC |
| −25 | 1110 0111 0000 | E70 |
| −55 | 1100 1001 0000 | C90 |

### 7.3.2 Serial Interface

The TMP275-Q1 operates only as a slave device on the SMBus, two-wire, and I$^2$C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP275-Q1 supports the transmission protocol for fast (up to 400 kHz) and high-speed (up to 2.38 MHz) modes. All data bytes are transmitted most significant bit (MSB) first.

### 7.3.3 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device a START condition is initiated, indicated by pulling the data line (SDA) from a high to a low logic level when SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the master generates a STOP condition indicated by pulling SDA from low to high when SCL is high.

## 7.3.4 Serial Bus Address

To communicate with the TMP275-Q1, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP275-Q1 features three address pins, allowing up to eight devices to be connected per bus. Pin logic levels are described in Table 2. The address pins of the TMP275-Q1 are read after reset, at the start of communication, or in response to a two-wire address acquire request. Following reading the state of the pins, the address is latched to minimize power dissipation associated with detection.

**Table 2. Address Pins and Slave Addresses for the TMP275-Q1**

| A2 | A1 | A0 | SLAVE ADDRESS |
|---|---|---|---|
| 0 | 0 | 0 | 1001000 |
| 0 | 0 | 1 | 1001001 |
| 0 | 1 | 0 | 1001010 |
| 0 | 1 | 1 | 1001011 |
| 1 | 0 | 0 | 1001100 |
| 1 | 0 | 1 | 1001101 |
| 1 | 1 | 0 | 1001110 |
| 1 | 1 | 1 | 1001111 |

### 7.3.4.1 Writing and Reading to the TMP275-Q1

Accessing a particular register on the TMP275-Q1 is accomplished by writing the appropriate value to the Pointer register. The value for the Pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the TMP275-Q1 requires a value for the Pointer register; see Figure 8.

When reading from the TMP275-Q1, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register. This action is accomplished by issuing a slave address byte with the R/W bit low, followed by the Pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/W bit high to initiate the read command; see Figure 9 for details of this sequence. If repeated reads from the same register are desired, the Pointer register bytes do not have to be continually sent because the TMP275-Q1 remembers the Pointer register value until it is changed by the next write operation.

Note that register bytes are sent most-significant byte first, followed by the least significant byte.

### 7.3.4.2 Slave Mode Operations

The TMP275-Q1 can operate as a slave receiver or slave transmitter.

#### 7.3.4.2.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{\text{W}}$ bit low. The TMP275-Q1 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer register. The TMP275-Q1 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The TMP275-Q1 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

#### 7.3.4.2.2 Slave Transmitter Mode

The first byte is transmitted by the master and is the slave address, with the R/$\overline{\text{W}}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a Not-Acknowledge bit on reception of any data byte, or by generating a START or STOP condition.

### 7.3.4.3 SMBus Alert Function

The TMP275-Q1 supports the SMBus alert function. When the TMP275-Q1 is operating in interrupt mode (TM = 1), the ALERT pin of the TMP275-Q1 can be connected as an SMBus alert signal. When a master senses that an Alert condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP275-Q1 is active, the device acknowledges the SMBus Alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding $T_{HIGH}$ or falling below $T_{LOW}$ caused the Alert condition. This bit is high if the temperature is greater than or equal to $T_{HIGH}$. This bit is low if the temperature is less than $T_{LOW}$; see Figure 10 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device clears its Alert status. If the TMP275-Q1 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP275-Q1 loses the arbitration, its ALERT pin remains active.

### 7.3.4.4 General Call

The TMP275-Q1 responds to a two-wire, general-call address (0000000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 00000100, the TMP275-Q1 latches the status of its address pins but does not reset. If the second byte is 00000110, the TMP275-Q1 latches the status of its address pins and resets its internal registers to their power-up values.

### 7.3.4.5 High-Speed Mode

For the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP1275 device does not acknowledge this byte, but does switch its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, thus allowing transfers at up to 2.38 MHz. After the Hs-mode master code is issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP275-Q1 switches the input and output filter back to fast-mode operation.

### 7.3.4.6 Time-Out Function

The TMP275-Q1 resets the serial interface if either SCL or SDA is held low for 54 ms (typical) between a START and STOP condition. The TMP275-Q1 releases the bus if it is pulled low and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained for the SCL operating frequency.

### 7.3.5 Timing Diagrams

The TMP275-Q1 is two-wire, SMBus, and I$^2$C interface compatible. Figure 7 to Figure 10 describe the various operations on the TMP275-Q1. The following list provides bus definitions. Parameters for Figure 7 are defined in the *Timing Requirements* table.

**Bus Idle:** Both the SDA and SCL lines remain high.

**Start Data Transfer:** A change in the state of the SDA line, from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge bit on the last byte that is transmitted by the slave.
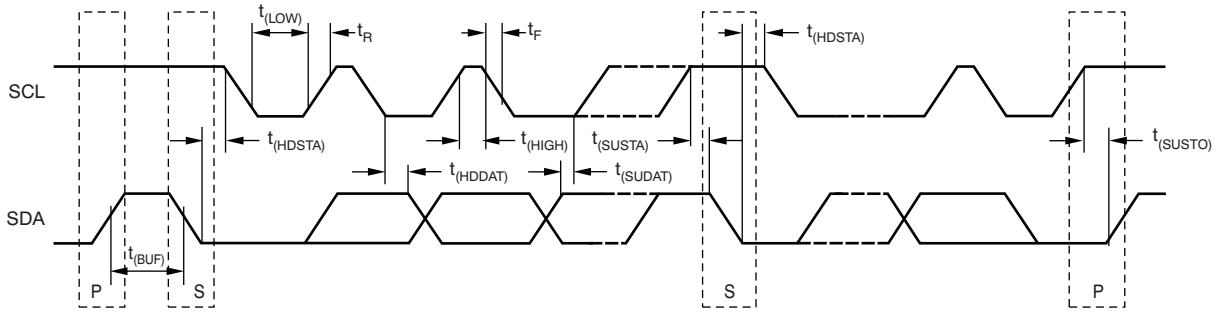
### 7.3.5.1 Two-Wire Timing Diagrams
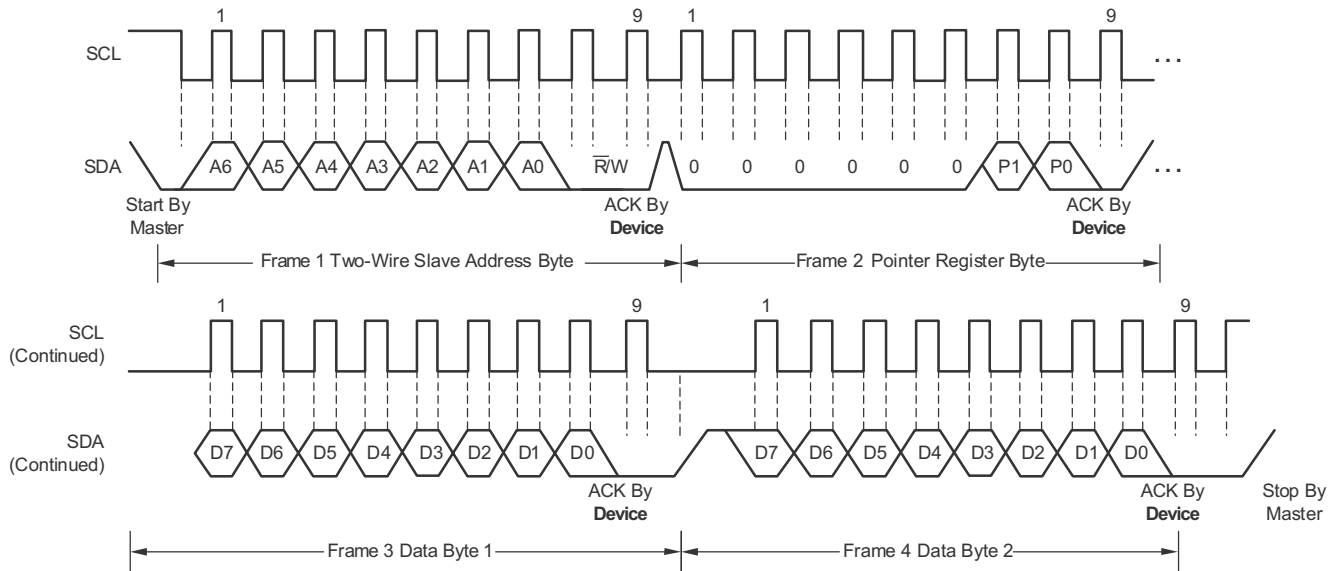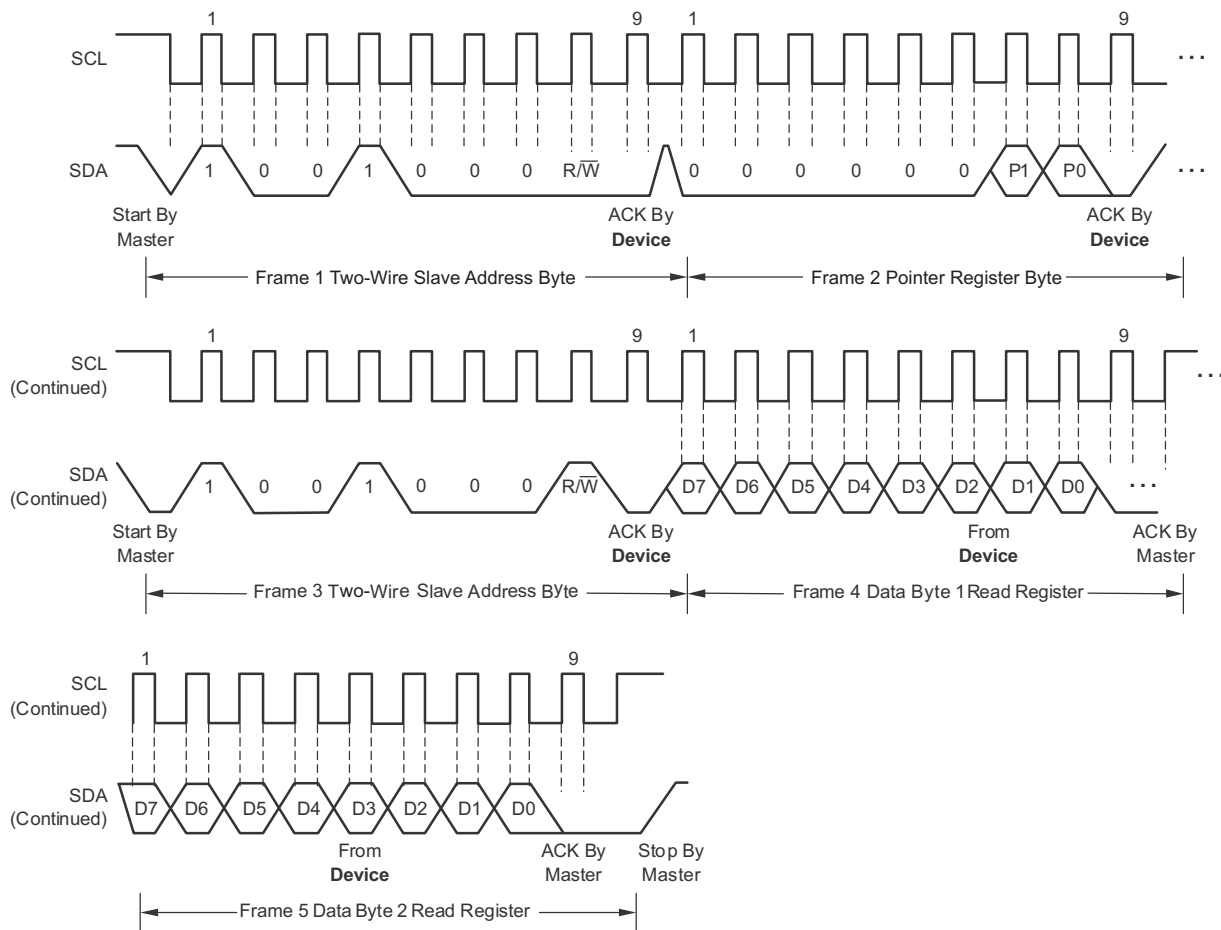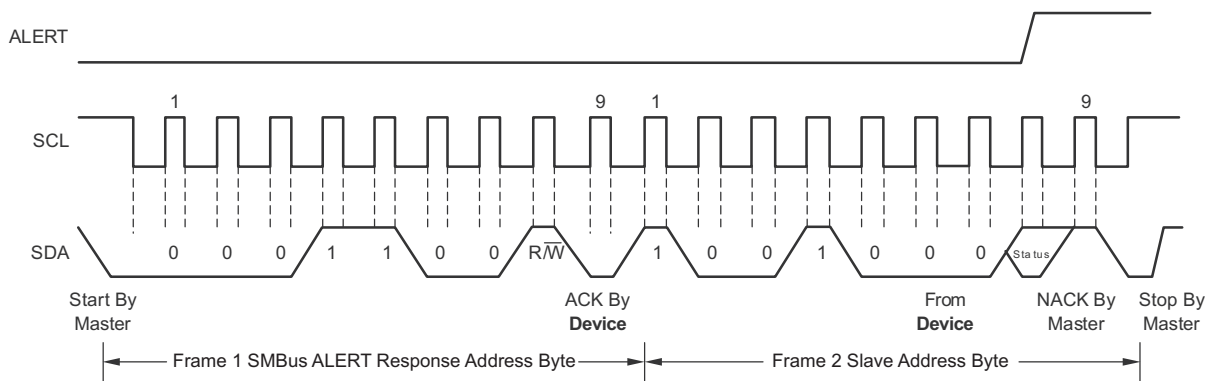


**Figure 7. Two-Wire Timing Diagram**



**Figure 8. Two-Wire Timing Diagram for TMP275-Q1 Write Word Format**

NOTE: Address pins A0, A1, and A2 = 0.

**Figure 9. Two-Wire Timing Diagram for Read Word Format**



NOTE: Address pins A0, A1, and A2 = 0.

**Figure 10. Timing Diagram for SMBus ALERT**

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Mode (SD)

The shutdown mode of the TMP275-Q1 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, thus reducing current consumption to typically less than 0.1 µA. Shutdown mode is enabled when the SD bit is 1; the device shuts down when the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

### 7.4.2 Thermostat Mode (TM)

The thermostat mode bit of the TMP275-Q1 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

#### 7.4.2.1 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin is activated when the temperature equals or exceeds the value in the $T_{HIGH}$ register and remains active until the temperature falls below the value in the $T_{LOW}$ register. For more information on the comparator mode, see the *High- and Low-Limit Registers* section.

#### 7.4.2.2 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the ALERT pin is activated when the temperature exceeds $T_{HIGH}$ or goes below the $T_{LOW}$ register. The ALERT pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High- and Low-Limit Registers* section.

### 7.4.3 One-Shot (OS)

The TMP275-Q1 features a one-shot temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful for reducing power consumption in the TMP275-Q1 when continuous temperature monitoring is not required. When the configuration register is read, OS always reads zero.

## 7.5 Programming

### 7.5.1 Pointer Register

Figure 11 shows the internal register structure of the TMP275-Q1. The 8-bit Pointer register of the device is used to address a given data register. The Pointer register uses the two LSBs to identify which of the data registers must respond to a read or write command. Table 3 identifies the bits of the Pointer register byte. Table 4 describes the pointer address of the registers available in the TMP275-Q1. The power-up reset value of P1/P0 is 00.
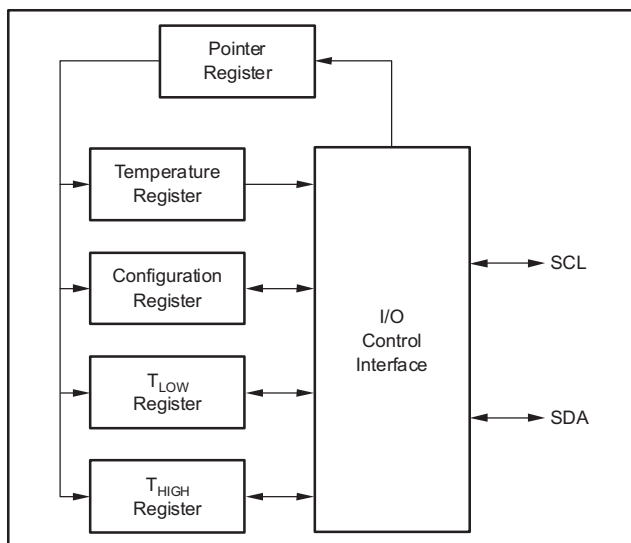


**Figure 11.  Internal Register Structure of the TMP275-Q1**

**Table 3. Pointer Register Byte (pointer = N/A) [reset = 00h]**

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | Register Bits | |

**Table 4. Pointer Addresses of the TMP275-Q1**

| P1 | P0 | TYPE | REGISTER |
|----|----|------|----------|
| 0 | 0 | R only, default | Temperature register |
| 0 | 1 | R/W | Configuration register |
| 1 | 0 | R/W | $T_{LOW}$ register |
| 1 | 1 | R/W | $T_{HIGH}$ register |

### 7.5.2 Temperature Register

The Temperature register of the TMP275-Q1 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are described in Table 5 and Table 6. Note that byte 1 is the most significant byte and is followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 1. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

**Table 5. Byte 1 of the Temperature Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |

**Table 6. Byte 2 of the Temperature Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| T3 | T2 | T1 | T0 | 0 | 0 | 0 | 0 |

### 7.5.3 Configuration Register

The Configuration register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the TMP275-Q1 is shown in Table 7, followed by a breakdown of the register bits. The power-up or reset value of the Configuration register is all bits equal to 0.

**Table 7. Configuration Register Format**

| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|----|----|----|----|
| 1 | OS | R1 | R0 | F1 | F0 | POL | TM | SD |

### 7.5.4 Polarity (POL)

The Polarity bit of the TMP275-Q1 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin is active low, as shown in Figure 12. For POL = 1, the ALERT pin is active high and the state of the ALERT pin is inverted.
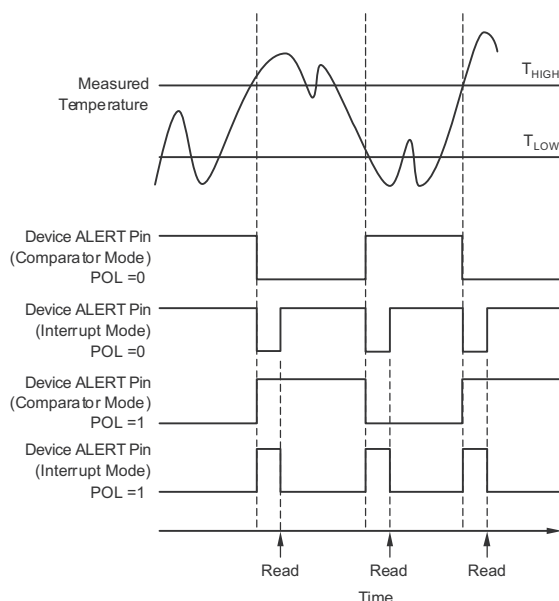


**Figure 12. Output Transfer Function Diagrams**

### 7.5.5 Fault Queue (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the $T_{HIGH}$ and $T_{LOW}$ registers. Additionally, the number of fault conditions required to generate an alert can be programmed using the fault queue. The fault queue is provided to prevent a false alert resulting from environmental noise. The fault queue requires consecutive fault measurements to trigger the Alert function. Table 8 defines the number of measured faults that can be programmed to trigger an Alert condition in the device. For the $T_{HIGH}$ and $T_{LOW}$ register format and byte order, see the *High- and Low-Limit Registers* section.

**Table 8. Fault Settings**

| F1 | F0 | CONSECUTIVE FAULTS |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

### 7.5.6 Converter Resolution (R1/R0)

The converter resolution bits control the resolution of the internal analog-to-digital converter (ADC). This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 9 identifies the resolution bits and the relationship between resolution and conversion time.

**Table 9. Resolution of the TMP275-Q1**

| R1 | R0 | RESOLUTION | CONVERSION TIME (Typical) |
|---|---|---|---|
| 0 | 0 | 9 bits (0.5°C) | 27.5 ms |
| 0 | 1 | 10 bits (0.25°C) | 55 ms |
| 1 | 0 | 11 bits (0.125°C) | 110 ms |
| 1 | 1 | 12 bits (0.0625°C) | 220 ms |

### 7.5.7 High- and Low-Limit Registers

In comparator mode (TM = 0), the ALERT pin of the TMP275-Q1 becomes active when the temperature equals or exceeds the value in $T_{HIGH}$ and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated $T_{LOW}$ value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds $T_{HIGH}$ for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When cleared, the ALERT pin only becomes active again by the temperature falling below $T_{LOW}$. When the temperature falls below $T_{LOW}$, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds $T_{HIGH}$. The ALERT pin can also be cleared by resetting the device with the General-Call Reset command. This action also clears the state of the internal registers in the device, returning the device to comparator mode (TM = 0).

Both operational modes are represented in Figure 12. Table 10, Table 11, Table 12, and Table 13 describe the format for the $T_{HIGH}$ and $T_{LOW}$ registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for $T_{HIGH}$ and $_{TLOW}$ are:

$T_{HIGH}$ = 80°C and $T_{LOW}$ = 75°C

The format of the data for $T_{HIGH}$ and $T_{LOW}$ is the same as for the Temperature register.

**Table 10. Byte 1 the $T_{HIGH}$ Register**

| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | H11 | H10 | H9 | H8 | H7 | H6 | H5 | H4 |

**Table 11. Byte 2 of the $T_{HIGH}$ Register**

| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 2 | H3 | H2 | H1 | H0 | 0 | 0 | 0 | 0 |

**Table 12. Byte 1 the $T_{LOW}$ Register**

| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 |

**Table 13. Byte 2 of the $T_{LOW}$ Register**

| BYTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| 2 | L3 | L2 | L1 | L0 | 0 | 0 | 0 | 0 |

All 12 bits for the Temperature, $T_{HIGH}$, and, $T_{LOW}$ registers are used in the comparisons for the Alert function for all converter resolutions. The three LSBs in $T_{HIGH}$ and $T_{LOW}$ can affect the Alert output even if the converter is configured for 9-bit resolution.

# 8 Application and Implementation

## 8.1 Application Information

The TMP275-Q1 is a digital output temperature sensor with SMBus, two-wire, and I$^2$C compatible interfaces. The device features three address pins (A0, A1, A2), allowing up to eight devices to be connected per bus. The TMP275-Q1 requires no external components for operation except for pullup resistors on SCL, SDA, and ALERT, although a 0.1-µF bypass capacitor is recommended. The TMP275-Q1 measures the printed circuit board (PCB) temperature of where the device is mounted. The sensing device of the TMP275-Q1 is the device itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

## 8.2 Typical Applications

### 8.2.1 Typical Connections of the TMP275-Q1
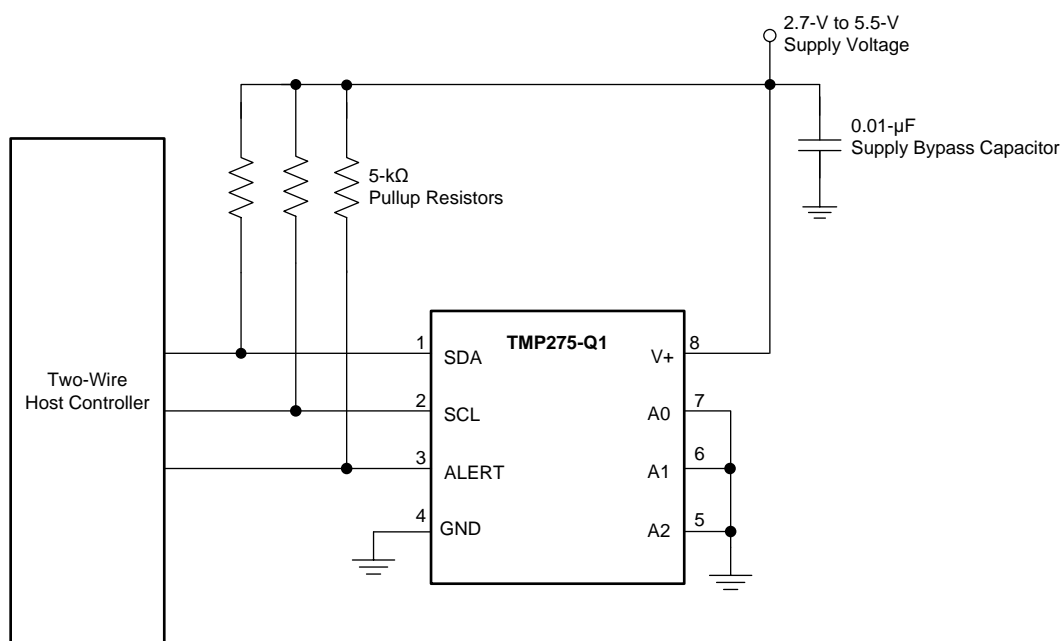


**Figure 13. Typical Connections of the TMP275-Q1 Schematic**

#### 8.2.1.1 Design Requirements

Figure 13 shows the TMP275-Q1 typical connections. The TMP275-Q1 device requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistor is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ, but must not exceed 3 mA of current on the SCL and SDA pins and must not exceed 4 mA on the ALERT pin. If the resistors are missing, the SCL and SDA lines are always low (nearly 0 V) and the I$^2$C bus does not work. A 0.1-µF bypass capacitor is recommended, as shown in Figure 13. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V+ through the pullup resistors.

## Typical Applications (continued)

The ALERT pin can be configured to respond to one of the two Alert functions available: *comparator mode* and *interrupt mode*. To configure one of eight different addresses on the bus, connect A0, A1, and A2 to either the GND or V+ pin. In the circuit shown in Figure 13, the comparator mode is selected and the address pins (A0, A1, A2) are connected to ground.

### 8.2.1.2  Detailed Design Procedure

Place the TMP275-Q1 device in close proximity to the heat source that must be monitored with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

### 8.2.1.3  Application Curve

Figure 14 shows the step response of the TMP275-Q1 device to a submersion in an oil bath of 100ºC from room temperature (27ºC). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 s. The time-constant result depends on the PCB where the TMP275-Q1 devices are mounted. For this test, the TMP275-Q1 device was soldered to a two-layer PCB that measured 0.375 inches × 0.437 inches.
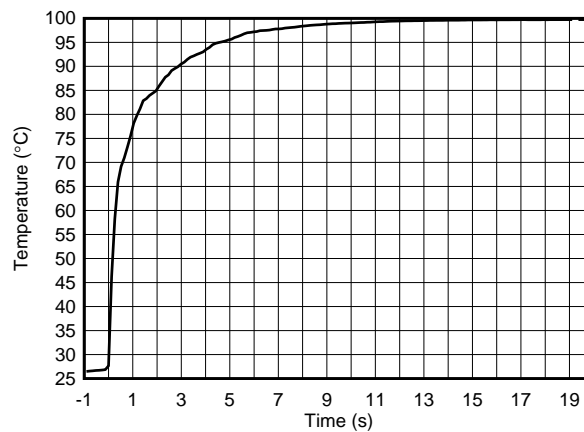


**Figure 14. Temperature Step Response**

## Typical Applications (continued)

### 8.2.2  Connecting Multiple Devices on a Single Bus

The TMP275-Q1 features three address pins, allowing up to eight devices to be connected per bus. When the TMP275-Q1 is operating in interrupt mode (TM = 1) , the ALERT pin of the TMP275-Q1 can be connected as an SMBus Alert signal. Figure 15 shows eight TMP275-Q1 devices connected to an MCU (master) using one single bus. Each device that exists as a slave on the SMBus has one unique 7-bit address; see Table 2 for the TMP275-Q1 address options. When a master senses that an Alert condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP275-Q1 is active, the device acknowledges the SMBus Alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding $T_{HIGH}$ or falling below $T_{LOW}$ caused the ALERT condition. This bit is high if the temperature is greater than or equal to $T_{HIGH}$. This bit is low if the temperature is less than $T_{LOW}$.

This application has eight devices connected to the bus. If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device clears its ALERT status. If the TMP275-Q1 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP275-Q1 loses the arbitration, its ALERT pin remains active.

---

**NOTE**

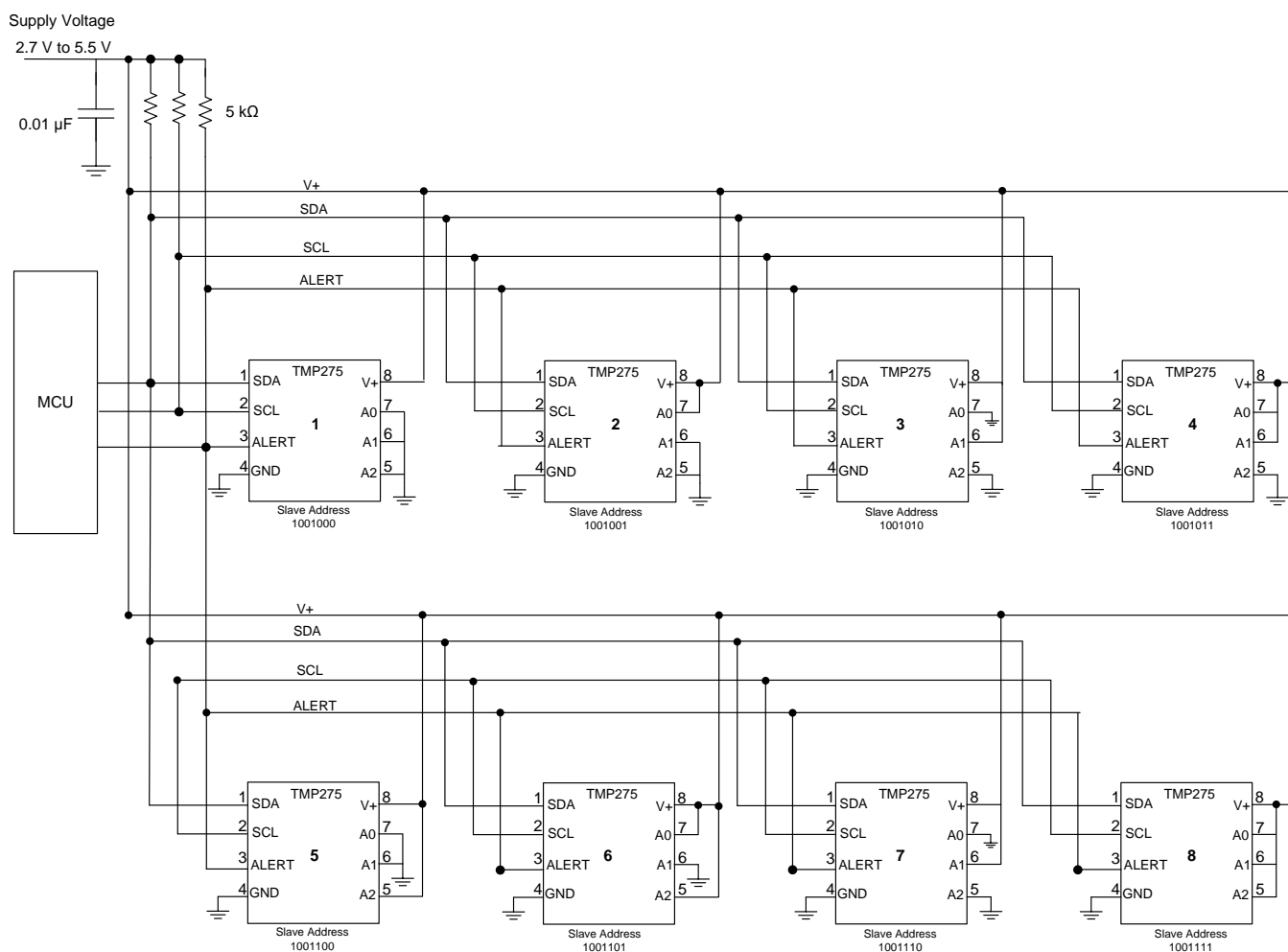Make sure you device is configured to operate in interrupt mode to enable the SMBus feature.

---



**Figure 15.  Connecting Multiple Devices on a Single Bus**

## Typical Applications (continued)

### 8.2.3 Temperature Data Logger for Cold Chain Management Applications

Cold chain management includes all of the means used to ensure a constant temperature for a product that is not heat stable from the time it is manufactured or farmed until the time it is used. This cold chain management includes industries such as food, retail, medical, and pharmaceutical. Figure 16 implements a cold chain monitoring system that measures temperature, then logs the sensor data to nonvolatile (FRAM) memory in the MCU. Figure 16 uses a near field communication (NFC) interface for wireless communication and is powered from a CR2032 coin cell battery with a focus on low power to maximize the battery lifetime.

The microcontroller communicates with all of the sensor devices through an $I^2C$ compatible interface. The MCU also communicates with the NFC transponder through this interface. An NFC-enabled smartphone can be used to send configurations to the application board. For a detailed design procedure and requirements of this application, see *Ultralow Power Multi-sensor Data Logger with NFC Interface Reference Design*, TIDU821.
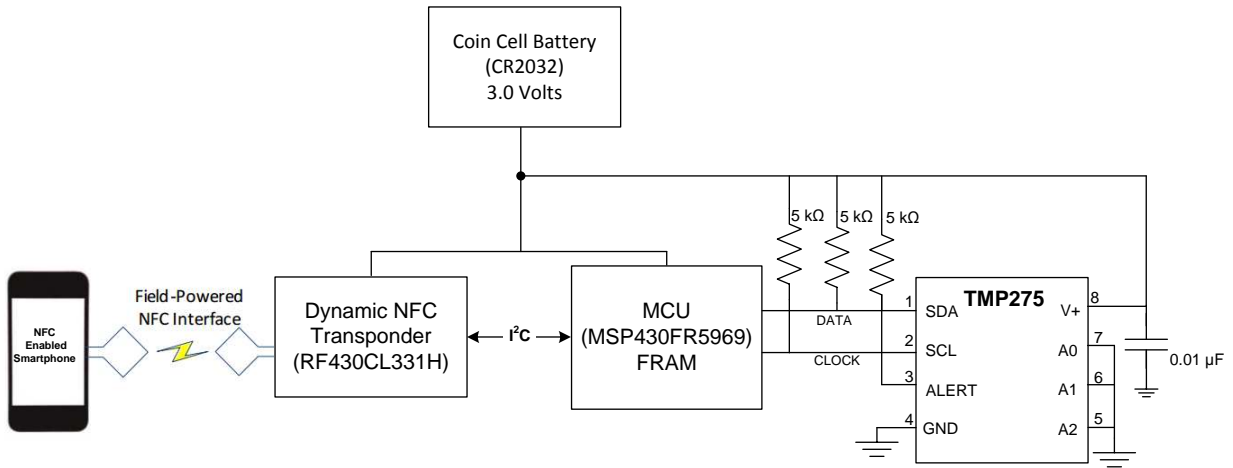


**Figure 16. Temperature Data Logger**

# 9 Power Supply Recommendations

The TMP275-Q1 device operates with power supplies in the range of 2.7 V to 5.5 V. A power-supply bypass capacitor is required for stability; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

# 10 Layout

## 10.1 Layout Guidelines

Mount the TMP275-Q1 to a PCB as shown in Figure 17. For this example the A0, A1, and A2 address pins are connected directly to ground. Connecting these pins to ground configures the device for slave address 1001000b.

- Bypass the V+ pin to ground with a low-ESR ceramic bypass-capacitor. The typical recommended bypass capacitance is a 0.1-µF ceramic capacitor with a X5R or X7R dielectric. The optimum placement is closest to the V+ and GND pins of the device. Take care in minimizing the loop area formed by the bypass-capacitor connection, the V+ pin, and the GND pin of the device. Additional bypass capacitance can be added to compensate for noisy or high-impedance power supplies.
- Pull up the open-drain output pins SDA, SCL, and ALERT through 5-kΩ pullup resistors.
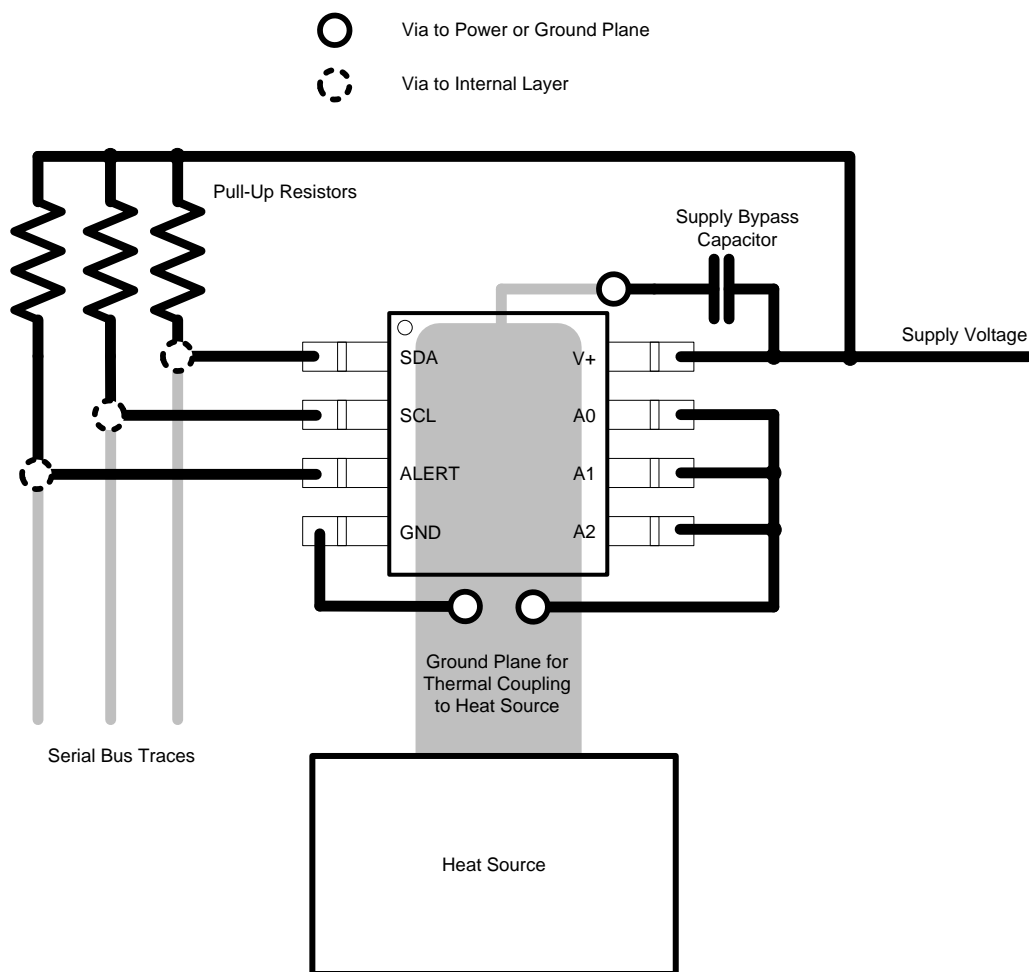
## 10.2 Layout Example



**Figure 17. TMP275-Q1 Layout Example**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:
- LM75 Data Sheet, SNOS808
- TMP75, TMP175 Data Sheet, SBOS288
- TMP75B Data Sheet, SBOS706
- *Ultralow Power Multi-sensor Data Logger with NFC Interface Reference Design*, TIDU821

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
SMBus is a trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP275AQDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 275Q | Samples |
| TMP275AQDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T275Q1 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

11-Jan-2016

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TMP275-Q1 :**

● Catalog: TMP275

NOTE: Qualified Version Definitions:

     ● Catalog - TI's standard catalog product

## DGK (S−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE
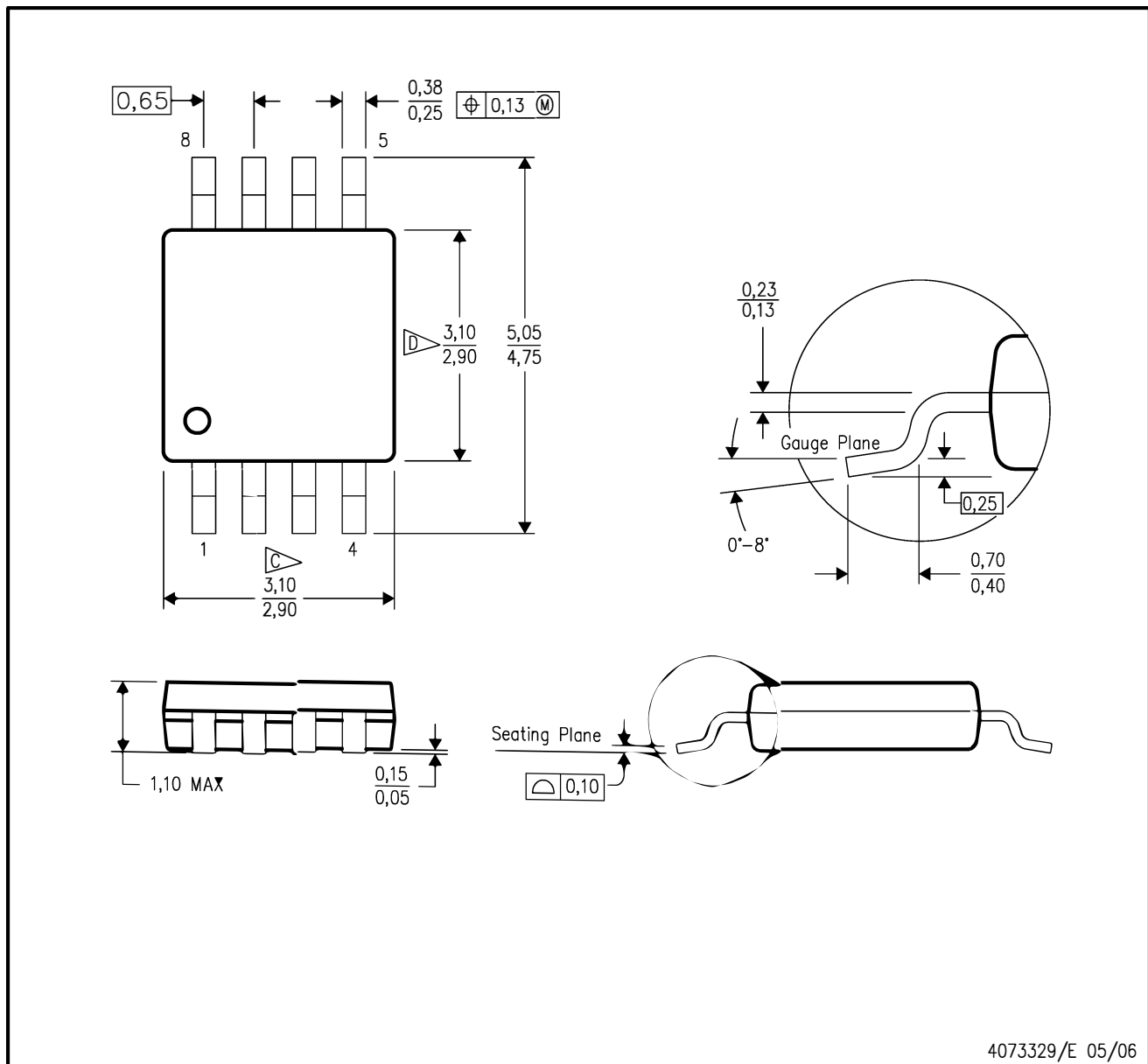
0,65

0,38 / 0,25   ⊕ | 0,13 Ⓜ

8

5

▷D 3,10 / 2,90

5,05 / 4,75

1

4

▷C

3,10 / 2,90

0,23 / 0,13

Gauge Plane

0°−8°

0,25

0,70 / 0,40

1,10 MAX

0,15 / 0,05

Seating Plane

⌂ | 0,10

4073329/E 05/06

NOTES:   A.  All linear dimensions are in millimeters.
  B.  This drawing is subject to change without notice.
  ▷C  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
      not exceed 0.15 per end.
  ▷D  Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  E.  Falls within JEDEC MO−187 variation AA, except interlead flash.
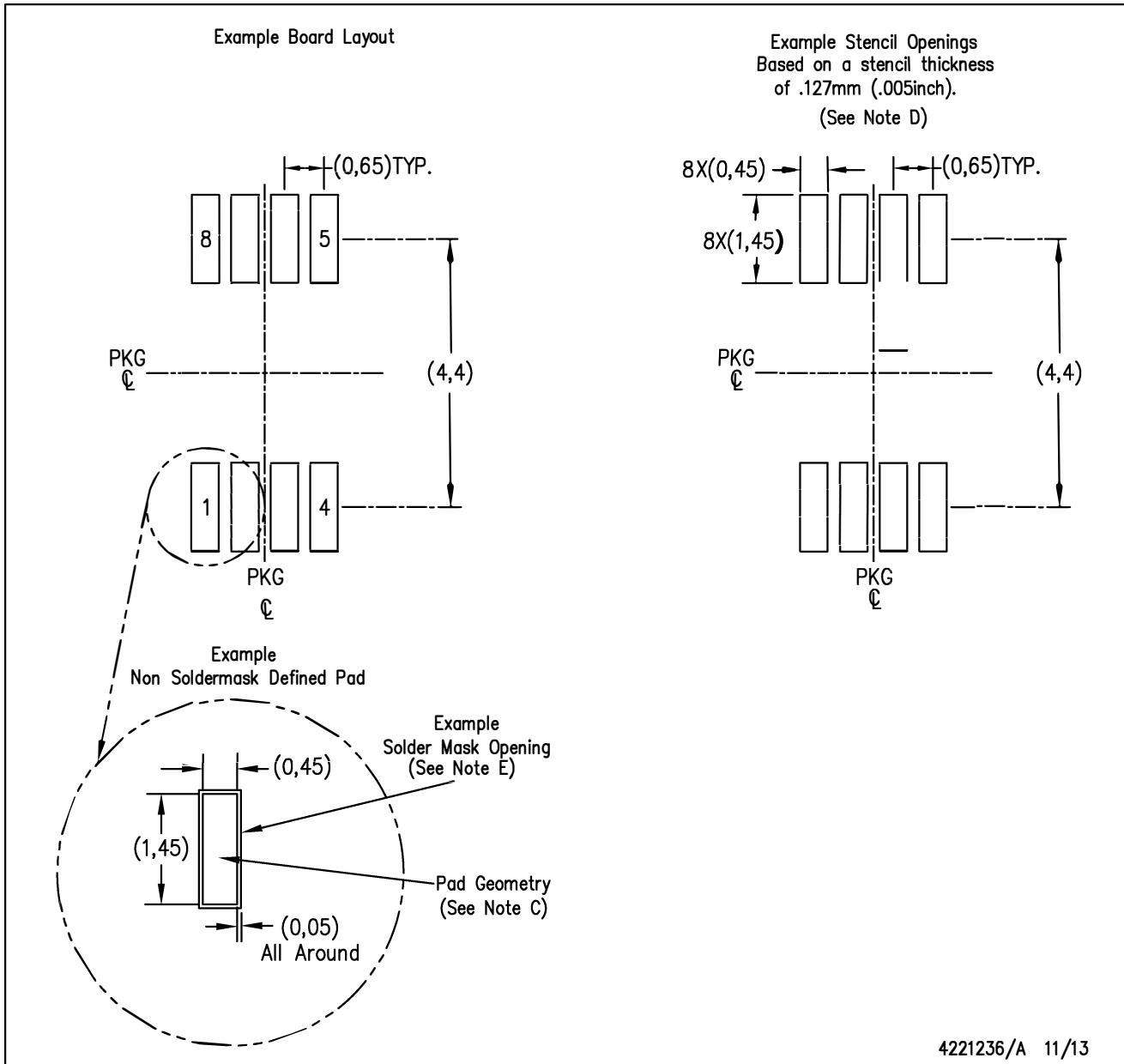
DGK (S-PDSO-G8)                    PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

|←→|(0,65)TYP.

8
5

PKG
℄

(4,4)

1
4

PKG
℄

8X(0,45) →|     |←     |←→|(0,65)TYP.

8X(1,45)

PKG
℄

(4,4)

PKG
℄

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

|←(0,45)

(1,45)

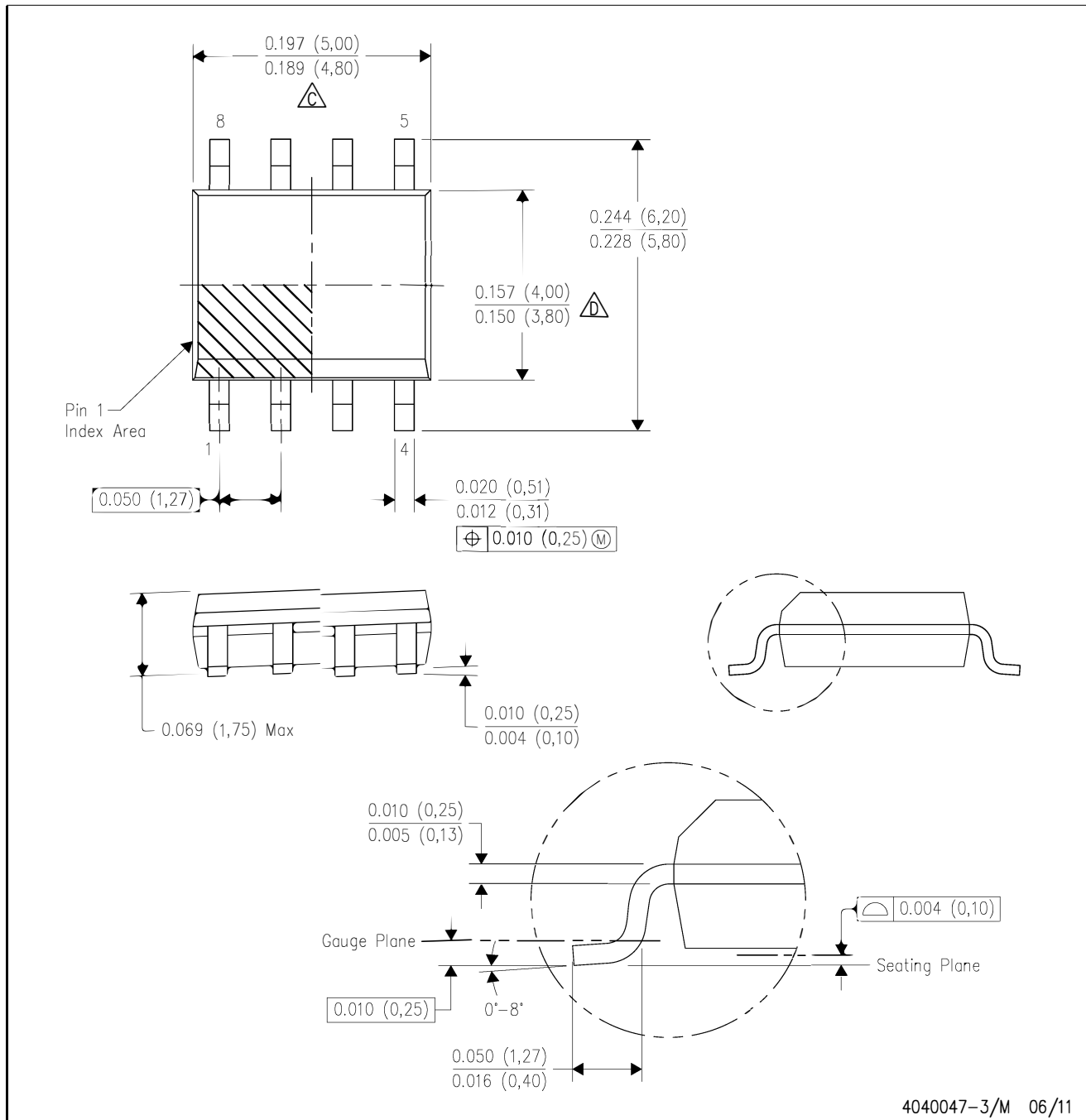Pad Geometry
(See Note C)

|←(0,05)
All Around

4221236/A  11/13

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC-7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations.  Refer to IPC-7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
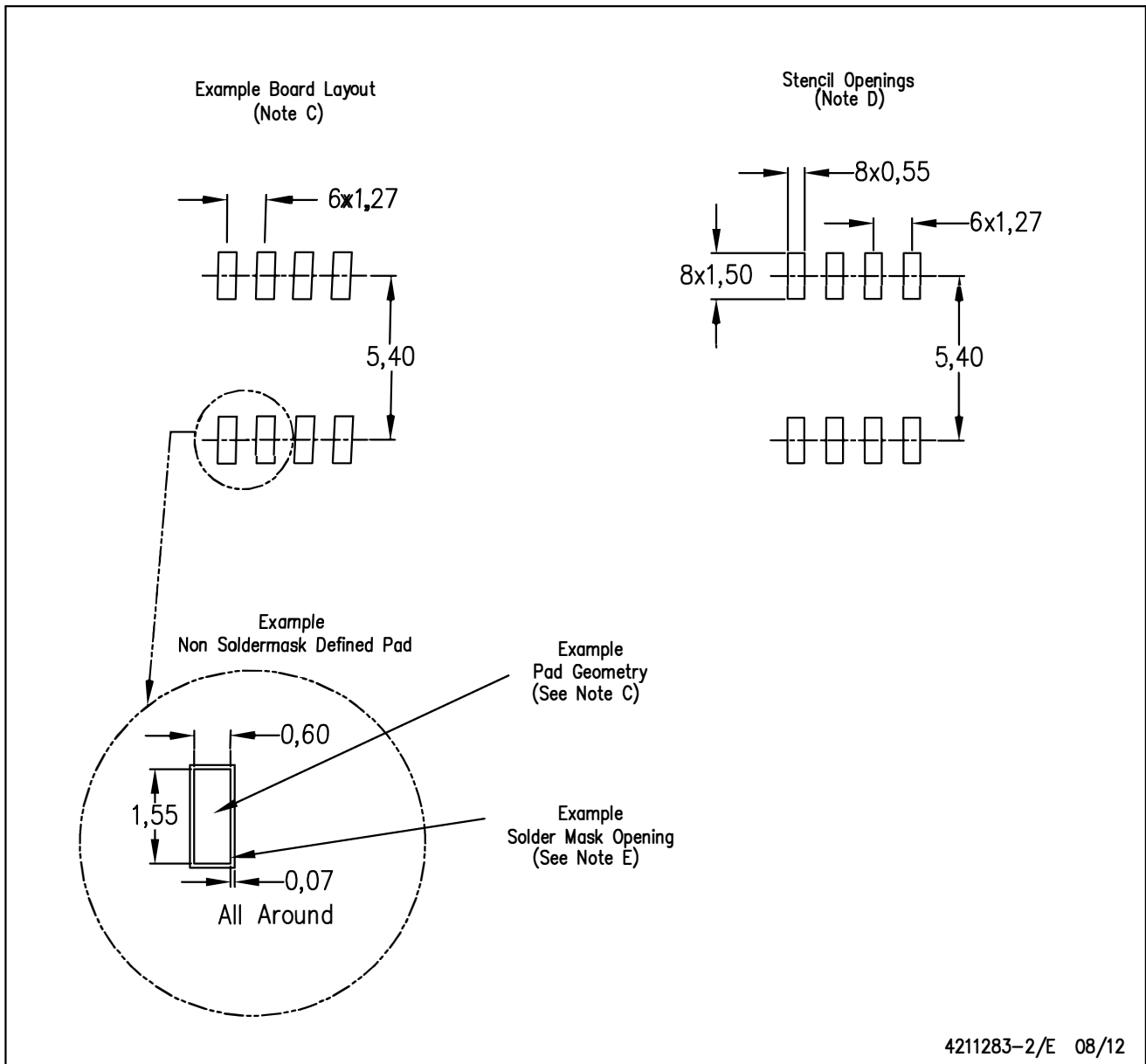
D (R−PDSO−G8) PLASTIC SMALL OUTLINE



0.197 (5,00)
0.189 (4,80)
⟨C⟩

8

5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

Pin 1
Index Area

1

4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         ⟨C⟩  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         ⟨D⟩  Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.

D (R−PDSO−G8)                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

8x1,50

6x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

0,07

All Around

Example
Solder Mask Opening
(See Note E)

4211283−2/E  08/12

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.