SGM2566A/SGM2566B
5.5V, 6A, 19mΩ On-Resistance Load Switches

GENERAL DESCRIPTION

The SGM2566A and SGM2566B are single channel load switches that provide configurable rise time to minimize inrush current. These devices contain an N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and can support a maximum continuous current of 6A. The switches are controlled by an on and off input (EN/FAULT), which is capable of interfacing directly with low-voltage control signals. In the SGM2566A, a 265Ω on-chip load resistor is added for quick output discharge when switch is turned off.

The SGM2566A and SGM2566B are available in Green TDFN-2×2-8L package. They are rated over the -40℃ to +85℃ temperature range.

FEATURES

- **Input Voltage Range: 0.8V to 5.5V**
- **Ultra-Low On-Resistance**
  $R_{DS(ON)}$ = 19mΩ at V_{IN} = 3.3V (V_{BIAS} = 5V)
- **6A Maximum Continuous Switch Current**
- **Low Quiescent Current:**
  15μA (V_{BIAS} = 5V)
  9μA (V_{BIAS} = 2.5V)
- **Reverse Current Blocking Support**
- **Built-In Thermal Shutdown**
- **Over-Current/Short-Circuit Protection**
- **Soft-Start Function**
- **Enable/Fault Pin**
- **Low Control Input Threshold Enables Use of 1.2V, 1.8V, 2.5V and 3.3V Logic**
- **Configurable Rise Time**
- **SGM2566A: Quick Output Discharge**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in the Green TDFN-2×2-8L Package**

APPLICATIONS

Ultrabook
Notebooks and Netbooks
Tablet PC

TYPICAL APPLICATION

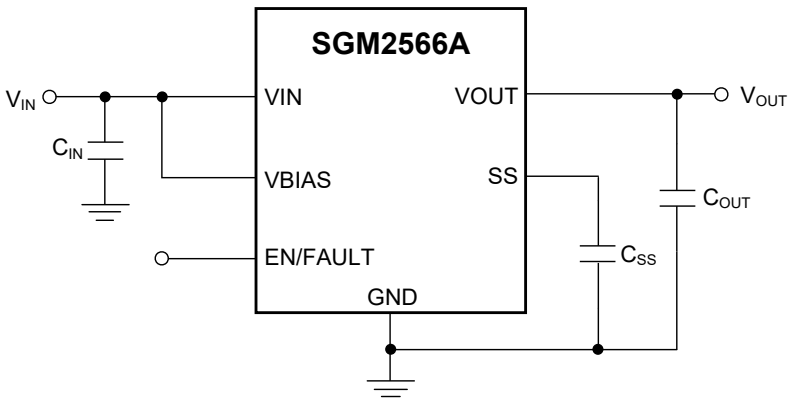


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2566A	TDFN-2×2-8L	-40℃ to +85℃	SGM2566AYTDE8G/TR	GP7 XXXX	Tape and Reel, 3000
SGM2566B	TDFN-2×2-8L	-40℃ to +85℃	SGM2566BYTDE8G/TR	GP8 XXXX	Tape and Reel, 3000

NOTE: XXXX = Date Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_{IN} ..... -0.3V to 6V
Output Voltage, V_{OUT} ..... -0.3V to 6V
Bias Voltage, V_{BIAS} ..... -0.3V to 6V
EN/FAULT Voltage, $V_{EN/FAULT}$ ..... -0.3V to 6V
EN/FAULT Sink Current 25mA
PIN Voltage, SS ..... <V_{BIAS}
Maximum Continuous Switch Current, I_{MAX} ..... <6A
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{IN} ..... 0.8V to V_{BIAS}
Bias Voltage, V_{BIAS} ..... 2.5V to 5.5V
EN/FAULT Voltage, $V_{EN/FAULT}$ ..... 0V to 5.5V
Output Voltage, V_{OUT} ..... <V_{IN}
Input Capacitor, C_{IN} ..... >1μF
Operating Junction Temperature ..... -40℃ to +125℃
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

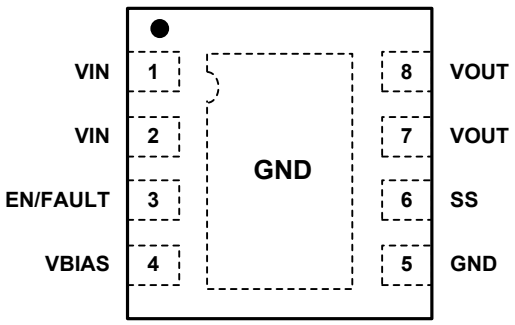
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-8L

PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
1	VIN	I	Switch Input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2.
2			
3	EN/FAULT	I	Enable Input or Alert Output ($V_{EN/FAULT} \leq V_{BIAS}$). Asserting EN/FAULT pin high enables the device. When any of over-temperature protection or over-current protection occurs, the device sinks current from EN/FAULT, pulling the pin down to alert the host (pin as output port).
4	VBIAS	I	Bias Voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V.
5	GND	—	Device Ground.
6	SS	O	Switch Slew Rate Control. Can be left floating.
7	VOUT	O	Switch Output. Must be connected to Pin 7 and Pin 8.
8			
Thermal Pad	GND	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND.

ELECTRICAL CHARACTERISTICS

(V_{BIAS} = 5V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES AND CURRENTS							
Bias Voltage Range	V_{BIAS}			2.5		5.5	V
Input Voltage Range	V_{IN}			0.8		V_{BIAS}	V
V_{BIAS} Quiescent Supply Current	I_{Q_BIAS}	I_{OUT} = 0mA, V_{IN} = $V_{EN/FAULT}$ = V_{BIAS} = 5V			15		μA
V_{BIAS} Shutdown Supply Current	I_{SD_BIAS}	$V_{EN/FAULT}$ = GND, V_{OUT} = 0V			0.1		μA
V_{IN} Shutdown Supply Current	I_{SD_IN}	$V_{EN/FAULT}$ = GND, V_{OUT} = 0V	V_{IN} = 5V		0.1		μA
			V_{IN} = 3.3V		0.1		
			V_{IN} = 1.8V		0.1		
			V_{IN} = 1.5V		0.1		
			V_{IN} = 1.2V		0.1		
			V_{IN} = 0.8V		0.1		
LOGIC LEVEL INPUTS							
EN/FAULT Input Current	I_{EN}	$V_{EN/FAULT}$ = 5.5V			0.1		μA
EN/FAULT Input Low Voltage	V_{IL}				0.4		V
EN/FAULT Input High Voltage	V_{IH}				1.0		V
RESISTANCE CHARACTERISTICS							
On-State Switch Resistance	$R_{DS(ON)}$	I_{OUT} = -200mA, V_{BIAS} = 5V	V_{IN} = 5V		19		mΩ
			V_{IN} = 3.3V		19		mΩ
			V_{IN} = 1.8V		19		mΩ
			V_{IN} = 1.5V		19		mΩ
			V_{IN} = 1.2V		19		mΩ
			V_{IN} = 0.8V		19		mΩ
QUICK DISCHARGE RESISTOR (SGM2566A ONLY)							
Output Shutdown Discharge Resistance	R_{DIS}	V_{IN} = 5V, $V_{EN/FAULT}$ = 0V			265		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{BIAS} = 2.5V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES AND CURRENTS							
V_{BIAS} Quiescent Supply Current	I_{Q_BIAS}	I_{OUT} = 0mA, V_{IN} = $V_{EN/FAULT}$ = V_{BIAS} = 2.5V			9		μA
V_{BIAS} Shutdown Supply Current	I_{SD_BIAS}	$V_{EN/FAULT}$ = GND, V_{OUT} = 0V			0.1		μA
V_{IN} Shutdown Supply Current	I_{SD_IN}	$V_{EN/FAULT}$ = GND, V_{OUT} = 0V	V_{IN} = 2.5V		0.1		μA
			V_{IN} = 1.8V		0.1		
			V_{IN} = 1.5V		0.1		
			V_{IN} = 1.2V		0.1		
			V_{IN} = 0.8V		0.1		
LOGIC LEVEL INPUTS							
EN/FAULT Input Current	$I_{EN/FAULT}$	$V_{EN/FAULT}$ = 5.5V			0.1		μA
EN/FAULT Input Low Voltage	V_{IL}				0.4		V
EN/FAULT Input High Voltage	V_{IH}				1.0		V
RESISTANCE CHARACTERISTICS							
On-State Switch Resistance	R_{DSON}	I_{OUT} = -200mA, V_{BIAS} = 2.5V	V_{IN} = 2.5V		28		mΩ
			V_{IN} = 1.8V		23		mΩ
			V_{IN} = 1.5V		21		mΩ
			V_{IN} = 1.2V		20		mΩ
			V_{IN} = 0.8V		19		mΩ
QUICK DISCHARGE RESISTOR (SGM2566A ONLY)							
Output Shutdown Discharge Resistance	R_{DIS}	V_{IN} = 2.5V, $V_{EN/FAULT}$ = 0V			270		Ω

SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
V_{IN} = $V_{EN/FAULT}$ = V_{BIAS} = 5V, T_A = +25℃, unless otherwise noted.						
Turn-On Time	t_{ON}	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		1420		μs
Turn-Off Time	t_{OFF}	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		9		
V_{OUT} Rise Time	t_R	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		2170		
V_{OUT} Fall Time	t_F	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		4		
ON Delay Time	t_D	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		260		
V_{IN} = 0.8V, $V_{EN/FAULT}$ = V_{BIAS} = 5V, T_A = +25℃, unless otherwise noted.						
Turn-On Time	t_{ON}	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		240		μs
Turn-Off Time	t_{OFF}	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		10		
V_{OUT} Rise Time	t_R	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		320		
V_{OUT} Fall Time	t_F	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		4		
ON Delay Time	t_D	R_L = 10Ω, C_{OUT} = 0.1μF, C_T = 1000pF		90		

PARAMETER MEASUREMENT INFORMATION

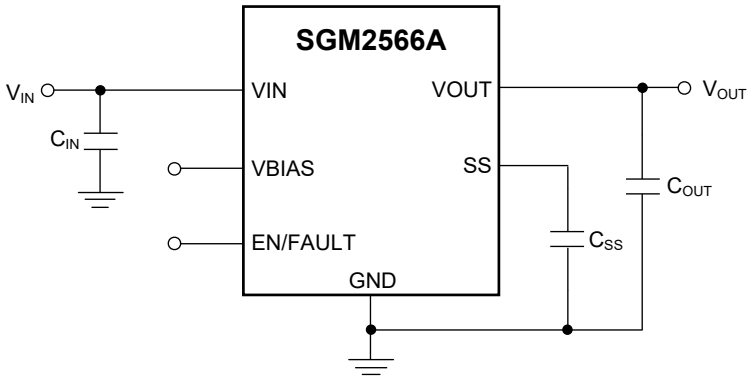


Figure 2. Test Circuit

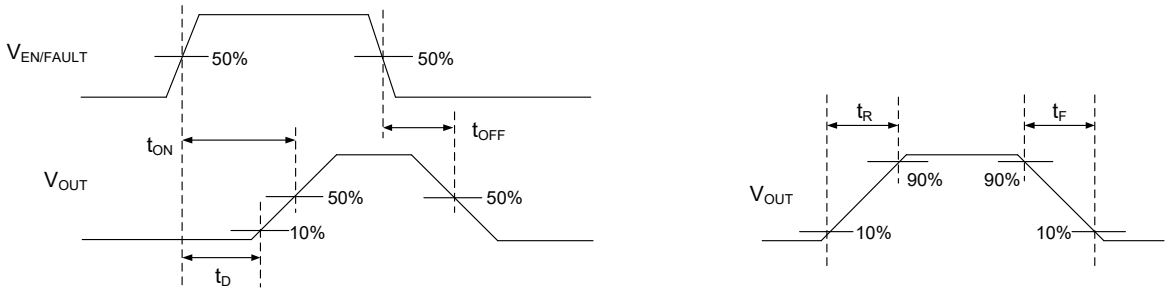


Figure 3. Response Time to Short-Circuit Waveform

FUNCTIONAL BLOCK DIAGRAM

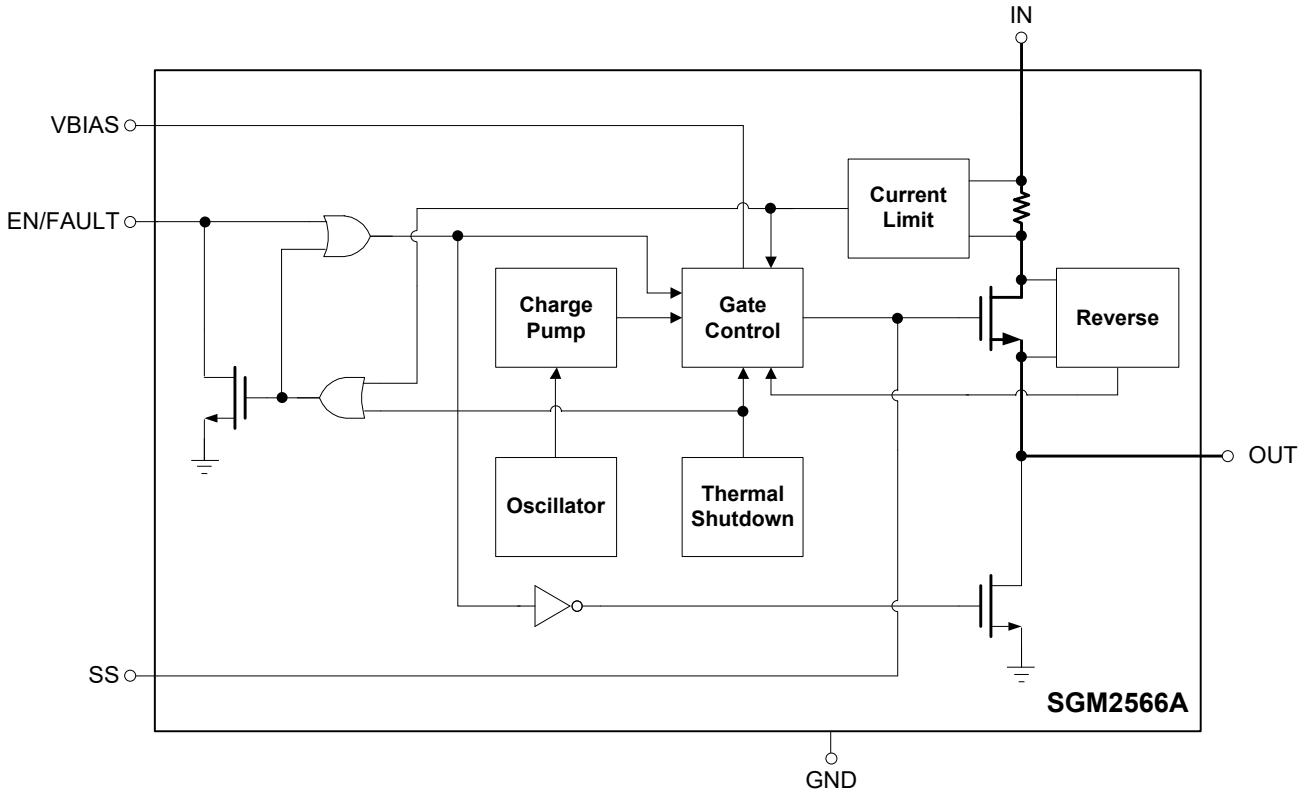


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM2566A and SGM2566B devices are single channel, 6A load switch in a TDFN package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise-time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

Adjustable Rise Time

A capacitor to GND on the SS pin sets the slew rate. An approximate formula for the relationship between SS and slew rate when V_{BIAS} is set to 5V is shown in equation 1. This equation accounts for 10% to 90% measurement on V_{OUT} and does not apply for SS = 0pF.

$$SR = 0.38 \times SS + 34 \quad (1)$$

where:

- SR is the slew rate (in μs/V)
- SS is the the capacitance value on the SS pin (in pF)
- The units for the constant 34 are μs/V. The units for the constant 0.38 are μs/(V × pF).

Rise time can be calculated by multiplying the input voltage by the slew rate.

Quick Output Discharge (QOD) (Optional)

The SGM2566A includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 265Ω and prevents the output from floating while the switch is disabled.

Low Power Consumption During Off State

The V_{IN} Shutdown supply current is 0.1μA (TYP). Typically, the downstream loads must have a significantly higher off-state leakage current. The load switch allows system standby power consumption to be reduced.

EN/FAULT Pin

EN/FAULT is a dual function bi-directional input or output. Asserting EN/FAULT pin high enables the device. When any of over-temperature protection or over-current protection occurs, the device sinks current from EN/FAULT, pulling the pin down to alert the host (pin as output port). EN/FAULT changes back to an input port, only after the device is released from a protection action.

Reverse-Voltage Protection

The reverse-voltage protection feature turns off the N-channel MOSFET switch whenever the output voltage exceeds the input voltage by 2mV (TYP).

APPLICATION INFORMATION

Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1μF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications.

Output Filter Capacitor

Between VOUT and GND, connect a low-ESR 10μF ceramic capacitor to meet the maximum drop requirement. Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the down-stream connector. This will reduce EMI and improve the transient performance. If long cables are connected to the output terminals, an anti-parallel schottky diode such as BAT54 is suggested to be placed in parallel with the output terminals to absorb the negative ringing due to the cable inductance.

V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$.

Typical Application

This application demonstrates how the SGM2566A and SGM2566B can be used to power downstream modules.

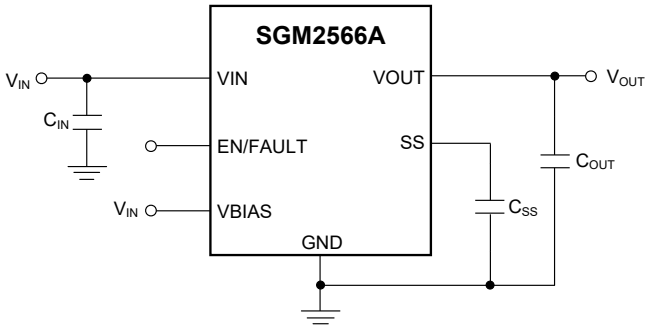


Figure 5. Powering a Downstream Module

Design Requirements

Table 1 shows the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3V
V_{BIAS}	5V
C_{OUT}	22μF
Maximum Acceptable Inrush Current	400mA

Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0V to the set value (3.3V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using equation 2.

$$\text{Inrush Current} = C_{OUT} \times dV/dt \quad (2)$$

where:

- C_{OUT} is the output capacitance
- dV is the output voltage
- dt is the rise time

The SGM2566A and SGM2566B offer adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on. The appropriate rise time can be calculated using the design requirements and the inrush current equation. See equation 3 and equation 4.

$$400mA = 22\mu F \times 3.3V/dt \quad (3)$$

$$dt = 181.5\mu s \quad (4)$$

To ensure an inrush current of less than 400mA, choose a SS value that yields a rise time of more than 181.5μs. See the oscilloscope captures in the Application Curves section for an example of how the SS capacitor can be used to reduce inrush current.

APPLICATION INFORMATION (continued)

Thermal Considerations

The maximum IC junction temperature must be restricted to +125℃ under normal operating conditions.

To calculate the maximum allowable dissipation, $P_{D(MAX)}$ for a given output current and ambient temperature, use equation 5 as a guideline:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where:

$P_{D(MAX)}$ is the maximum allowable power dissipation

$T_{J(MAX)}$ is the maximum allowable junction temperature (+125℃ for the SGM2566A and SGM2566B)

T_A is the ambient temperature of the device

θ_{JA} = junction to air thermal impedance. This parameter is highly dependent upon board layout.

See layout recommendation; notice that the thermal vias are located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5V to 5.5V and a V_{IN} range of 0.8V to V_{BIAS}.

Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The SS trace must be as short as possible to avoid parasitic capacitance.

Layout Example

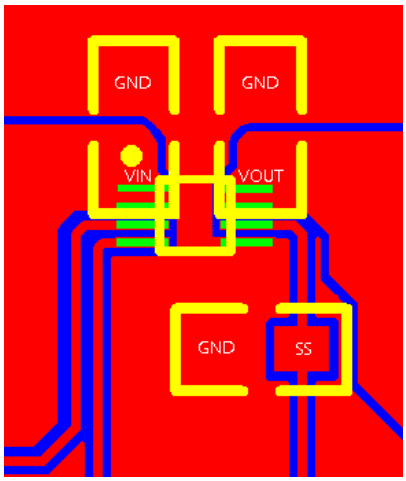
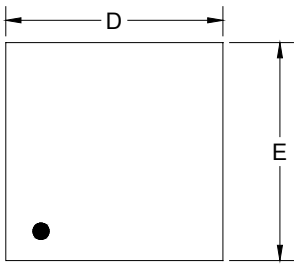


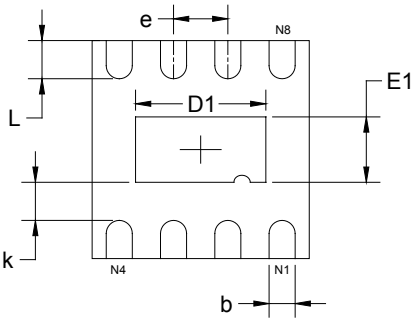
Figure 6. Layout Recommendation

PACKAGE OUTLINE DIMENSIONS

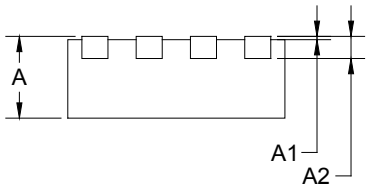
TDFN-2×2-8L



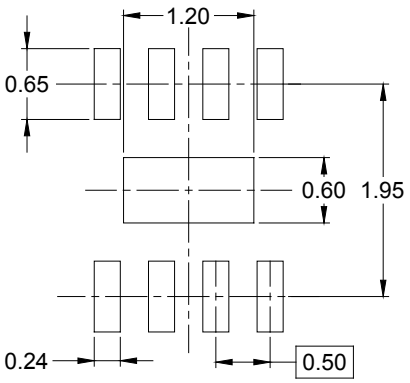
TOP VIEW



BOTTOM VIEW



SIDE VIEW

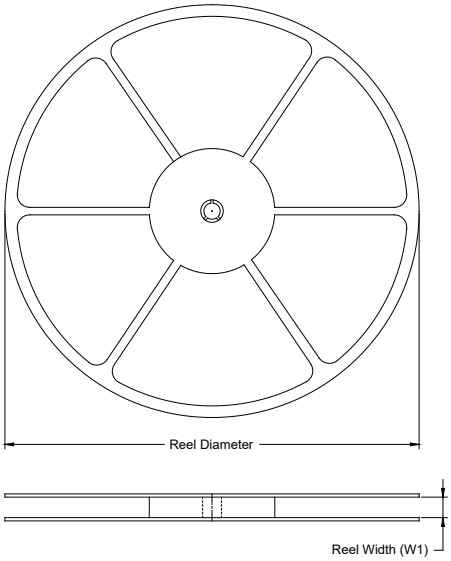


RECOMMENDED LAND PATTERN (Unit: mm)

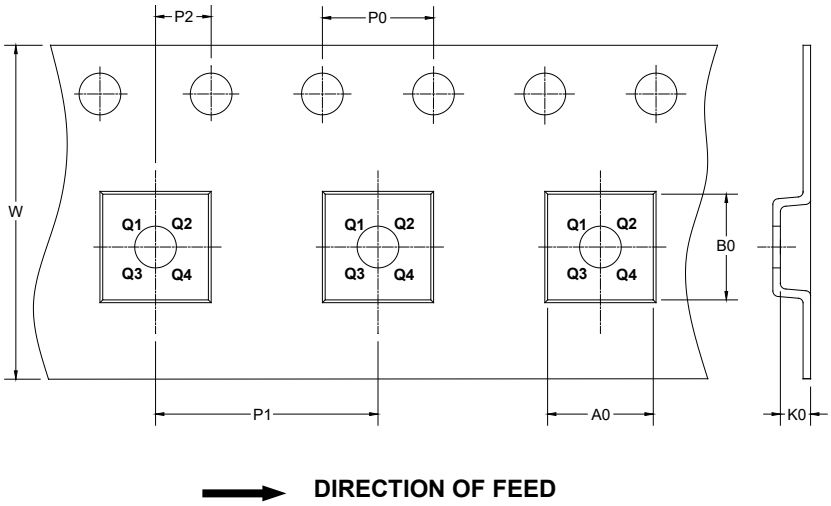
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.250	0.450	0.010	0.018

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



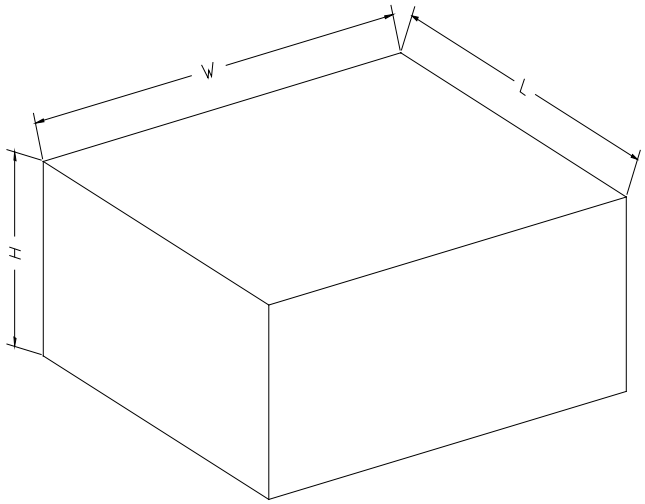
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8L	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002