TPS342x Low-Power, Push-Button Controllers With Configurable Delay

1 Features

- Very Small Package: 1.45-mm × 1.00-mm SON
- Operating Range: 1.6 V to 6.5 V
- Single (TPS3422) or Dual (TPS3420 and TPS3421) Push-Button Inputs
- Low Supply Current: 250 nA (Typical)
- Two-State Logic, User-Selectable Input Delay:
  - For Example: 7.5 s and 0 s
  - Multiple Timing Options Available
- Fixed Time-out Pulse at $\overline{RST}$ (TPS3421 and TPS3422): 400 ms (Typical)
  - Other Timing Options Available on Request
- Active Low, Open-Drain Output

2 Applications

- Smart Phones
- Tablets, Ultrabooks™
- Gaming Consoles
- Portable Consumers
- Navigation Devices
- Consumer Medical
- Toys

3 Description

The TPS3420, TPS3421, and TPS3422 (TPS342x) are low-current, ultrasmall, push-button reset timers. These devices use a long timing setup delay to provide the intended system reset, and avoid resets from short push-button closures or key presses. This reset configuration also allows for differentiation between software interrupts and hard system resets.

The TPS3420 and TPS3421 monitor two inputs (PB1 and PB2) and output an active-low reset pulse signal ($\overline{RST}$) when both inputs are low for the selected time delay. For the TPS3421, $\overline{RST}$ remains low for a factory-programmed fixed time. For the TPS3420, $\overline{RST}$ remains low until one of the PBx inputs is released. The need for a dedicated reset button is eliminated because two inputs are used to ensure reset. The TPS3422 monitors one input (PB1) and outputs an active-low reset pulse signal ($\overline{RST}$) when PB1 is low for the selected time delay.

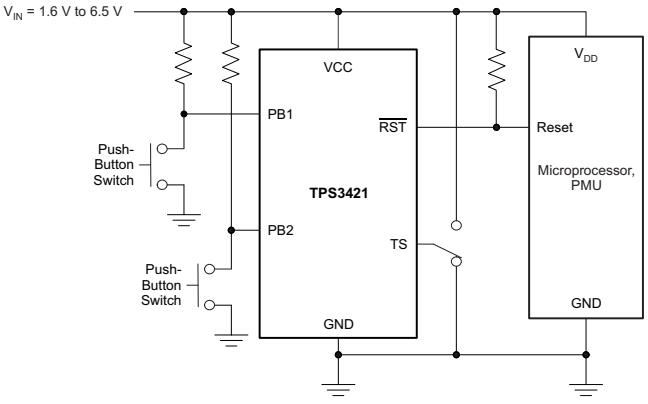
The TPS342x have an open-drain output that can be wire-ORed with other open-drain devices. The TPS342x operate from 1.6 V to 6.5 V over the –40°C to +125°C temperature range, and provide a precise, space-conscious micropower solution for system resetting needs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS342x	USON (6)	1.45 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPS3421 Typical Application Diagram



Standby Supply Current vs Supply Voltage

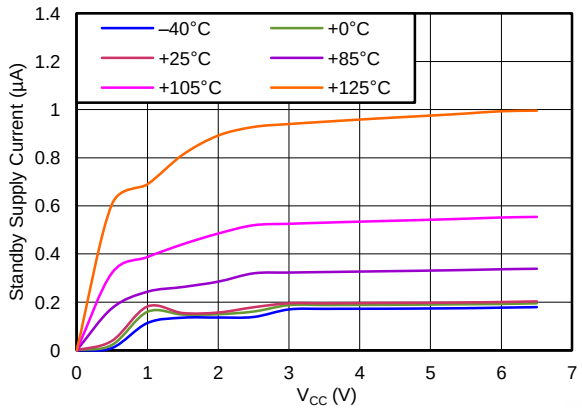


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2012) to Revision B — **Page**

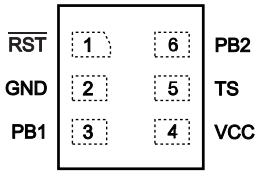
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Typical* to *Low supply current* bullet in *Features* list ... 1
- Added *Typical* to *Fixed time-out pulse* bullet in *Features* list ... 1
- Changed *Pin Configuration and Functions* section; updated table format ... 3
- Changed Absolute Maximum Ratings table; added storage temperature range (T_{stg}) specification ... 4
- Changed *Start-up time* to *start-up delay*, added parametric symbol ... 5

Changes from Original (August 2012) to Revision A — **Page**

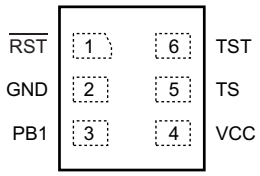
- Changed data sheet from product preview to production data ... 1

5 Pin Configuration and Functions

TPS3420, TPS3421: DRY Package
6-Pin USON
Top View



TPS3422: DRY Package
6-Pin USON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS3420/21	TPS3422		
GND	2	2	—	Ground.
PB1	3	3	I	Push-button input. PB1 and PB2 must be held low for greater than t_{TIMER} time to assert the reset output.
PB2	6	—	I	Second push-button input. PB1 and PB2 must be held low for greater than t_{TIMER} time to assert the reset output.
$\overline{RST}$	1	1	O	Active low, open-drain output. Reset is asserted (goes low) when both PB1 and PB2 are held low for longer than t_{TIMER} time (only PB1 for TPS3422). For TPS3420: Reset is deasserted when either PBx input goes high. For TPS3421,TPS3422: Reset is deasserted after fixed time of t_{RST}.
TS	5	5	I	Time delay selection input. Connect to VCC or GND for different t_{TIMER} selections. In normal operation, the TS pin state should not be changed because it is intended to be permanently connected to either GND or VCC. If switching the TS pin is required, it should be done during power off, or when either PBx input is high.
TST	—	6	—	Connect this pin to GND or VCC during normal device operation.
VCC	4	4	I	Supply voltage input. Connect a 1.6-V to 6.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	VCC	–0.3	7	V
	$\overline{RST}$	–0.3	7	
	PB1, PB2	–0.3	7	
	TS	–0.3	V_{CC} + 0.3	
Current	$\overline{RST}$ pin	–20	20	mA
Temperature (2)	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input supply voltage	1.6		6.5	V
V_{TS}	TS pin voltage	0		V_{CC}	V
V_{PB1}, V_{PB2}	PB1 and PB2 pin voltage	0		6.5	V
V_{RST}	RST pin voltage	0		6.5	V
I_{RST}	RST pin current	0.00035		8	mA

6.4 Thermal Information

THERMAL METRIC (1)		TPS342x DRY (USON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	322	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1185.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	184.7	
ψ_{JT}	Junction-to-top characterization parameter	34.9	
ψ_{JB}	Junction-to-board characterization parameter	182.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	69.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All specifications are over the operating temperature range of –40°C < T_J < 125°C and 1.6 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = 25°C and V_{CC} = 3.3 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Input supply			1.6		6.5	V
I_{CC}	Supply current (standby)	TPS3421, TPS3422	V_{CC} = 3.3 V		250		nA
			V_{CC} = 6.5 V, –40°C < T_J < 85°C			1	µA
			V_{CC} = 6.5 V			3.3	µA
		TPS3420	V_{CC} = 3.3 V		350		nA
			V_{CC} = 6.5 V, –40°C < T_J < 85°C			1.2	µA
			V_{CC} = 6.5 V			3.4	µA
	Supply current (active timer)(1)	TPS3420, TPS3421	PB1, PB2 = 0 V, V_{CC} = 6.5 V		6	12	µA
		TPS3422	PB1, PB2 = 0 V, V_{CC} = 6.5 V		106	136	
V_{IH}	High-level input voltage	TPS3421, TPS3422	PB1, PB2	0.7 V_{CC}			V
		TPS3420	PB1, PB2	0.85			
V_{IL}	Low-level input voltage	TPS3421, TPS3422	PB1, PB2	0		0.3 V_{CC}	V
		TPS3420	PB1, PB2	0		0.3	
R_{PB1}	PB1 internal pullup resistance (TPS3422)				65		kΩ
I_{PB}	Input current (PB1, PB2)	TPS3420 TPS3421	PB1, PB2 = 0 V or V_{CC}	–50		50	nA
		TPS3422	PB1, PB2 = V_{CC}	–50		50	
V_{OL}	Low-level output voltage		V_{CC} ≥ 4.5 V, I_{SINK} = 8 mA			0.4	V
			V_{CC} ≥ 3.3 V, I_{SINK} = 5 mA			0.3	
			V_{CC} ≥ 1.6 V, I_{SINK} = 3 mA			0.3	
$I_{lkg(OD)}$	Open-drain output leakage current		High impedance, V $\overline{RST}$ = 6.5 V	–0.35		0.35	µA

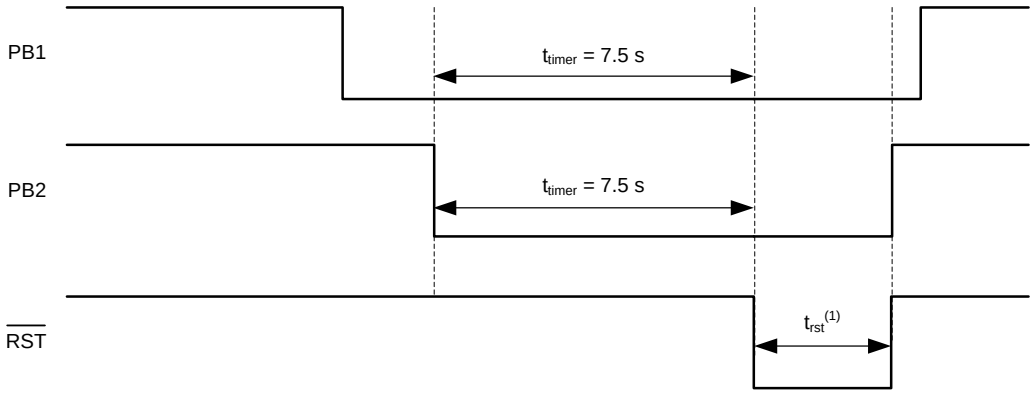
(1) Includes current through pullup resistor between input pin (PB1) and supply pin (VCC) for TPS3422.

6.6 Timing Requirements

All specifications are over the operating temperature range of –40°C < T_J < 125°C and 1.6 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = 25°C and V_{CC} = 3.3 V.

			MIN	TYP	MAX	UNIT
t_{TIMER}	Push-button timer(1)		–20%		20%	s
		TPS3420D: TS = GND	6	7.5	9	
		TPS3420D: TS = VCC	10	12.5	15	
		TPS3421Ey, TPS3422Ey: TS = GND	6	7.5	9	
		TPS3421Ey, TPS3422Ey: TS = VCC		0		
t_{RST}	Reset pulse duration		–20%		20%	ms
		TPS3421xC	64	80	96	
		TPS3421xG	320	400	480	
		TPS3422xG	320	400	480	
t_{DD}	Detection delay (from input to $\overline{RST}$)(2)	For 0-s t_{TIMER} condition		150		µs
t_{SD}	Start-up delay(2)	VCC rising		300		µs

(1) For devices with a 0-second delay while TS = VCC, this option is only for factory testing and is not intended for normal operation. In normal operation, the TS pin should be tied to GND.
(2) For devices with a 0-second delay when TS = VCC, reset asserts in t_{DD} time when both PB inputs go low in this configuration. During start-up, if the PB inputs are low, reset asserts after a start-up time delay. This value is specified by design.



(1) For the TPS3420, t_{RST} is not a fixed time, but instead depends on one of the PB pins going high.

Figure 1. TPS3420 Timing Diagram

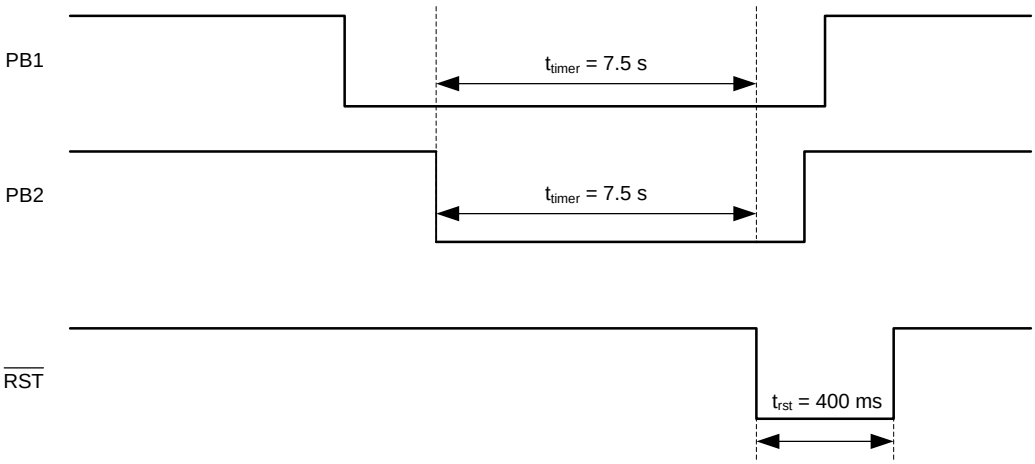


Figure 2. TPS3421 Timing Diagram

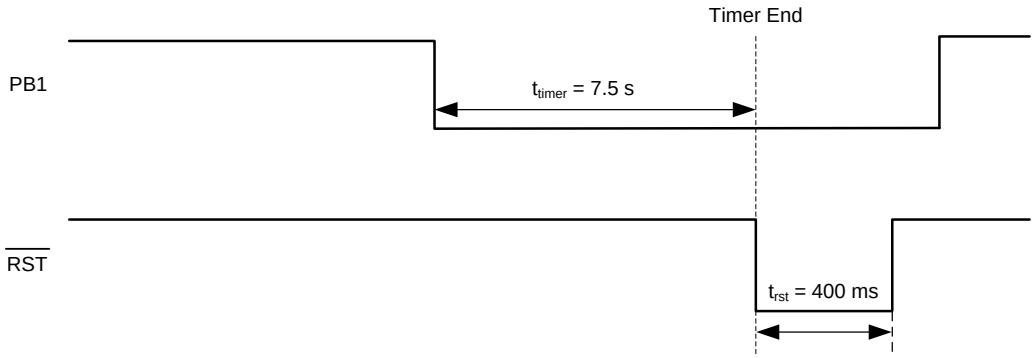


Figure 3. TPS3422 Timing Diagram

6.7 Typical Characteristics

At T_J = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

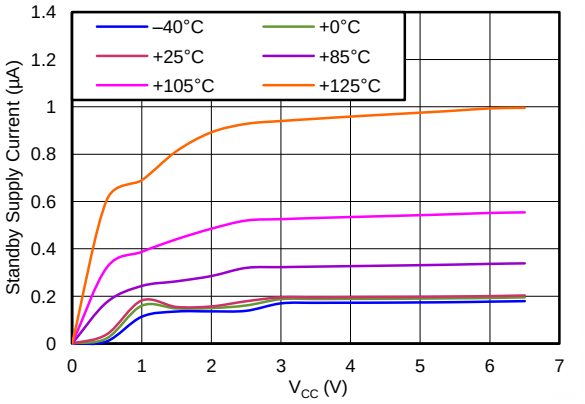


Figure 4. TPS3421: Standby Supply Current vs Supply Voltage

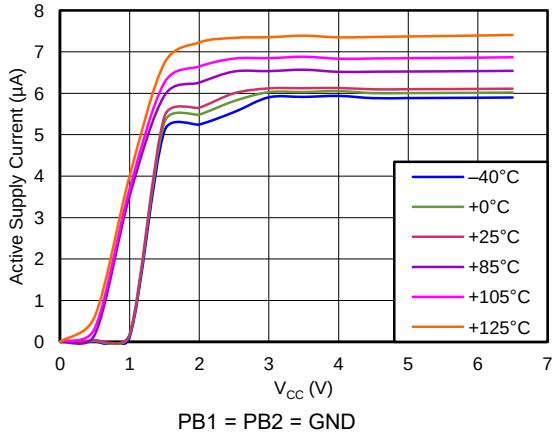


Figure 5. TPS3421: Active Supply Current vs Supply Voltage

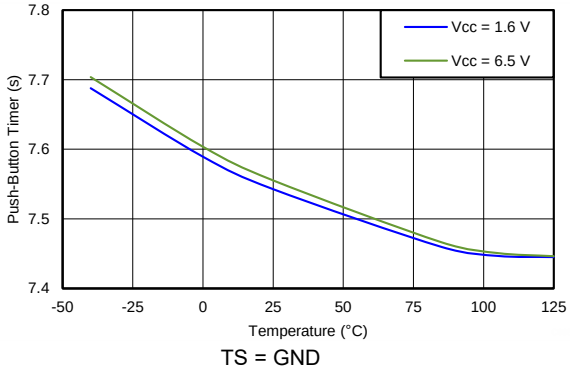


Figure 6. Push-Button Timer vs Temperature

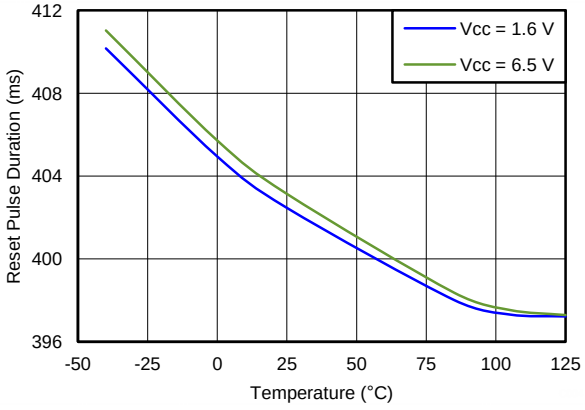


Figure 7. Reset Pulse Duration vs Temperature

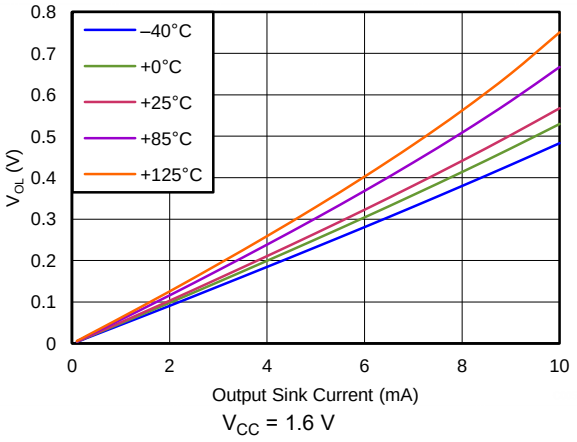


Figure 8. Output Voltage Low vs Output Sink Current

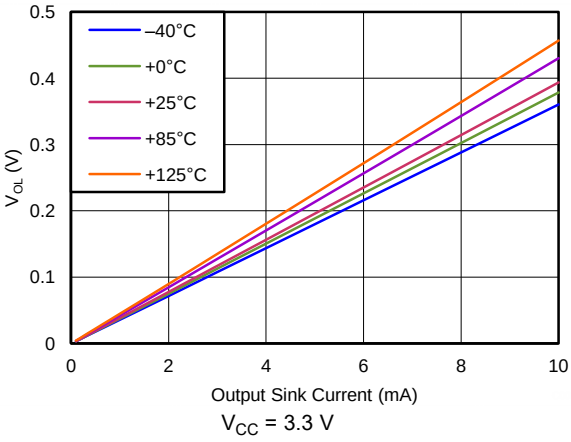


Figure 9. Output Voltage Low vs Output Sink Current

Typical Characteristics (continued)

At T_J = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

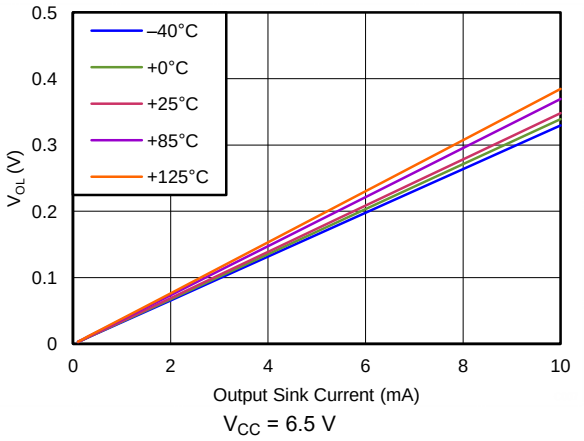


Figure 10. Output Voltage Low vs Output Sink Current

7 Detailed Description

7.1 Overview

The TPS342x are a family of push-button reset devices with an extended setup period that prevents resets from occurring as a result of short-duration switch closures. See Table 1 for details.

The TPS3420 is a dual-channel device with an output that asserts when both inputs (PB1 and PB2) are held low for the push-button timer duration, and deasserts when either input PBx is released.

The TPS3421 is a dual-channel device with an output that asserts when both inputs (PB1 and PB2) are held low for the push-button timer duration, and deasserts after the reset time-out duration.

The TPS3422 is a single-channel device with an output that asserts when the PB1 input is held low for the push-button timer duration, and deasserts after the reset time-out duration.

The TPS342x family also has a TS pin that selects between two different push-button timing options by connecting the pin to either GND or V_{CC}.

Table 1. Device Family Options

DEVICE	CHANNELS	INPUT	RESET BEHAVIOR (DEASSERTION)
TPS3420	2	NMOS-based threshold	Input (PBx) dependent
TPS3421	2	External pullup to VCC	Fixed pulse
TPS3422	1	Internal pullup	Fixed pulse

7.2 Functional Block Diagrams

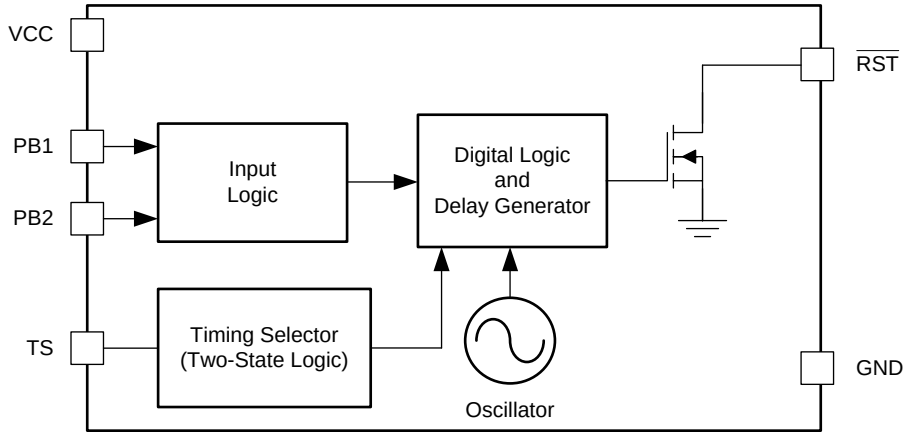


Figure 11. TPS3420 Block Diagram

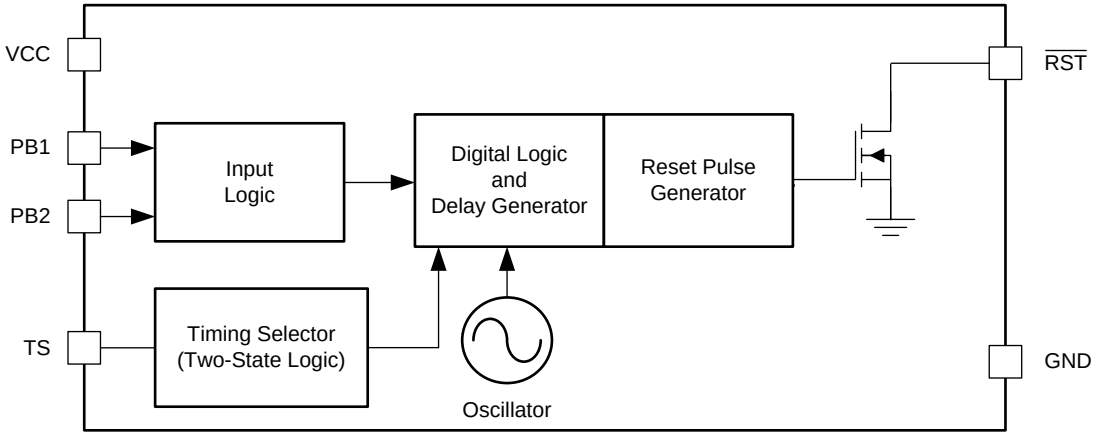


Figure 12. TPS3421 Block Diagram

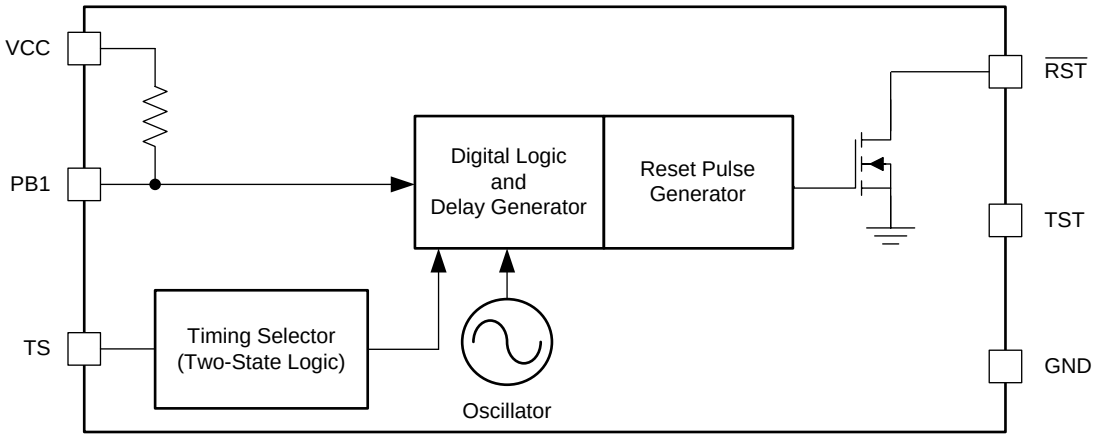


Figure 13. TPS3422 Block Diagram

7.3 Feature Description

7.3.1 Push-Button Timer Selection (TS)

The TPS342x offer two different push-button timer options (t_{TIMER}) for system flexibility with the use of the TS pin. Connect the TS pin to either GND or VCC for two different timing options, as shown in Table 2.

Table 2. Push-Button Timer Option Examples

PRODUCT	PUSH-BUTTON TIMER		RESET PULSE
	TS = VCC	TS = GND	
TPS3420DDRYR/T	12.5 s	7.5 s	N/A
TPS3421EGDRYR/T	0 s	7.5 s	400 ms
TPS3422EGDRYR/T	0 s	7.5 s	400 ms

During normal operation, the TS pin state should not be changed because TS is intended to be permanently connected to either ground or VCC. The state of the TS pin is checked during power up and when either PBx input is high. Therefore, if a different timing option is desired, the state must be changed during power off, or when either PBx input is high, to avoid false operation.

7.3.2 Inputs

This section discusses the inputs of the TPS342x devices.

7.3.2.1 TPS3420 Inputs (PB1, PB2)

The TPS3420 has two NMOS-based threshold inputs (PB1, PB2) with a $V_{IH} \geq 0.85$ V, and a $V_{IL} \leq 0.3$ V. When input conditions are met (that is, when both inputs are simultaneously held low for the push-button timer period, t_{TIMER}), the device asserts a reset low, as shown in Figure 1. Reset deassertion occurs when either input goes high. The reset pulse occurs only one time after each valid input condition. At least one input pin must be released (goes high) and then driven low for the t_{TIMER} period before $\overline{RST}$ asserts again.

7.3.2.2 TPS3421 Inputs (PB1, PB2)

The TPS3421 has two inputs: PB1 and PB2. External pullup resistors to VCC are required to pull the input pins high. When input conditions are met (that is, when both inputs are held low simultaneously for the push-button timer period, t_{TIMER}), the device asserts a single reset pulse of a fixed time (t_{RST}); see Figure 2. Reset deassertion is independent of the inputs because t_{RST} is a fixed time pulse. A reset pulse occurs only one time after each valid input condition. At least one input pin must be released (go high) and then driven low for the t_{TIMER} duration before $\overline{RST}$ asserts again.

7.3.2.3 TPS3422 Inputs (PB1)

The TPS3422 has only one input: PB1. This input has an internal pullup resistor to V_{CC}. When input conditions are met (that is, when the input is held low for the push-button timer period, t_{TIMER}), the device asserts a single reset pulse of a fixed time (t_{RST}); see Figure 3. Reset deassertion is independent of the input because t_{RST} is a fixed time pulse. A reset pulse occurs only one time after each valid input condition. The input pin must be released (go high) and then driven low for the t_{TIMER} period before $\overline{RST}$ asserts again.

7.3.3 Output ($\overline{RST}$)

The TPS342x have an open-drain output. A pullup resistor must be used to hold the line high when the output is in a high-impedance state (not asserted). By connecting a pullup resistor to the proper voltage rail, the output can be connected to other devices at correct interface voltage levels. The TPS342x output can be pulled up to 6.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pullup resistor values. The pullup resistor value is determined by V_{OL}, sink current capability, and output leakage current ($I_{lkg(OD)}$). These values are specified in *Electrical Charactersitcs*.

The *Inputs (PB1, PB2)* describes how the output is asserted or deasserted. See Figure 1 (TPS3420), Figure 2 (TPS3421), or Figure 3 (TPS3422) for a timing diagram that describes the relationship between the PB1 and PB2 inputs and the output. Figure 14 shows the TPS3421 reset timing.

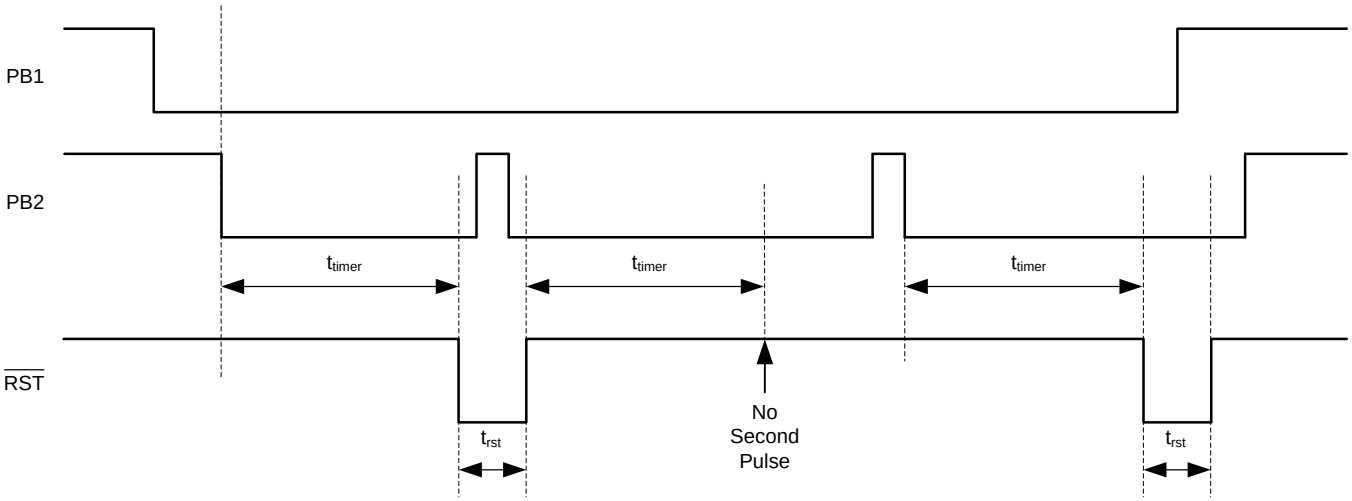


Figure 14. TPS3421 Reset Timing Diagram

Any change in input condition is detected after reset is deasserted. If input PB1 or PB2 has a pulse (low-to-high-to-low) during the t_{RST} period, the change is not recognized by the device. If input PB1 or PB2 go high during the t_{RST} period, the change is detected after reset is deasserted.

7.4 Device Functional Modes

7.4.1 Normal Operation (V_{DD} > 1.6 V)

When the voltage on VDD is greater than 1.6 V ($V_{DD(min)}$) for approximately 300 µs (t_{SD}), the $\overline{RST}$ signal corresponds to the state of the PB1 and PB2 pins; see Table 1.

7.4.2 Below $V_{DD(min)}$ (1.6 V > V_{DD} > 1.3 V)

When the voltage on VDD is less than 1.6 V but greater than 1.3 V (typical), the $\overline{RST}$ signal corresponds to the state of the PB1 and PB2 pins; however, the electrical specifications in the *Electrical Characteristics* and *Timing Requirements* tables do not apply when V_{DD} < $V_{DD(min)}$.

7.4.3 Power-On Reset (V_{DD} < 1.3 V)

When the voltage on VDD is lower than 1.3 V (typical), the $\overline{RST}$ output should be high-impedance. However, it is not ensured to be in a high impedance state under all conditions.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS342x family of devices are small, low-current, push-button reset timers. These devices use a long timing setup delay to provide the system reset signals, and avoid resets from short push-button closures. This reset configuration allows for differentiation between user inputs and hard system resets. TPS342x uses an open drain output, has an input voltage range of 1.6 V to 6.5 V, and is specified from –40°C to +125°C.

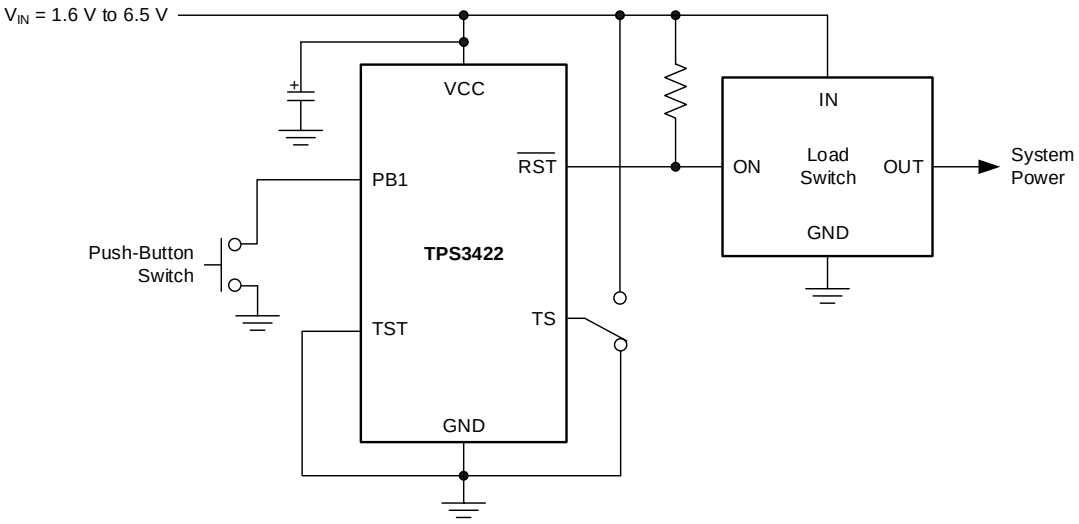
The TPS3420 and TPS3421 are used to monitor two inputs while TPS3422 is used to monitor a single input.

8.2 Typical Applications

8.2.1 Single Input With Fixed Reset Pulse Duration

If only one input must be monitored to set the state of a logic pin, such as the enable pin of a load switch, use the TPS3422. After a reset event has occurred, $\overline{RST}$ is held low for a fixed amount of time (t_{RST}) regardless of the state of the PB1 pin.

An application diagram is shown in Figure 15.



A. Connect TS to VCC or ground for different PB time delays.

Figure 15. TPS3422 Application Diagram

8.2.1.1 Design Requirements

Table 3 lists the design requirements for Figure 15.

Table 3. Design Requirements and Results

DESIGN REQUIREMENTS	DESIGN RESULT
Single input	PB1
Does not react to input signal less than 5 s	6 s (minimum)
Reset pulse greater than 240 ms	320 ms (minimum)
I_{CC} < 5 µA	3.3 µA (maximum)

8.2.1.2 Detailed Design Procedure

When the output switches to the high-*Z* state, the rise time of the $\overline{RST}$ node depends on the pullup resistance and the capacitance on that node. Choose pullup resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 1-kΩ to 1-MΩ resistors are a good choice for low-capacitive loads.

8.2.1.3 Application Curve

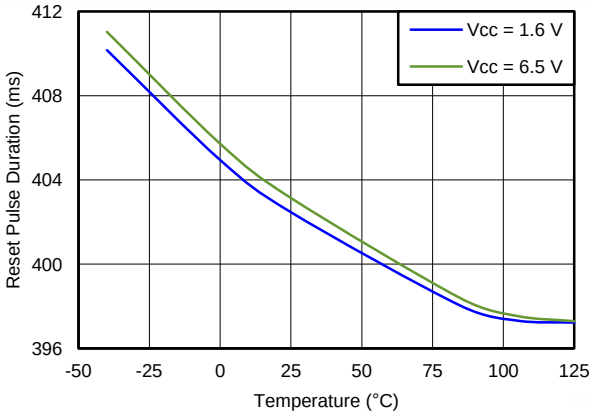
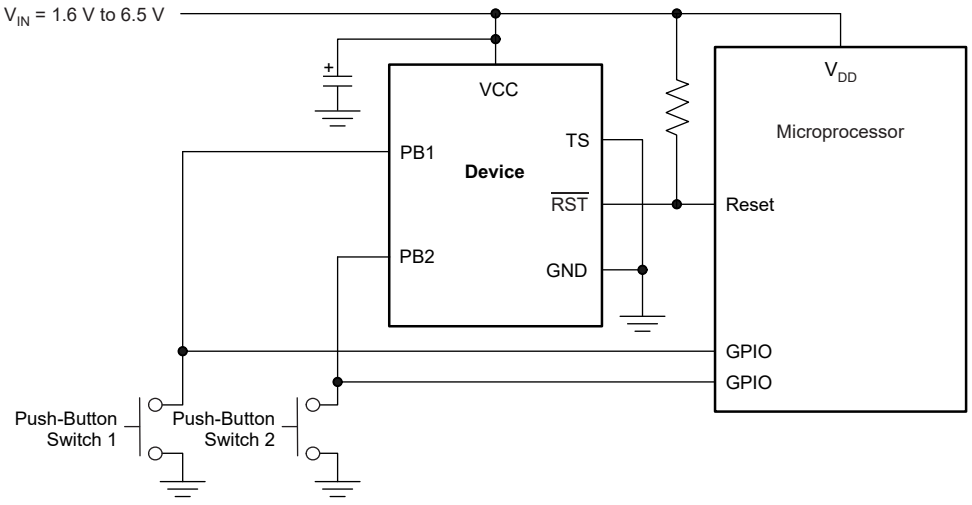


Figure 16. Reset Pulse Duration vs Temperature

8.2.2 Dual Input Applications

If two inputs must be monitored to set the state of a microprocessor reset pin, either the TPS3420 or the TPS3421 can be used. The system functionality determines which device to use. Use the TPS3420 if $\overline{RST}$ must be held low until the signal on one of the PBx pins transitions to a logic high state. Use the TPS3421 if $\overline{RST}$ should only be held low for a fixed amount of time (t_{RST}) regardless of the state of the PBx pins.

An application diagram that is suitable for either the TPS3420 and the TPS3421 is shown in Figure 17.



A. Connect TS to VCC or ground for different PB time delays. Connect one PB input to ground for use as a single channel.

Figure 17. TPS3420 or TPS3421 Application Diagram

8.2.2.1 Design Requirements

Table 4 lists the design requirements for Figure 17.

Table 4. Design Requirements and Results

DESIGN REQUIREMENTS	DESIGN RESULT	
	TPS3420	TPS3421
Dual input	PB1 and PB2	PB1 and PB2
Does not react to input signal less than 5 s	6 s (minimum)	6 s (minimum)
Reset pulse greater than 140 ms	Depends on PBx timing	320 ms (minimum)
Reset pulse ends after at least one input goes high	True	Does not depend on PBx timing

8.2.2.2 Detailed Design Procedure

Determine which version of the TPS342x family best suits the functional performance required.

When the output switches to the high-*Z* state, the rise time of the $\overline{RST}$ node depends on the pullup resistance and the capacitance on that node. Choose pullup resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 1-kΩ to 1-MΩ resistors are a good choice for low-capacitive loads.

8.2.2.3 Application Curve

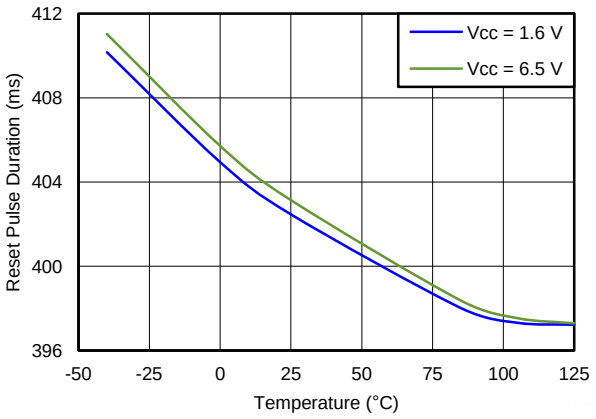


Figure 18. Reset Pulse Duration vs Temperature

8.2.3 Latched Reset Signal

Some applications require the reset signal ($\overline{RST}$) to be latched and only change state after a second low input signal is received. To achieve a latched version of the $\overline{RST}$ signal, a D-flip-flop can be used. The output of the D-flip-flop, *Q*, is then connected to the device to be reset.

See Figure 19 for an example of a latched reset signal configuration.

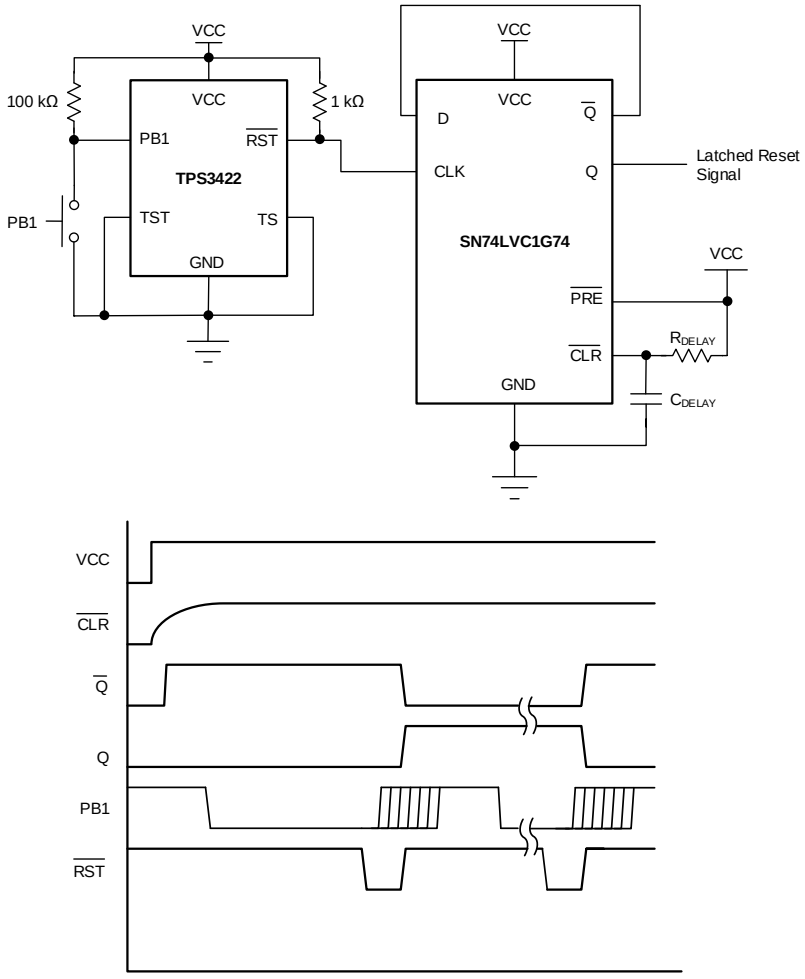


Figure 19. Latched Reset Schematic and Timing Diagram

8.2.3.1 Design Requirements

Table 5 summarizes the design requirements for Figure 19.

Table 5. Design Requirements and Results

DESIGN REQUIREMENTS	DESIGN RESULT
Single input	PB1
Latched output	Q
Does not react to input signal less than 5 s	6 s (minimum)
Reset pulse greater than 200 ms	320 ms (minimum)
I_{CC} < 20 µA	13.3 µA (maximum)

8.2.3.2 Detailed Design Procedure

Once a positive-edge triggered D-flip-flop is chosen, make sure the slew rate of the $\overline{RST}$ signal is fast enough to trigger the flip-flop. For the SN74LVC1G74 shown in Figure 19, TI recommends a 1-kΩ pullup resistor. The RC time constant of the delay cap (C_{DELAY}) and delay resistor (R_{DELAY})should be 10 times the rise time of the input voltage to VCC so that a clear signal is sent to the D-flip-flop, to initialize it into a known state.

8.2.3.3 Application Curve

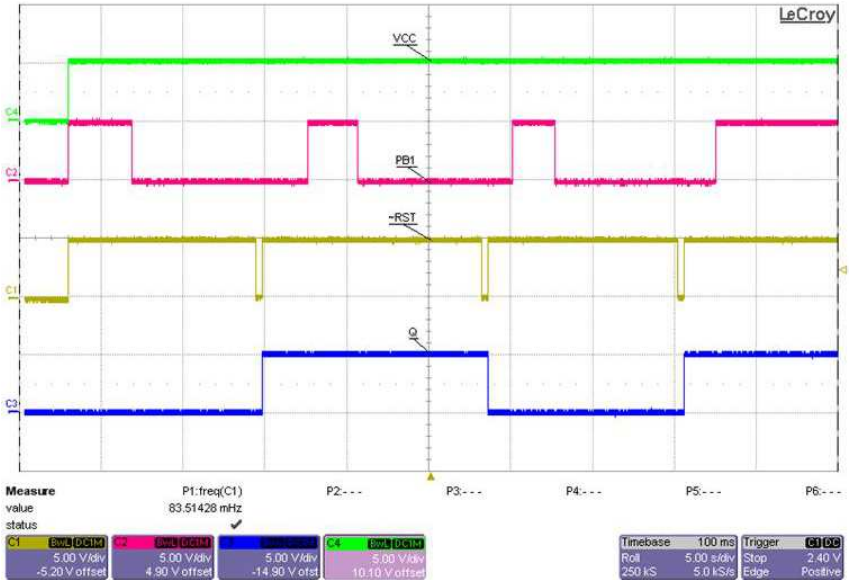


Figure 20. Latched Reset Waveforms Using SN74LVC1G74

9 Power Supply Recommendations

The input power supply should range from 1.6 V to 6.5 V and should be well regulated. Though not required, it is good analog design practice to place a 0.1-µF ceramic capacitor close to the VCC pin.

10 Layout

10.1 Layout Guidelines

Follow these guidelines for laying out the printed circuit board (PCB) that is used for the TPS342x.

- Place the VCC decoupling capacitor close to the device.
- Avoid using long traces for the VCC supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum VCC voltage.

10.2 Layout Example

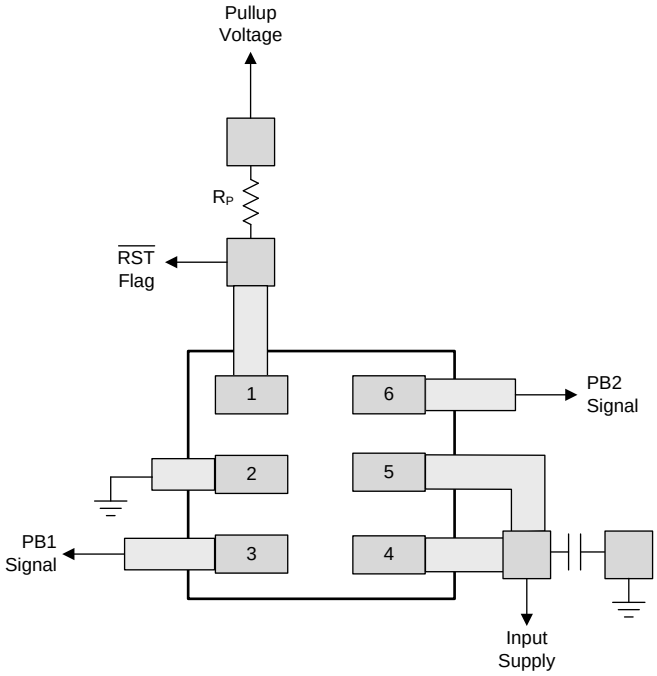


Figure 21. Layout Example (DRY Package)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS3421EG. The TPS3421EGEVM-156 Evaluation Module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS3421EG is available through the product folder under *Tools & Software*.

11.1.2 Device Nomenclature

Table 6. Device Nomenclature

PRODUCT	DESCRIPTION
TPS3420**xzzza** TPS3421**xyzzza** TPS3422**xyzzza**	**x** is the push-button timer option. **y** is the different reset timeout pulse option. **zzz** is the package designator. **a** is the tape or reel quantity.

11.2 Documentation Support

11.2.1 Related Documentation

- *TPS3421EGEVM-156 User's Guide*, SLVU781

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3420	Click here	Click here	Click here	Click here	Click here
TPS3421	Click here	Click here	Click here	Click here	Click here
TPS3422	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

Ultrabooks is a trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

16-Jan-2022

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3420DDRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD	Samples
TPS3420DDRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD	Samples
TPS3421ECDRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB	Samples
TPS3421ECDRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB	Samples
TPS3421EGDRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC	Samples
TPS3421EGDRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC	Samples
TPS3422EGDRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE	Samples
TPS3422EGDRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

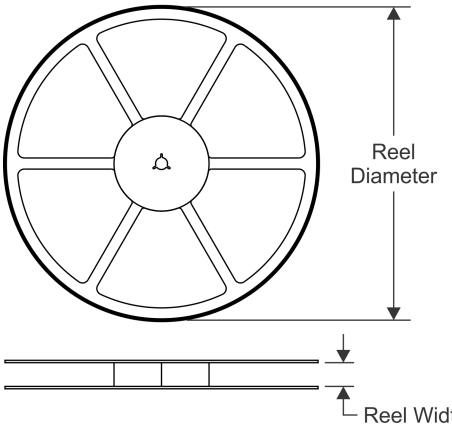
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

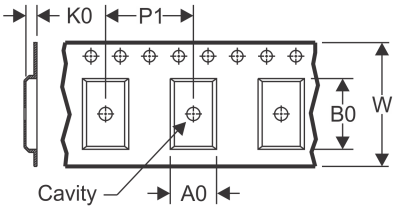
13-Mar-2022

TAPE AND REEL INFORMATION

REEL DIMENSIONS

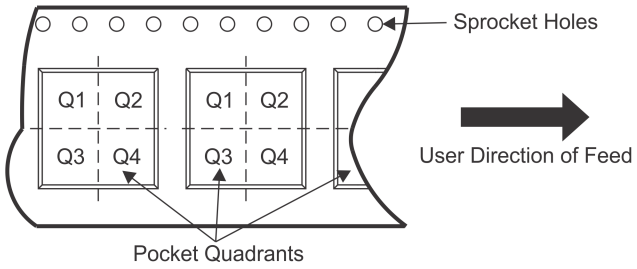


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



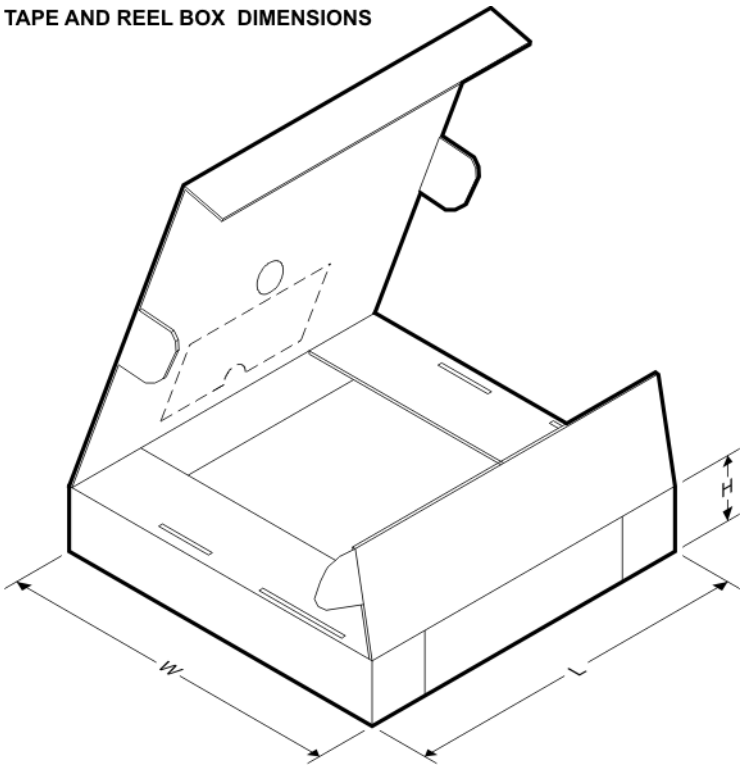
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3420DDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3421ECDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3421ECDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3421EGDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3421EGDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3422EGDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3422EGDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

13-Mar-2022

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3420DDRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3421ECDRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3421ECDRYT	SON	DRY	6	250	200.0	183.0	25.0
TPS3421EGDRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3421EGDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3422EGDRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3422EGDRYT	SON	DRY	6	250	200.0	183.0	25.0

GENERIC PACKAGE VIEW

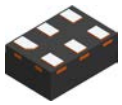
DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

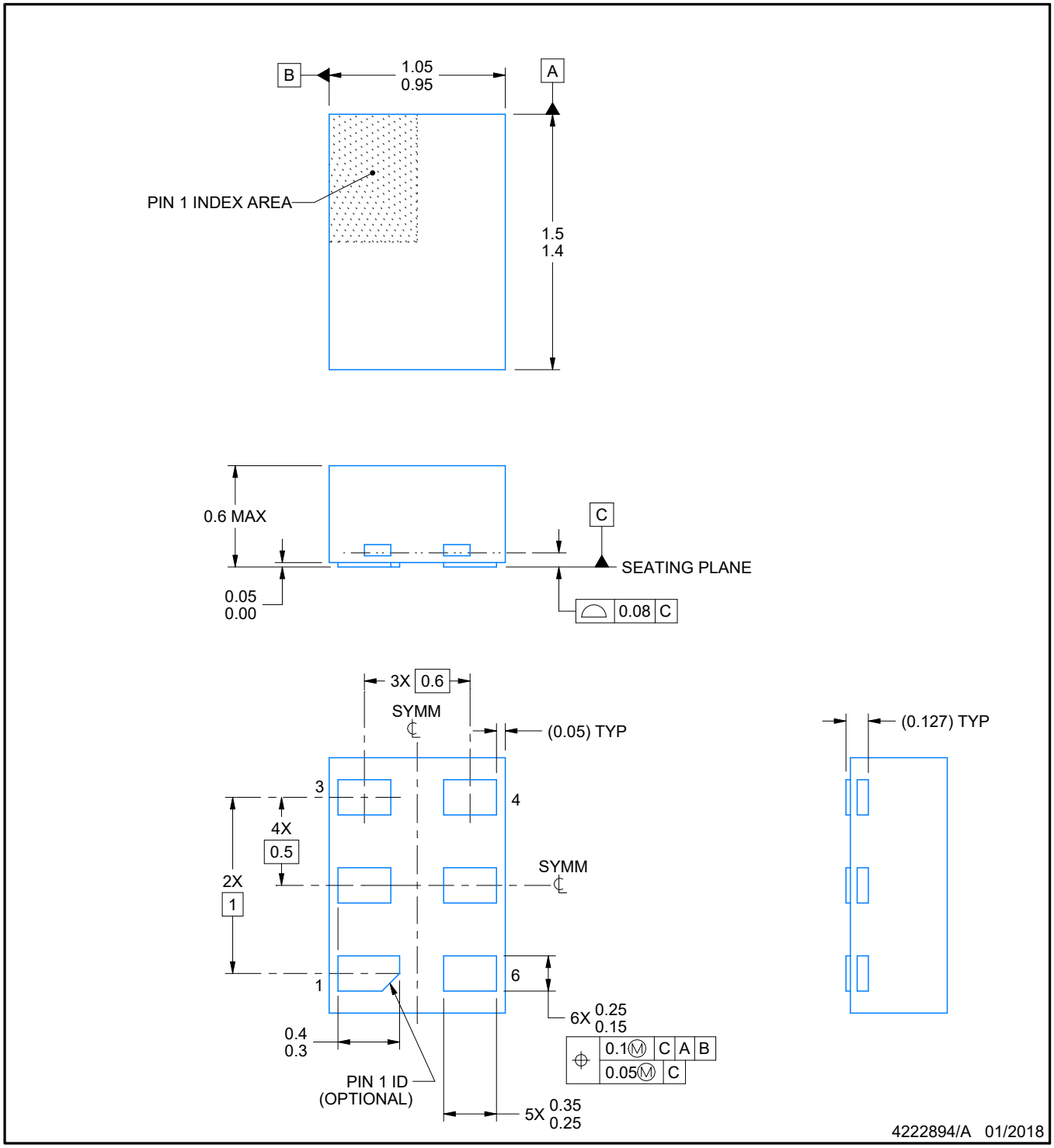
DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

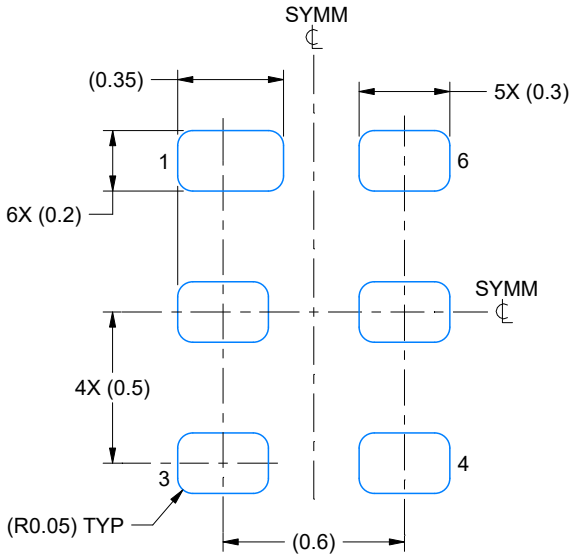
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

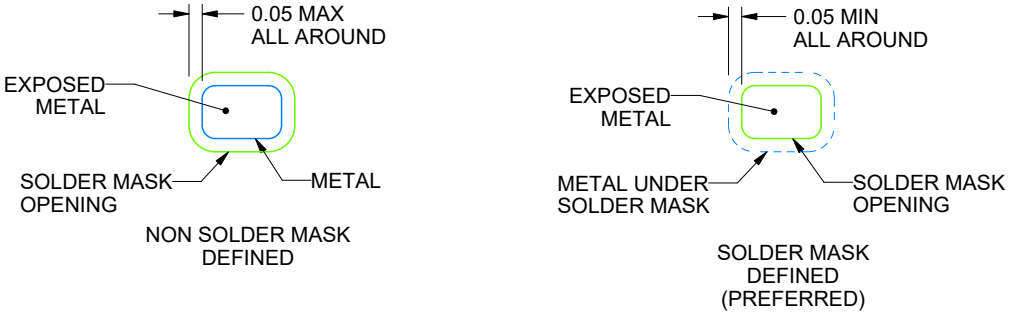
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

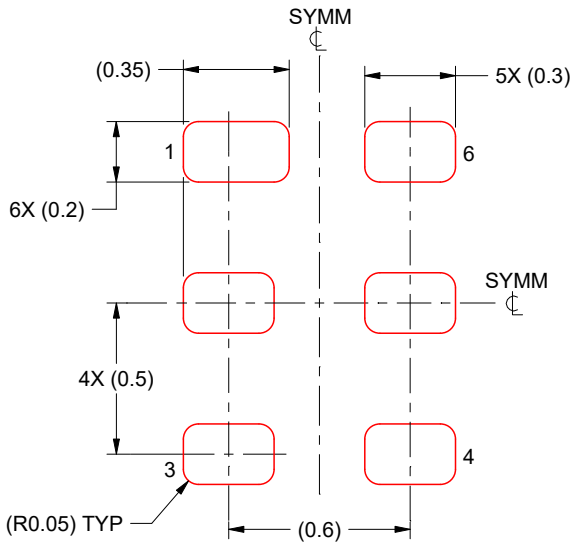
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.