SGM61232
28V, 3A, Buck DC/DC Converter

GENERAL DESCRIPTION

The SGM61232 is a current mode controlled non-synchronous Buck converter with 4V to 28V input range, 3A rated output current and adjustable output voltages from 0.8V up to 25V. A low R_{DSON} N-MOSFET is integrated as high-side switch. Pulse-skip mode (PSM) feature is activated automatically for power-save mode at light loads to improve efficiency. Because of its low shutdown current (1.2μA), this device can be used in battery operated applications. The internal current mode controller with slope compensation allows ceramic capacitors at the output and simplifies compensation network design. The UVLO level can be adjusted (increased) by an external resistor divider. Protection against over-voltage transient is provided to limit the startup or other transient overshoots. Secure operation in overload conditions is ensured by cycle-by-cycle current limit, frequency fold-back and thermal shutdown protection.

The SGM61232 is offered in a Green SOIC-8 (Exposed Pad) package and can operate in the -40℃ to +125℃ ambient temperature range.

FEATURES

- **4V to 28V Input Voltage Range**
- **0.8V Internal Voltage Reference**
- **0.8V to 25V Adjustable Output Voltage Range**
- **Integrated 77mΩ High-side MOSFET Supports up to 3A Continuous Output Current**
- **Fixed 540kHz Switching Frequency**
- **Typical 1.2μA Shutdown Quiescent Current**
- **High Light Load Efficiency**
- **Adjustable Soft-Start to Limit Inrush Current**
- **Programmable UVLO Threshold**
- **Over-Voltage Transient Protection**
- **Cycle-by-Cycle Current Limit**
- **Frequency Fold-Back Protection**
- **Thermal Shutdown Protection**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Industrial Power Supplies
Distributed Power Systems
CPE Equipment
Set-Top Boxes
LCD Displays
Battery Chargers

TYPICAL APPLICATION

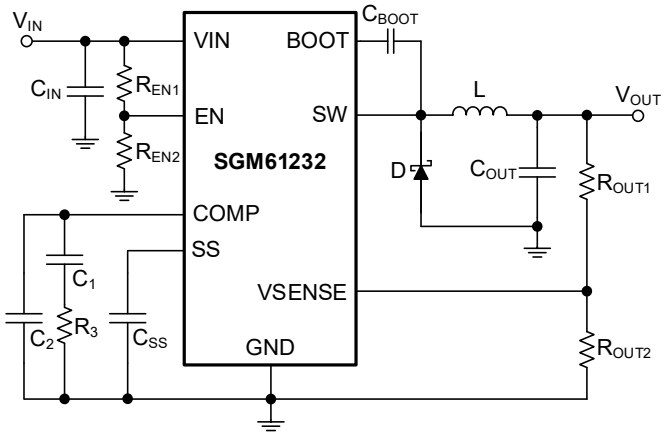


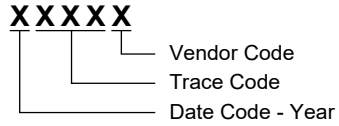
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61232	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61232XPS8G/TR	SGM 61232XPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN Voltage ..... -0.3V to 30V
EN Voltage ..... -0.3V to 6V
VSENSE, COMP, SS Voltages ..... -0.3V to 3V
BOOT-SW Voltage 6V
SW Voltage ..... -0.6V to 30V
SW Voltage 10ns Transient ..... -5V
Package Thermal Resistance
SOIC-8 (Exposed Pad), θ_{JA} ..... 45℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 3000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 4V to 28V
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

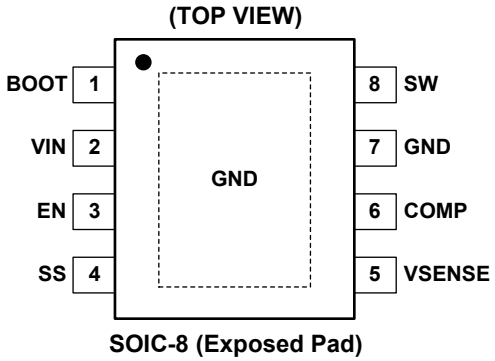
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
1	BOOT	O	Bootstrap Input (for N-MOSFET gate driver supply voltage). Connect it to SW pin with a 0.1μF ceramic capacitor. The MOSFET will turn off if the BOOT capacitor voltage drops below its BOOT-UVLO level to get the capacitor voltage refreshed.
2	VIN	P	Input Supply Voltage. Connect to a 4V to 28V power source.
3	EN	I	Active High Enable Input. Float or pull up to enable, or pull down below 1.25V to disable the device. VIN UVLO level can be programmed using a resistor divider from VIN.
4	SS	I	Soft-Start Input. Connect an external capacitor to SS pin to program the output rise time during startup.
5	VSENSE	I	Transconductance (gm) Error Amplifier (EA) Inverting Input. It is used as the feedback input to sense and regulate V_{OUT}. Output voltage is set by a resistor divider from the output.
6	COMP	O	EA Output (internally connected to the PWM comparator input). Place the compensation network between COMP and GND. The EA output current is injected into this network to create the control voltage (V_C). It will be compared with the compensated sensed current signal to generate the switching pulses (set duty cycle).
7	GND	G	Ground Pin.
8	SW	P	Switching Node of the Converter (source of the internal MOSFET). Connect it to the cathode of the external power diode (catch diode), the bootstrap capacitor and the inductor.
Exposed Pad	GND	G	Exposed Pad. It helps cooling the device junction and must be connected to GND pin for proper operation.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

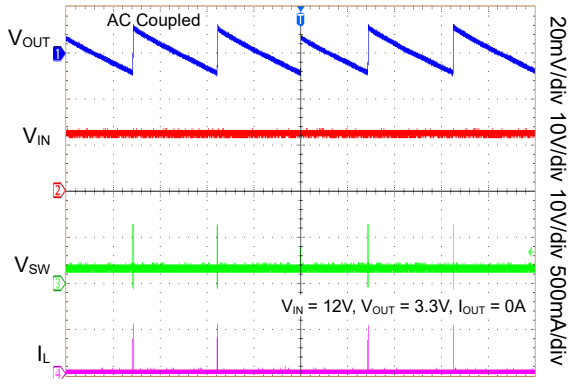
(V_{IN} = 4V to 28V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (VIN Pin)						
Operating Input Voltage	V_{IN}		4		28	V
Internal UVLO Threshold	V_{UVLO}	Rising and falling			3.7	V
Shutdown Supply Current	I_{SHDN}	EN = 0V, V_{IN} = 12V		1.2	2.5	μA
Operating Supply Current (Non-switching)	I_Q	V_{SENSE} = 1V, V_{IN} = 12V		120	180	μA
Enable and UVLO (EN Pin)						
Enable Threshold	V_{EN_th}	Rising and falling		1.25	1.35	V
Input Current	I_{EN}	Enable threshold - 50mV		-0.8		μA
		Enable threshold + 50mV		-3.7		μA
Voltage Reference						
Voltage Reference	V_{REF}	T_J = +25℃	0.78	0.80	0.83	V
High-side MOSFET						
On-Resistance	R_{DSON}	BOOT-SW = 3V, V_{IN} = 4V		85	150	mΩ
		BOOT-SW = 5V, V_{IN} = 12V		77	140	mΩ
Error Amplifier						
Error Amplifier Transconductance	gm	-2μA < I_{COMP} < 2μA, V_{COMP} = 1V		92		μA/V
Error Amplifier DC Gain	V_{ggm}	V_{SENSE} = 0.8V		800		V/V
Error Amplifier Unity Gain Bandwidth	G_{BW}	5pF capacitance from COMP to GND pins		2.7		MHz
Error Amplifier Source/Sink Current	I_{gm}	V_{COMP} = 1V, 100mV input overdrive		±7		μA
Switch Current to COMP Transconductance	GM_{COMP}	V_{IN} = 12V		12		A/V
Power-Save Mode						
Power-Save Mode Switch Current Threshold	I_{L_th}			340		mA
Current Limit						
Current Limit Threshold	I_{LIMIT}	V_{IN} = 12V, T_J = +25℃	4.6	5.5		A
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}			165		℃
Soft-Start (SS Pin)						
SS Charge Current	I_{SS}	V_{SS} = 0.4V		2		μA
SS to VSENSE Matching (Difference)		V_{SS} = 0.4V		10		mV
Switching Frequency						
Switching Frequency	f_{SW}	V_{IN} = 12V, T_J = +25℃	400	540	700	kHz
Minimum Controllable On-Time	t_{ON}	V_{IN} = 12V		105		ns
Maximum Controllable Duty Cycle	D			96		%

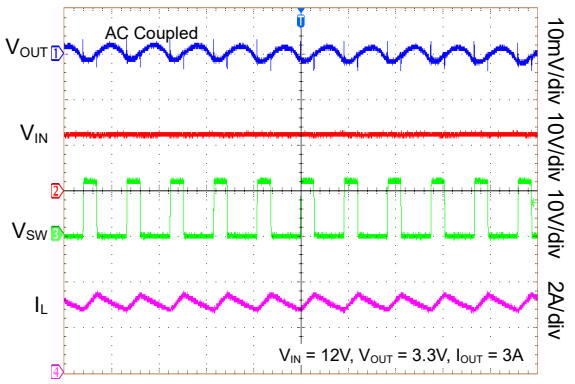
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, unless otherwise noted.

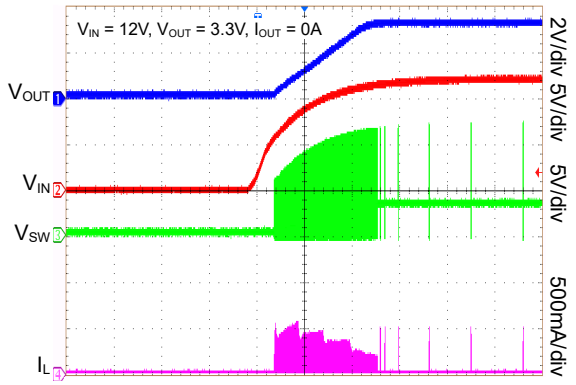
Output Voltage Ripple



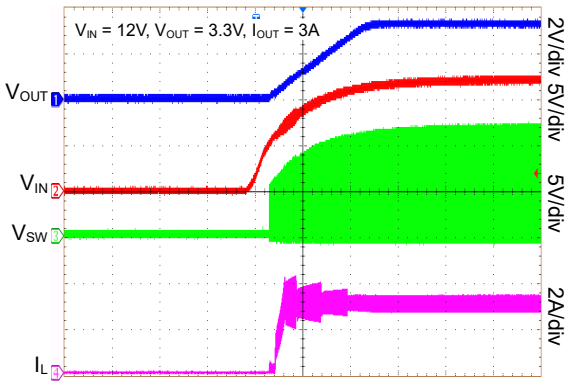
Output Voltage Ripple



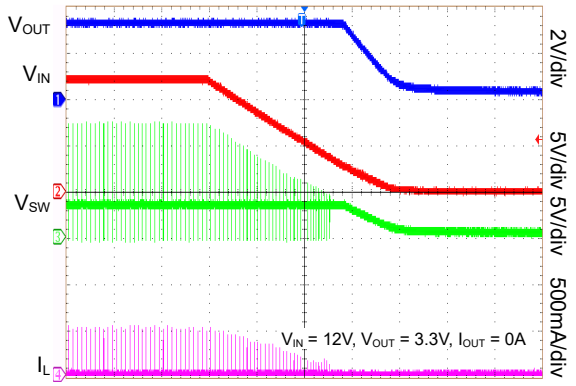
Startup through VIN



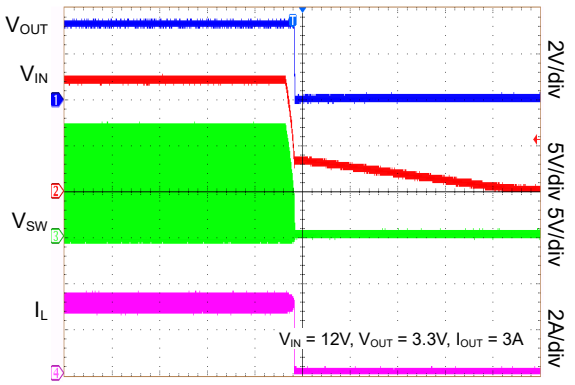
Startup through VIN



Shutdown through VIN



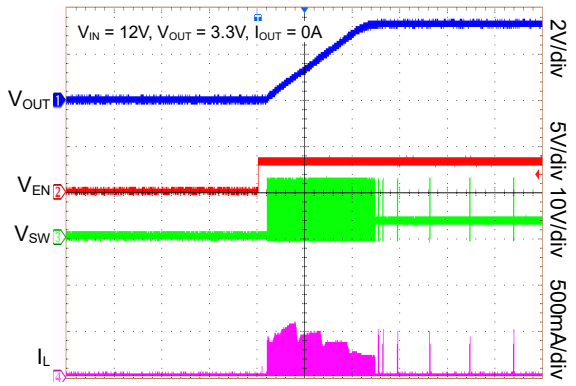
Shutdown through VIN



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

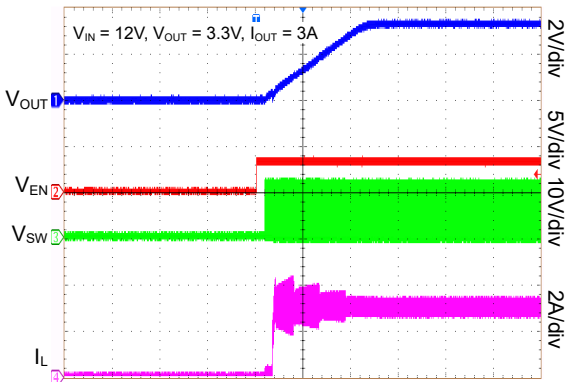
T_J = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, unless otherwise noted.

Startup through EN



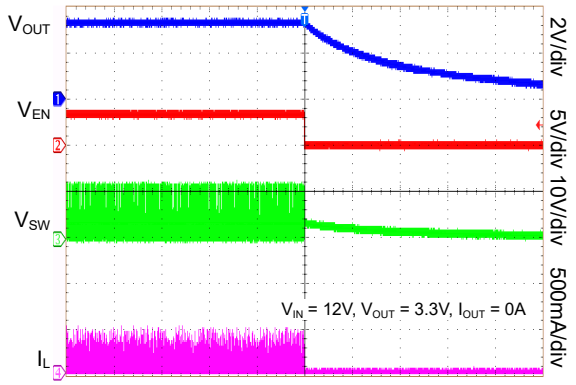
Time (2ms/div)

Startup through EN



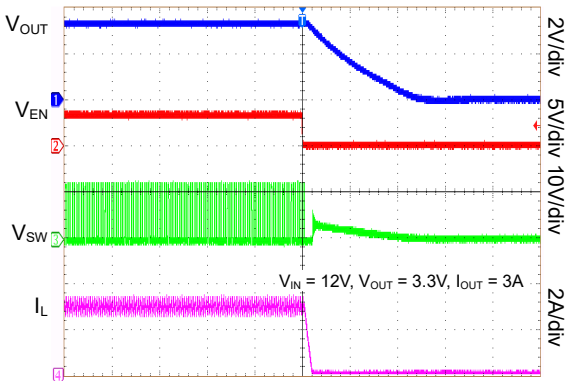
Time (2ms/div)

Shutdown through EN



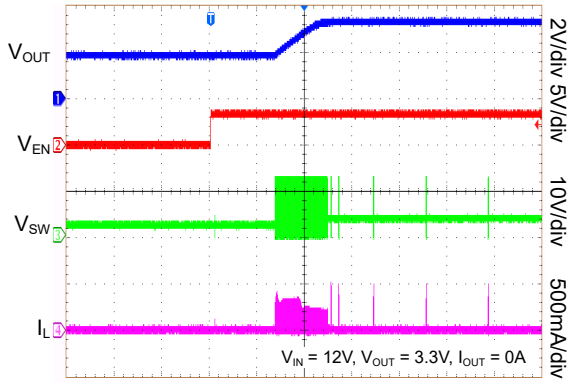
Time (400ms/div)

Shutdown through EN



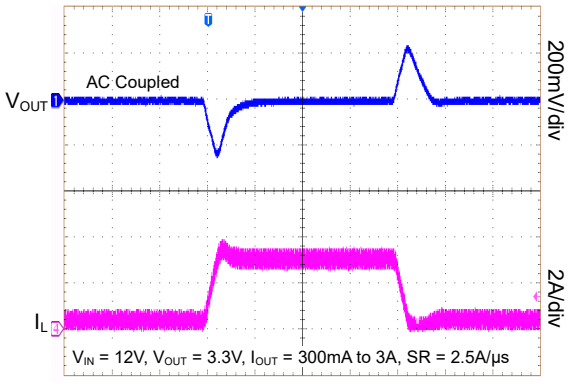
Time (40μs/div)

Pre-biased Startup



Time (2ms/div)

Load Transient Response

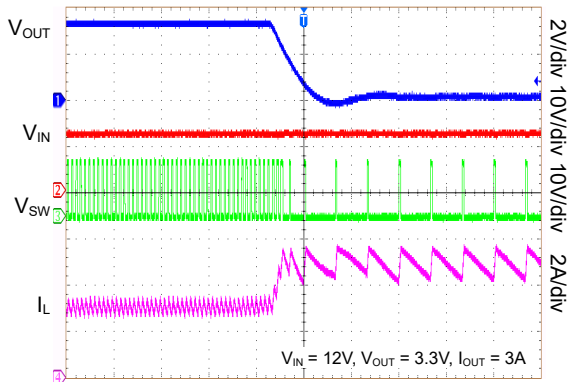


Time (100μs/div)

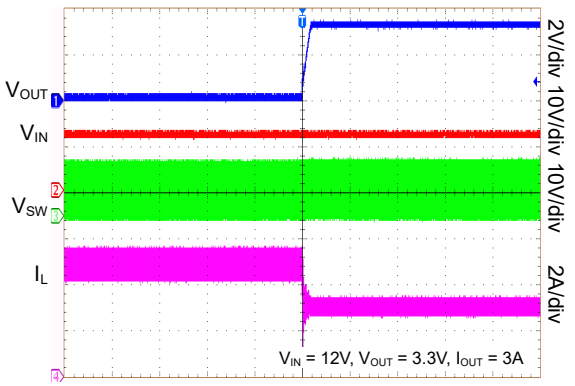
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, unless otherwise noted.

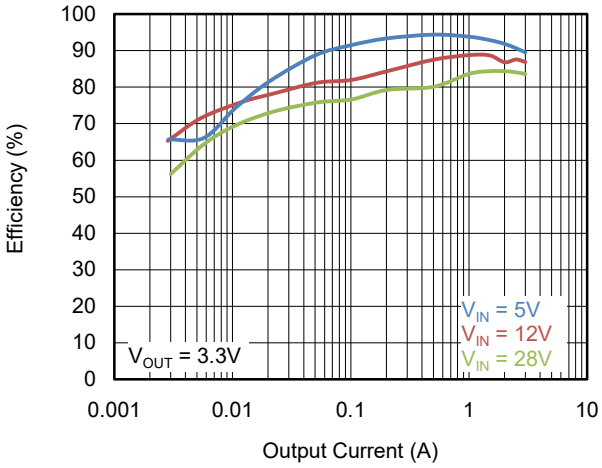
Short-Circuit Entry



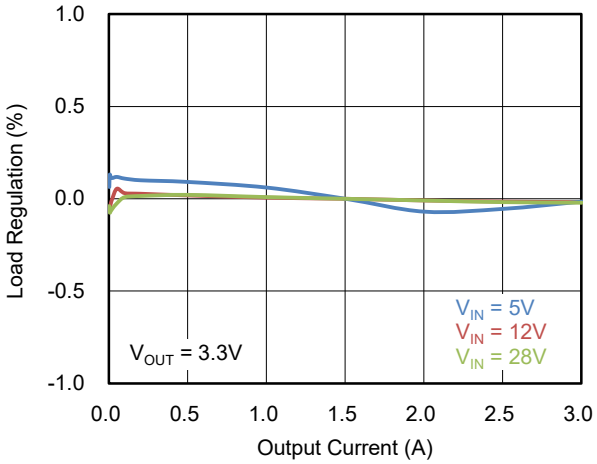
Short-Circuit Recovery



Efficiency vs. Load Current



Load Regulation



FUNCTIONAL BLOCK DIAGRAM

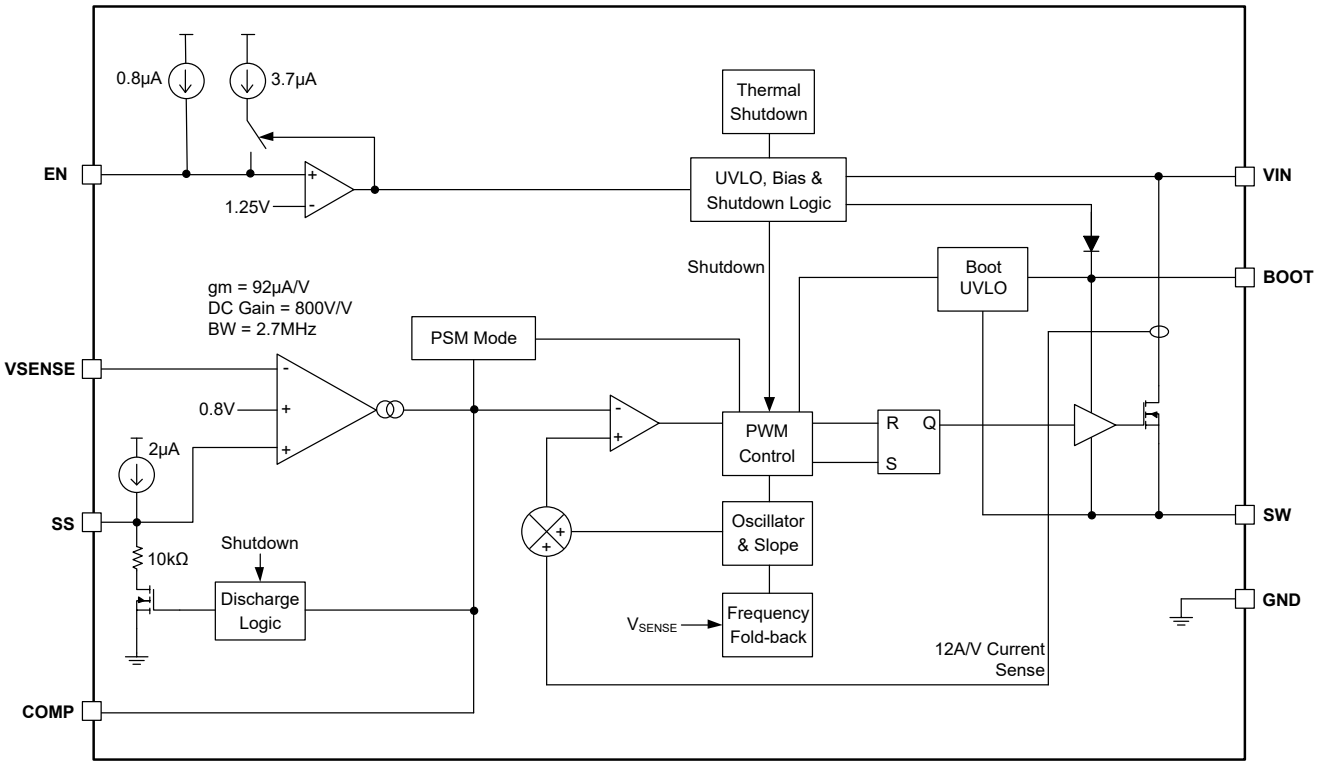


Figure 2. SGM61232 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61232 is a 28V Buck converter with integrated N-MOSFET power switch and 3A continuous output current capability. Using peak current mode control and operating at fixed PWM frequency, this device provides good line and load transient responses with reduced output capacitance and simple compensation.

The minimum operating input voltage of the device is 4V and its nominal frequency is 540kHz. The output voltage can be set down to 0.8V (reference voltage). Typical no-load operating current is 120μA. It reduces to 1.2μA if the device is disabled. The low R_{DSON} high-side switch (77mΩ) allows high operating efficiency.

The EN pin is internally pulled up by a current source that can keep the device enable if EN is floating. It can also be used to increase the input UVLO threshold using a resistor divider.

The bootstrap diode is integrated and only a small capacitor between BOOT and SW pins (C_{BOOT}) is needed for the MOSFET gate driving bias. A separate UVLO circuit monitors C_{BOOT} voltage and turns the switch off if this voltage falls below a preset threshold.

The SS pin internal current source allows soft-start time adjustments with a small external capacitor. This feature provides more flexibility in output filter design.

Light load efficiency is enhanced by a special pulse-skip mode that is activated when the peak inductor current falls below 340mA (TYP).

During startup and over-current, the frequency is reduced (frequency fold-back) to allow easy maintenance of low inductor current. The thermal shutdown provides an additional protection in fault conditions.

Minimum Input Voltage (4V) and UVLO

The recommended minimum operating input voltage is 4V, however, the actual UVLO threshold can be less than this value and the device may operate at voltages below 4V. The UVLO threshold is not specified. If V_{IN} falls below UVLO voltage, the device will stop switching. If the EN pin is left floating or pulled high and V_{IN} exceeds the UVLO threshold, the device will start up with a soft-start.

Enable Input and UVLO Adjustment

An internal current source pull-up keeps the EN pin voltage at high state by default. The device will disable if the EN voltage is externally pulled low. It will also disable if VIN pin voltage falls below its under-voltage lockout threshold. If V_{IN} minimum range is less than V_{OUT} + 2V, an external VIN UVLO adjustment (resistor divider in Figure 3) is recommended to increase the VIN turn-on threshold and add hysteresis to UVLO comparator. Figure 3 shows how UVLO and hysteresis are increased using R_{EN1} and R_{EN2}. A 3.7μA additional current is injected to the divider when EN voltage exceeds V_{EN} = 1.25V to provide hysteresis. Use Equations 1 and 2 to calculate these resistors. V_{START} is the input start (turn-on) threshold voltage and V_{STOP} is the input stop (turn-off) threshold voltage. The selected V_{STOP} threshold must be higher than 4V.

$$R_{EN1} = \frac{V_{START} - V_{STOP}}{3.7\mu A} \quad (1)$$

$$R_{EN2} = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{R_{EN1}} + 0.8\mu A} \quad (2)$$

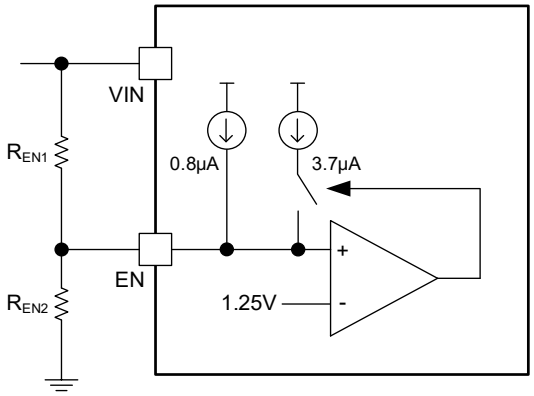


Figure 3. VIN UVLO Adjustment

Bootstrap Gate Driving (BOOT)

An internal regulator provides the bias voltage for gate driver using a 0.1μF ceramic capacitor. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor must have a 10V or higher voltage rating. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low-side diode conducts.

DETAILED DESCRIPTION (continued)

SS Pin and Soft-Start Adjustment

It is recommended to add a soft-start capacitor (C_{SS}) between SS pin and GND to set the soft-start time from 1ms to 10ms for a proper startup. The lower of the SS pin voltage V_{SS} and V_{REF} is applied to the error amplifier to regulate the output. The internal I_{SS} = 2μA current charges C_{SS} and provides a linear voltage ramp on the SS pin. Use Equation 3 to calculate the soft-start time (10% to 90% rise). It is recommended that C_{SS} be less than 27nF.

$$t_{SS}\ (ms) = \frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)} \quad (3)$$

Error Amplifier (EA)

This device uses a transconductance amplifier to compare the sensed output voltage (V_{SENSE}) and the internal reference as error amplifier (EA). The gain of EA amplifier in normal operation is 92μA/V. The output current is injected into the frequency compensation network (between COMP and GND pins) to produce the control signal (V_C) for the PWM comparator.

Slope Compensation

Without implementing some slope compensation, the PWM pulse widths will be unstable and oscillatory at duty cycles above 50%. To avoid sub-harmonic oscillations in this device, an internal compensation ramp is added to the measured switch current before comparing it with the control signal by the PWM comparator.

Power-Save Mode

To reduce light load loss and increase the efficiency, pulse-skip mode (PSM) feature is included in the SGM61232. When the peak inductor current is below 340mA (TYP), the COMP pin voltage (V_C) will be lower than 0.5V (TYP). The device will enter power-save mode in such conditions. In this mode, V_C is internally clamped at 0.5V that inhibits the MOSFET switching. The device can exit PSM if V_C rises above the clamp level and the peak inductor current exceeds 340mA. Since the peak inductor current is the sensed parameter for entering the PSM, the actual load current (DC) threshold for PSM will depend on the output filter.

Over-Current Protection and Frequency Fold-back

Over-current protection (OCP) is naturally provided by current mode control. In each cycle, the high-side (HS) current sensing starts a short time (blanking time) after the HS switch is turned on. The sensed HS switch current is continuously compared with the current limit threshold and when the HS current reaches to that threshold, the HS switch is turned off.

The natural OCP of the peak current mode control may not be able to provide a complete protection when an output short-circuit occurs and an extra protection mechanism for short-circuit is needed. During an output short, inductor current may runaway above over-current limits. Current runaway can saturate the inductor and the current may even increase higher until the device is damaged. This is because the inductor current cannot be reset (volt-second balance) during the off-time. During the output short, only a small negative diode forward voltage appears across the inductor during the off-time. Note that the minimum on-time is limited, and in each cycle, all input voltage appears on the inductor during the minimum on-time. The circuit delays and reaction time makes these conditions even worse, and in each cycle, the current is increased to a new higher level. In the SGM61232, this problem is effectively solved by increasing the off-time during short-circuit by reducing the switching frequency (frequency fold-back). As the output voltage drops and VSENSE voltage falls from 0.8V to 0V, the frequency will be divided by 1, 2, 4, and 8 depending on the drop as shown in Table 1.

Table 1. Frequency Fold-Back with V_{OUT} Drop

Switching Frequency	VSENSE Pin Voltage
540kHz	$V_{SENSE} \geq 0.6V$
540kHz / 2	$0.6V > V_{SENSE} \geq 0.4V$
540kHz / 4	$0.4V > V_{SENSE} \geq 0.2V$
540kHz / 8	$0.2V > V_{SENSE}$

Over-Voltage Transient Protection

When an overload or an output fault condition is removed, large overshoots may occur on the output. The SGM61232 includes a protection circuit to reduce such over-voltage transients. If VSENSE voltage exceeds 109% of the V_{REF} threshold, the MOSFET is turned off. When it returns below 107% of the V_{REF}, the MOSFET is released again.

Thermal Shutdown (TSD)

If the junction temperature (T_J) exceeds +165℃, the TSD protection circuit will stop switching to protect the device from overheating. The device will automatically restart with a power up sequence when the die temperature drops below +140℃.

APPLICATION INFORMATION

A typical application circuit for the SGM61232 as a Buck converter is shown in Figure 4. It is used for converting a 5.5V to 28V supply voltage to a lower voltage level supply voltage (3.3V) suitable for the system.

Typical Application

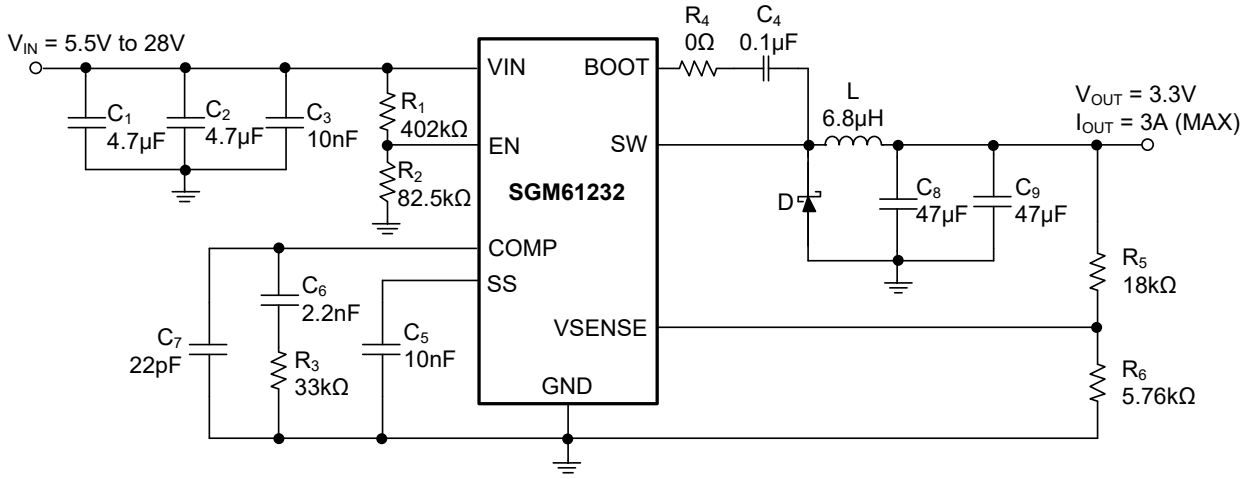


Figure 4. SGM61232 Typical Application Circuit

Requirements

The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	12V nominal, 5.5V to 28V
Start Input Voltage (Rising V_{IN})	7V
Stop Input Voltage (Falling V_{IN})	5.5V
Input Ripple Voltage	360mV, 3% of V_{IN_NOM}
Output Voltage	3.3V
Output Ripple Voltage	33mV, 1% of V_{OUT}
Output Current Rating	3A
Transient Response 1.5A to 3A Load Step	165mV, 5% of V_{OUT}
Operating Frequency	540kHz

Input Capacitors Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61232. At least 3μF of effective capacitance (after deratings) is needed on the VIN input. In some applications, additional bulk capacitance may also be required for the VIN input, for example, when the SGM61232 is more than 5cm away from the input source. The VIN capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 4 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 3A, yields an RMS input ripple current of 1.5A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (4)$$

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. So, two 4.7μF/50V capacitors in parallel are selected for VIN to cover all DC bias, thermal and aging deratings. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 5. In this example, the total effective capacitance of the two 4.7μF/50V capacitors is around 3.7μF at 12V input, and the input voltage ripple is 300mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR_{CIN} \quad (5)$$

It recommended to place an additional small size 10nF ceramic capacitor right beside VIN and GND pins (anode of the diode) for high frequency filtering.

APPLICATION INFORMATION (continued)

Inductor Design

Equation 6 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor, and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 20% to 40% ripple is selected (K_{IND} = 0.2 ~ 0.4). Choosing a higher K_{IND} value reduces the selected inductance, but a too high K_{IND} factor may result in insufficient slope compensation.

$$L = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (6)$$

K_{IND} = 0.3 is a suitable choice when low-ESR ceramic capacitors are used for output capacitors. K_{IND} = 0.2 is preferred when a high-ESR output capacitor is used. In this example, the calculated inductance will be 6μH with K_{IND} = 0.3, so the nearest larger inductance of 6.8μH is selected. The ripple, RMS and peak inductors current calculations are summarized in Equations 7, 8 and 9 respectively.

$$\Delta I_L = \frac{V_{IN\_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (7)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (8)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (9)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

External Diode (Catch Diode)

An external power diode between the SW and GND pins is needed for the SGM61232 to complete the converter. This diode must tolerate the application's absolute maximum ratings. The reverse blocking voltage must be higher than V_{IN_MAX} and its peak current must be above the maximum inductor current. Choose a diode with small forward voltage drop for higher efficiency. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 30V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SGM61232.

Output Capacitor Design

Three primary criteria must be considered for design of the output capacitor (C_{OUT}): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 10 can be used to calculate the minimum output capacitance that is needed to supply a current step (ΔI_{OUT}) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

APPLICATION INFORMATION (continued)

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (10)$$

where:

- ΔI_{OUT} is the change in output current.
- ΔV_{OUT} is the allowable change in the output voltage.

For example, if the acceptable transient from 1.5A to 3A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 3.3V = 0.165V and ΔI_{OUT} = 1.5A, the minimum required capacitance will be 33.7μF. Note that the impact of output capacitor ESR on the transient is not taken into account in Equation 10. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The energy stored in the inductor can produce an output voltage overshoot when the load current decreases rapidly. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 11 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT\_H}^2 - I_{OUT\_L}^2}{\left(V_{OUT} + \Delta V_{OUT}\right)^2 - V_{OUT}^2} \quad (11)$$

where:

- I_{OUT_H} is the output current under heavy load.
- I_{OUT_L} is the output current under light load.

For example, if the acceptable transient from 3A to 1.5A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 3.3V = 0.165V, the minimum required capacitance will be 41.1μF.

Equation 12 can be used for the output ripple criteria and finding the minimum output capacitance needed. V_{OUT_RIPPLE} is the maximum acceptable ripple. In this example, the allowed ripple is 33mV that results in minimum capacitance of 6.1μF.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (12)$$

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 12. For a specific output capacitance value, use Equation 13 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{COUT} < \frac{V_{OUT\_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (13)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, two 47μF/10V X5R ceramic capacitors with 3mΩ of ESR are used. There is a limit to the amount of ripple current that a capacitor can handle without damaging or overheating. The inductor ripple is bypassed through the output capacitor. Equation 14 calculates the RMS current that the output capacitor must support. In this example, it is 229mA.

$$I_{COUT\_RMS} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{\sqrt{12} \times V_{IN\_MAX} \times L \times f_{SW}} \quad (14)$$

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor (C_4). It is recommended to add a resistor R_4 in series with C_4 to slow down switch-on speed of the HS switch and improve radiated EMI problems. The R_4 value depends on the size of the HS switch. For most applications, it's approximately 5Ω ~ 10Ω. Too high values for R_4 may cause insufficient C_4 charging in high duty-cycle applications. Slower switch-on will also increase switch losses and reduce efficiency.

UVLO Setting

The under-voltage lockout (UVLO) can be programmed using an external voltage divider on the EN pin of the SGM61232. In this design R_1 is connected between VIN and the EN pin and R_2 is connected between EN and GND (see Figure 4). The UVLO has two thresholds, one for power-up (turn-on) when the input voltage is rising, and one for power-down or brownout (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 7V (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input falls below 5.5V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_1 = 402kΩ and R_2 = 82.5kΩ.

APPLICATION INFORMATION (continued)

Soft-Start Capacitor Selection

The soft-start capacitor programs the ramp-up time of the output voltage during power-up. Due to the limited voltage slew rate required by the load or limited available input current, a ramp is needed in many applications to avoid input voltage sag during startup (UVLO) or to avoid over-current protection that can occur during output capacitor charging. Soft-start will solve all these issues by limiting the output voltage slew rate.

Equation 3 (with I_{SS} = 2μA and V_{REF} = 0.8V) can be used to calculate the soft-start capacitor for a required soft-start time (t_{SS}). In this example, the output capacitor value is relatively small (2 × 47μF) and the soft-start time is not critical because it does not require too much charge for 3.3V output voltage. However, it is better to set a small arbitrary value, like C_{SS} = 10nF that results in 4ms startup time.

Feedback Resistors Setting

Use resistor dividers (R_5 and R_6) to set the output voltage using Equations 15 and 16.

$$R_6 = \frac{R_5 \times V_{REF}}{V_{OUT} - V_{REF}} \quad (15)$$

$$V_{OUT} = V_{REF} \times \left(\frac{R_5}{R_6} + 1 \right) \quad (16)$$

Recommended to choose R_5 around 10kΩ and calculate R_6 from Equation 15. Use accurate and stable resistors (1% or better) to enhance output accuracy. For this example, the selected values are R_5 = 18kΩ and R_6 = 5.76kΩ, resulting in a 3.3V output voltage.

Compensation Network Setting

Several techniques are used by engineers to compensate a DC/DC regulator. The method presented here uses simple calculations and generally results in high phase margins. In most conditions, the phase margin will be between 60 and 90 degrees. In this method the effects of the slope compensation are ignored. Because of this approximation, the actual cross over frequency is usually lower than the calculated value.

First, the converter pole (f_P) and ESR-zero (f_Z) are calculated from Equations 17 and 18. For C_{OUT}, the worst derated value of 47.6μF should be used. Equations 19 and 20 can be used to find an estimation for closed-loop crossover frequency (f_{CO}) as a starting point (choose the lower value).

$$f_P = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}} \quad (17)$$

$$f_Z = \frac{1}{2\pi \times ESR_{COUT} \times C_{OUT}} \quad (18)$$

$$f_{CO} = \sqrt{f_P \times f_Z} \quad (19)$$

$$f_{CO} = \sqrt{f_P \times \frac{f_{SW}}{2}} \quad (20)$$

For this design, f_P = 3.04kHz and f_Z = 1.11MHz. Equation 19 yields 58.21kHz for crossover frequency and Equation 20 gives 28.65kHz. The lower value 28.65kHz will be chosen as the intended crossover frequency. Having the crossover frequency, the compensation network (R_3 and C_6) can be calculated. R_3 sets the gain of the compensated network at the crossover frequency and can be calculated by Equation 21.

$$R_3 = \frac{2\pi \times f_{CO} \times V_{OUT} \times C_{OUT}}{g_m \times V_{REF} \times GM_{COMP}} \quad (21)$$

C_6 sets the location of the compensation zero along with R_3. To place this zero on the converter pole, use Equation 22.

$$C_6 = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_3} \quad (22)$$

From Equations 21 and 22, the standard selected values are R_3 = 33kΩ and C_6 = 2.2nF.

A compensation pole can be implemented if desired by adding capacitor C_7 in parallel with the series combination of R_3 and C_6. Use the larger value calculated from Equation 23 and Equation 24 for C_7 to set the compensation pole. The selected value of C_7 is 22pF.

$$C_7 = \frac{ESR_{COUT} \times C_{OUT}}{R_3} \quad (23)$$

$$C_7 = \frac{1}{\pi \times f_{SW} \times R_3} \quad (24)$$

APPLICATION INFORMATION (continued)

Layout Considerations

A PCB layout example is provided in Figure 5 and Figure 6. This layout has been proved to bring good results although other layout designs may also obtain good performance.

• Bypass the VIN pin to GND pin (where it connects to the anode pin of the power diode) with low-ESR ceramic capacitors (10μF/X5R or better) and place them as close as possible to the device.

• Connect the diode as close as possible to SW and GND pins.

• Share the same GND connection point with the input and output capacitors.

• Connect the device GND to the PCB ground plane right at the GND pin.

• Minimize the length and the area of the connection route from SW pin to the cathode of the diode and the inductor to reduce the noise coupling from this area.

• Consider sufficient ground plane area on the top side for proper heat dissipation. Because the SGM61232 has a fused lead frame, the GND pin acts as a heat conduction path from the die to the PCB for better cooling. Connect the large internal or back-side ground planes to the top-side ground near the device with thermal vias for better heat dissipation.

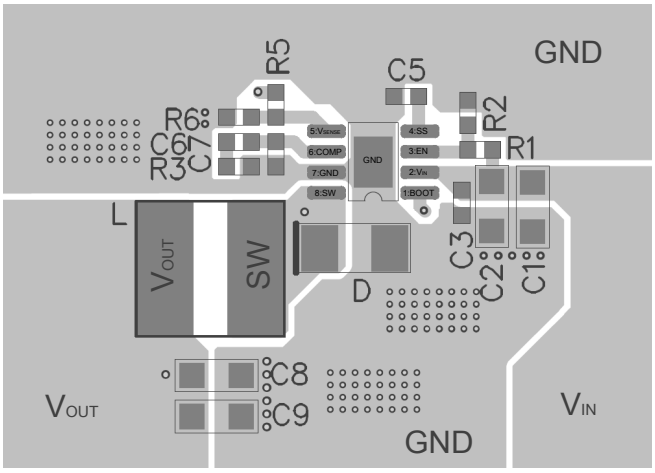


Figure 5. Top Layer

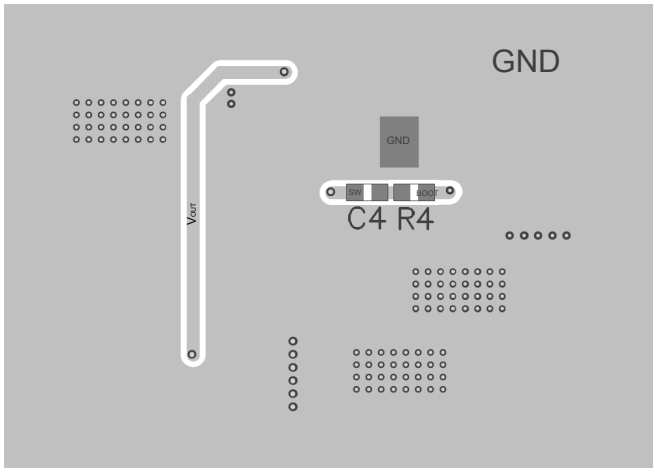


Figure 6. Bottom Layer

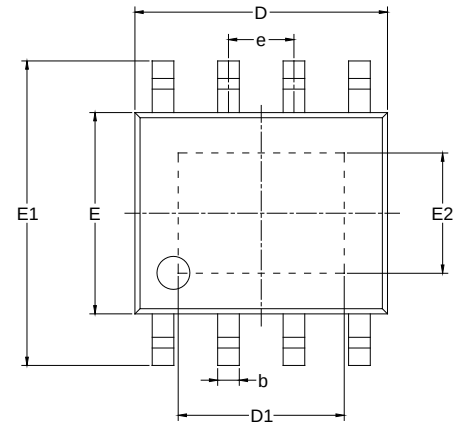
REVISION HISTORY

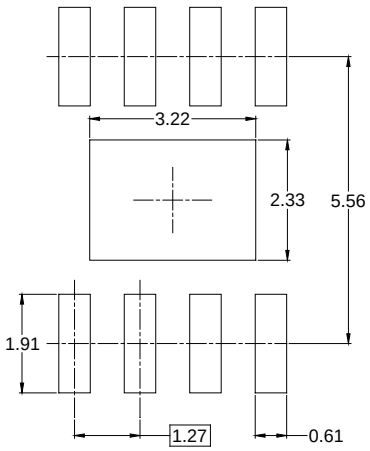
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (JANUARY 2022) to REV.A	Page
Changed from product preview to production data	All

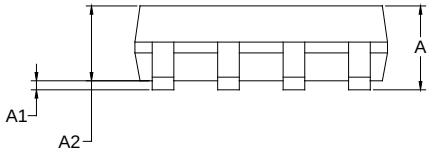
PACKAGE OUTLINE DIMENSIONS

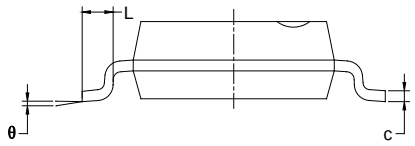
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





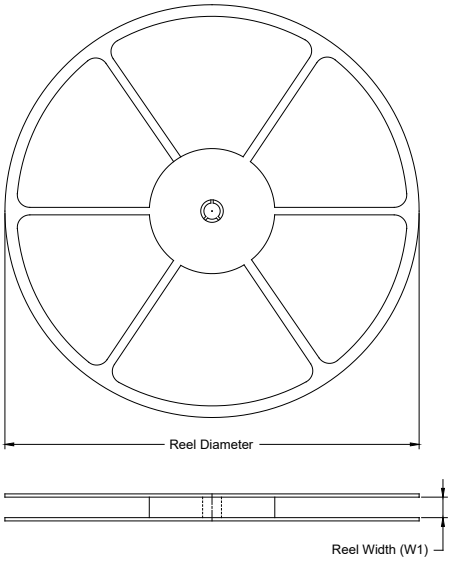
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°

NOTES:

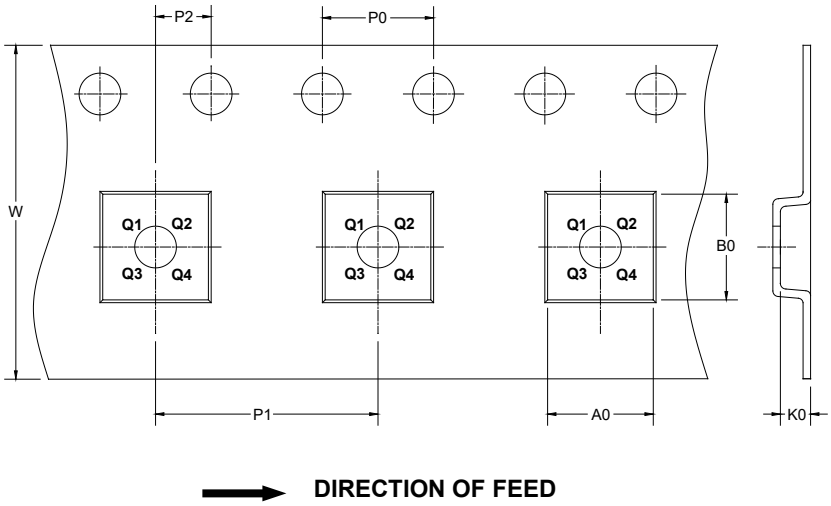
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



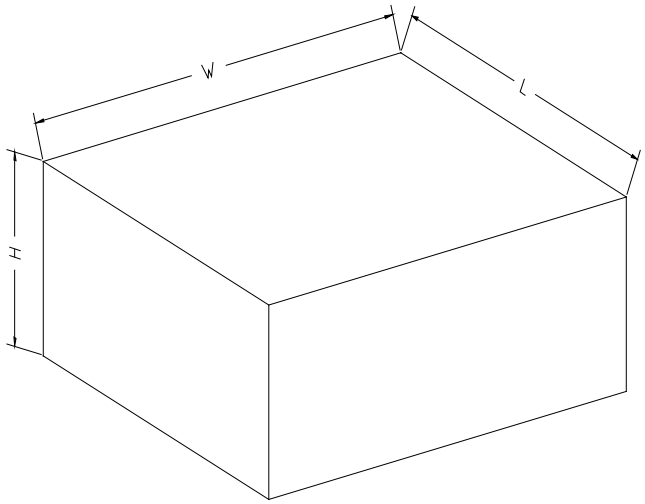
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002