TPS61046 28-V Output Voltage Boost Converter in WCSP Package

1 Features

- Input Voltage Range: 1.8 V to 5.5 V, 1.6 V after Startup
- Output Voltage Up to 28 V
- Integrated Power Diode and Isolation Switch
- 900-mA (typical) Switch Current
- Up to 85% Efficiency at 3.6-V Input and 12-V Output
- 500-nA Ultra-low Shutdown Current
- ±2% Output Voltage Accuracy
- Power Save Operation Mode at Light Load
- Internal 10-ms Soft Start Time
- True Disconnection between Input and Output during Shutdown
- Output Short Circuit Protection
- Output Over-Voltage Protection
- Thermal Shutdown Protection
- 0.80-mm × 1.20-mm WCSP package

2 Applications

- PMOLED Power Supply
- Wearable Devices
- Portable Medical Equipment
- Sensor Power Supply

3 Description

The TPS61046 is a highly integrated boost converter designed for applications requiring high voltage and tiny solution size such as PMOLED panel and sensor module. The TPS61046 integrates a 30-V power switch, input/output isolation switch, and power diode. It can output up to 28 V from input of a Li+ battery or two cell alkaline batteries in series.

The TPS61046 operates with a switching frequency at 1.0 MHz. This allows the use of small external components. The TPS61046 has an internal default 12-V output voltage setting by connecting the FB pin to the VIN pin. Thus it only needs three external components to get 12-V output voltage. Together with WCSP package, the TPS61046 gives a very small overall solution size. The TPS61046 has typical 900-mA switch current limit. It has 10-ms built-in soft start time to minimize the inrush current. When the TPS61046 is in shutdown mode, the isolation switch disconnects the output from input to minimize the leakage current. The TPS61064 also implements output short circuit protection, output over-voltage protection and thermal shutdown.

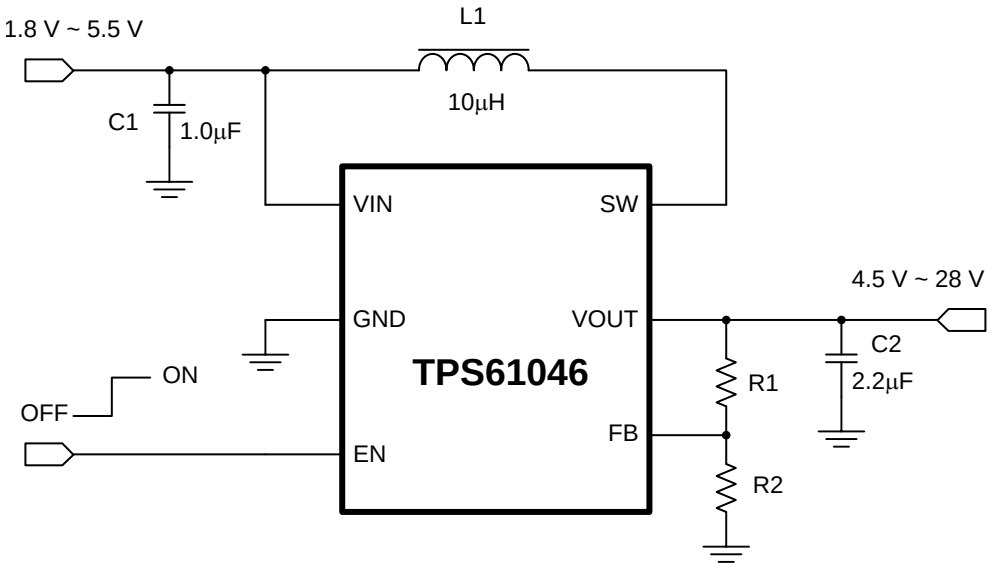
The TPS61046 is available in a 6-pin 0.80-mm x 1.20-mm WCSP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61046	WCSP (6)	0.80 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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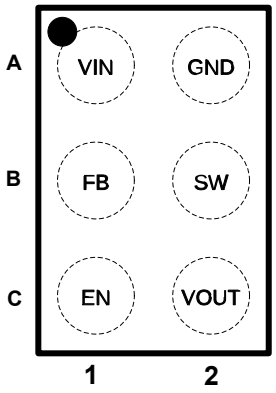
5 Revision History

DATE	REVISION	NOTES
April 2015	*	Initial release.

6 Pin Configuration and Functions

YFF Package
6-Ball WCSP
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
EN	C1	I	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode.
FB	B1	I	Voltage feedback of adjustable output voltage. Connect to the center tap of a resistor divider to program the output voltage. When it is connected to the VIN pin, the output voltage is set to 12 V by an internal feedback.
GND	A2	PWR	Ground
SW	B2	PWR	The switch pin of the converter. It is connected to the drain of the internal power MOSFET.
VIN	A1	I	IC power supply input
VOUT	C2	PWR	Output of the boost converter

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, EN, FB	– 0.3	6	V
	SW, VOUT	–0.3	32	V
Operating junction temperature range, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	±500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	1.8		5.5	V
V_{OUT}	Output voltage range	4.5		28	V
L	Effective inductance range	1.0×0.7	10	22×1.3	µH
C_{IN}	Effective input capacitance range	0.22	1.0		µF
C_{OUT}	Effective output capacitance range	0.22	1.0	10	µF
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS61046 YFF (WCSP) 6 BALLS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.3	
ψ_{JT}	Junction-to-top characterization parameter	5.6	
ψ_{JB}	Junction-to-board characterization parameter	22.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

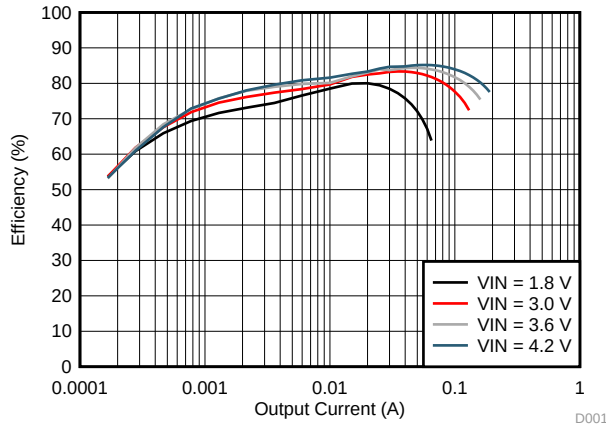
7.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 3.6 V and V_{OUT} = 12 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		1.8		5.5	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		1.75	1.8	V
		V_{IN} falling		1.55	1.6	
V_{IN_HYS}	VIN UVLO hysteresis			200		mV
I_{Q_VIN}	Quiescent current into VIN pin	IC enabled, no load, no switching, V_{IN} = 1.8 V to 5.5 V, V_{OUT} = 12 V		110	200	µA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} = 1.8 V to 5.5 V, T_J up to 85°C		0.1	0.8	µA
		IC disabled, V_{IN} = 1.8 V to 5.5 V, T_J up to 60°C			0.5	µA
OUTPUT						
V_{OUT}	Output voltage range		4.5		28	V
V_{OUT_12V}	12-V output voltage accuracy	FB pin connected to VIN pin, T_J=0°C to 125°C	11.7	12	12.3	V
V_{REF}	Feedback voltage	PWM mode, T_J=0°C to 125°C	0.779	0.795	0.811	V
		PFM mode, T_J=0°C to 125°C		0.803		V
V_{OVP}	Output overvoltage protection threshold		28	29.2	30.4	V
V_{OVP_HYS}	Over voltage protection hysteresis			0.8		V
I_{FB_LKG}	Leakage current into FB pin				200	nA
I_{SW_LKG}	Leakage current into SW pin	IC disabled, T_J up to 85°C			500	nA
POWER SWITCH						
$R_{DS(on)}$	Isolation MOSFET on resistance	V_{OUT} = 12 V		850		mΩ
	Low-side MOSFET on resistance	V_{OUT} = 12 V		450		
f_{SW}	Switching frequency	V_{IN} = 3.6 V, V_{OUT} = 12 V, PWM mode	850	1050	1250	kHz
t_{ON_min}	Minimal switch on time			150	250	ns
I_{LIM_SW}	Peak switch current limit	V_{IN} = 3.6 V, V_{OUT} = 12 V	600	900	1200	mA
I_{LIM_CHG}	Pre-charge current	V_{IN} = 3.6 V, V_{OUT} = 0 V		30	50	mA
$t_{STARTUP}$	Startup time	V_{OUT} from V_{IN} to 12 V, $C_{OUT\_effective}$ = 2.2 µF, I_{OUT} = 0 A	2	5		ms
LOGIC INTERFACE						
V_{EN_H}	EN Logic high threshold				1	V
V_{EN_L}	EN Logic Low threshold		0.4			V
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

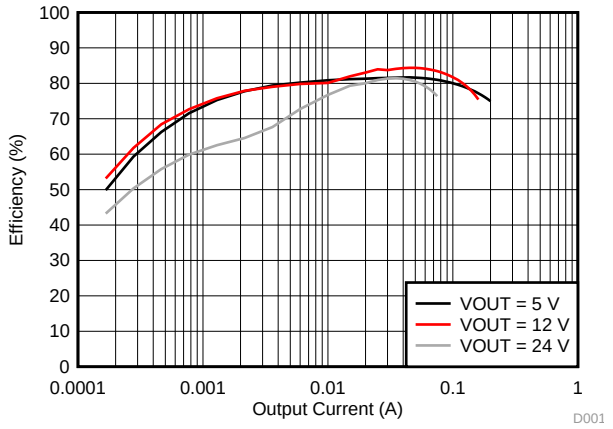
7.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 12 V, T_J = –40°C to 125°C, unless otherwise noted.



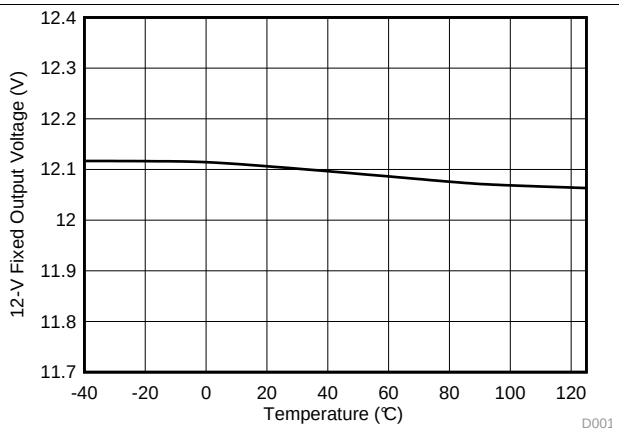
V_{IN} = 1.8 V, 3.0 V, 3.6 V, 4.2 V, V_{OUT} = 12 V

Figure 1. Efficiency vs Output Current



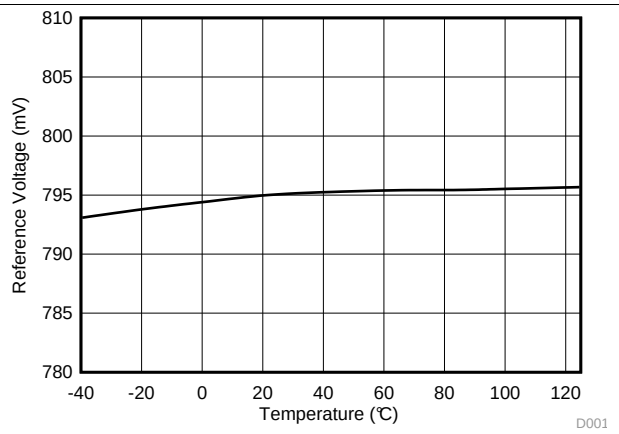
V_{IN} = 3.6 V, V_{OUT} = 5 V, 12 V, 24 V

Figure 2. Efficiency vs Output Current



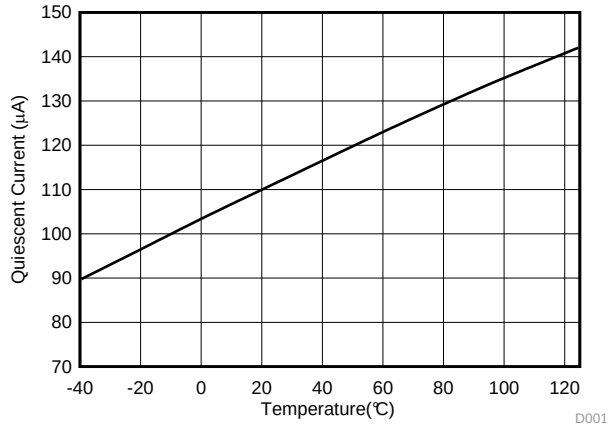
V_{IN} = 3.6 V, V_{OUT} = 12 V, FB pin connected to VIN pin

Figure 3. 12-V Fixed Output Voltage vs Temperature



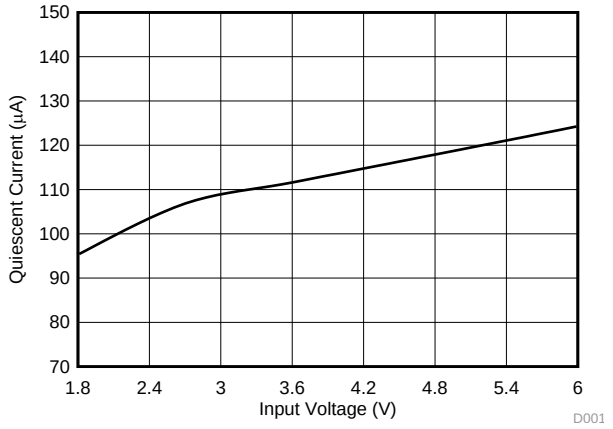
V_{IN} = 3.6 V, V_{OUT} = 12 V

Figure 4. Reference Voltage vs Temperature



V_{IN} = 3.6 V, V_{OUT} = 12 V, No switching

Figure 5. Quiescent Current vs Temperature

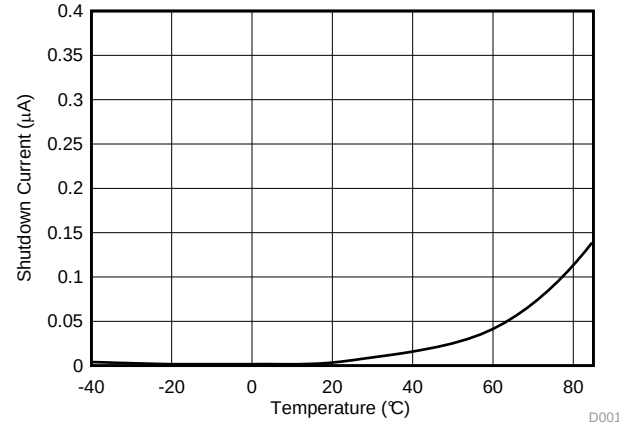


V_{IN} = 1.8 V ~ 6 V, V_{OUT} = 12 V, No switching

Figure 6. Quiescent Current vs Input Voltage

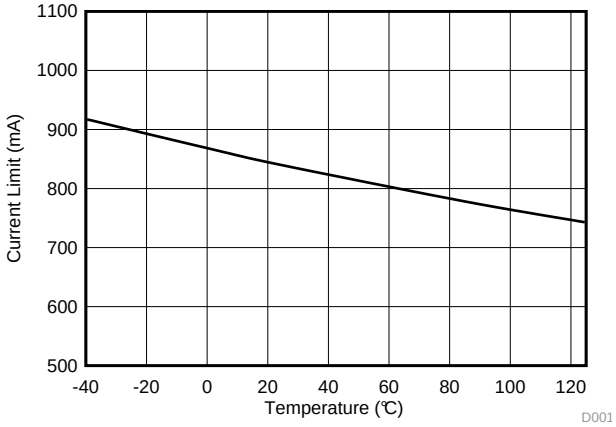
Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 12 V, T_J = –40°C to 125°C, unless otherwise noted.



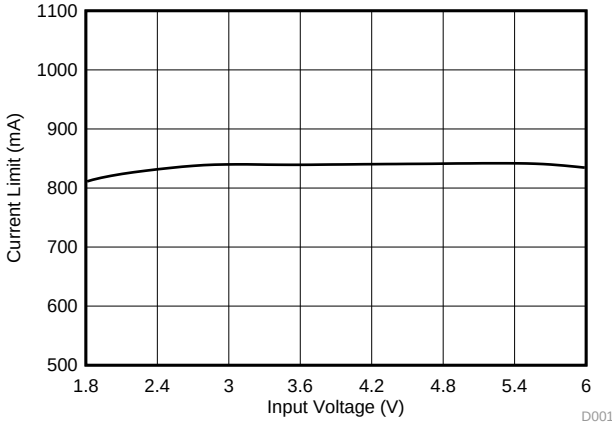
V_{IN} = 3.6 V

Figure 7. Shutdown Current vs Temperature



V_{IN} = 3.6 V, V_{OUT} = 12 V

Figure 8. Current Limit vs Temperature



V_{IN} = 1.8 V ~ 6 V, V_{OUT} = 12 V

Figure 9. Current Limit vs Temperature

8 Detailed Description

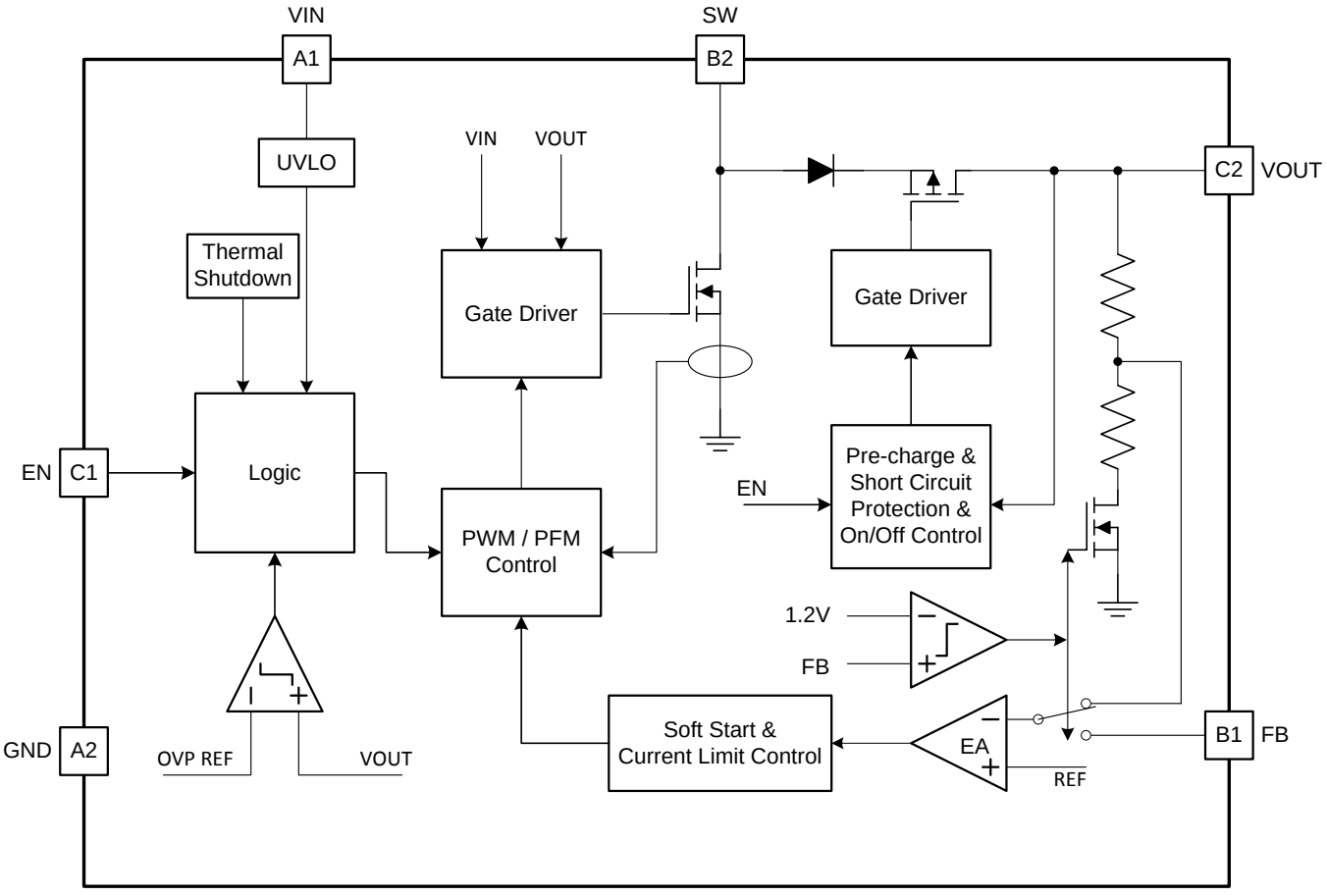
8.1 Overview

The TPS61046 is a highly integrated boost converter designed for applications requiring high voltage and tiny solution size such as PMOLED panel power supply and sensor module. The TPS61046 integrates a 30-V power switch, input/output isolation switch, and power diode. It can output up to 28 V from input of a Li+ battery or two cell alkaline batteries in series.

One common issue with conventional boost regulators is the conduction path from input to output even when the power switch is turned off. It creates three problems, which are inrush current during start-up, output leakage current during shutdown and excessive over load current. In the TPS61046, the isolation switch is turned off under shutdown mode and over load conditions, thereby opening the current path. Thus the TPS61046 can truely disconnect the load from the input voltage and minimize the leakage current during shutdown mode.

The TPS61046 operates with a switching frequency at 1.0 MHz. This allows the use of small external components. The TPS61046 has an internal default 12-V output voltage setting by connecting the FB pin to the VIN pin. Thus it only needs three external components to get 12-V output voltage. Together with WCSP package, the TPS61046 gives a very small overall solution size. The TPS61046 has typical 900-mA switch current limit. It has 10-ms built-in soft start time to minimize the inrush current. The TPS61064 also implements output short circuit protection, output over-voltage protection and thermal shutdown.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Under-Voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 1.55 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 1.75 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 1.55 V and 1.75 V.

8.3.2 Enable and Disable

When the input voltage is above maximal UVLO rising threshold of 1.8 V and the EN pin is pulled high, the TPS61046 is enabled. When the EN pin is pulled low, the TPS61046 goes into shutdown mode. The device stops switching and the isolation switch is turned off providing the isolation between input and output. In shutdown mode, less than 1-µA input current is consumed.

8.3.3 Soft Start

The TPS61046 begins soft start when the EN pin is pulled high. at the beginning of the soft start period, the isolation FET is turned on slowly to charge the output capacitor with 30-mA current for about 5 ms. This is called the pre-charge phase. After the pre-charge phase, the TPS61046 starts switching. This is called switching soft start phase. An internal soft start circuit limits the peak inductor current according to the output voltage. When the output voltage is below 3 V, the peak inductor current is limited to 140 mA. Along with the output voltage going up from 3 V to 5 V, the peak current limit is gradually increased to the normal value of 900 mA. The switching soft start phase is about 5 ms typically. The soft start funciton reduces the inrush current during startup.

8.3.4 Over-voltage Protection

The TPS61046 has internal output over-voltage protection (OVP) function. When the output voltage exceeds the OVP threshold of 29.2 V, the device stops switching. Once the output voltage falls 0.8 V below the OVP threshold, the device resumes operation again.

8.3.5 Output Short Circuit Protection

The TPS61046 starts to limit the output current whenever the output voltage drops below 4 V. The lower output voltage, the smaller output current limit. When the VOUT pin is shorted to ground, the output current is limited to less than 200 mA. This function protects the device from being damaged when the output is shorted to ground.

8.3.6 Thermal Shutdown

The TPS61046 goes into thermal shutdown once the junction temperature exceeds 150°C. When the junction temperature drops below the thermal shutdown temperature threshold less the hysteresis, typically 130°C, the device starts operating again.

8.3.7 Device Functional Modes

The TPS61046 has two operation modes, PWM mode and power save mode.

8.3.7.1 PWM Mode

The TPS61046 uses a quasi-constant 1.0-MHz frequency pulse width modulation (PWM) at moderate to heavy load current. Based on the input voltage to output votlage ratio, a circuit predicts the required off-time. At the beginning of the switching cycle, the NMOS switching FET, shown in the functional block diagram, is turned on. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the inductor current hits the current threshold that is set by the output of the error amplifier, the PWM switch is turned off, and the power diode is forward-biased. The inductor transfers its stored energy to replenish the output capacitor and supply the load. When the off-time is expired, the next switching cycle starts again. The error amplifier compares the FB pin voltage with an internal reference votlage, and its output determines the inductor peak current.

The TPS61046 has a built-in compensation circuit that can accommodate a wide range of input voltage, output voltage, inductor value and output capacitor value for stable operation.

Feature Description (continued)

8.3.8 Power Save Mode

The TPS61046 integrates a power save mode with pulse frequency modulation (PFM) to improve efficiency at light load. When the load current decreases, the inductor peak current set by the output of the error amplifier declines to regulate the output voltage. When the inductor peak current hits the low limit of 140 mA, the output voltage will exceed the setting voltage as the load current decreases further. When the FB voltage hits the PFM reference voltage, the TPS61046 goes into the power save mode. In the power save mode, when the FB voltage rises and hits the PFM reference voltage, the device continuous switching for several cycles because of the delay time of the internal comparator. Then it stops switching. The load is supplied by the output capacitor and the output voltage declines. When the FB voltage falls below the PFM reference voltage, after the delay time of the comparator, the device starts switching again to ramp up the output voltage.

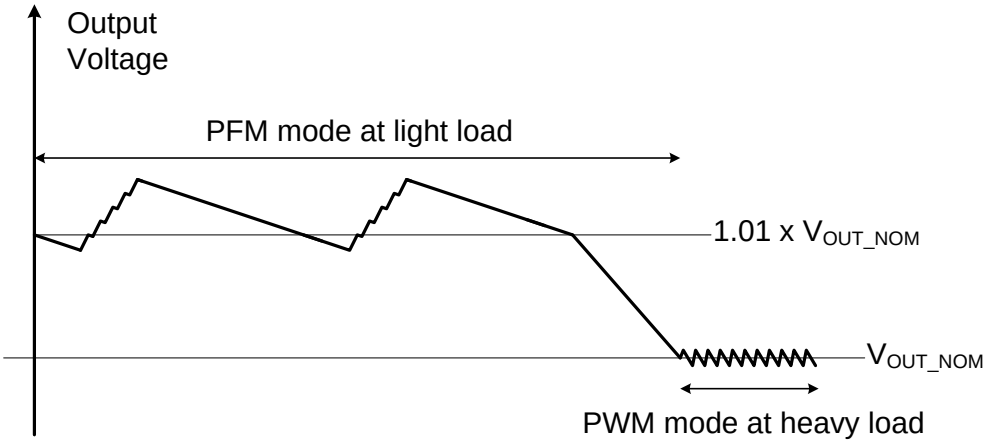


Figure 10. Output Voltage in PWM Mode and PFM Mode

9 Application and Implementation

9.1 Application Information

The TPS61046 is a boost DC-DC converter with a PWM switch, a power diode and an input/output isolation switch integrated. The device supports up to 28-V output with the input range from 1.8 V to 5.5 V. The TPS61046 adopts the current-mode control with adaptive constant off-time. The switching frequency is quasi-constant at 1.0 MHz. The isolation switch disconnects the output from the input during shutdown to minimize leakage current.

The following design procedure can be used to select component values for the TPS61046.

9.2 Typical Application - 12-V Output Boost Converter

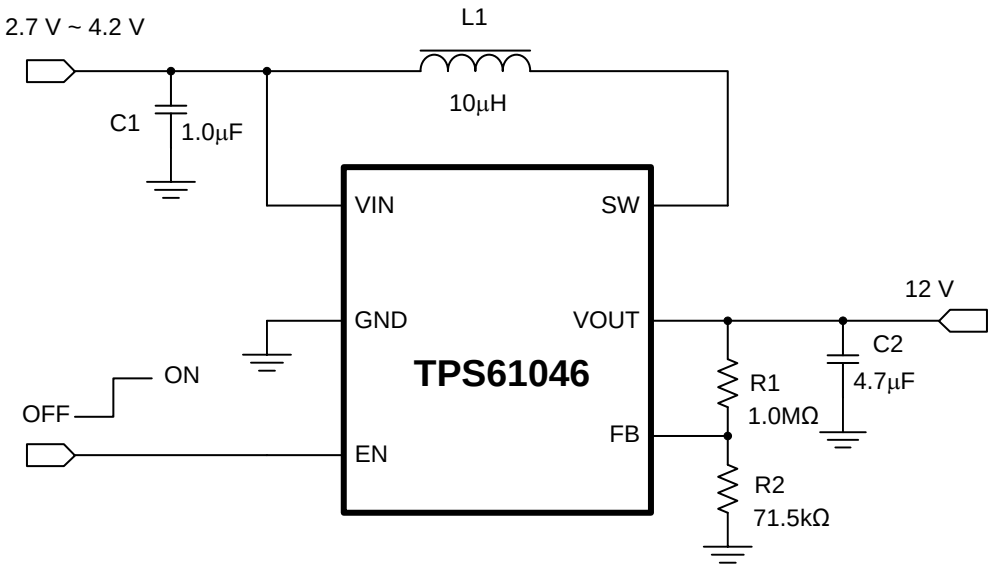


Figure 11. 12-V Boost Converter

9.2.1 Design Requirements

Table 1. Design Requirements

PARAMETERS	VALUES
Input Voltage	2.7 V ~ 4.2 V
Output Voltage	12 V
Output Current	50 mA
Output Voltage Ripple	±50mV

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Output Voltage

There are two ways to set the output voltage of the TPS61046. When the FB pin is connected to the input voltage, the output voltage is fixed to 12 V. This function makes the TPS61046 only need three external components to minimize the solution size. The second way is to use an external resistor divider to set the desired output voltage.

By selecting the external resistor divider R1 and R2, as shown in Equation 1, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is V_{REF} of 795 mV.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (1)$$

Where:

V_{OUT} is the desired output voltage

V_{REF} is the internal reference voltage at the FB pin

For best accuracy, R2 should be kept smaller than 80 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. Changing the R2 towards a higher value reduces the quiescent current for achieving highest efficiency at low load currents.

9.2.2.2 Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The TPS61046 is designed to work with inductor values between 1.0 µH and 22 µH. Follow Equation 2 to Equation 4 to calculate the inductor's peak current for the application. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margin, choose the inductor value with -30% tolerance, and a low power-conversion efficiency for the calculation.

In a boost regulator, the inductor dc current can be calculated with Equation 2.

$$I_{L(DC)} \quad \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{2}$$

Where:

V_{OUT} = output voltage

I_{OUT} = output current

V_{IN} = input voltage

η = power conversion efficiency, use 80% for most applications

The inductor ripple current is calculated with the Equation 3 for an asynchronous boost converter in continuous conduction mode (CCM).

$$\Delta I_{L(P-P)} \quad \frac{V_{IN} \times \left(V_{OUT} + 0.8V - V_{IN}\right)}{L \times f_{SW} \times \left(V_{OUT} + 0.8V\right)} \tag{3}$$

Where:

$\Delta I_{L(P-P)}$ = inductor ripple current

L = inductor value

f_{SW} = switching frequency

V_{OUT} = output voltage

V_{IN} = input voltage

Therefore, the inductor peak current is calculated with Equation 4.

$$I_{L(P)} \quad I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \tag{4}$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. Bit in the same way, load transient response time is increased. Because the TPS61046 is for relatively small output current application, the inductor peak-to-peak current could be as high as 200% of the average current with a small inductor value, which means the TPS61046 always works in DCM mode.Table 2 lists the recommended inductor for the TPS61046.

Table 2. Recommended Inductors for the TPS61046

PART NUMBER	L(µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (LxWxH)	VENDOR
FDSD0420-H-100M	10	200	2.5	4.2x4.2x2.0	Toko
CDRH3D23/HP	10	198	1.02	4.0x4.0x2.5	Sumida

Table 2. Recommended Inductors for the TPS61046 (continued)

PART NUMBER	L(µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (LxWxH)	VENDOR
1239AS-H-100M	10	460	1.0	2.5x2.0x1.2	Toko
VLS4012-4R7M	4.7	132	1.1	4.0x4.0x1.2	TDK
0420CDMCBDS	22	379	1.6	4.5x4.1x2.0	Sumida

9.2.2.3 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} \quad \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \tag{5}$$

Where:

D_{MAX} = maximum switching duty cycle

V_{RIPPLE} = peak to peak output voltage ripple

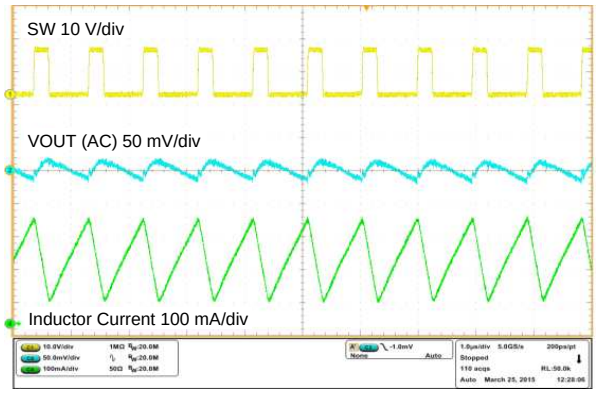
The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, the dc bias can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

It is recommended to use the output capacitor with effective capacitance in the range of 0.47 µF to 10 µF. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output voltage ripple smaller in PWM mode.

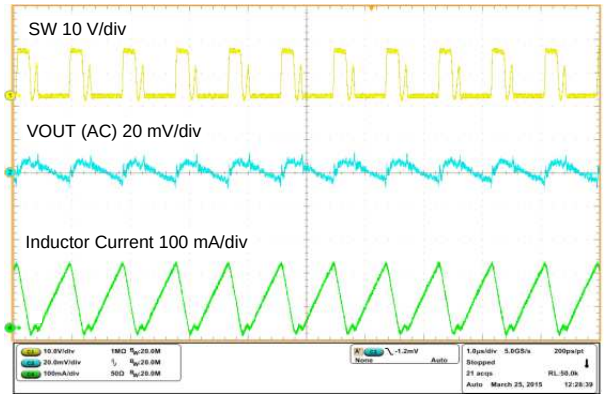
For input capacitor, a ceramic capacitor with more than 1.0 µF is enough for most applications.

9.2.3 Application Performance Curves



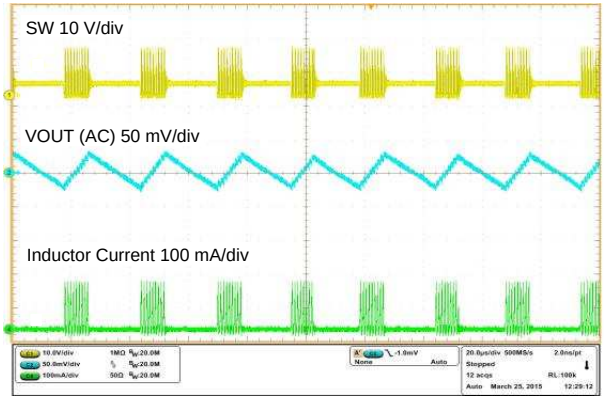
V_{IN} = 3.6 V, V_{OUT} = 12 V, I_{OUT} = 50 mA

Figure 12. Switching Waveforms in PWM CCM Mode



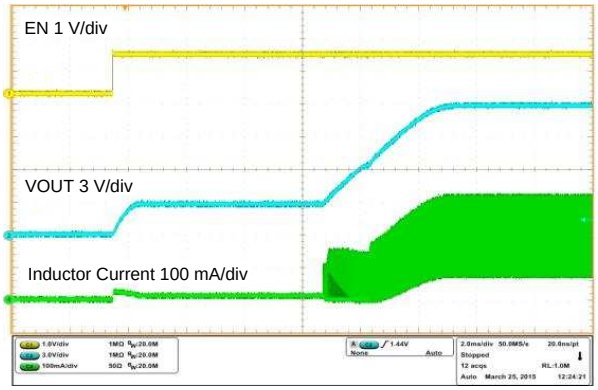
V_{IN} = 3.6 V, V_{OUT} = 12 V, I_{OUT} = 20 mA

Figure 13. Switching Waveforms in PWM DCM Mode



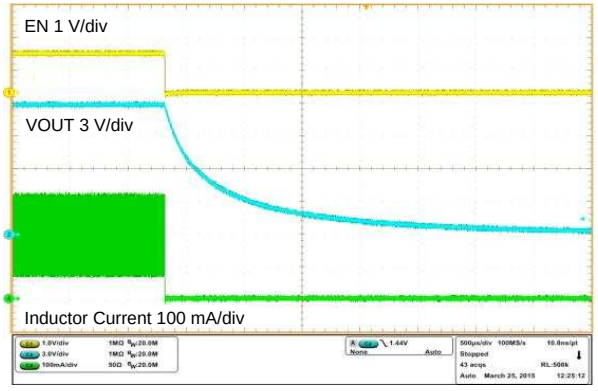
V_{IN} = 3.6 V, V_{OUT} = 12 V, I_{OUT} = 3 mA

Figure 14. Switching Waveforms in Power Save Mode



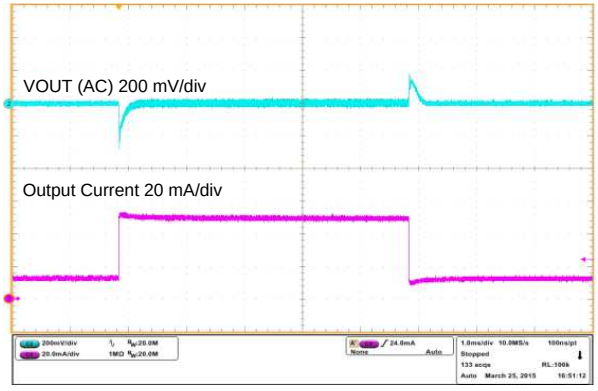
V_{IN} = 3.6 V, V_{OUT} = 12 V, I_{OUT} = 50 mA

Figure 15. Soft Startup



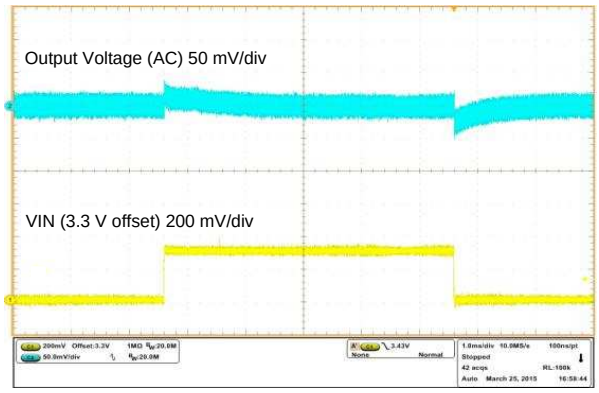
V_{IN} = 3.6 V, V_{OUT} = 12 V, I_{OUT} = 50 mA

Figure 16. Shutdown Waveforms



V_{IN} = 3.6 V, V_{OUT} = 12 V

Figure 17. 10-mA to 50-mA Load Transient Response



VOUT = 12V, IOUT = 50 mA

Figure 18. Input Voltage from 3.3-V to 3.6-V Line Transient Response

9.3 System Examples

9.3.1 Fixed 12-V Output Voltage with Three External Components

The TPS61046 can output fixed 12-V voltage by connecting the FB pin to the VIN pin to save the external resistor divider. The Figure 19 shows the application circuit.

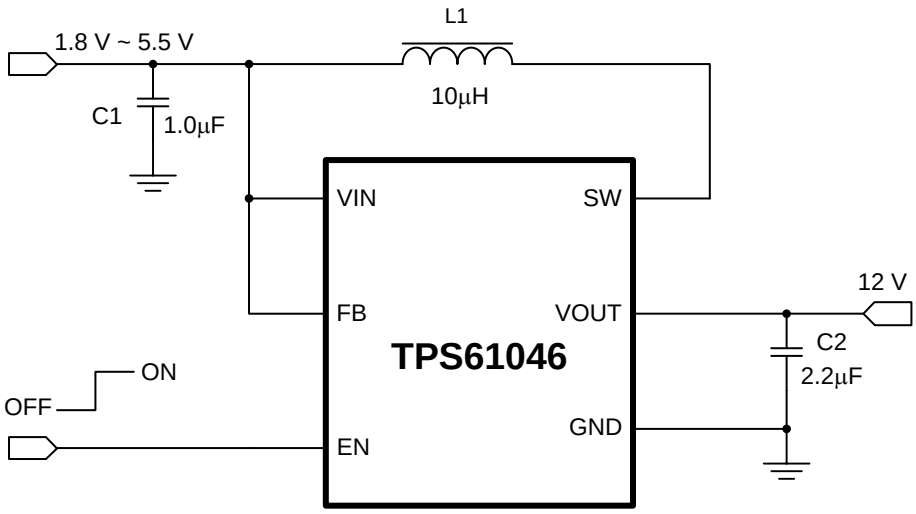


Figure 19. Fixed 12-V Output Voltage by Connecting the FB Pin to VIN Pin

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 µF. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS61046.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise and fall time and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin.

11.2 Layout Example

A large ground plane on the bottom layer connects the ground pins of the components on the top layer through vias.

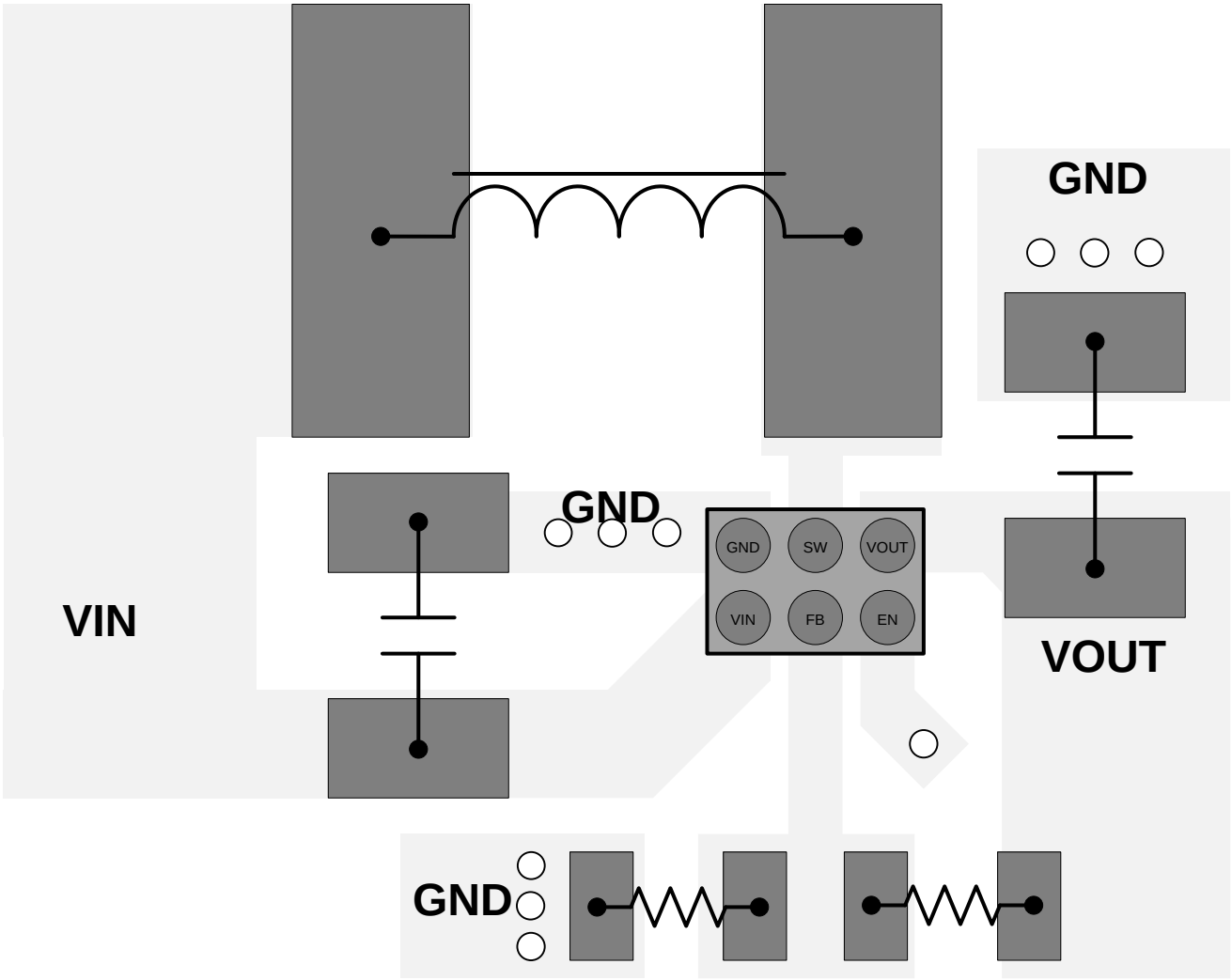


Figure 20. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided *AS IS* by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E, NanoFree are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Package summary

Chip scale package dimensions

The TPS61046 is available in a 6-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

D=ca. 1192 ± 30µm

E=ca. 792 ± 30µm

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61046YFFR	ACTIVE	DSBGA	YFF	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SJS	Samples
TPS61046YFFT	ACTIVE	DSBGA	YFF	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SJS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

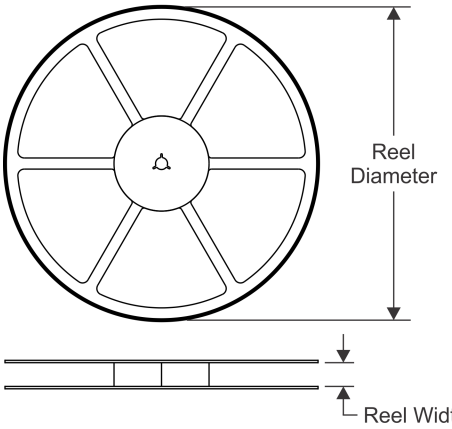
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

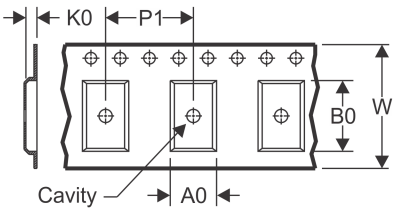
29-Sep-2018

TAPE AND REEL INFORMATION

REEL DIMENSIONS

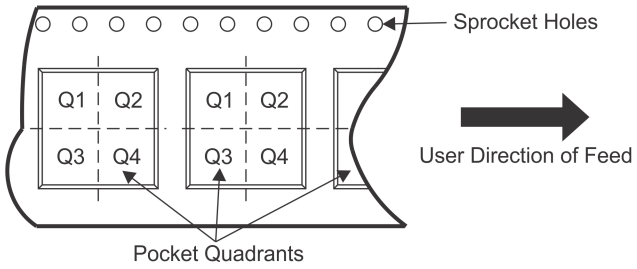


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



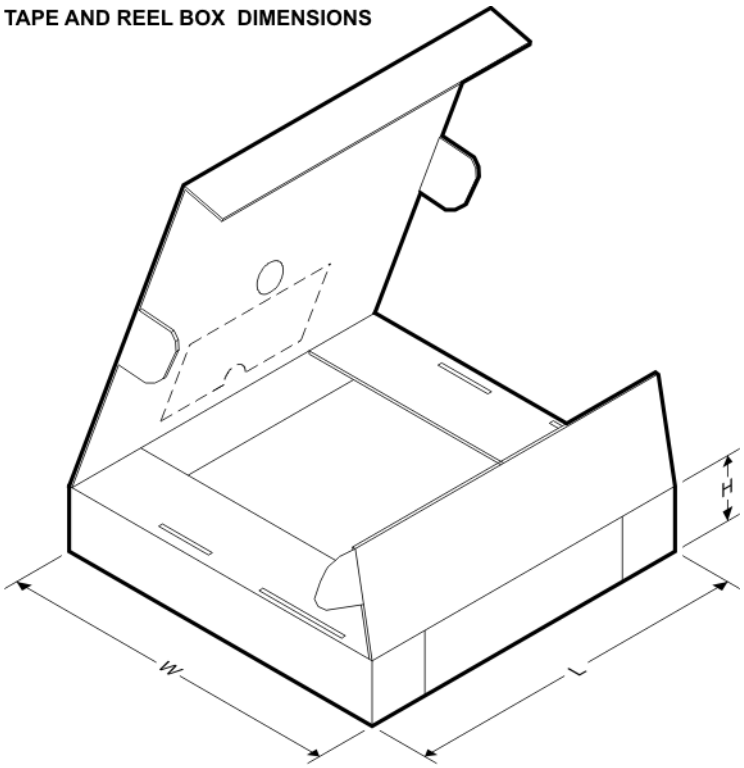
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61046YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.89	1.29	0.69	4.0	8.0	Q1
TPS61046YFFT	DSBGA	YFF	6	250	180.0	8.4	0.89	1.29	0.69	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

29-Sep-2018

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

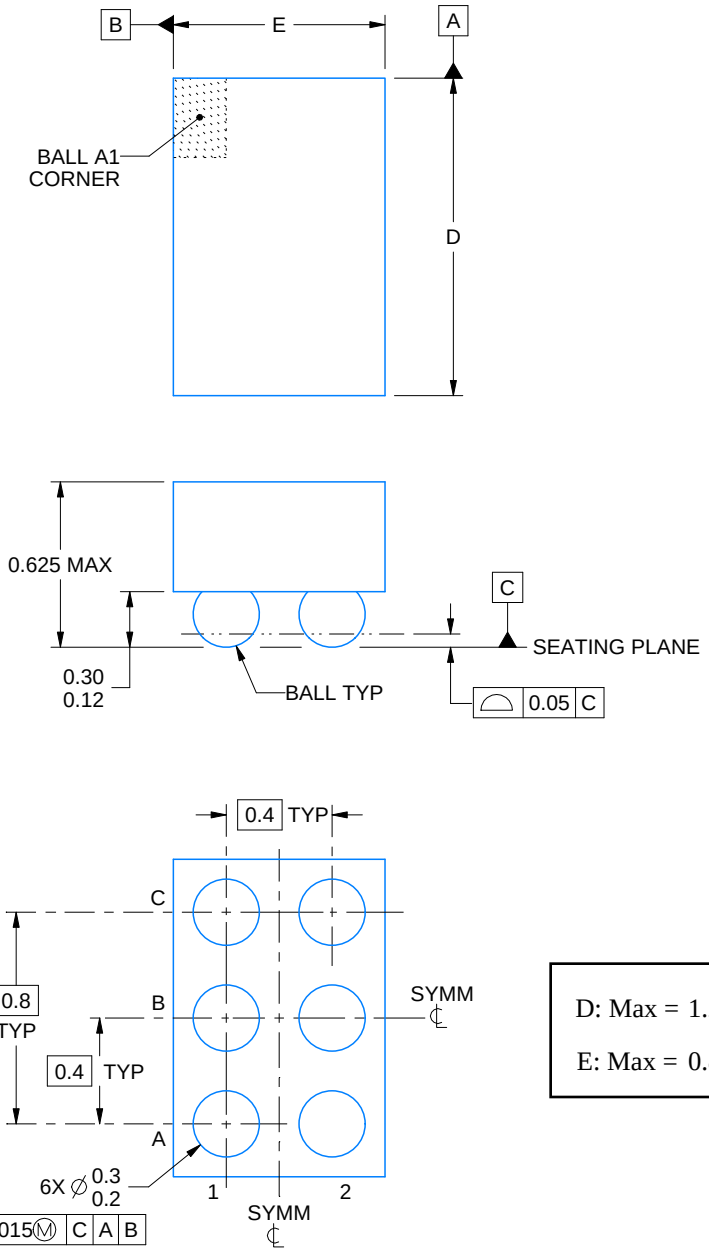
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61046YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS61046YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.222 mm, Min =1.162 mm

E: Max = 0.822 mm, Min =0.762 mm

4223785/A 06/2017

NOTES:

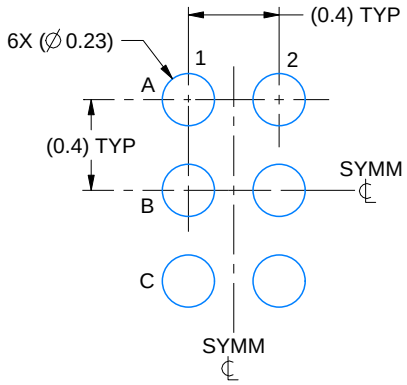
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

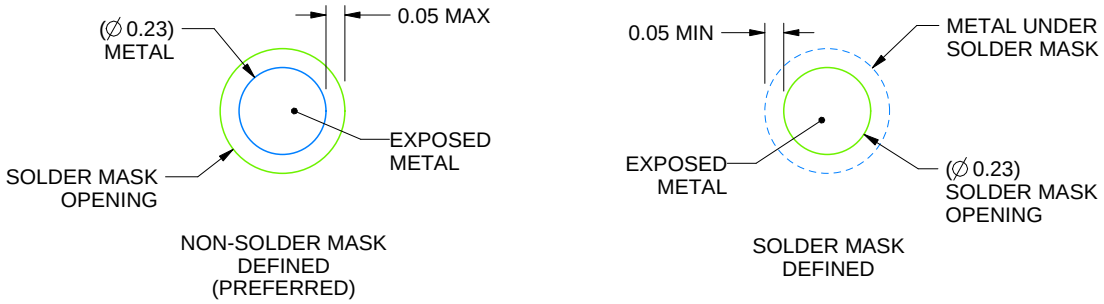
YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4223785/A 06/2017

NOTES: (continued)

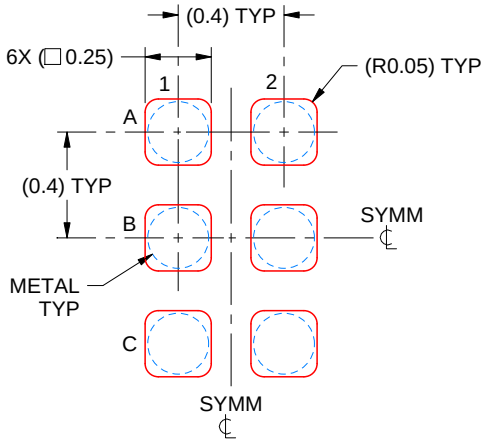
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.